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Nonlinear Conduction in Tantalum Oxide Resistive Memory Without a Select Device

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ABSTRACT

We demonstrate a high degree of nonlinearity in both the ON (low resistance) and OFF (high resistance) states of pure tantalum oxide resistive switches. This nonlinearity could be used to facilitate implementation of crossbar arrays for high density memory storage without the need for select devices or other complex designs. Our demonstration uses CMOS-compatible wafer scale tantalum oxide switches with tantalum and titanium nitride electrode interfaces.

INTRODUCTION

Among the main remaining challenges in resistive memory (RRAM) in high density crossbar implementations is the half-select or "sneak-path" problem. A possible solution is to implement devices with nonlinearity in their current-voltage characteristic. This is being addressed through Complementary resistive switching [1] and a variety of select devices [2] such as negative differential resistance materials [3]. The ideal solution would not require these extra materials but would utilize a resistive switching material that is itself nonlinear. Tantalum oxide has shown excellent performance as a switching material but is considered to have a linear ON-state (low resistance). Tantalum oxide (TaO_x) is clearly capable of very large nonlinearity in the pre-forming state and is highly nonlinear in its OFF state (high resistance). By controlling the forming behavior and ON switching it is possible to maintain nonlinearity throughout a wide switching range.

FABRICATION

CMOS-compatible TaO_x crossbar arrays were fabricated in Sandia's silicon fab with device dimensions ranged from 0.35 to 1.5 microns. The wafer consisted of crossbars of varying numbers of interconnections from single isolated devices to 32x32 arrays.

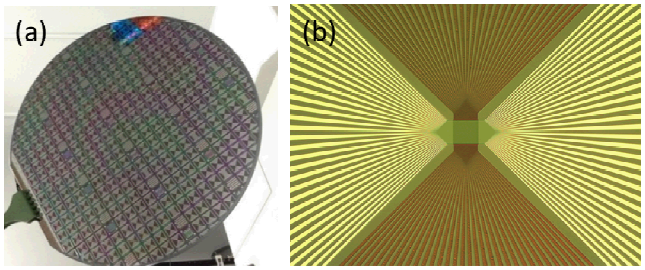

Figure 1: Optical photographs of (a) a wafer patterned with tantalum oxide crossbar arrays fabricated in Sandia's silicon fab and (b) a single crossbar array from the wafer shown in (a), where the lateral lines are the top electrodes and the vertical lines are bottom electrodes.

The devices are accessed by both top and bottom vias from the crossed electrodes and isolated by a SiO_2 interlayer dielectric. We compare to similarly prepared devices using a blanket bottom electrode and only a top via. [4]

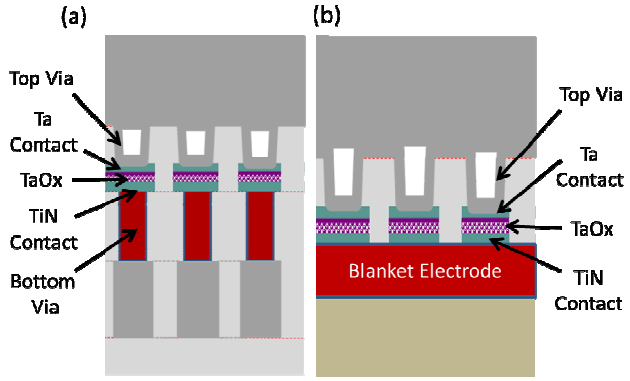

Figure 2: Schematic Diagrams illustrating (a) the double via devices and (b) the blanket bottom electrode devices. The figures show the large difference in parasitic capacitance that can be expected between the two configurations.

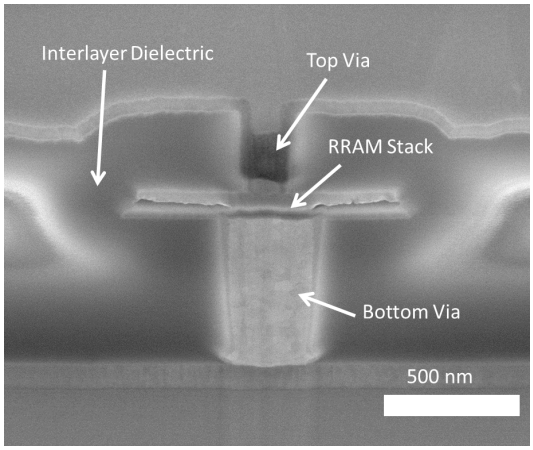

Figure 3: Cross sectional scanning electron micrographs show the as fabricated tantalum oxide resistive memories in the double via configuration.

Tantalum oxide (10 nm) is deposited using a precision feedback approach [5] directly on titanium nitride. Tantalum metal is deposited as the top contact. As compared to those with a blanket bottom electrode, the devices with top and bottom vias have larger electrode separation and much smaller electrode areas, substantially decreasing parasitic capacitance.

ELECTRICAL PERFORMANCE

These devices can be made to have linear ON states as is typically observed (Fig 4) with switching in the milliamp range. The devices are stable in accelerated retention testing and are reproducible with high yield. The milliamp currents and linear ON-states are not ideal for large-scale implementations but are common among our devices and those in the literature if efforts are not made to reduce them. These large currents and linear behavior are the result of strong forming currents that cannot be controlled in large area devices.

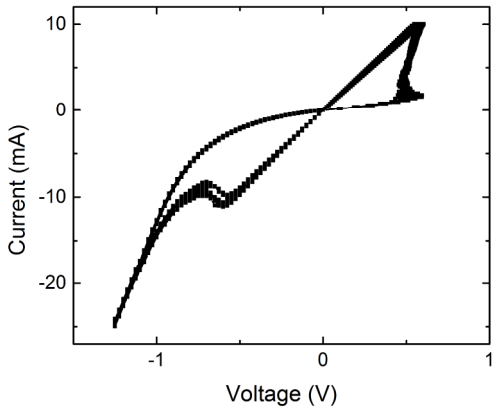

Figure 4: Electrical behavior typical of pure tantalum oxide resistive memory with linear ON state and milliamp switching.

In contrast, the reduced parasitic capacitance in our double via stack can lead to more controlled electroforming behavior. During electroforming the energy stored in the electrodes is dumped through the device. Reducing parasitic capacitance reduces this energy and can lead to weakly formed devices. Weakly formed devices are capable of high degrees of nonlinearity even in the low resistance state while still maintaining good (> 10) OFF/ON ratio. Weakly formed devices also typically switch at reduced currents but the same voltages, leading to large power reductions.

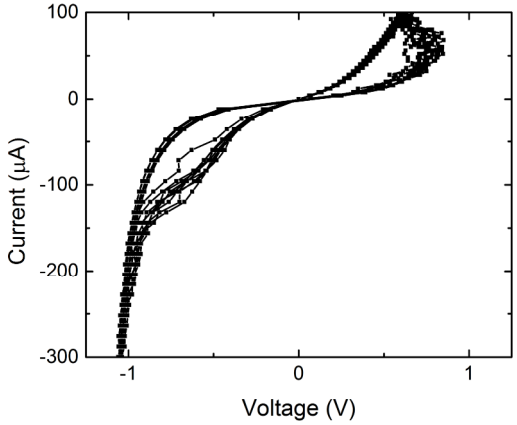

Figure 5: Electrical behavior in weakly formed double via pure tantalum oxide resistive memory devices. Shown is 100 microamp switching with a high degree of nonlinearity.

The switching currents in Fig. 5 are 100 microamps and can be reduced below that well into the tens of microamps for the device shown. It is believed that this difference is due to more controlled electroforming. Electroforming creates a high density of localized defects within a conducting filament. The density of defects and the radius of the conducting filament are the two variables that determine the resistance as well as the nonlinearity. A large forming step leads to a large density of defects over a large area which is detrimental for both power consumption and nonlinearity. During switching, the OFF state is a modulation of the post-forming defect density and location and is highly nonlinear and highly resistive. During ON switching, the defect density is modulated to increase defect density and decrease resistance and decreases nonlinearity. A strong forming step likely impacts the degree to which the nonlinear pre-forming state can be recovered by post-forming modulation.

The defect density and filament radius can also be increased to a detrimental degree after forming during switching. This is easier to avoid, but to do so requires careful control of the switching power. If the resistance is reduced using a voltage-limited supply the power will increase continually during switching. Likewise, if the resistance is increased using current-limited supply the power will increase continually during switching. Therefore, we use current-limited supply during ON switching and voltage-limited supply during OFF switching.

CONCLUSION

We fabricated wafer-scale CMOS compatible crossbar arrays with double via configurations that reduce parasitic capacitance as compared to either bottom blanket electrode or via-less crossbar designs. The reduced capacitance can enable weak electroforming which results in reduced power consumption and nonlinearity in the current-voltage characteristics even with the use of a select device or other nonlinear element. This increased nonlinearity in the ON state may help achieve high density crossbar implementations for resistive memory with a facile and inexpensive approach.

ACKNOWLEDGMENT

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