SAND2015-6771C

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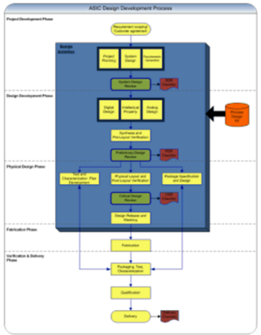

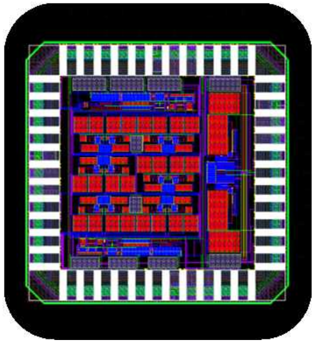

An overview of the Ultra-Fast X-ray Imager (UXI) program at Sandia Labs

L. Claus, L. Fang, R. Kay, M. Kimmel, J. Long, G. Robertson, M. Sanchez, J. Stahoviak, D. Trotter, J.L. Porter

8/13/2015

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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Hybrid CMOS Camera System Motivation

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Currently On NIF, Z, OMEGA ➡ Image Plate & Film

<u>Image Plate Disadvantages</u>

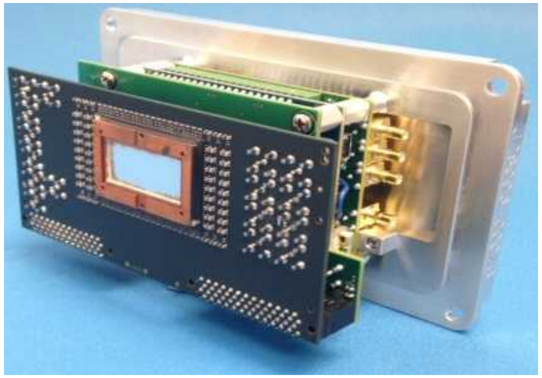
- MCP front end required to time gate
- Multiple shots required to perform a time scan
- Measurement at a single point in time
- Expensive to process
- Issue with experimental reproducibility

Image Plate Replacement

Potential Future For All Facilities ➡ Hybrid CMOS (hCMOS) Imager

<u>Potential Hybrid CMOS Capabilities</u>

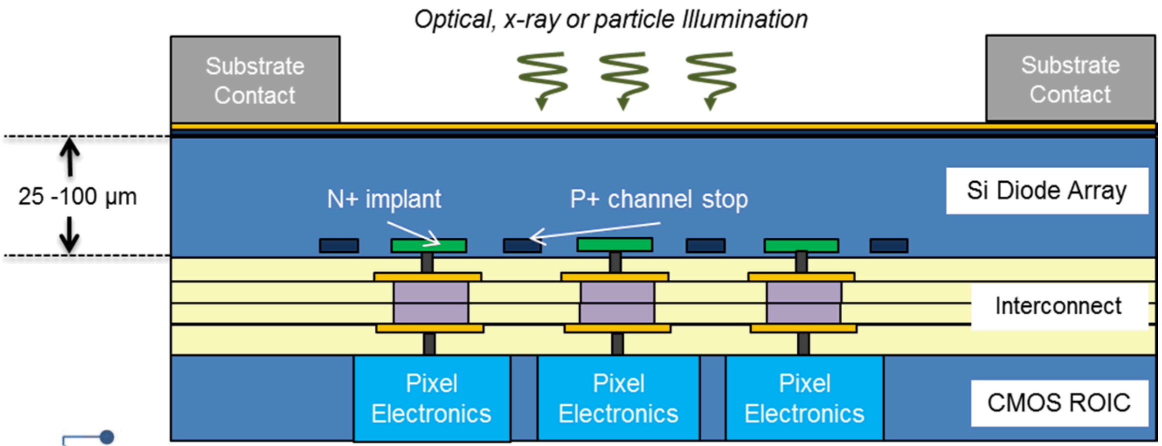
- Large detector area
- Multiple frames
- 1 ns integration time possible
- Multiple detector options for various energy spectra of interest



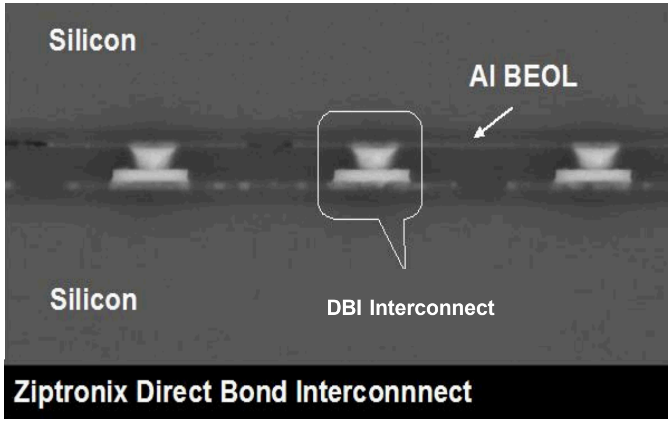
A hCMOS image sensor can, with X-ray source development, eliminate the need for multiple shots by capturing multiple images at user defined times within one shot

Photodiode and Hybridization

- Photodiodes can be optimized for sensitivity to relevant spectrum of interest (visible light, x-rays, electrons)
- Existing Si photodetector arrays are fabricated at SNL
- ROIC stores charge from each photodiode on in-pixel capacitors during selected integration time for each frame
- Each pixel of the photodiode array is directly connected to CMOS ROIC through wafer-to-wafer bonding (Ziptronix 3D oxide-to-oxide bond process)
- A hybrid sensor enables independent optimization of the diode array & the readout electronics (ROIC)



CMOS Hybrid Image Sensor



DBI Hybridization

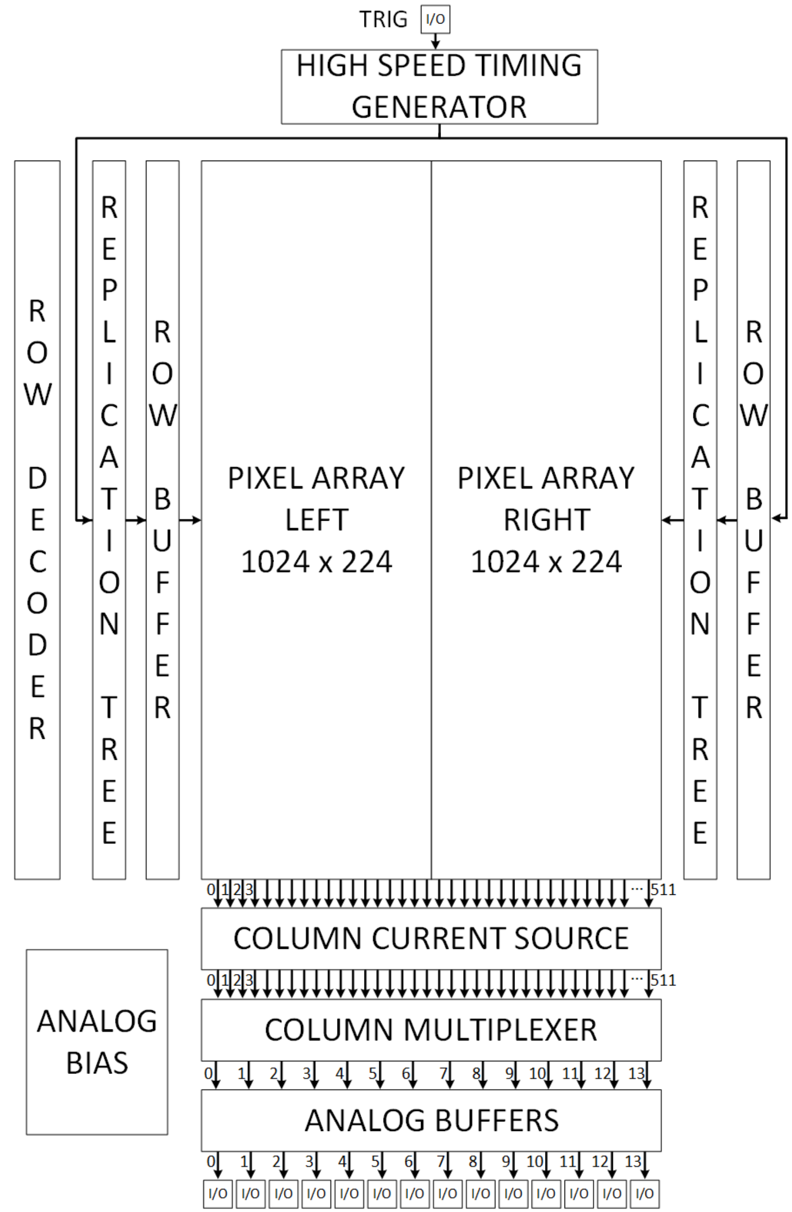
UXI Programmatic Goals

- High spatial resolution (25 µm or better)
- High speed shutters (1 ns or better)
- Many frames (8 or more frames)
- High sensitivity to visible light and single keV X-rays (~100% fill-factor)
- Large dynamic range (1000:1 or better)
- Large format sensor (multi-cm scale)
- High timing precision (50 ps or better)
- Low trigger insertion delay (few 10's ns)
- Compact, rugged, and easy to integrate into diagnostic systems and experiments
- Radiation tolerant to operate in High Energy Density Physics facilities

Mixed Signal ASIC/SoC

Furi Design Goals

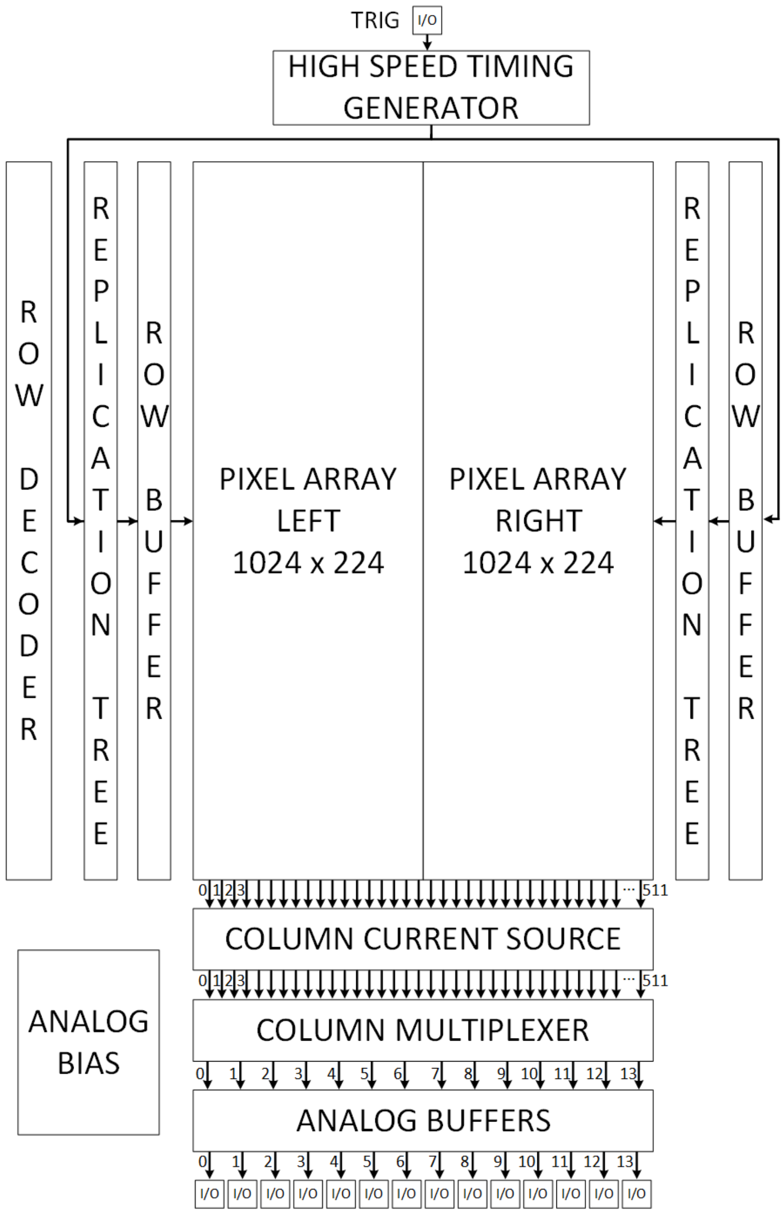
- SNL 0.35 µm rad hard SOI technology node
- 2 frame, 25 µm pixel array
- Integration time goal < 2 ns
- Inter-frame target < 2ns
- 1024 x 448 pixel array
- 25.6 mm x 11.2 mm detector area
- 60 dB (1000:1) Dynamic Range
- Single photon (6 keV) sensitive (1600 e-)
- 1.6 million e- full well
- External, asynchronous trigger initiated
- User configurable shutter and inter-frame times



Mixed Signal ASIC/SoC

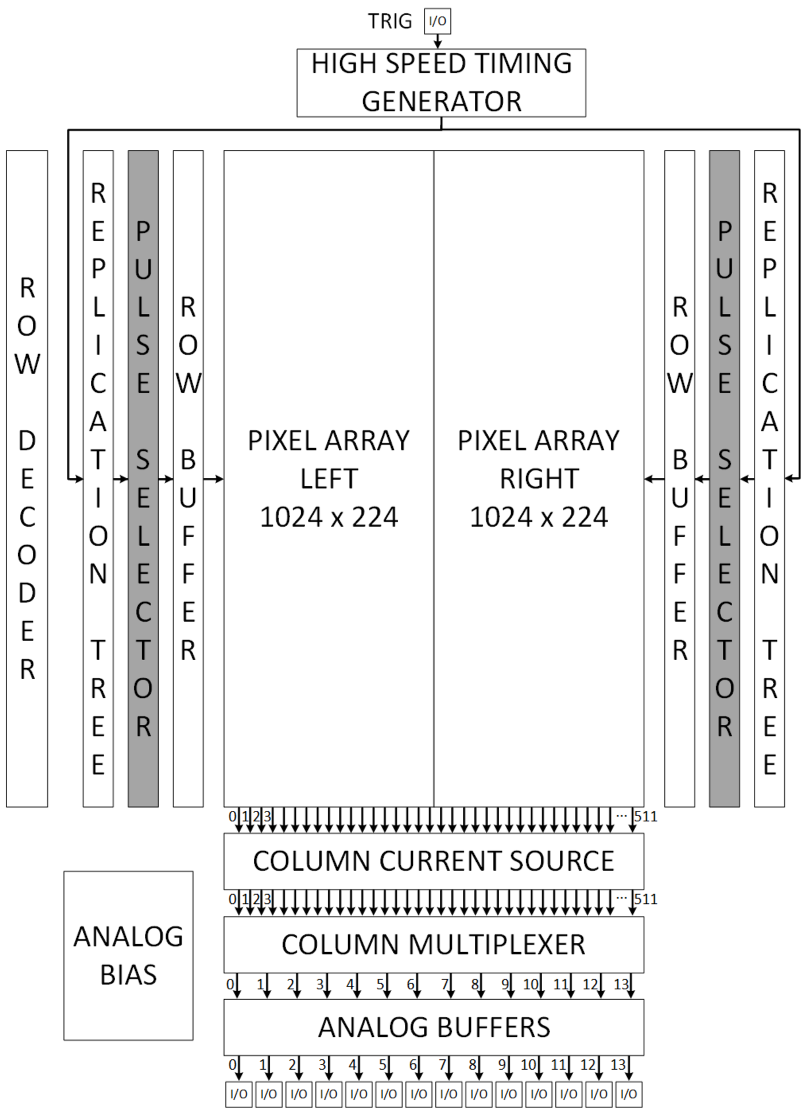
Furi Architecture

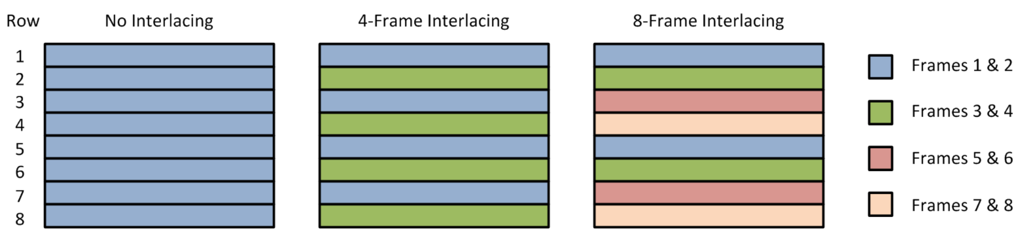
- External asynchronous trigger initiates high speed timing generator to produce the user configured shutter and inter-frame time pulses
- High speed shutter pulses are propagated from HSTGen to the pixel array through identical timing paths via a binary replication tree on both left and right hemispheres
- 2 frames of image data are stored in-situ on the pixel array and read off post experiment to external ADCs



Hippogriff Architecture

- Virtually identical to Furi with the exception of a Pulse Selector block inserted between replication tree and pixel row buffer
  - This enables row-wise interlacing so the user can trade spatial resolution for additional frames of temporal data





# Frames	Frame Resolution
2	1024 x 448
4	512 x 448
8	256 x 448

Packaging and System

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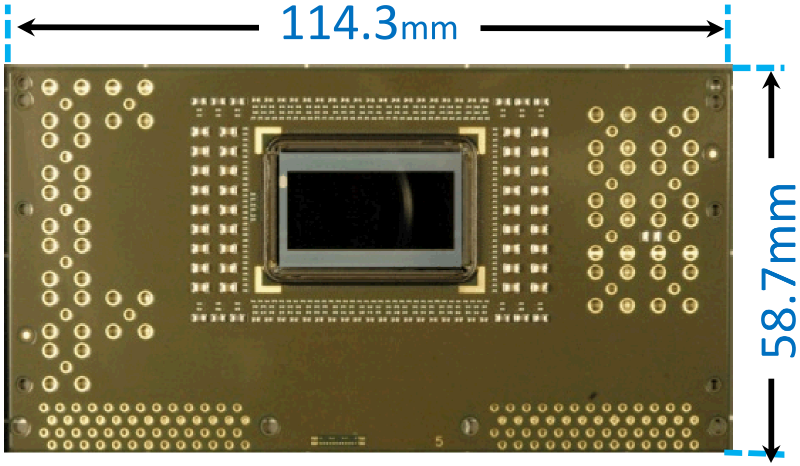
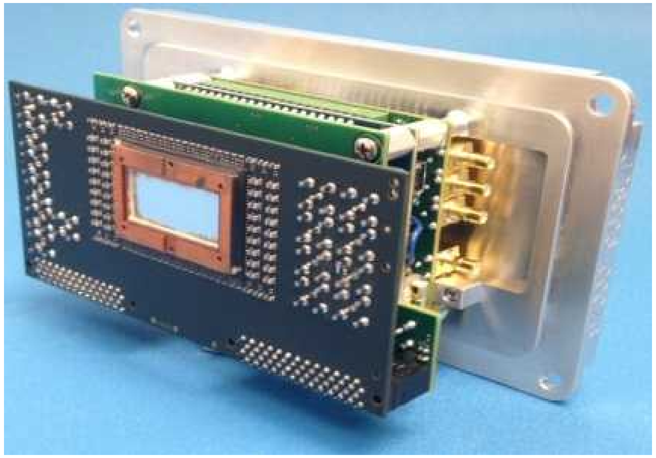
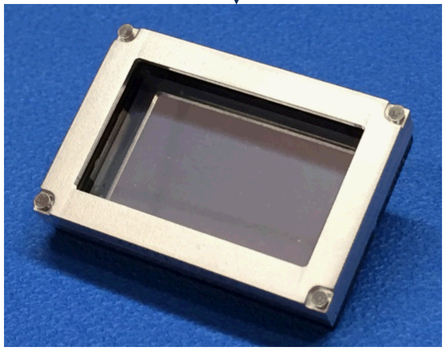


FURI Prototype Package

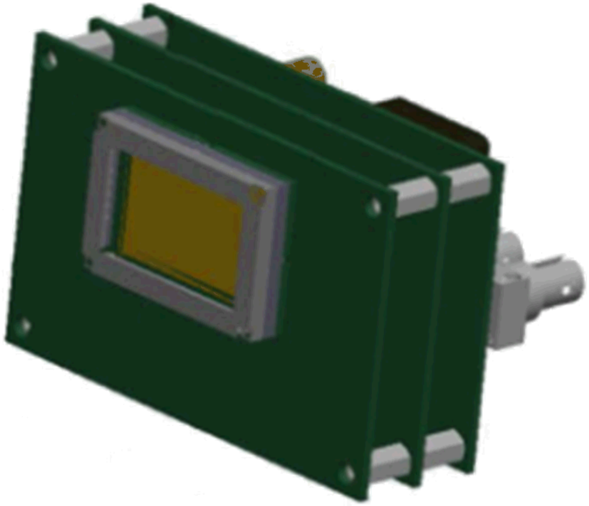


FURI Prototype Camera System

2nd Gen



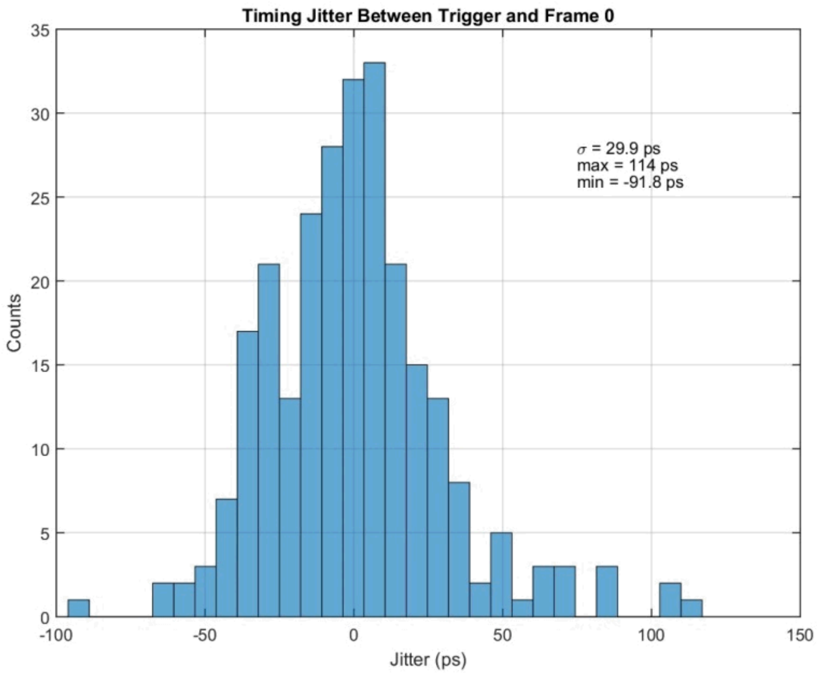
SOP Package



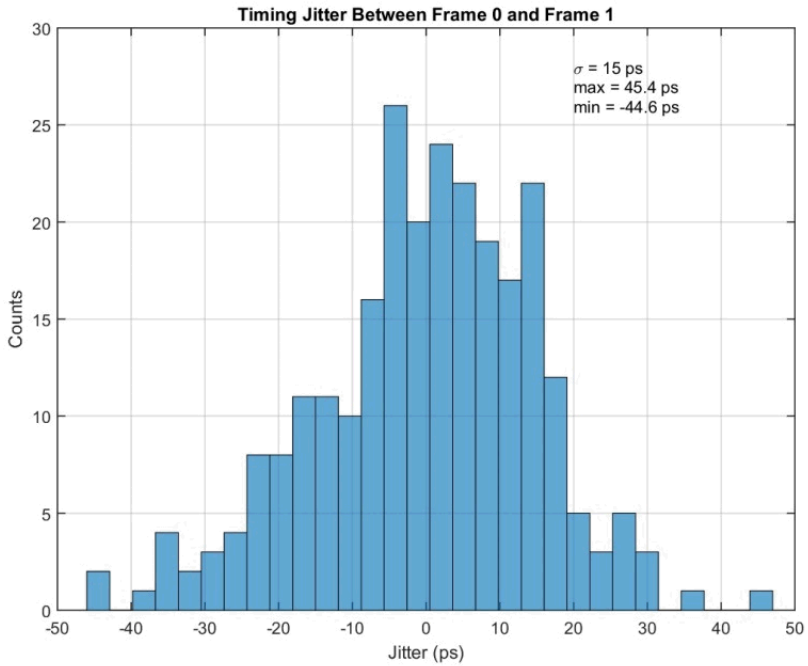
SOP Camera System-In Fabrication

Electrical Test Results-Timing

- Timing jitter tests



Measured jitter from external trigger to first frame shutter output from high speed timing generator = 30 ps rms



Measured jitter between shutters = 15 ps rms

Mixed Signal ASIC/SoC

Electrical Test Results-Timing

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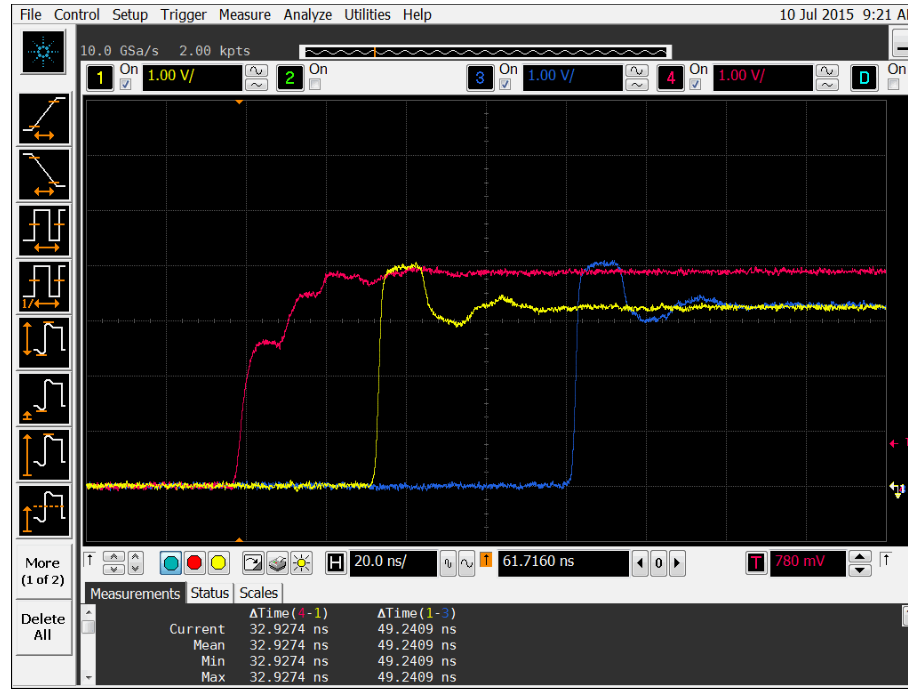
- Insertion delay tests



Insertion delay from external trigger (red) to output of shutter pulses (Frame 0 = yellow, Frame 1 = blue) Timing configured for 10 ns on, 10 ns inter-frame time. Delay from high speed timing generator to first shutter pulse = 34 ns

Delay from external trigger (red) to frame 0 output from high speed timing generator (yellow) and frame 0 output from row buffer (blue). Total propagation delay = 83ns

Electrical Test Results-Readout

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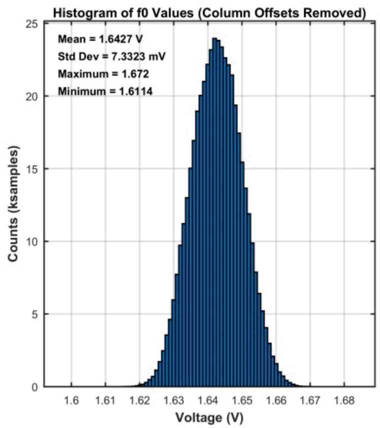
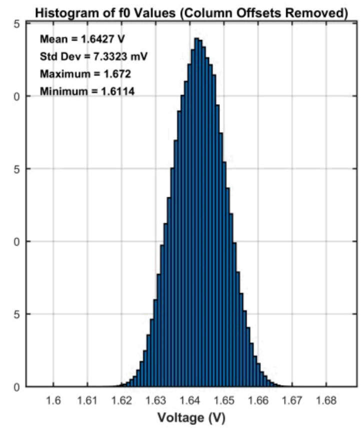
- Fixed Pattern Noise removal with electrical flat field

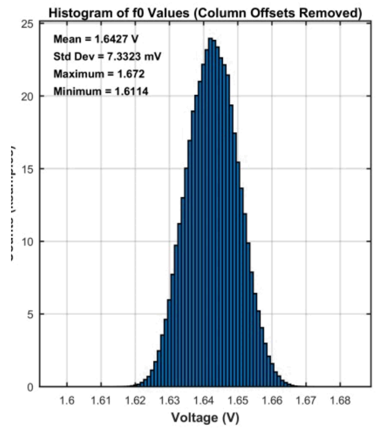
Frame 0



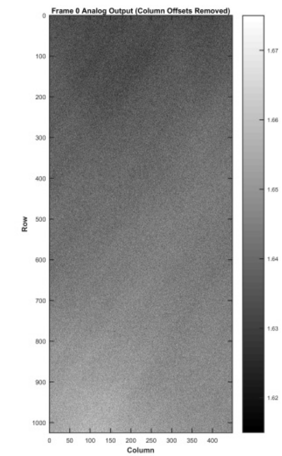
All FPN



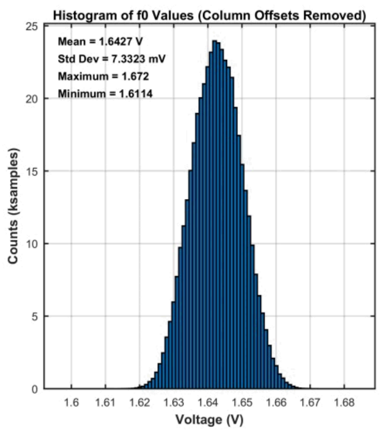
Analog Buffers Removed



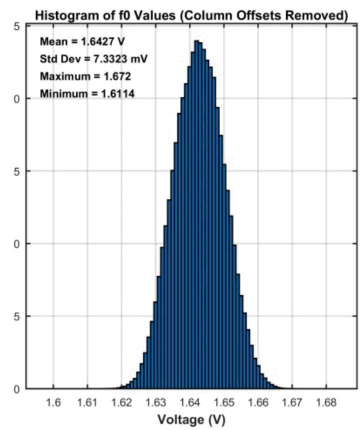
Columns Removed



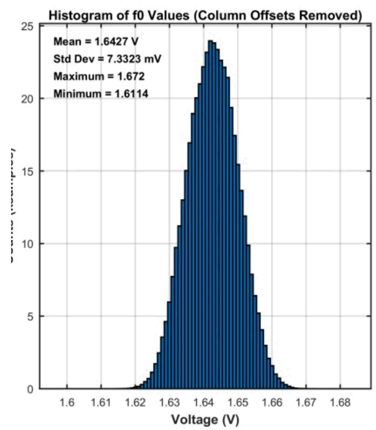
Frame 1



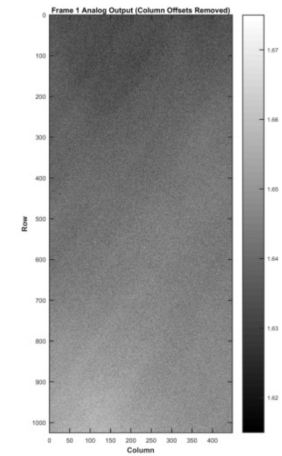
All FPN



Analog Buffers Removed



Columns Removed



Mixed Signal ASIC/SoC

Optical Test Setup

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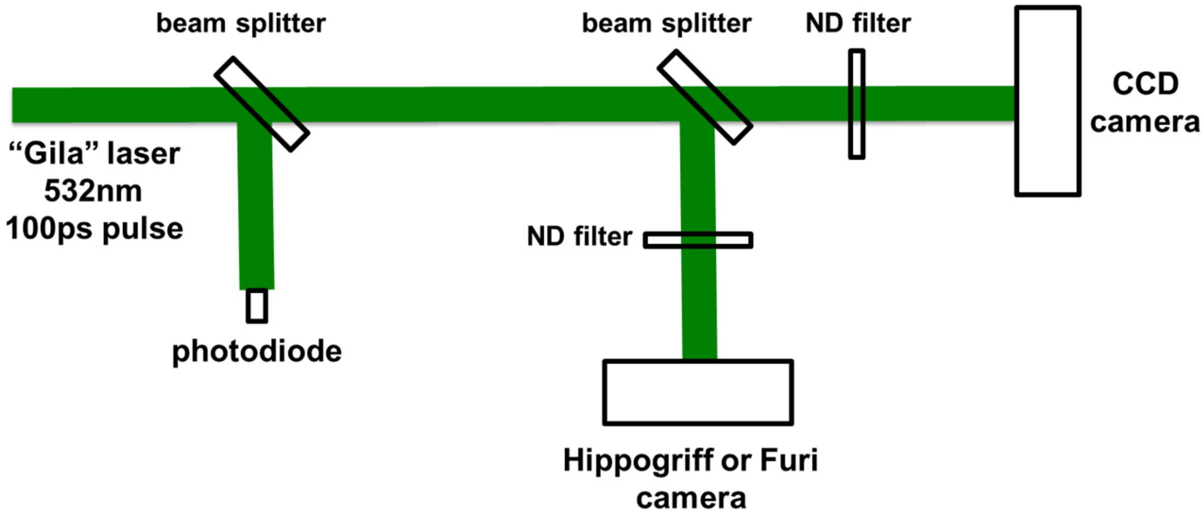
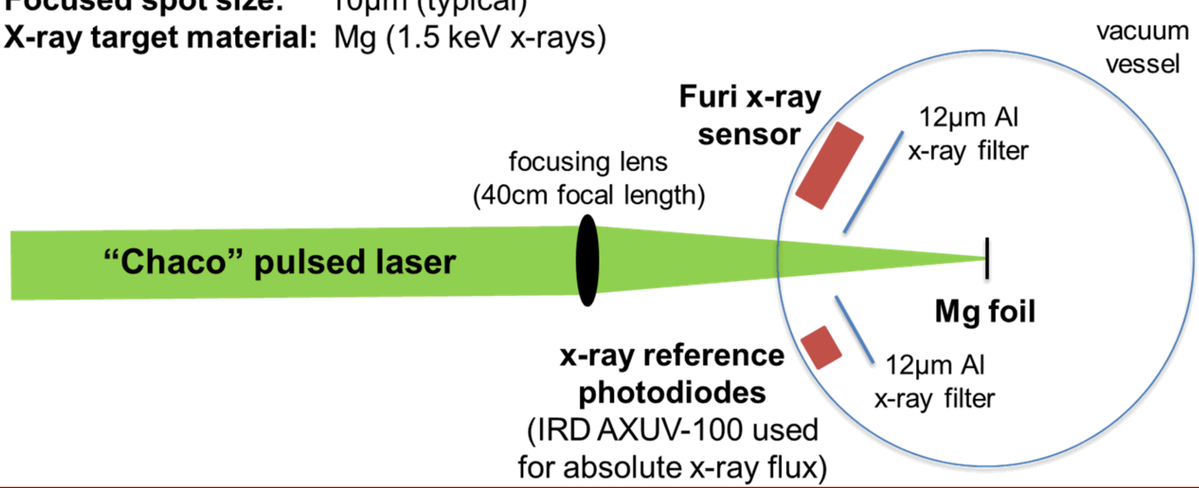
Visible test configuration: Produces 532 nm monochromatic light



Laser wavelength:	532 nm (frequency doubled)
Laser energy:	1J at 2ω (typical)
Laser beam dia.:	50 mm
Pulse duration:	0.2ns
Focused spot size:	10μm (typical)
X-ray target material:	Mg (1.5 keV x-rays)

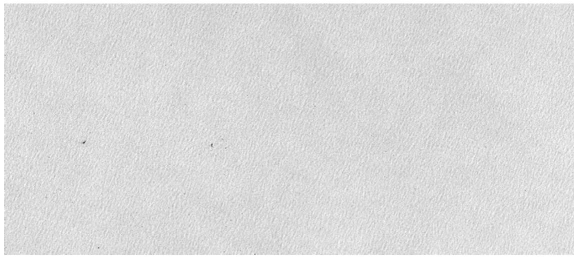
X-ray test configuration: Produces 1.5 keV X-rays



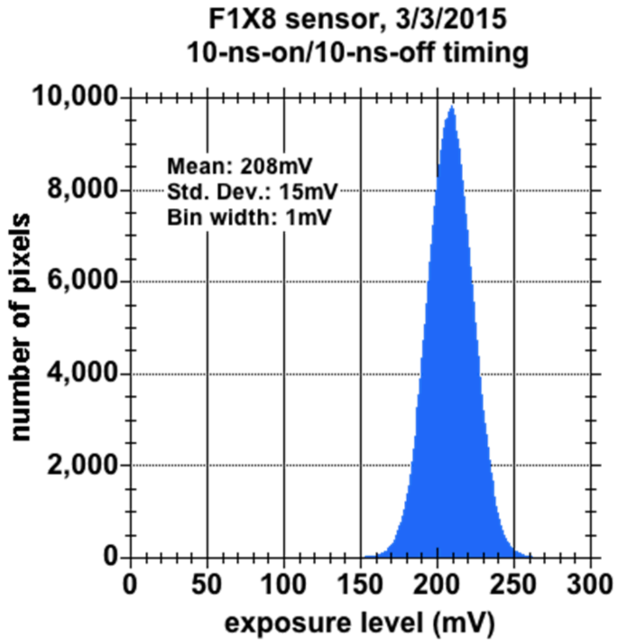
Furi X-ray flat field measurements

Sandia National Laboratories

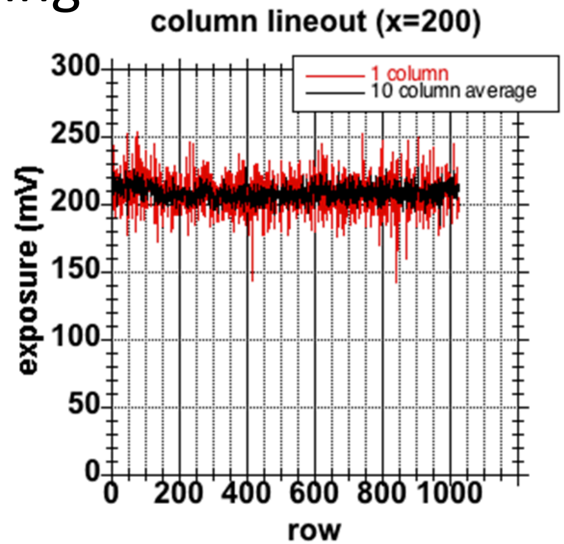
- 1.5 keV X-ray fluence, 10ns shutter timing

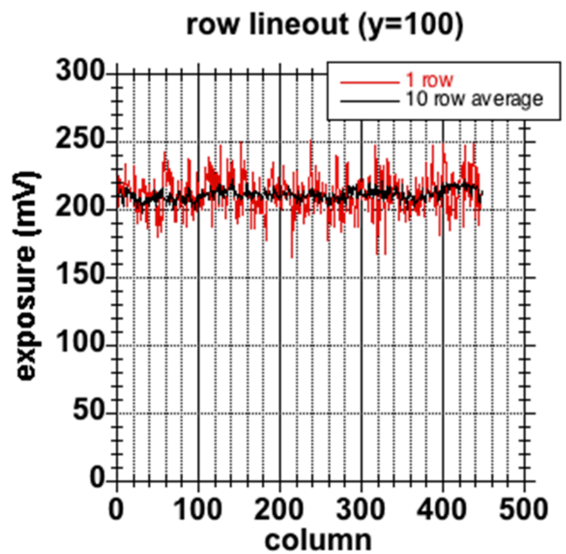


208 mV average exposure, ~500 photons/pixel



Histogram of flat fielded pixels





Mixed Signal ASIC/SoC

X-ray spatial resolution/DR measurements

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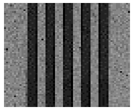
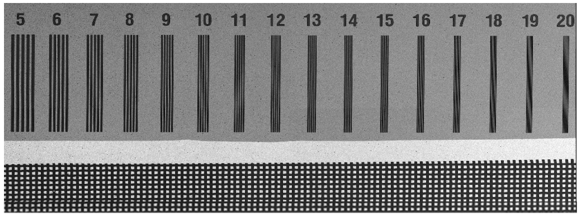
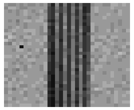
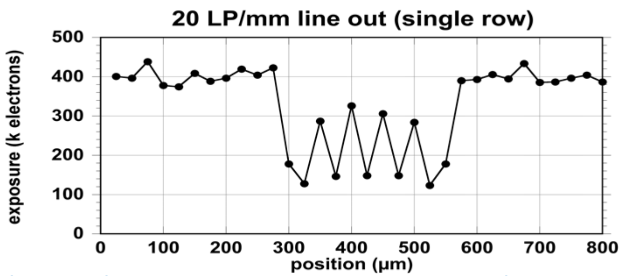


5 LP/mm
64 x 64
pixels

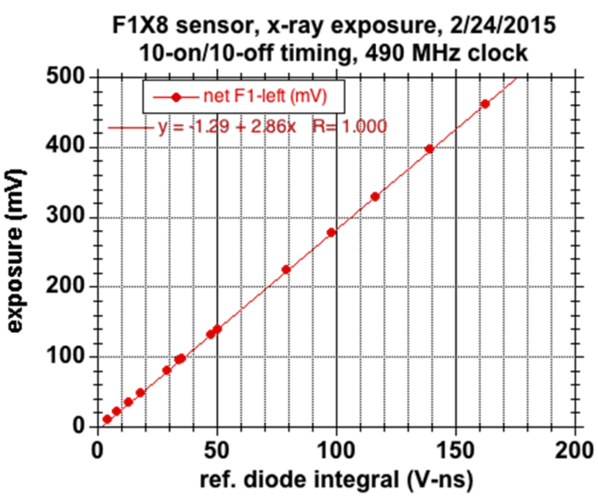




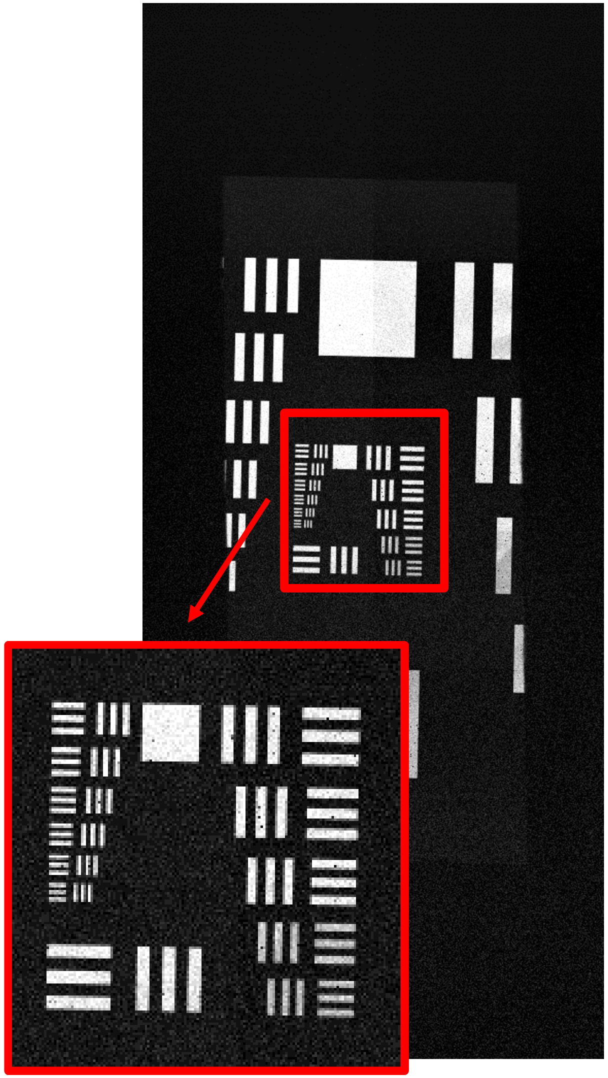
20 LP/mm
32 x 32
pixels



Line Pair X-Ray Test Pattern: 2 ns integration time



Dynamic Range Sweep: 10 ns integration time



Air Force Test Pattern: 2 ns integration time

Mixed Signal
ASIC/SoC

Spatial analysis for 1 ns-on/1 ns-off timing, visible illumination

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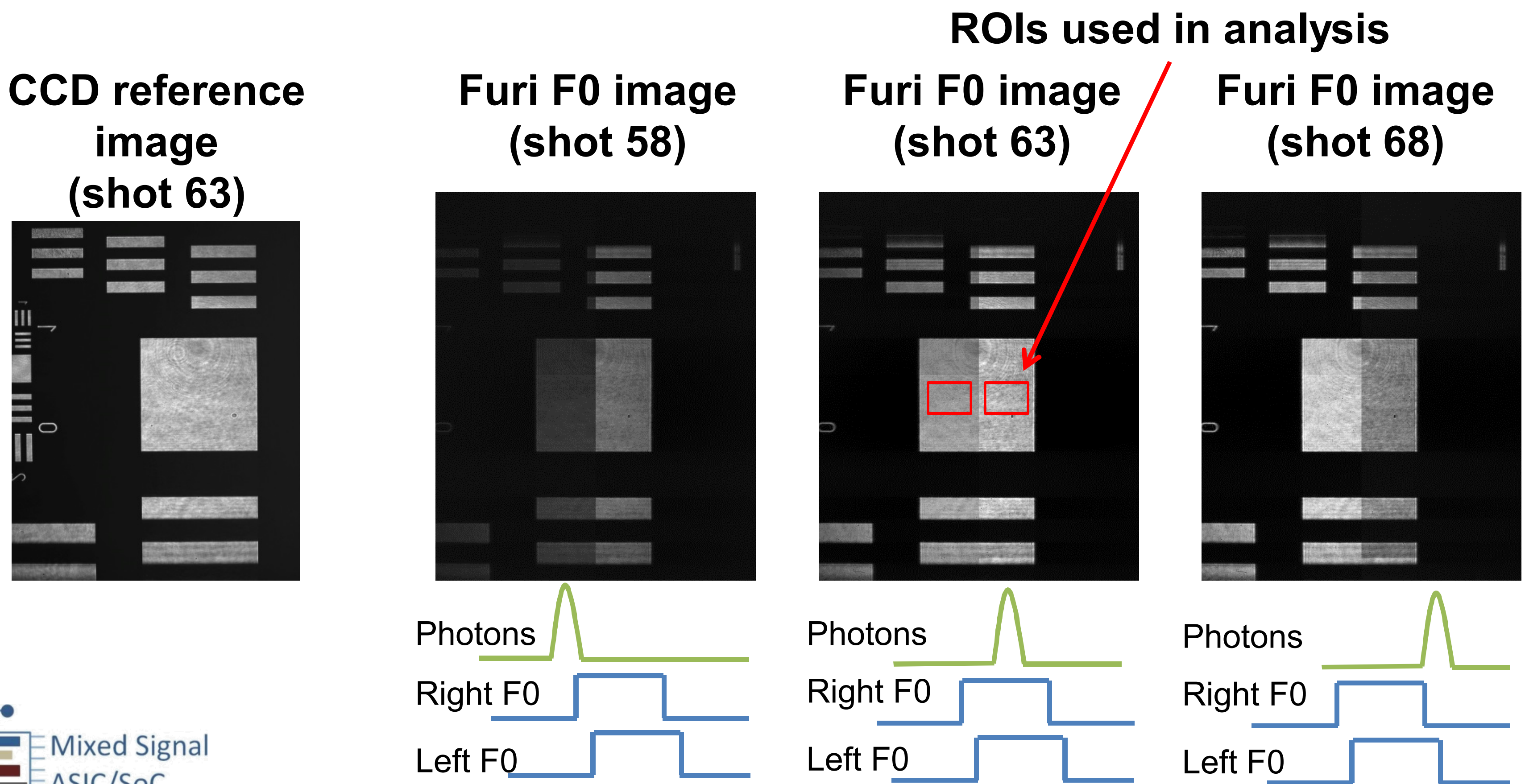
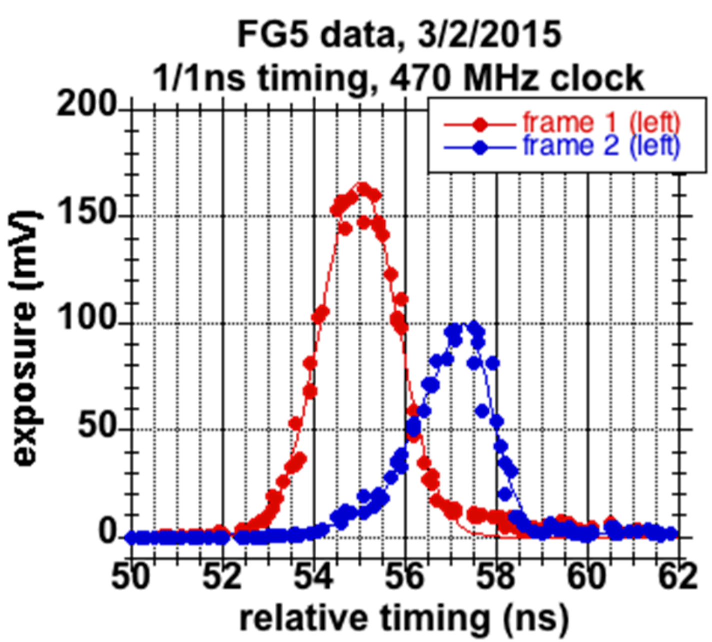
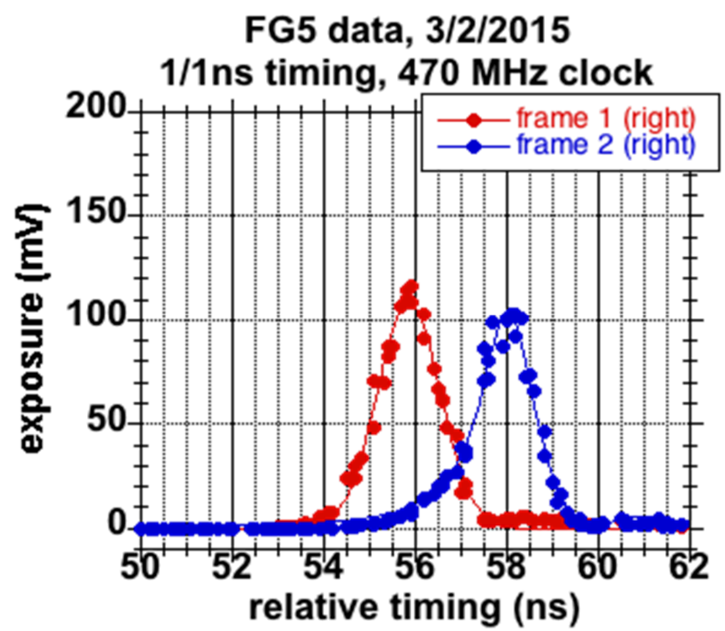
- Swept the optical pulse through the shutter window in 100 ps time steps
- Observed a fixed hemispheric skew from left to right



Temporal analysis for 1 ns-on/1 ns-off timing, visible illumination

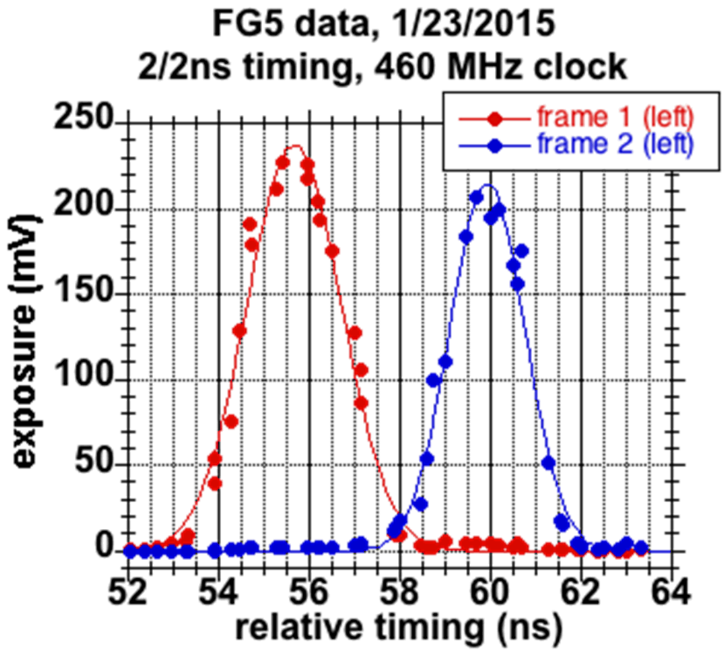


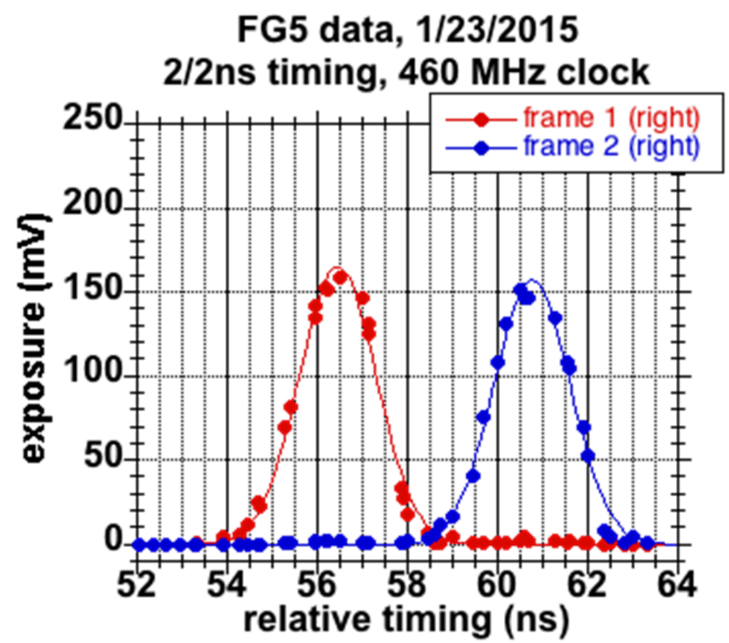
	FWHM (ns)	Frame Δt (ns)	left/right Δt (ns)
frame 1	2.0		0.9
frame 2	1.9	2.3	0.8



	FWHM (ns)	Frame Δt (ns)	left/right Δt (ns)
frame 1	1.6		0.9
frame 2	1.6	2.1	0.8

Temporal analysis for 2 ns-on/2 ns-off timing, visible illumination



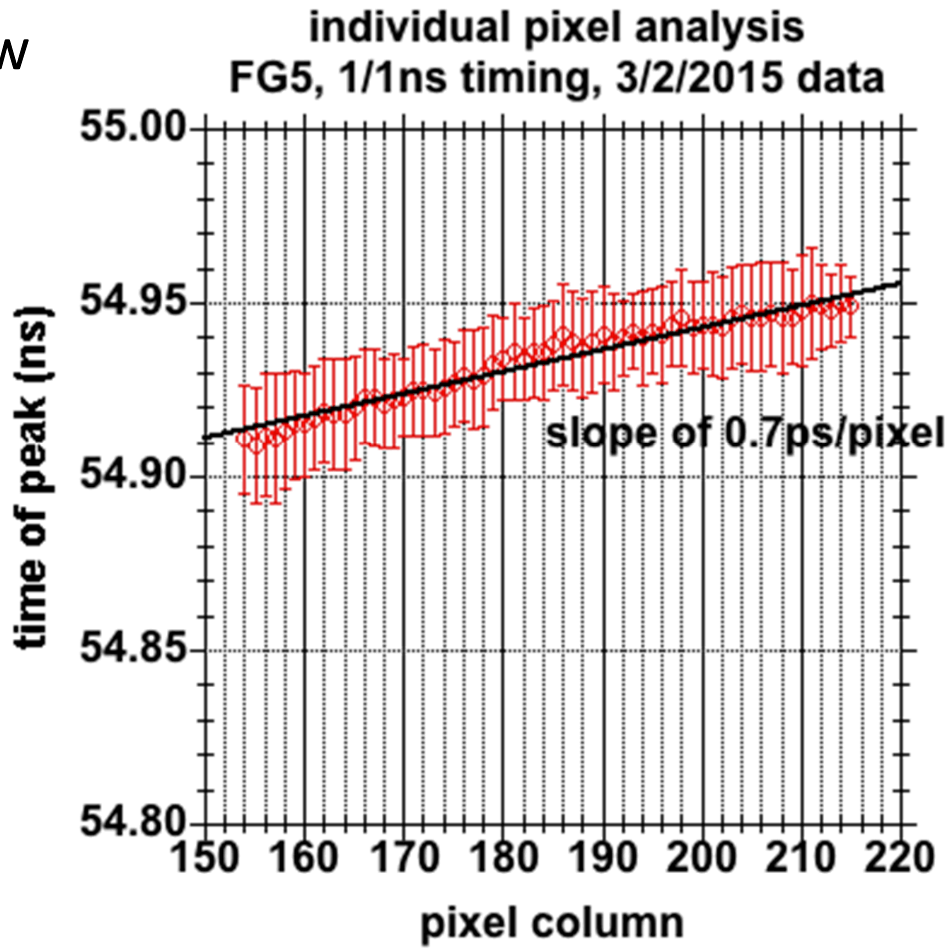


	FWHM (ns)	Frame Δt (ns)	left/right Δt (ns)
frame 1	2.4		0.8
frame 2	1.9	4.2	0.9

	FWHM (ns)	Frame Δt (ns)	left/right Δt (ns)
frame 1	2.0		0.9
frame 2	2.0	4.3	0.8

Timing distribution "skew" for 1ns-on/1ns-off timing, visible illumination

- Expected timing skew across the array due to RC of pixel row
- Simulated to be ~1ps/pixel



Dynamic Optical Results (X-ray and Visible)

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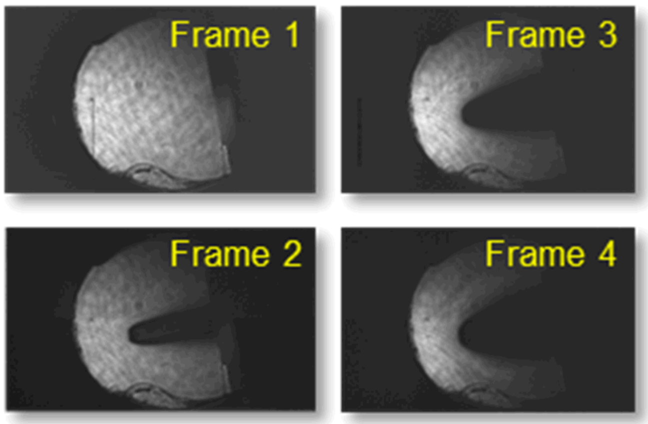
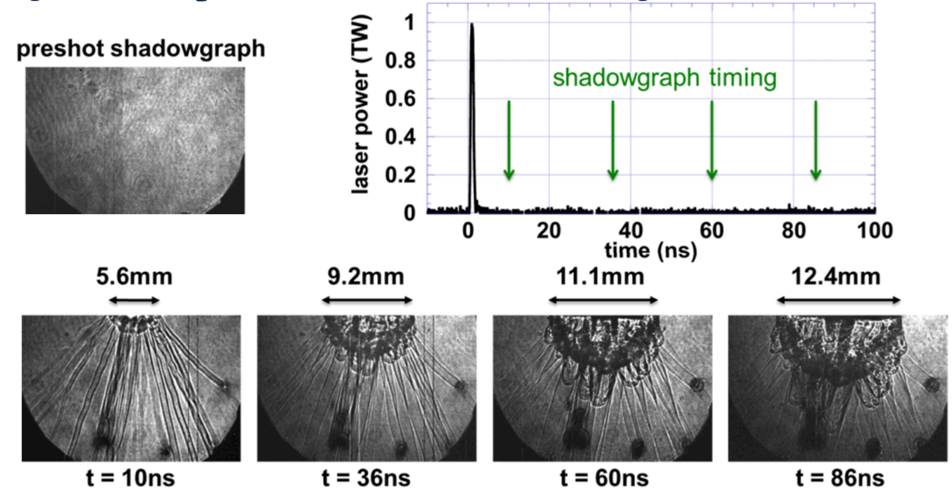
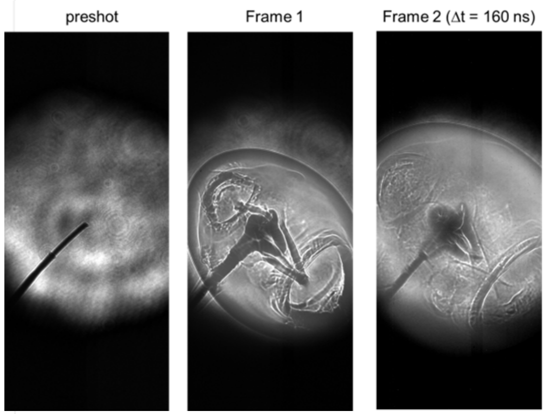


Hippogriff, 4 ns timing, x nm (kev) illumination

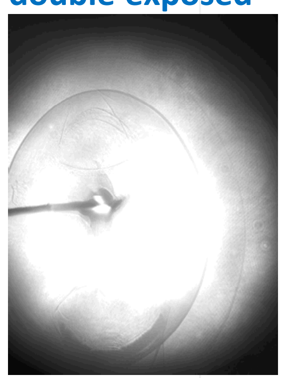


2 Furi cameras, x ns timing, 532 nm illumination

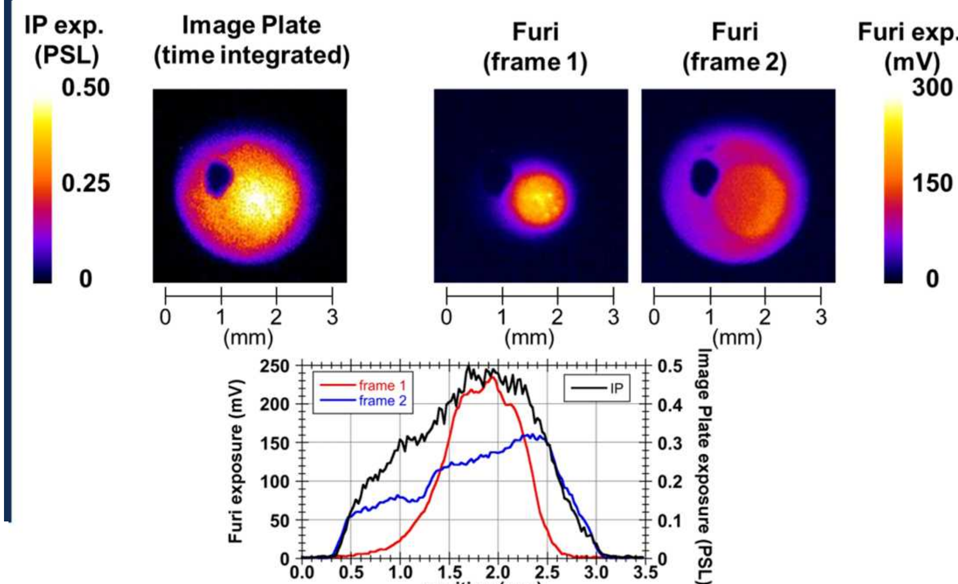
Furi Sensor



Commercial CCD, double exposed



Furi, 10 ns integration, 150 ns inter-frame, 532 nm illumination



Furi, 9ns integration, 1ns inter-frame, X-ray illumination

Conclusion and Team

Sandia National Laboratories

- Team Members also?

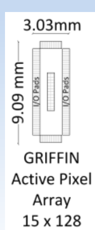
Spec	Goal	Furi
Spatial Resolution	25 um	25 um
High Speed Shutters	< 1ns	1.5-2 ns
Many Frames	> 8	2 (8 with Hippogriff)
Sensitivity	Visible and 6 keV X-ray	Yes
Dynamic Range	60 dB	Yes
Large Sensor Area	cm scale	2.56 cm x 1.12 cm
Timing Precision	50 ps	900 ps
Trigger Delay	10's of ns	83 ns
Camera Physical Size	Small	Reasonable (2^{nd} gen SOP)
Radiation Tolerance	Survive Z-shot	In progress but confident

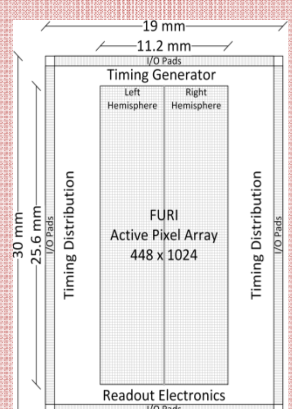
Mixed Signal ASIC/SoC

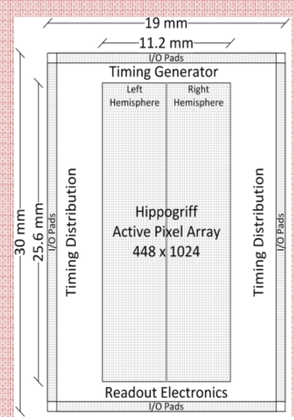
ROIC Timeline

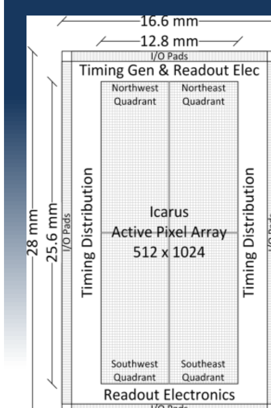
Sandia National Laboratories

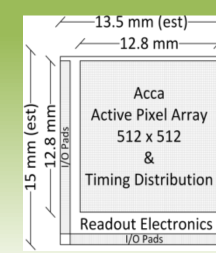
	Griffin	Furi	Hippogriff	Icarus	Acca
Year	FY13	FY14	FY15	FY16	FY17
Min. Gate Time		1.5ns			
Pixels		448 x 1024			
Frames		2	2 ,4, or 8 (interlaced)		
Sensor Types		500-900nm, 0.7-6keV			
Tiling Option		No			
CMOS Process		350nm			
Status		pleted	Packaging & Characterization		











Mixed Signa
ASIC/SoC