SAND2013-9364C

A CMOS Compatible, Forming Free TaOx ReRAM

Electrochemical Socity Fall Meeting

San Francisco, CA

October 31, 2013

Matthew J. Marinella*, Andrew J. Lohn, James E. Stevens, Patrick R. Mickel, David R. Hughart

Sandia National Laboratories

***matthew.marinella@sandia.gov**

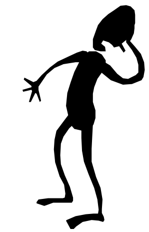
Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Emerging Memory

- This is a great era for emerging memory
- <u>NAND Scaling is visibly slowing</u>
  - Memory manufacturers refusing to name nodes by physical dimensions (now we have 2x and 1x nodes)
  - 20 nm retention is horrible, endurance is suffering
- <u>DRAM scaling is also becoming a problem</u>
  - struggling to maintain reasonable equivalent oxide thickness
  - Dielectric for cells 30nm to 20 nm still TBD
- New memory technologies on the horizon are rapidly maturing which can replace NAND *and* DRAM
- These changes will occur within the next decade
- Companies beginning to sink serious money into memory R&D

Emerging Nonvolatile Memories

The infamous comparison chart***



Biggest challenge for ReRAM: Catch-up

	DRAM	Flash (NOR-NAND)	ReRAM/Memristor	STT-MRAM	PC-RAM
2013 Maturity	Production (30 nm)	Production (18 nm)	Development	Production (65 nm)	Production (45 nm)
Min device size (nm)	20	18	<10	16	<10
Density (F^2)	6	4	4	8-20	$4F^2$
Read Time (ns)	< 10	10^5	2	10	20
Write Time (ns)	< 10	10^6	2	13	50
Write Energy (pJ/bit)	0.005	100	<1	4	6
Endurance (W/E Cycles)	$>10^{16}$	10^4	10^{12}	10^{12}	$>10^9$
Retention	64 ms	> 10 y	> 10 y	weeks	> 10 y
BE Layers	FE	FE	4	10-12	4
Process complexity	High/FE	High/FE	Low/BE	High/BE	Low/BE

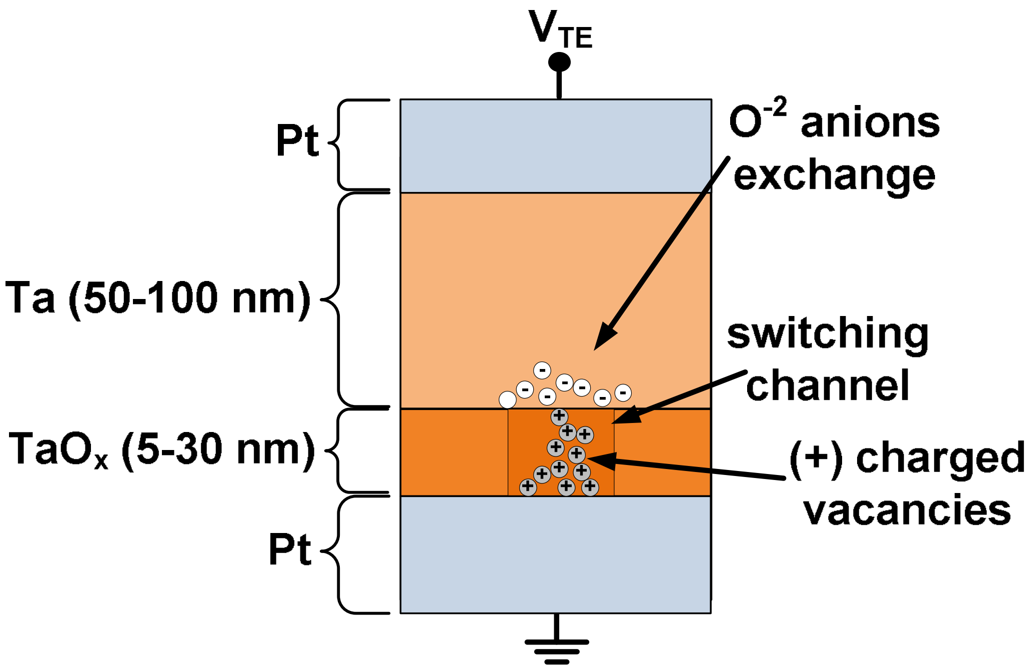
Biggest challenge for STT-MRAM: Balancing Retention/Scaling/Temperature/Write current

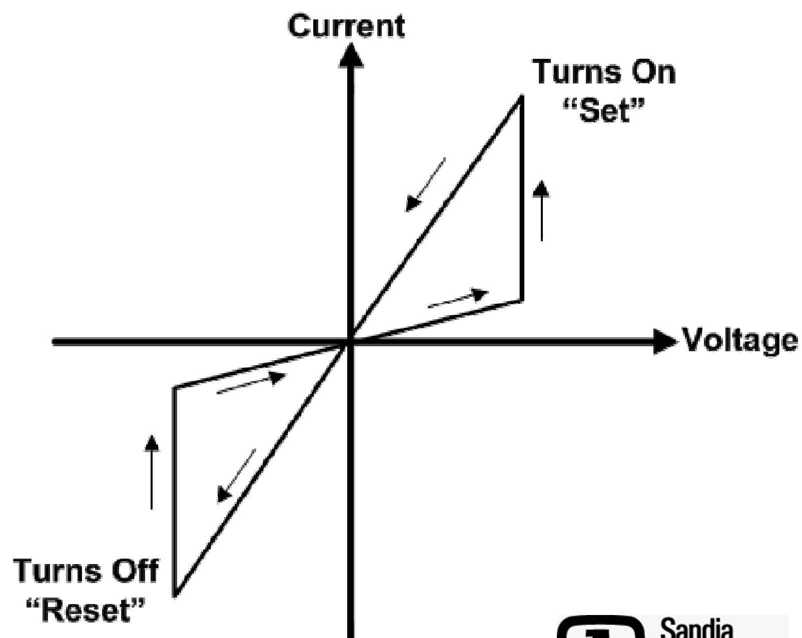
Biggest challenge for PCM: High erase current

*****DISCLAIMER: Due to 10s of thousands of references on these technologies – many of these numbers are not universally agreed on! We are updating this for the ITRS 2013 Edition ERD Chapter.**

Valence Change ReRAM

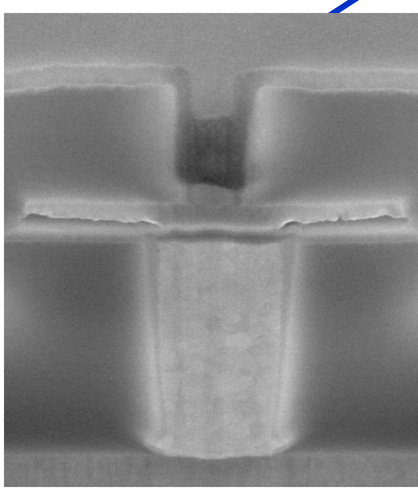
- "Hysteresis loop" is simple method to visualize operation
  - (real operation through positive and negative pulses)
- Resistance Change Effect (polarities depend on device):
  - Positive voltage/electric field: low R – O^{-2} anions leave oxide
  - Negative voltage/electric field: high R – O^{-2} anions return
- Common switching materials: TaO_x, HfO_x, TiO_2, ZnO

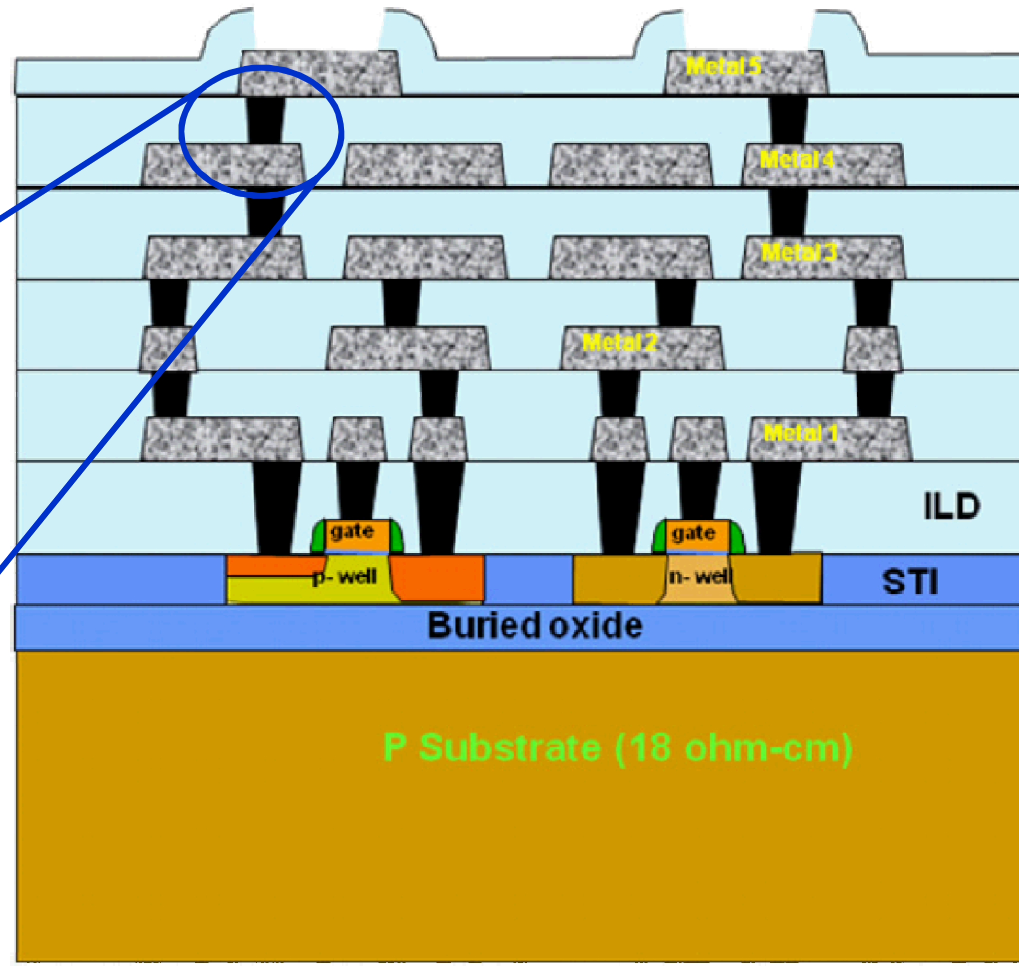




Memristors + CMOS

- Sandia CMOS7 Process
  - 3.3V, 350 nm, MOSFETs
  - Rad-hard
- Baseline for memristor integration



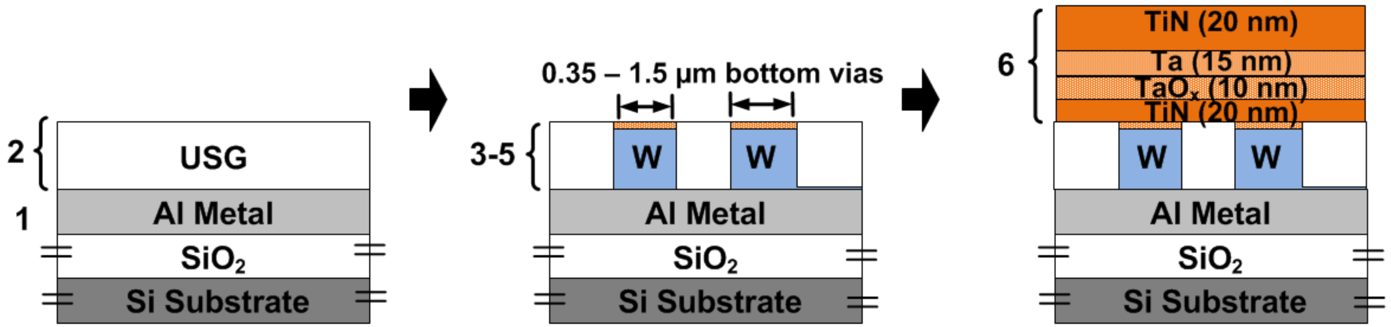


Process Flow

1. Deposit Bottom Metal (Al)
2. Deposit USG

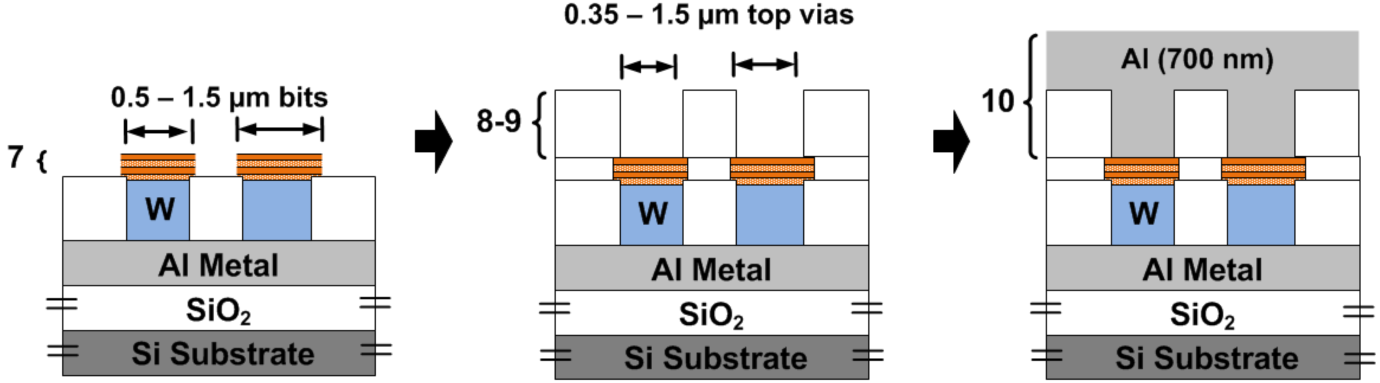
3. Etch via holes in USG
4. Deposit W and TiN layers
5. CMP

6. Deposit bit stack
(layers enlarged for clarity)

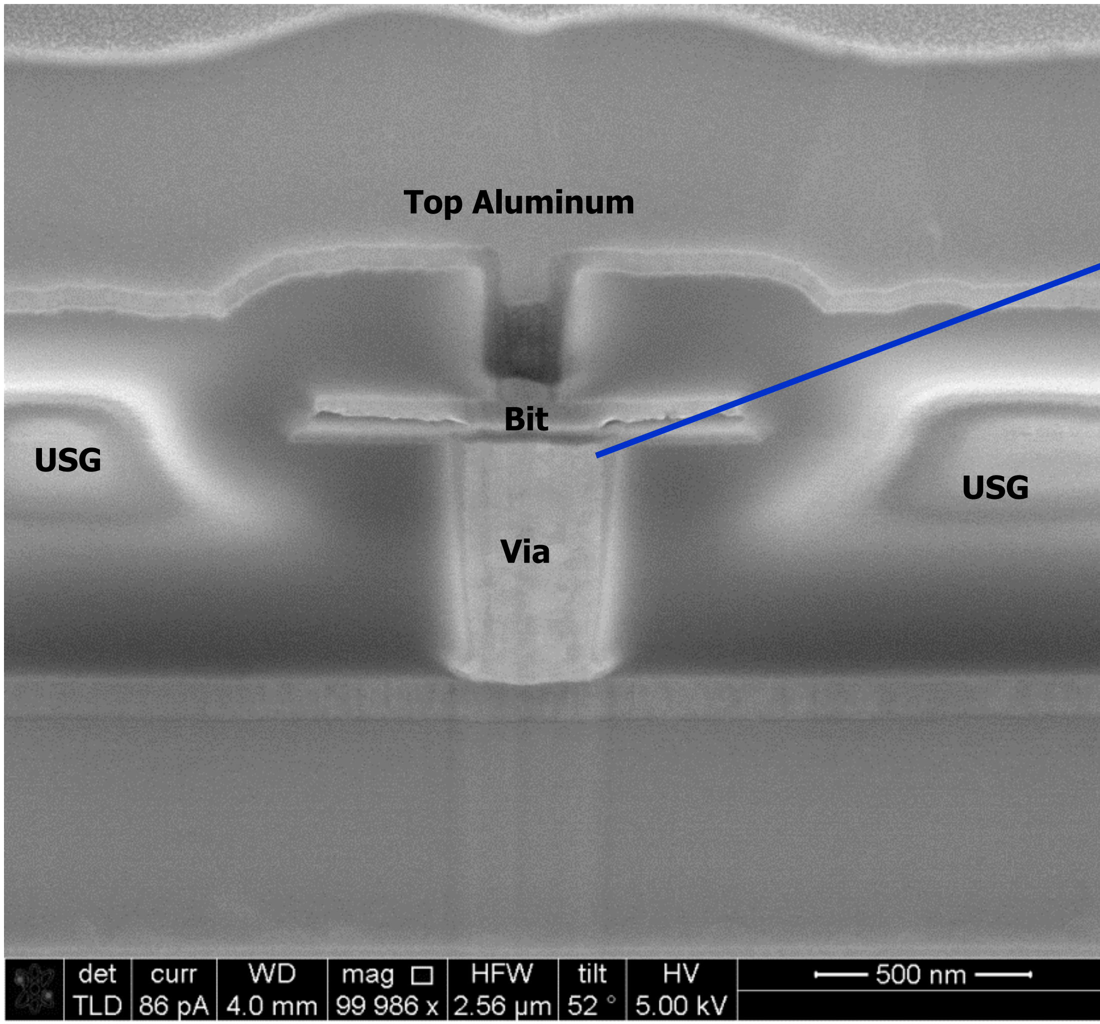


7. Etch bits

8. Deposit top USG
9. Etch top via holes in USG

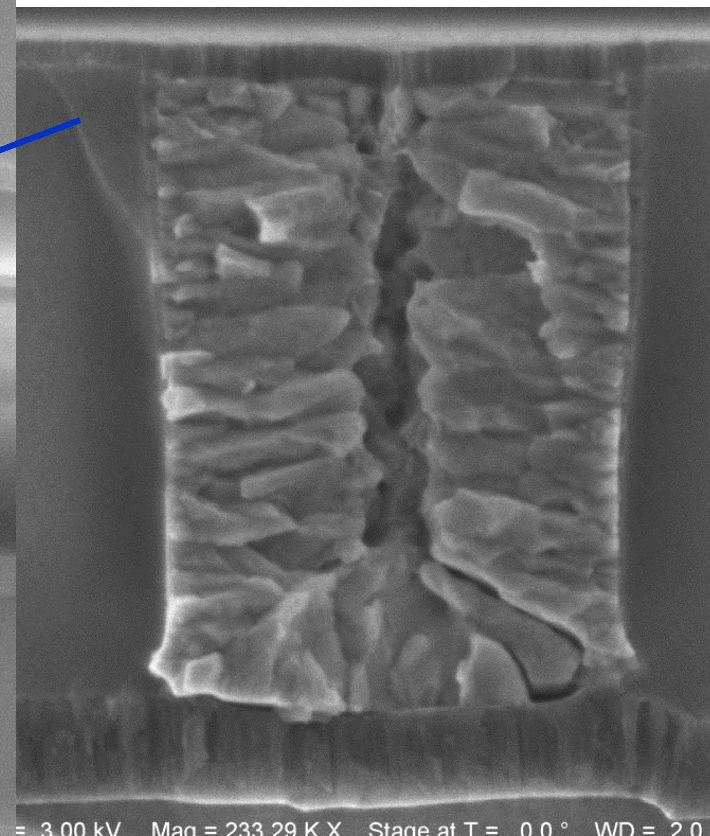


Final Structure

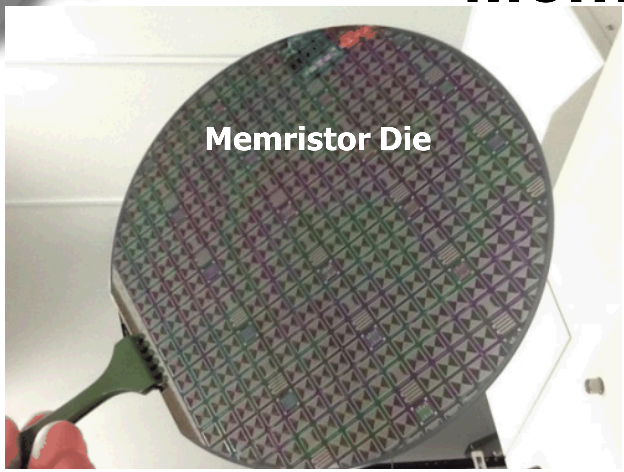


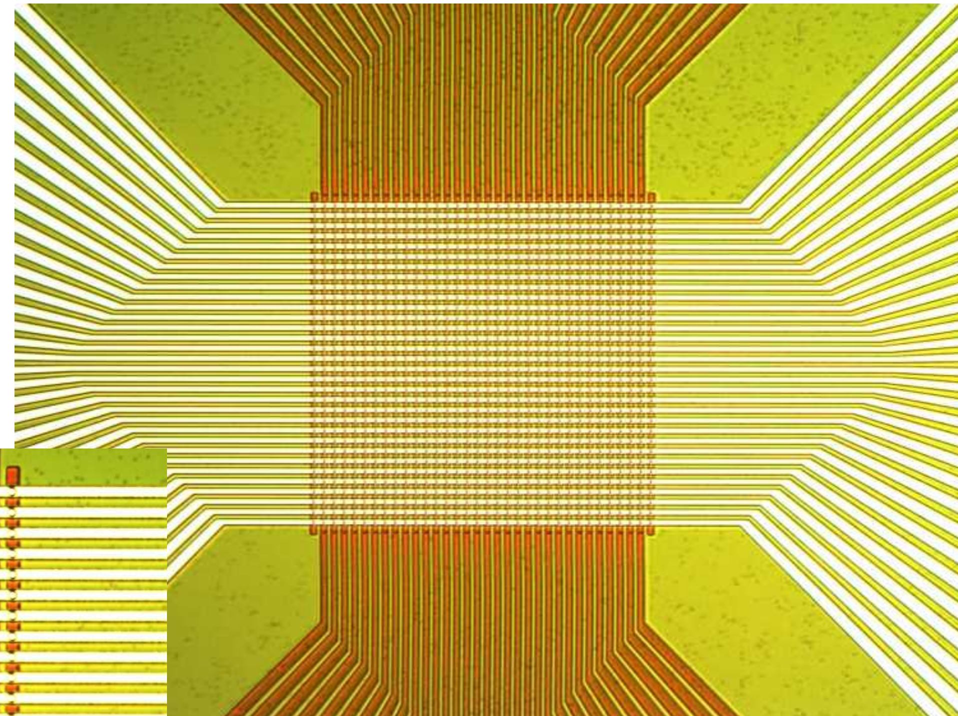
Important to have extremely flat surface under bit

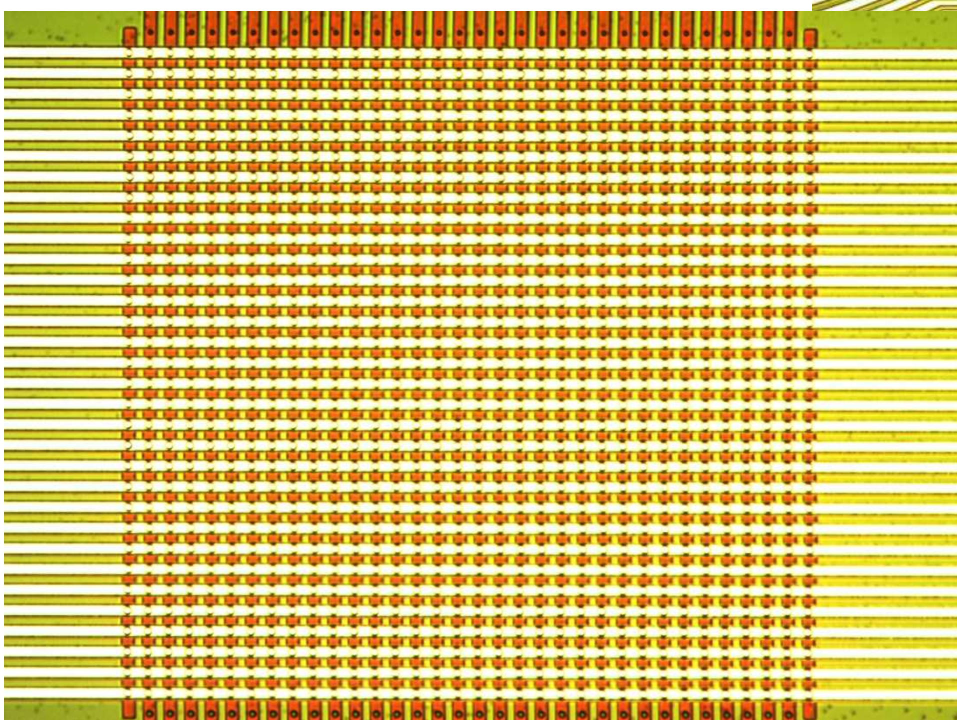
Polished TiN Surface



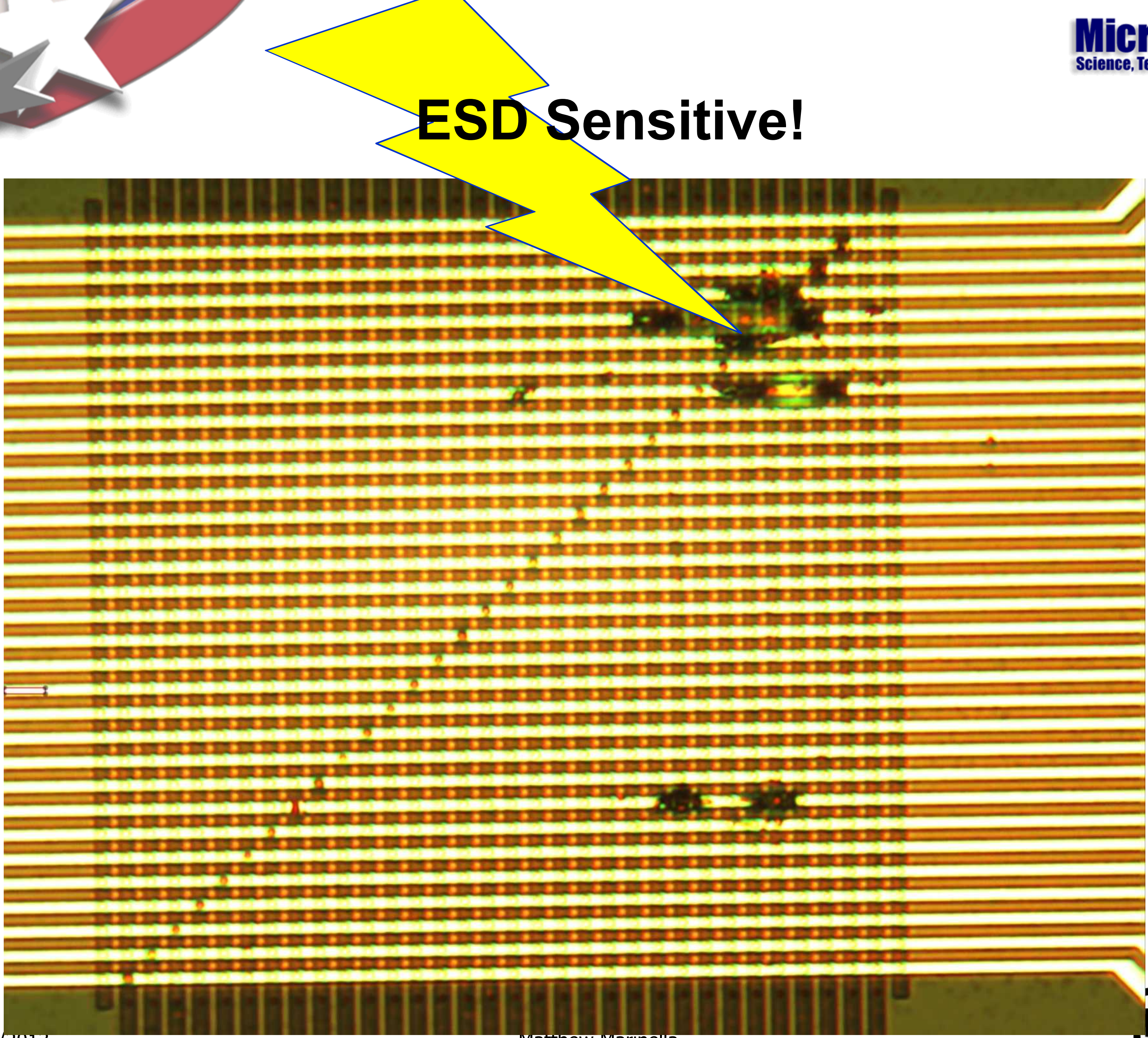
Memristor Crossbar Die



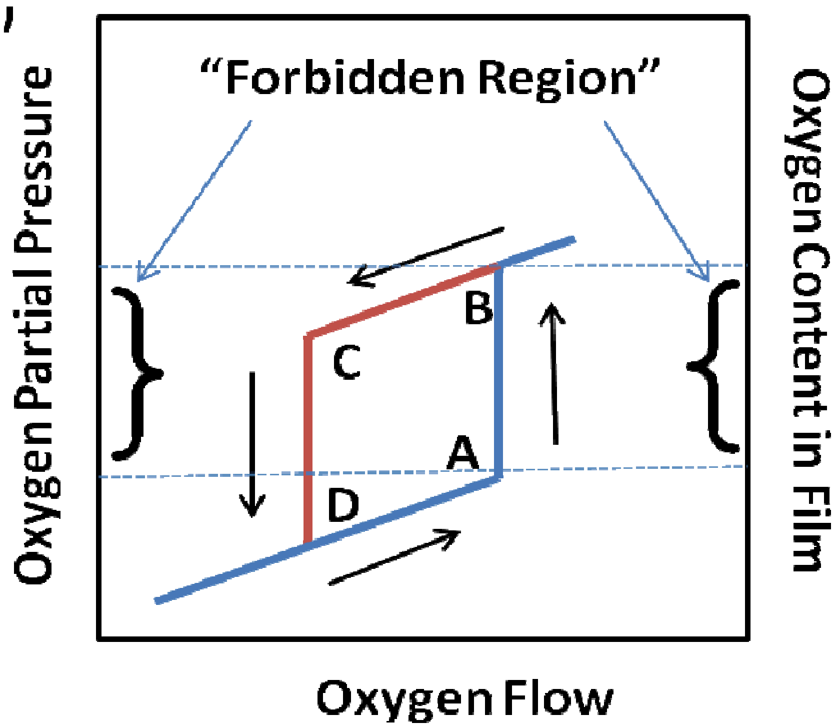




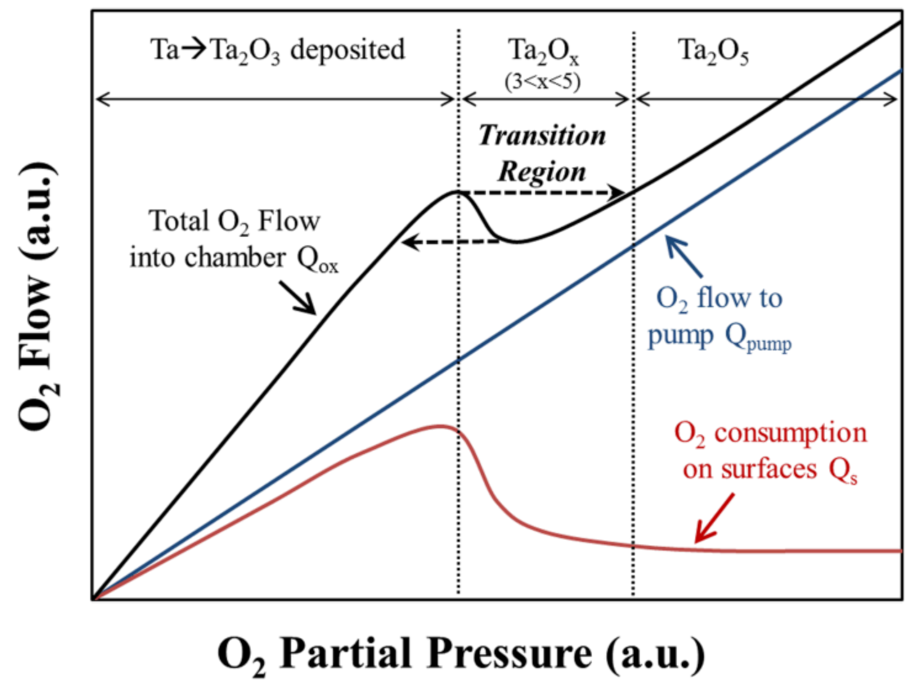
ESD Sensitive!



Film Development – "Forbidden Region"



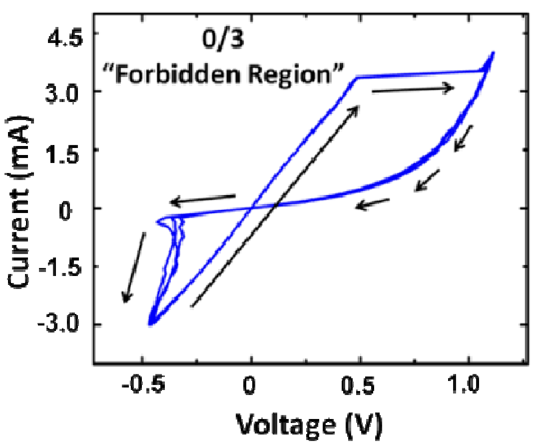
A.J. Lohn et al APL , 2013

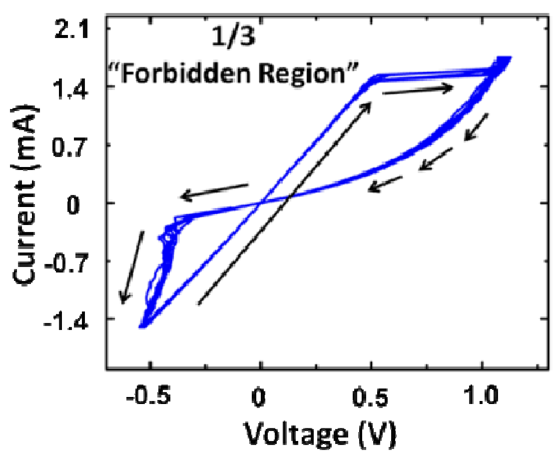


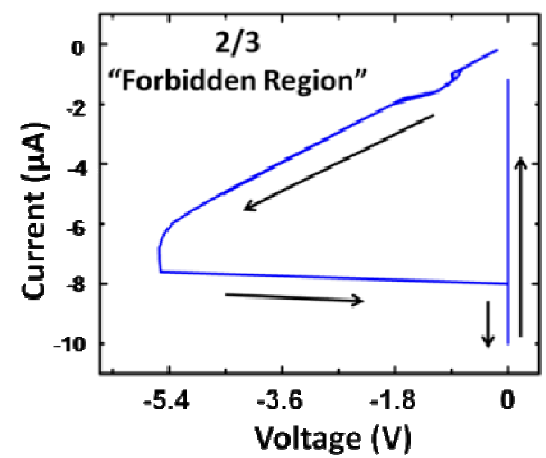
J.E. Stevens et al, accepted for publication by J. Vac Sci. Tech., 2013.

Effect on Device Behavior

Fraction of "forbidden region"	Partial Pressure Set #1	x: Ta_2O_x Set #1	Working Devices?	Partial Pressure Set #2	X: Ta_2O_x Set #2
0	50.0	1.9 ± 0.5	Some	43.0	2.1 ± 0.5
1/3	52.5	3.3 ± 0.5	Yes	44.6	3.5 ± 0.5
2/3	55.0	4.2 ± 0.5	No	46.2	4.0 ± 0.5
1	57.5	4.6 ± 0.5	No	48.0	4.4 ± 0.5
4/3	60.0	5.0 ± 0.5	No	49.5	5.0 ± 0.5

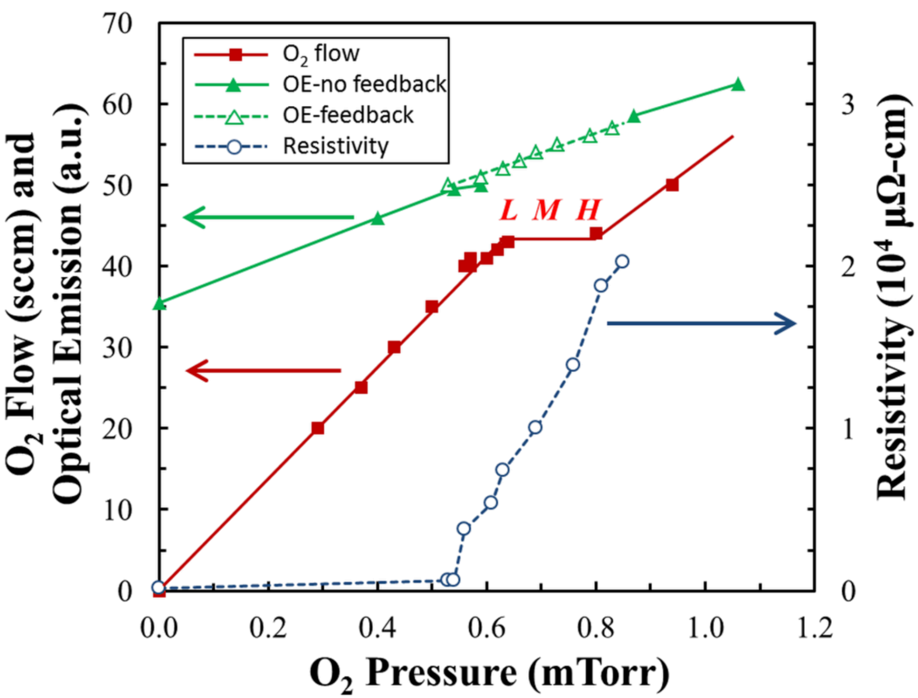


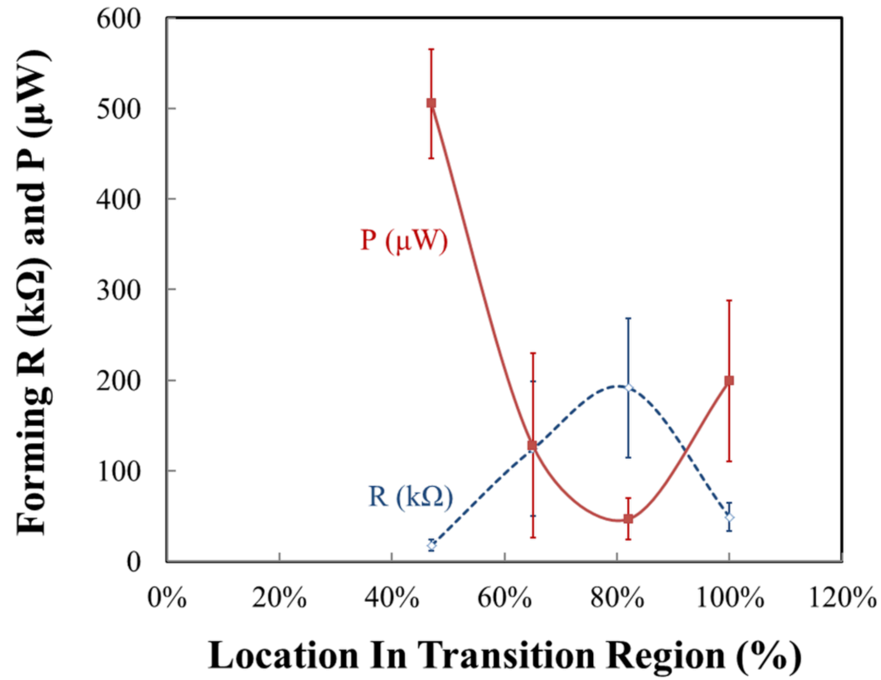




A.J. Lohn et al APL , 2013

Effect on Forming

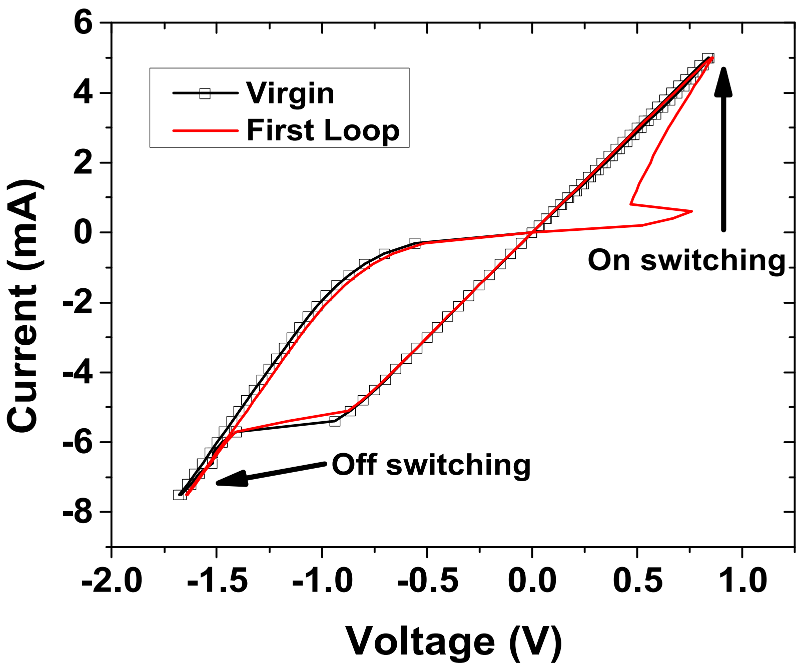


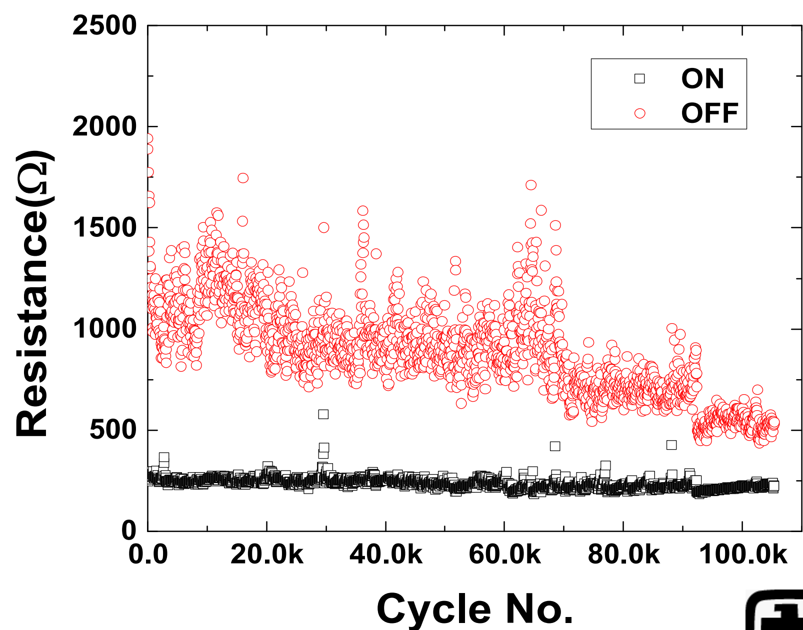


J.E. Stevens et al, accepted for publication by J. Vac Sci. Tech., 2013.

Basic Device Performance

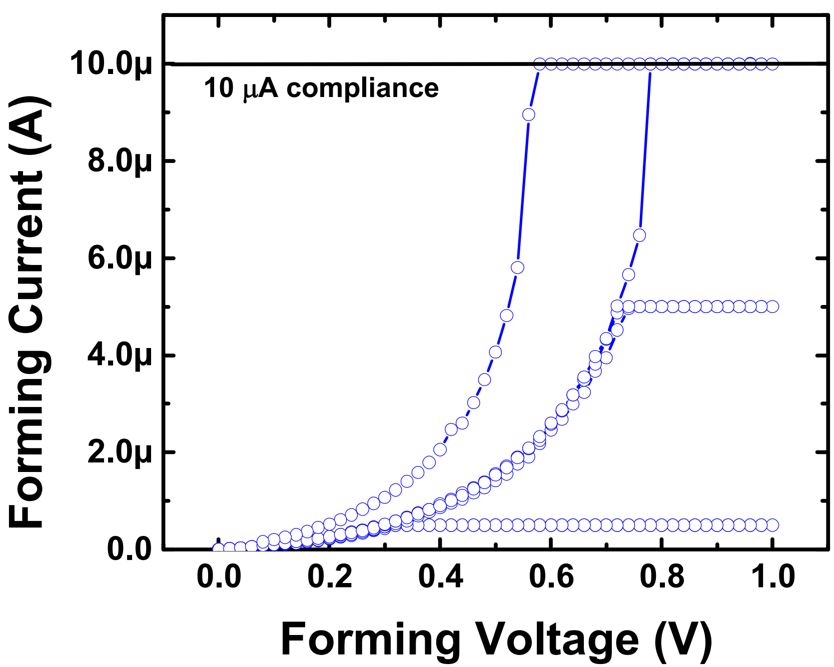
- Typical devices form at very low currents
- Appear “forming free” in current sweep mode
- Do not need a high voltage transistor!!
  - Unlike flash/SONOS
- Can be tailored by stoichiometry

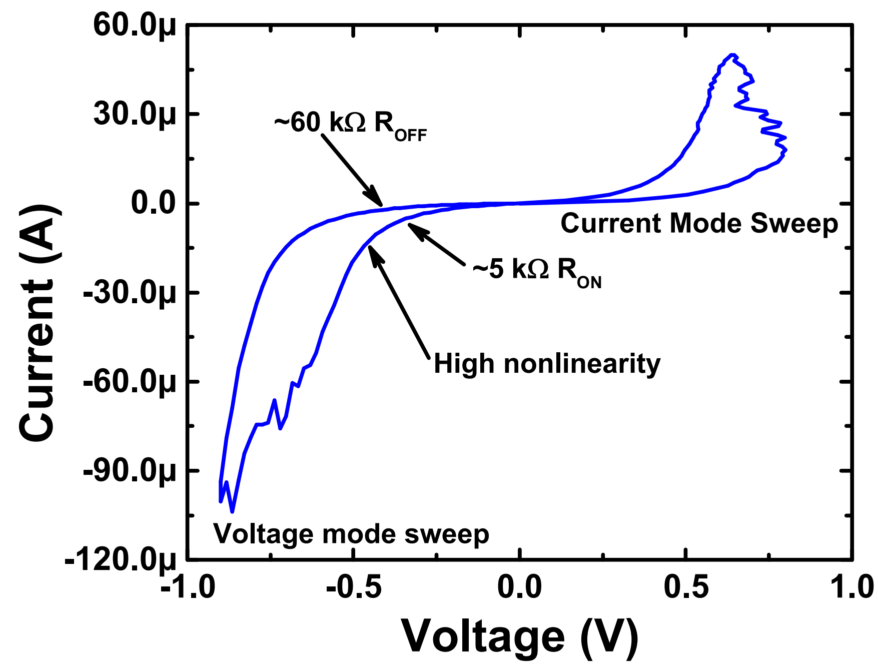




High Resistance Behavior

- Significant performance improvement can be achieved by careful electrical forming and control
- Very high resistance and R_{OFF}/R_{ON} possible

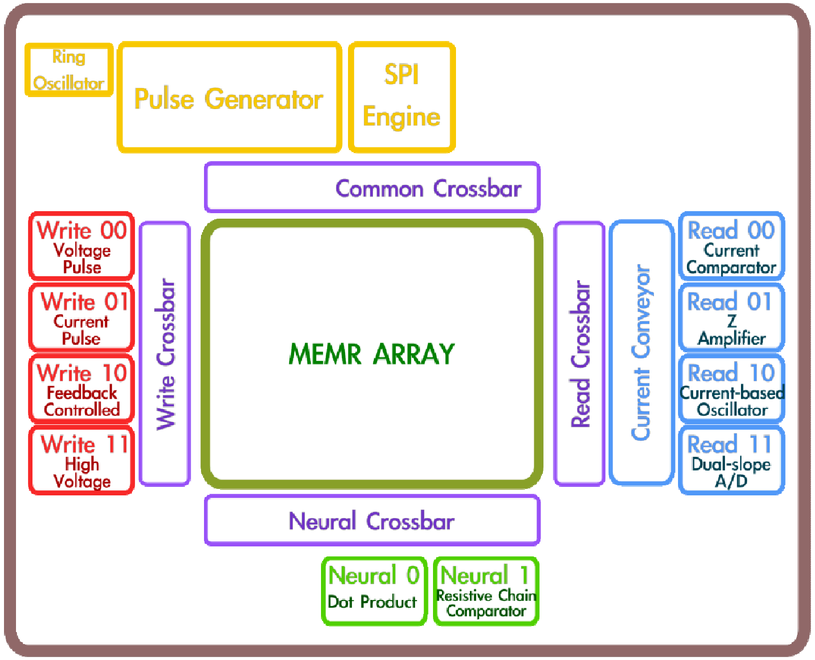




Future Work

- Integrating with CMOS ASIC controller (first generation under test/debug)
- Improve endurance, R_{OFF}/R_{ON} ratios, retention, and analog behavior through materials/device research and electrical read/write algorithms
- Develop analog circuitry for neuromorphic and other novel applications
- Continue to study radiation effects – ReRAM is a strong candidate for a future rad-hard memory

2nd Gen Memristor ASIC Controller Block Diagram



Microsystems
Science, Technology & Components

Conclusions

- ReRAM or Memristor technology shows promise to replace traditional magnetic hard drives, flash, DRAM, and SRAM
- Sandia, in collaboration with HP Labs, has developed a TaO_x memristor technology that is compatible with our rad-hard CMOS process
- The bits form and operate well within our CMOS voltage capabilites
- Through electrical conditioning it is possible to obtain very high on R_{OFF}, R_{ON} and ratio of these
- Future work includes improving performance through materials, device, and circuits research

Sandia National Laboratories

Acknowledgements

- Very grateful to our collaborators at HP Labs, esp. Jianhua Yang, Yoocharn Jeon, John Paul Strachan, Sity Lam, Dick Henze, and Stan Williams

Interesting App: Analog Computing

- Vector matrix operations often comprise >> 90% of operations in pattern matching algorithms
- A monolithically integrated memristor accelerator can greatly improve power and throughput for these operations
- This could comprise a node of a future HPC system