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A CMOS Compatible, Forming Free TaO_x ReRAM

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Resistive random access memories (ReRAM), also referred to as memristors, have emerged in the past several years as a leading emerging nonvolatile memory device due to excellent scalability and stackability, low energy, and high endurance. Furthermore, the analog properties of this device are a potential enabler of neuromorphic computing. Of particular interest are the class of ReRAM based on based on the mechanism named valence change memory (VCM) and fabricated from transition metal oxides (TMOs) such as TaO_x, HfO_x, and TiO_2 [1]. Switching in of VCM ReRAM is the subject of continued research, but is thought to occur as a result of oxygen vacancy motion in a small (50-200 nm) channel created in the TMO region of the device [1]. This particular class of ReRAM has achieved record endurance (10^{12} cycles) [2], sub-nanosecond switching speeds [3], and demonstrated operation in 10x10 nm devices [4]. Note that all of these metrics are for research devices, not integrated with a CMOS process. In fact, two of the significant hurdles to overcome with ReRAM technology are integrating high performance ReRAM devices with a CMOS back end of line (BEOL) processes and eliminating the high voltage electroforming step. This work reports on initial results from the integration of a TiN/Ta/TaOx/TiN ReRAM stack using a process compatible with CMOS. These initial results demonstrate that a CMOS integrated process which does not require a high voltage forming step and exhibits performance on par with integrated flash memory.

The details of the fabrication process are illustrated schematically in Fig. 1. This is a "short loop" process used to evaluate process parameters, and is intentionally simplified from the full BEOL CMOS process which is being integrated with Sandia's in-house CMOS7 BEOL. The process beings with PVD deposition and CMP polishing of a 300 nm W layer on a standard p-type wafer. Next, the ReRAM stack is deposited using reactive PVD without breaking vacuum. The ReRAM stack consists of (top to bottom) TiN(20nm)/Ta(15nm)/TaO_x(5-15nm)/TiN(20nm). Experiments varying oxygen flow during the reactive PVD deposition of the TaO_x allow optimization of switching behavior. Next, the ReRAM stack bits are dry etched (note the active bit area is defined by the top via rather than this step), followed by the CVD deposition of the standard BEOL SiO_2 interlayer dielectric (ILD). The standard ILD SiO_2 recipe reaches 400°C and hence there was concern that the TaO_x film would be damaged, however results below indicate that the film was still functional. Finally, vias were etched above the bits with diameters ranging 0.35 to 1.5 μm – defining the active switching area and filled with the Al top metal. The best switching performance was obtained from the smallest (0.35 and 0.5 μm). In this step, through vias were etched to contact the bottom metal (not shown in Fig. 1). Fig. 2 gives a photomicrograph of a final 32x32 crossbar produced from this process. Fig. 3 shows an SEM cross section of a typical bit with key regions identified and Fig. 4 give a zoomed-in cross section of the bit area.

Basic current-voltage (I-V) characterization was performed on a probe station in a dark box, using an Agilent 4156C. I-V hysteresis loops (often associated with a memristor [5]) were used as a method of initial characterization (Fig. 5). The remarkable characteristic of Fig. 5 is that the virgin I-V curve demonstrates off-state forming at approximately the same voltage as initial off-state switching. Hence, the device does not need a high voltage forming step, but simply switches off during the first negative cycle. The reason for this excellent result is a topic of investigation and may be related to specifics of the BOEL processes employed, such as the brief 400°C anneal required for the SiO_2 ILD. This result is a major advancement in our CMOS integration work, as we no longer will require forming voltages above the capability of our standard logic transistors (3.3V).

Endurance was measured using an Agilent 81130A Pulse/Arbitrary Waveform Generator and an oscilloscope. Figs. 6 and 7 show an endurance of over 100k before R_{OFF}/R_{ON} drops below 2, which is comparable with state of the art flash memory. CMOS compatible ReRAM processes exhibit lower endurance than individual devices. Present work indicates that this endurance can be improved by optimizing the process and switching conditions.

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[1] R. Waser et al., *Adv. Mater.* vol. 21, pp. 2632-2663. (maybe change to book chapter)
[2] M.-J. Lee, et al., *Nat. Mater.*, vol. 10, pp. 625-630, July 2011.
[3] C. T. Antonio, et al., *Nanotechnology*, vol. 22, p. 485203-1-8, Dec. 2011.
[4] B. Govoreanu et al., *IEDM 2011*, Dec. 2011.
[5] L. Chua, *IEEE Trans. Circuit Theory*, vol. 18, pp. 507-519, Sep 1971.

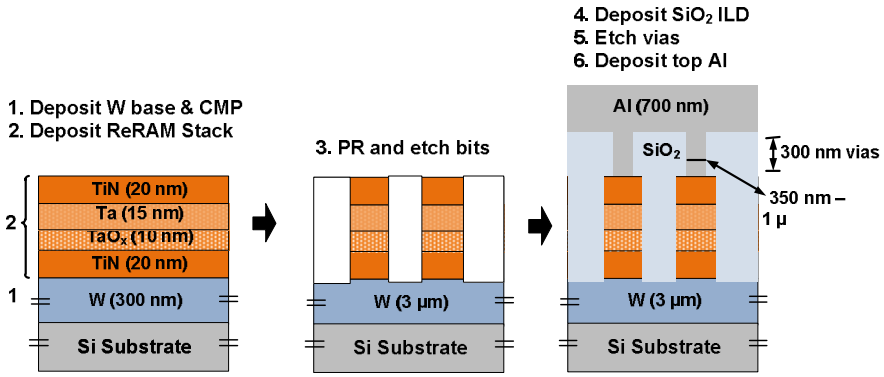

Fig. 1: Schematic illustration of the BEOL process used to create the TaOx ReRAM structures.

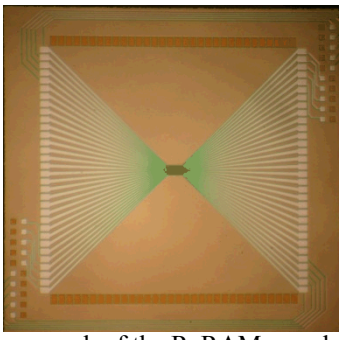

Fig. 2: Photomicrograph of the ReRAM crossbar die.

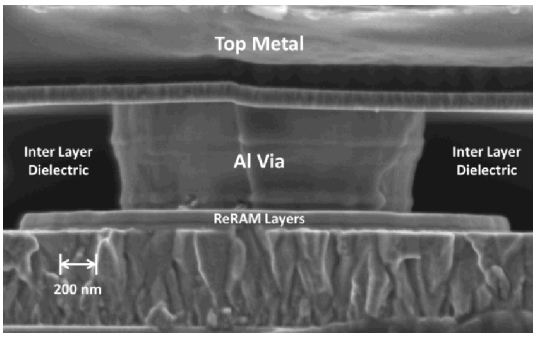

Fig. 3: SEM image of the ReRAM stack.

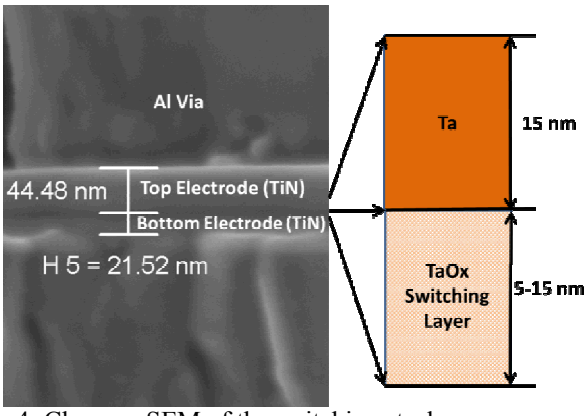

Fig. 4: Close-up SEM of the switching stack.

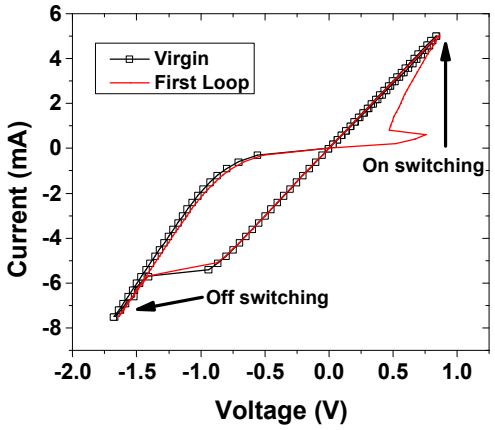

Fig. 5: Comparison of virgin and first I-V hysteresis. Forming occurs at the switching voltage of -1.5V.

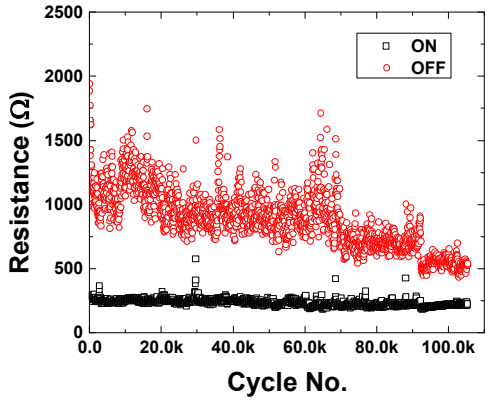

Fig. 6: Resistance vs cycle, indicating over 100k endurance.

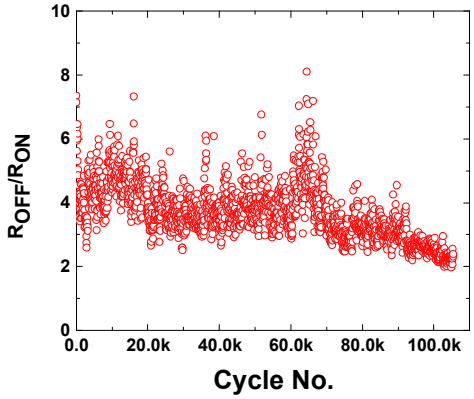

Fig. 7: R_{OFF}/R_{ON} vs cycle.