

ESTABLISHING A TI-CU-PT-AU THIN FILM – ON – LOW TEMPERATURE CO-FIRED CERAMIC (LTCC) TECHNOLOGY FOR HIGH TEMPERATURE ELECTRONICS

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ABSTRACT

A study was performed to evaluate the mechanical properties of solder of solder joints made to a 0.200Ti-4.0Cu-2.0Pt-0.25Au (μm) thin film conductor on low-temperature co-fired ceramic (LTCC) substrates. The solder joints were made with 63Sn-37Pb (wt.%, abbreviated Sn-Pb) or the 95.5Sn-3.9Ag-0.6Cu (SAC396) alloys. Pull strength and failure modes were analyzed as a function of soldering parameters. The effects of solid-state aging were also assessed for the Sn-Pb solder joints. Both Sn-Pb and SAC396 solder joints exhibited similar pull strength magnitudes as well as a nominal loss of such strength with increased severity of the process conditions. Solid-state aging of Sn-Pb solder joints caused a general decrease of pull strength. In all instances, the decreases of strength was accompanied by an increased occurrence of the solder failure mode. The fracture surface morphology (crack path) was more sensitive to the effects of both soldering process and solid-state aging than was the more generalized failure mode metric or the pull strength performance. Aside from the role of the Pt-Sn IMC layer in the fracture surface morphology (Area #1), the adhesion and integrity of the Ti-Cu-Pt-Au thin film did not control the mechanical performance of the Sn-Pb solder joints.

Key words: Thin film conductor, low-temperature co-fired ceramic, Pb-free solder.

INTRODUCTION

Ceramic substrates have traditionally been specified for printed circuit boards (PCBs) to meet the attenuation requirements of high-frequency signal transmission or to minimize the thermal mechanical fatigue (TMF) of solder joints made to large ceramic components. Although ceramic substrates still fulfill those roles within the telecommunications and military sectors of the electronics industry, these materials are also being targeted for use in other, high-temperature environments. Applications include those electronics that monitor conditions in oil, gas, and geothermal wells, where temperatures can exceed 350°C, to the very high reliability systems aboard deep-space probes to the planet Venus, which experience similar temperature environments [1 – 3].

Ceramic substrate-based electronics, or using the established industry terminology, *hybrid microcircuits (HMCs)*, have been based upon alumina substrates and thick film conductors that create the circuit pattern of pad and traces. That pattern is screen or stencil printed on the substrate with a thick film paste. The thick film paste has metal particles of Au, Ag, or alloy combinations that include Ag-Pd, Au-Pt, Au-Pt-Pd, etc. together with a glass and lastly, organic binder (thixotropic) materials that aid with the printing process. Once the paste pattern is printed on the alumina surface, it is dried to drive off the organic binder and is then fired at 850 – 900°C in air. The firing step allows two processes to take place: (a) the metal particles sinter together to form a continuously conductive layer and (b) the glass phase diffuses to the interface between that metal layer and alumina surface where it bonds the two materials, together.

These alumina PCBs are generally limited to two-layers that have patterns of pads and traces on one or both of the exposed surfaces. When both surfaces were used in the circuit, signal routing is achieved between them using mechanically drilled holes. Or, if the substrate was sufficiently thin (< 0.5 mm), laser drilling could be used to form vias. The via walls were covered with the same thick film conductor that was fired to the surface. These “through-alumina” holes exhibited suitable reliability, but can be expensive to fabricate. Often, edge-clips provide the most cost-effective avenue for conducting signals between the two surfaces.

The two-sided alumina substrate-plus-thick film conductor allow HMC technology to support many significant advances in the telecommunications and defense industries. However, this technology is reaching its limits with respect to meeting the needs for further miniaturization and increased functionality of electronic products. The development of low-temperature, co-fired ceramic (LTCC) technology has enabled the introduction of multi-layer substrates into HMC electronics. Similar to organic laminate PCBs, LTCC is a layer-by-layer build-up technology. Individual layers of “tape” are fabricated with

traces and filled vias such that, when all of them are laminated together and then fired to complete the bonding process, a ceramic PCB is created having the complex routing structures required for advanced electronics systems.

Initially, the development of surface pad and trace patterns relied upon the same thick film technology as was used on alumina HMCs. The internal thick films differed from those used on the surface because the former did not have to support the challenges posed by *soldering processes*, including conductor leaching and intermetallic compound (IMC) layer formation. Unfortunately, like the two-sided alumina substrate, surface thick film conductor traces and pads had reached their limits in terms of providing minimum dimensions and spacings that were reliable and capable of optimizing the functionality of multilayer LTCC substrates supporting the multi-chip module (MCM) sub-assembly [4].

An alternative approach was to replace thick film conductors with thin film layers. The thin films are deposited by physical vapor deposition (PVD) techniques – evaporation or sputtering. The glass adhesion layer was replaced with titanium (Ti), chromium (Cr), or other high-oxide potential elemental layer that was placed first on the LTCC surface. That layer was followed by conductor metals such as gold (Au) or Au-plus-nickel (Ni). While the adhesion layer is fractions of a micron, the conductor layer thickness could vary over several microns, depending on the signal requirements.

The patterning of the thin film conductor can be performed by three methods. The first method uses physical masks that are located over the substrate. The desired, thin film pattern was created by apertures in the mask. The mask-plus-substrate assembly is secured into the coater for the deposition process. Aside from fabrication of the mask, this technique provides a relatively rapid turnaround of patterns that do not require a great deal of geometric precision.

The second technique is photoimaging that is similar to that exercised by the integrated circuit industry. This method provides greater feature resolution that enables finer lines and spaces on the surface. The LTCC substrate is covered with the thin film system. The surface is then coated with a photoresist that is subsequently exposed to photons through a mask pattern. The unexposed photoresist is dissolve away, exposing the thin film in those locations. The film is subsequently removed by plasma etching. The photoresist that remains, which still has the coating underneath it, is chemically removed, leaving the desired thin film pattern. Additional thickness can be added to the thin film using electroplating or electroless plating processes.

There are drawbacks to the ion milling process. Besides the capital equipment costs, a long-time is required to complete the film removal process. The thicker is the film stack, all the longer is the milling interval. Also, the longer is the milling process, the higher is the temperature exposure to

the substrate; at times, surface temperatures can reach as high at 150 – 200°C.

A third technique that is being developed to replace photoimaging in some applications is laser ablation [5]. The particular attribute of laser ablation is that, in the case of thicker film layers, it reduces both the process time as well as exposure of the module to elevated temperatures as would be experienced with ion milling. Yet, laser ablation can provide nearly equivalent feature resolution to that of photoimaging. Several drawbacks, including metal and ceramic spatter as well as surface “microfractures” are being addressed through research and development as well as process development and reliability programs.

The study focused upon in this report examined the adhesion properties of thin film conductor “stacks” on LTCC substrates. A specially designed test specimen was used to document the effects of different soldering process conditions as well as isothermal aging treatments. These experiments formed a fundamental framework for using thin film/LTCC technology in high-reliability, HMC components.

EXPERIMENTAL PROCEDURES

Materials

The LTCC substrates were fabricated using Dupont™ 951 tape (Dupont is a registered trademark of the E.I. Dupont de Nemours Corp., Wilmington, DE). The final substrate thickness was 0.914 mm. The test specimen had an overall footprint of 25.4 mm x 25 mm. The substrates were not subjected to additional surface preparation steps (e.g., polishing) other than those routinely performed at the manufacturer. This surface condition is typically the starting point from which a thin film circuit is created for actual product.

A pattern of nine test sites was used to assess thin film adhesion as shown in Fig. 1. The pattern was created by evaporating the thin film through an aperture mask, which was considerably more cost effective for this particular structure.

Copper pins were soldered to each of the pads. A specially designed fixture held the LTCC substrate within a base plate (Fig. 2a). Solder paste was dispensed onto each pad to ensure a reproducible solder joint geometry. The Cu pins were fed through a frame that held them in an upright position. The frame was attached to the base plate after which, the pins were lowered onto the solder paste deposit. The entire assembly (Fig. 2b) was placed into furnace to complete the soldering process. Once the fixture had cooled to room temperature, the test specimen – substrate-plus-soldered pins – was cleaned of flux residues and inspected for solder joint quality (Fig. 2c).

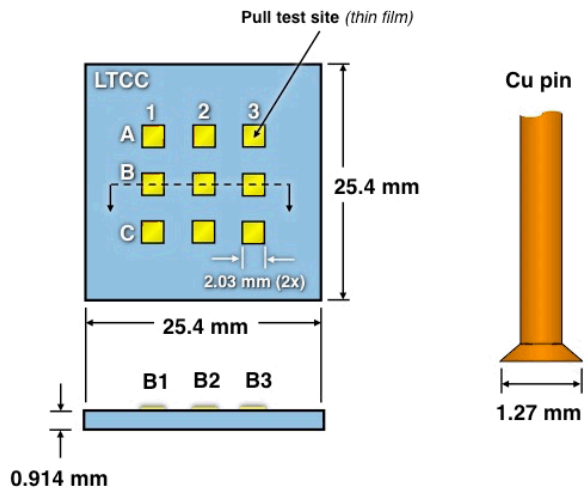


Fig. 1 LTCC pull test specimen and the Cu pin.

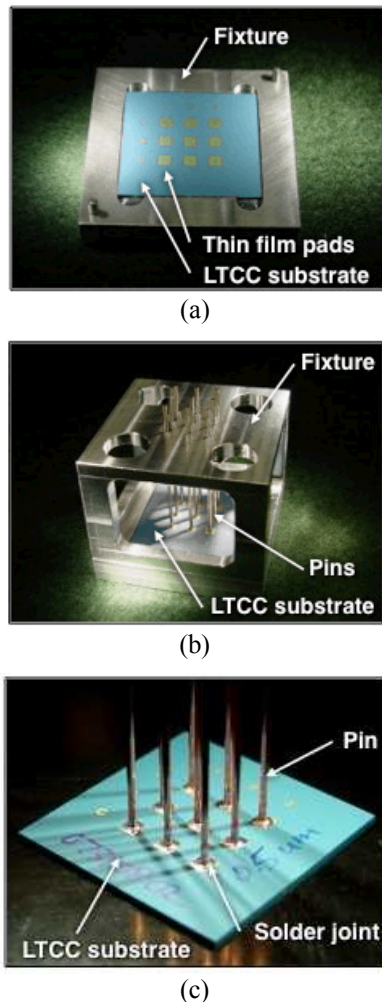


Fig. 2 (a) LTCC substrate is placed into the base plate of the fixture. (b) Fixture has been assembled with the LTCC substrate; solder paste; and pins in place; it would be placed into the furnace to make the joints. (c) Photograph of the typical test specimen.

The thin film stack used in this study is listed below:

- $0.200\text{Ti} - 4.0\text{Cu} - 2.0\text{Pt} - 0.25\text{Au}$ (μm)

Titanium is the adhesion layer. The Cu layer supported the electrical signal. The Pt layer was served as the solderable finish. (Signal integrity prevented the Cu layer from also serving this function.) The Au layer was the protective finish in both films. The $0.25\text{ }\mu\text{m}$ layer had the minimum thickness that will provide a protective function and could support wire and ribbon bonded interconnections.

The 63Sn-37Pb (wt.%, abbreviated Sn-Pb) solder provided the baseline data. The Pb-free solder, 95.5Sn-3.9Ag-0.6Cu (abbreviated, SAC396), was also used to fabricate solder joints to the Ti-Cu-Pt-Au thin film.

This study evaluated two aspects of the strength of solder joints that are made to the thin film conductor. The first property was the margin provided by the thin film against leaching and IMC layer growth when exposed to liquid (molten) solder as part of a *soldering process*. The time durations used for both solders were:

- 15s,
- 60s, and
- 120s.

These time parameters address the range of typical, automated soldering processes. The following temperatures were used for the two respective solders and were likewise based upon typical soldering process parameters:

Sn-Pb:

- 215°C , 240°C , 260°C , and 290°C

SAC396:

- 240°C , 260°C , and 290°C .

Duplicate samples were made and then tested for each combination of soldering temperature and time.

The second property is the effect had by *solid-state aging* on the joint strength. The discussion of this analysis will be limited to the Sn-Pb solder joints for brevity. However, the discussions to follow in the results section will leave little doubt that, at this juncture, it is reasonable to presume similar trends with the SAC396 solder.

It was observed in the first part of the study that the soldering process parameters *do affect* the mechanical properties of the Sn-Pb (and SAC396) solder joints. Therefore, test specimens were fabricated in two sets, using the most benign soldering parameters, 215°C , 15s, and the most severe conditions, 290°C , 120s, in order to determine if the effects of process conditions extended to the mechanical strength after solid-state aging. Duplicate test samples were fabricated for each of the following aging time and temperature combinations:

- Times: 5, 10, 25, 50, 100, and 200 days.
- Temperatures: 70°C, 100°C, 135°C, and 170°C

The “zero days” or baseline pull strengths were obtained from the soldering process data.

All pull tests were performed in a mechanical test frame. The displacement rate was 10 mm/min. Eight of the nine solder joints were pull tested per sample, leaving one joint for cross section and microanalysis. The pull strength was represented by the mean and the standard deviation of the sixteen (16) data points.

Failure mode analysis was also performed on the test samples. There were three predominant failure modes observed for these specimens:

- *Solder failure*: crack path that remains in the solder or associated IMC layers;
- *Thin film delamination*: a peeling of the thin film from the LTCC surface.
- *Divot failure*: loss of bulk LTCC from under the joint area

The assessment methodology began with each pull-tested site being given one of the three failure modes. It was not necessary to further discriminate minor failure modes *within an individual site* because, in general, there was on predominant mode per pin pull test. The failure modes were added up and the percentage determined by dividing that count by the total number of test sites (sixteen between duplicate in the absence of an anomalous test).

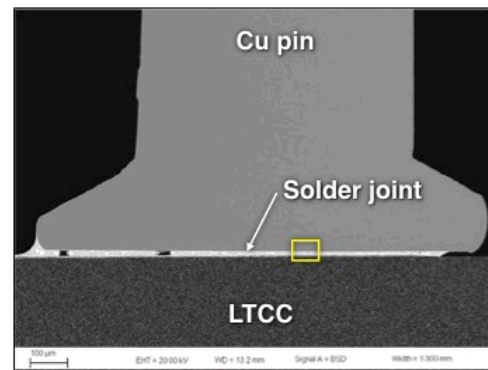
RESULTS

Sn-Pb solder – soldering process parameters

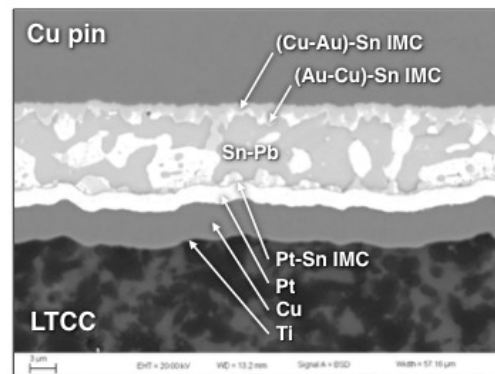
Solder joint microstructure

Metallographic cross section microanalyses were performed on the as-fabricated test samples in order to understand the structures that potentially control the failure mode behavior. The pull test solder joint is illustrated in Fig. 3a. This pin was soldered under the least-severe conditions of 215°C and 15s. Slight misalignments between the pad and pinhead, such as is Fig. 3a, did not have an effect on the pull strength or failure mode behavior. A high magnification SEM/BSE image is shown in Fig. 3b that was taken at the yellow box in Fig. 3a. The EDX analysis technique was used to identify, qualitatively, the phase structures in the joint at that location. At the pin was a (Cu-Au)-Sn IMC layer. Copper was predominant (listed first) and Au was present to a lesser amount in that phase. There was the intermittent presence of a second, less prevalent IMC phase, (Au-Cu)-Sn, in which Au dominated the Cu signal. It has the lighter gray tone. The Sn-Pb solder comprised the center portion of the joint. Only a thin, Pt-Sn IMC layer formed between the Sn-Pb solder and Pt. In addition, Pt is resistant to leaching by

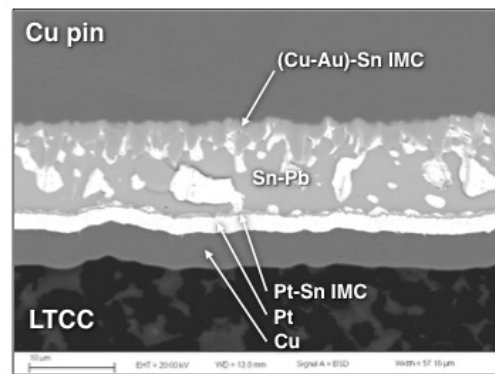
the molten Sn-Pb solder so there is a negligible loss of Pt layer thickness.



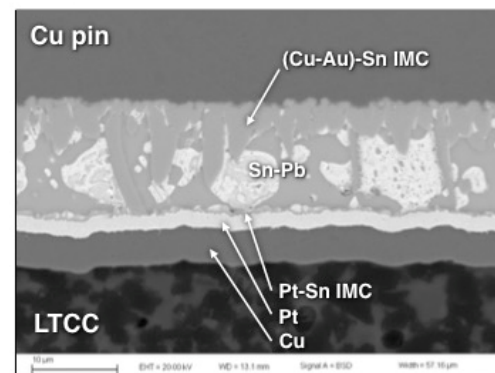
(a)



(b)



(c)



(d)

Fig. 3 (a) Low magnification, SEM/BSE image shows the pin pull test solder joint configuration for the sample fabricated of Sn-Pb solder under the least-severe conditions of 215°C and 15s. The yellow box denotes the location of the high magnification image in (b). (b) The SEM/BSE photograph shows the solder joint at high magnification. The phases have been identified across the gap. (c) SEM/BSE image is from the sample fabricated with the “intermediate” soldering process of 260°C and 60s. (d) SEM photograph shows the joint made under the most severe conditions of 290°C, 120s.

The third photograph, Fig. 3c is similar to Fig. 3b; but, it was taken of the joint made under the “intermediate” process conditions, 260°C, 60s. There was a noticeable growth of the (Cu-Au)-Sn IMC phase and almost the complete disappearance of the (Au-Cu)-Sn IMC phase. The EDX analysis indicated that the Au had become uniformly distributed in the (Cu-Au)-Sn IMC phase. There was a negligible loss of the Pt layer thickness. The image in Fig. 3d was taken of the solder joint fabricated under the most severe conditions of 290°C and 120s. There was significant growth of the (Cu-Au)-Sn IMC and no indication of the (Au-Cu)-Sn IMC composition. Also there was a small decrease in the Pt layer thickness ($\approx 0.1 \mu\text{m}$).

It is important to note that in the three cases shown in Figs. 3b – 3c, there was an absence of mechanical degradation to the solder joints as a whole. That is, cracks were not observed in the solder or within the IMC layers; they were also not recorded at the mutual interfaces. Lastly, delamination was not observed within the thin film layer structure of the Ti-Cu-Pt-Au thin film or at the Ti/LTCC interface.

Pull strength data

The pull strength values are shown in Fig. 4 as a function of the process temperature. The blue circles, magenta squares, and red diamonds represent the 15s, 60s, and 120s data, respectively. The data are presented in load (lb.). Stress values have been calculated at the two limiting loads. These very high stresses reflect the plain strain effect resulting from the confined geometry of the thin gap-versus-wide footprint geometry. By comparison, the tensile strength of bulk Sn-Pb solder is 40 – 50 MPa at a similar displacement rate [6].

The pull strength values in Fig. 4 declined as a function of soldering temperature for all three durations. The approximately 34 – 37% decrease was significant from the perspective of change in absolute values. However, even the lowest strengths remained well in-excess of those needed for most electronic packaging applications. Also, the data did not indicate a catastrophic failure of the materials system. The 15 s solder time maintained slightly higher strengths than the 60s and 120s process times. There was no statistical difference of strengths between the 60s and 120s data over the temperature range. Of course, it

would not be prudent to conclude that the pull strengths will continue to be insensitive to even longer solder times.

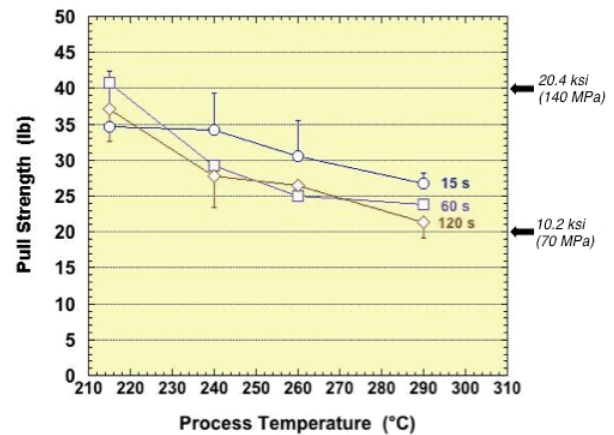


Fig. 4 Pull strength values are shown as a function process temperature and time for the Sn-Pb solder joints made to the Ti-Cu-Pt-Au thin film. The three curves of colored symbols and lines represent the three process times: 15s, 60s, and 90s. The error bars are one standard deviation. Stress values were calculated at the higher and lower limits of pull strengths.

Failure mode analysis

The failure mode data are shown as the stacked bar charts in Fig. 5. The results are presented separately according to each of the three time intervals, 15s, 60s, and 120s, beginning with the 15s data in Fig. 5a. Thin film delamination comprised 50% of the failure modes recorded under the 215°C temperature. The remaining failures were evenly split between solder failures and the LTCC divot mode.

Trends are described in further detail. An increase of soldering temperature to 240°C resulted in only a small drop in the frequency of thin film delamination to 45%. There was a decrease in the LTCC divot mode, which was compensated by an increase in solder failures. This trend continued at 260°C with (a) the elimination of the LTCC divot mode; (b) a decrease in the occurrence of thin film delamination to 30%; and (c) the corresponding predominance of the solder failure mode (70%). The failure mode percentages changed only slightly between the 260°C and 290°C soldering temperatures.

The general behavior observed in Fig. 5a is that, with increased process temperature, there was a loss of both LTCC divot and thin film delamination modes, which were replaced by an increased occurrence of the solder failure mode. A comparison was made between the pull strength data in Fig. 4 and failure mode data in Fig. 5a. The decrease of pull strength with increased process temperature in the former graph correlated to a weakening within the solder (joint) structure as indicated by the increase of solder failure mode.

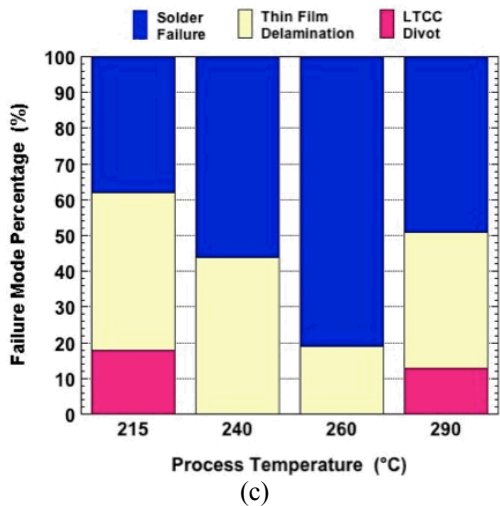
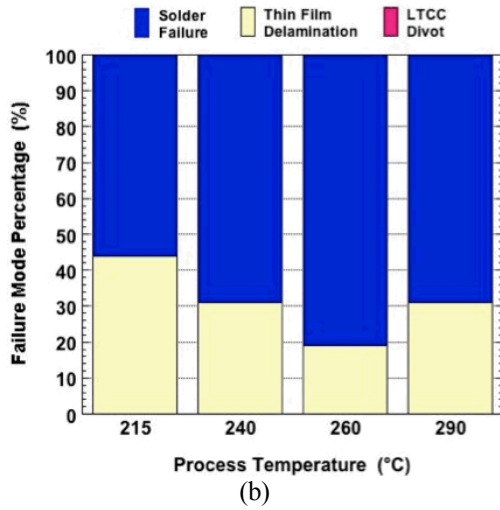
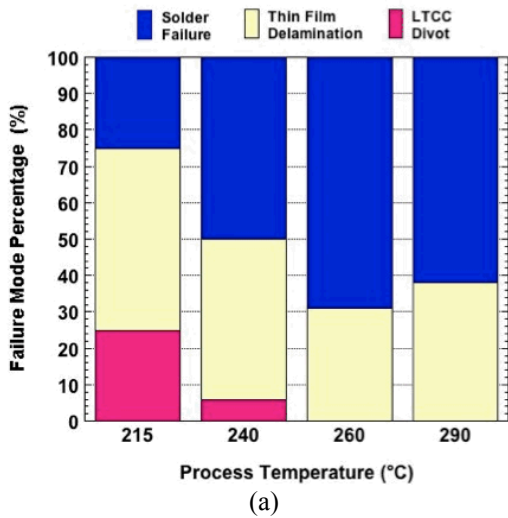
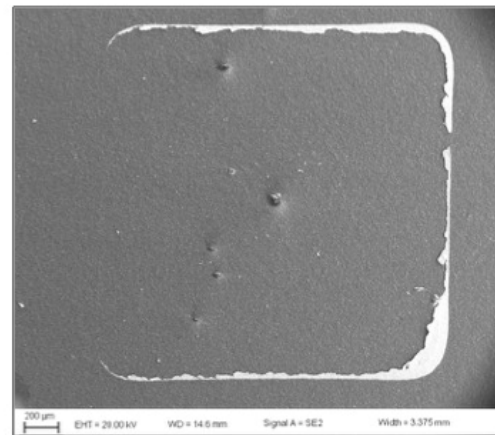
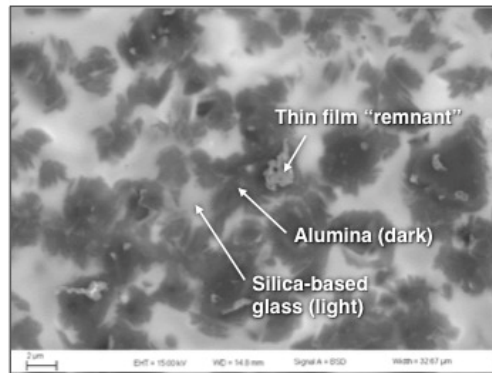


Fig. 5 Stacked bar charts show the percentages of each failure mode as a function of the process temperature for the three soldering times: (a) 15s, (b) 60s, and (c) 120s. These data were obtained from the Sn-Pb solder joints made to the Ti-Cu-Pt-Au thin film.

At this point, microanalysis was used to document the fracture surfaces that accompanied these failure modes. Scanning electron microscopy (SEM), secondary electron (SE) images are provided in Fig. 6 that illustrate the thin film delamination mode as viewed on the LTCC substrate. The low magnification image in Fig. 5a shows the featureless fracture surface. The high magnification, back scattered electron (BSE) image in Fig. 5b confirms a nearly complete separation at the thin film/LTCC interface. Aside from a few remnants of the thin film that remained attached to the surface, the photograph highlights the structure of the LTCC material that is comprised of alumina particles bonded together by a silica-based glass. The energy dispersive x-ray (EDX) analysis confirmed, qualitatively, the anticipated elemental distributions at the surface. For example, the silica-based glass also contains oxides of lead (Pb), sodium (Na), potassium (K), and calcium (Ca) as well as cobalt-chromium (Co-Cr) additions that are recognizable by the blue color of the LTCC.



(a)

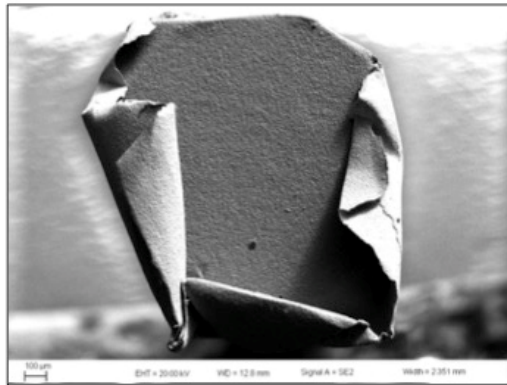


(b)

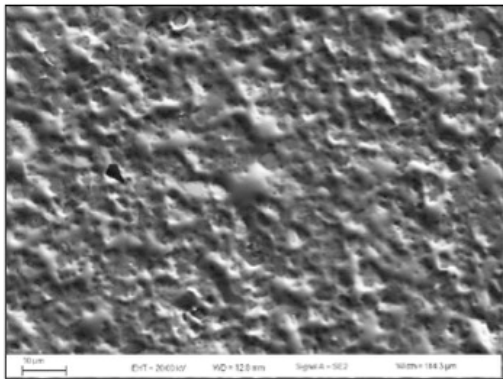
Fig. 6 (a) Low magnification photograph shows the thin film delamination failure mode as viewed on the LTCC substrate, using the secondary electron (SE) imaging technique. (b) High magnification image of the LTCC surface using the back scattered electron (BSE) imaging mode. The solder was Sn-Pb and the process conditions were 215°C and 15s.

The same analysis was performed on the complimentary surface that remained attached to the pin. A low

magnification SEM image shows the surface morphology in Fig. 7a. The film has curled up around its perimeter beyond the immediate footprint of the pinhead due to the “shock load” of the pull test as well as intrinsic residual stresses. The higher magnification image of the surface is provided in Fig. 7b, which further accentuates the featureless morphology that is characteristic of thin film delamination from the LTCC surface. An EDX analysis of the surface produced a spectrum that confirmed the presence of the Ti adhesion layer and underlying Cu layer that was also contacted by the electron beam sampling volume. These analyses confirmed that the separated surface did not incorporate fractured remnants of the LTCC surface.



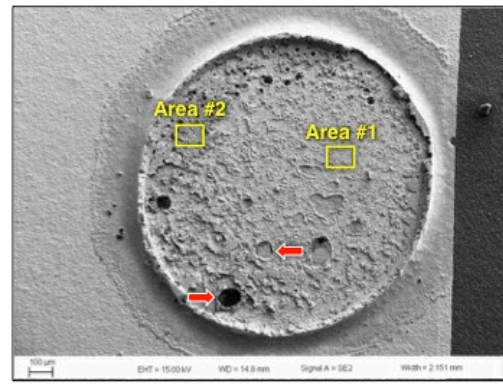
(a)



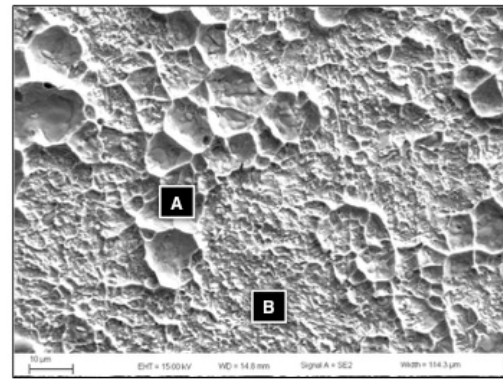
(b)

Fig. 7 (a, b) Low and high magnification photographs show the thin film delamination failure mode from the view of the pin pulled from the substrate. Both images were generated by the secondary electron (SE) imaging technique. The solder was Sn-Pb and the process conditions were 215°C and 15s.

The fracture surface of the *solder failure* mode was more complex due to the potential of multiple crack paths. Crack propagation could occur within the bulk solder or along either of the two interfaces. A low magnification, SEM/SE photograph is shown in Fig. 8a that is representative of this failure mode in the joints processed at 215°C for 15s. A few, small voids were exemplified by the red arrows; they were inconsequential to the pull strength or failure mode behavior.



(a)



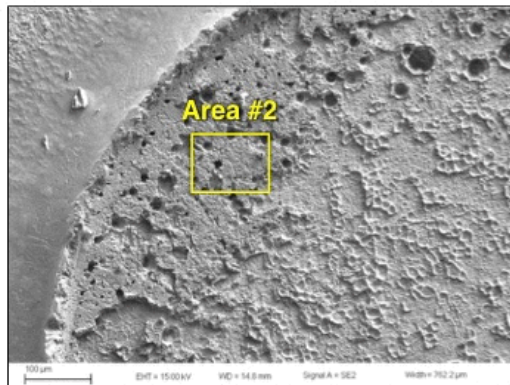
(b)

Fig. 8 (a) Low magnification SEM/SE image shows the *solder failure* mode from the view of the LTCC substrate. The yellow boxes, “Area #1” and “Area #2,” indicate two distinct fracture surface morphologies. (b) High magnification image illustrates “Area 1” of (a). Two fracture paths are labeled “A” and “B”. The solder was Sn-Pb and the process conditions were 215°C and 15s.

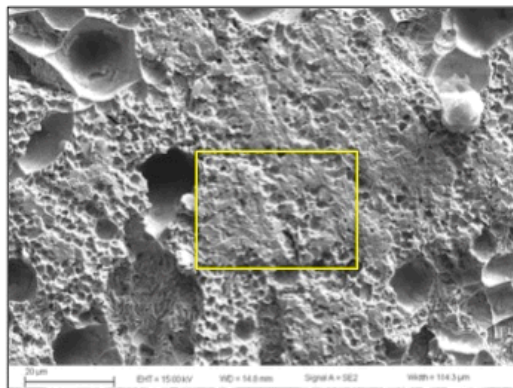
There are two areas in Fig. 8a having different gray tones; they are labeled “Area #1” and “Area #2.” The SEM image in Fig. 8b shows the lighter gray, Area #1 at high magnification. There were two features observed on the fracture surface that are labeled “A” and “B.” The region “A” shows the ductile tearing and microvoid coalescence that results from fracture within the Sn-Pb solder. The region “B,” which is decidedly more featureless, was caused by fracture along an IMC layer. The EDX analysis confirmed that the surface resulted from fracture in the Pt-Sn IMC that formed at the Pt layer belonging to the Ti-Cu-Pt-Au thin film.

The “Area #2” of Fig. 8a is shown at higher magnification in Fig. 9a. The surface has a darker gray tone in this SEM/SE image and Fig. 8a; nevertheless, Fig. 9b indicates a relatively featureless surface. A higher magnification image was taken of the area within the yellow box of Fig. 9b, which is shown in Fig. 9c. Figure 9c displays a surface that is characteristic of brittle, intergranular fracture that is frequently observed when a crack propagates through an IMC layer. The corresponding EDX analysis indicated that the surface in Fig. 9c is the (Au-Cu)-Sn IMC layer that had

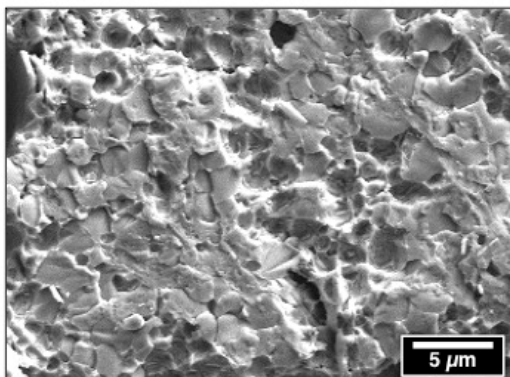
formed near pin/solder interface. The images in Figs. 8 and 9 illustrate the multiple crack paths that were observed in the solder failure mode.



(a)



(b)



(c)

Fig. 9 (a, b, c) Progressively higher magnification, SEM/SE images that highlight the Area #2 of the *solder failure* mode (LTCC substrate). The solder was Sn-Pb and the process conditions were 215°C and 15s.

The third failure mode has *divots* pulled from the LTCC substrate material. Three pull test sites that exhibited this behavior are identified by black arrows in the optical micrograph of Fig. 10. Those sites are also designated by the alphanumeric indicators A2, A3, and C2. The divot footprint often extended beyond the immediate footprint of the bond pad due to the speed of the failure.

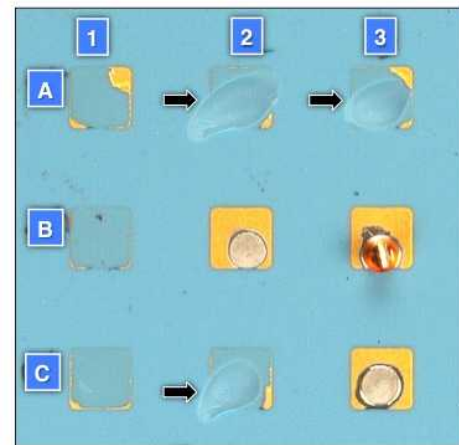


Fig. 10 Optical micrograph shows the fracture sites of the pull tested samples. The black arrows identified the *divot failure* mode. The solder was the Sn-Pb alloy and the process conditions were 215°C and 15s.

For the record, referring to Fig. 10, the solder failure mode took place at sites B2 and C3 while the thin film delamination mode is represented by sites A1, B1, and C1. The location B3 is the non-pulled solder joint that was left for microanalysis cross section.

At this juncture, a correlation is drawn between (a) the pull strength data in Fig. 4; (b) failure mode data in Fig. 5; and (c) the fracture surface analyses represented by Figs. 6 – 10. It was noted in Fig. 4 that pull strength decreased with process temperature and that, according to the plots in Fig. 5, that strength loss was accompanied by an increased preference for the solder failure mode. The morphology of the solder failure mode, which is described in Figs. 8 and 9, was compared between the three temperature and time combinations that represented least, intermediate, and most severe process conditions: (a) 215°C, 15s; (b) 260°C, 60s; and (c) 290°C, 120s. The SEM/BSE partner images were selected for this analysis because they highlight the compositional differences that identify the crack path as being in the IMC layers or being a ductile failure of the Sn-Pb solder.

The three photographs are shown in Fig. 11. The “Area #2” is highlighted because the extent of its presence corresponds, *inversely*, to the generalized strength trend observed in Fig. 4. Furthermore, these images imply that the lower strength of the 60s and 120s data is attributed to a greater presence of the “Area #2”, which results from fracture through the (Cu-Au)-Sn IMC layer along the pin/solder interface.

In summary, an analysis was made of the pull strength data and failure modes for the Sn-Pb solder joints as a function of the soldering process conditions. The joint strengths well exceeded the bulk strength of the solder due to the plane strain effect. There was a gradual, general loss of pull strength with increased soldering temperature and time. The strength loss correlated to the increased occurrence of the

solder failure mode and, specifically, fracture associated with the (Cu-Au)-Sn IMC layer that formed at the solder/pin interface. Although an indirect observation, it is prudent to note that the thickness of the IMC layer also increased with severity of the process conditions, suggesting that such growth weakened the Cu/(Cu-Au)-Sn IMC interface. Because there was an absence of voids or other large-scale defects at the immediate IMC layer/Cu interface, the increased process time and temperature altered, specifically, the fundamental adhesion between IMC layer and the pin's Cu surface. It was proposed that, based on the high Au signal of the fracture surface recorded for "Area 2," the accumulation of Au at that interface (which had originated from the 0.250 μm thick layer on the Ti-Cu-Pt-Au thin film) was the most probable, contributing factor to the strength loss.

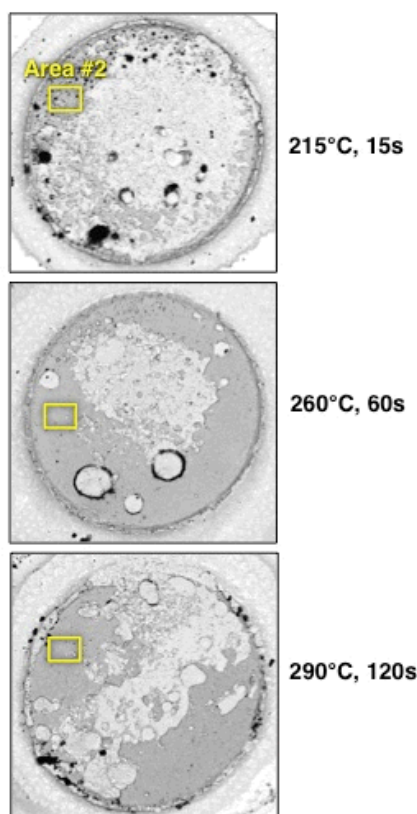


Fig. 11 SEM/BSE images highlight the fracture surfaces on the LTCC substrate for the three soldering conditions: 215°C, 15s; 260°C, 60s; and 290°C, 120s. The "Area 2" fracture surface is pointed-out by the yellow box.

In the broader context of understanding the robustness of these solder joints, the latter are considered to be comprised of a serial connection of these structures – the Cu pin; the solder joint, which includes the bulk solder as well as the IMC layers at both interfaces; the thin film/LTCC interface; and the bulk LTCC. The bulk strength of the Cu pin is not a significant factor versus the other structure and will be omitted from this discussion. The pull test and failure mode data indicate that the remaining structures have *comparable strengths* under the nominal process space of 215 – 240°C

and 15s because all three respective failure modes were represented amongst the test sites. See Fig. 5. However, under the more extreme process conditions of 240 – 290°C and 60 – 120s, the solder failure mode predominates due to the increased development of the (Cu-Au)-Sn IMC layer at the pin/solder interface and, more specifically, an apparent weakening of the IMC next to, or at, its interface with the Cu pin.

SAC396 solder – soldering process parameters

Solder joint microstructure

Metallographic cross sections are shown in Fig. 12 that represent the SAC396 solder joints fabricated using (a) 240°C, 15 s and (b) 290°C, 120s process conditions.

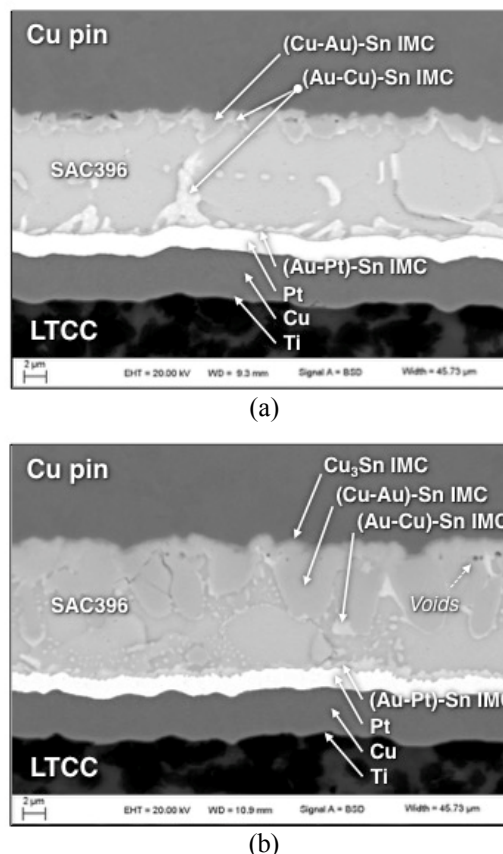


Fig. 12 High magnification SEM/BSE images show the SAC396 solder joints resulting from the following process conditions: (a) 240°C, 15s and (b) 290°C, 120s.

Besides the microstructural features in the bulk solder, the SAC396 solder joints differed from those of the Sn-Pb alloy at the two interfaces. In Fig. 12a, there is a significant presence of Au-containing IMC phase at *both* the solder/thin film (LTCC) interface as well as accompanying the IMC layer that formed at the solder/Cu pin interface. Under the more severe process conditions of 290°C, 120s (Fig. 12b), and unlike the Sn-Pb solder joints, the SAC396 retained those Au-containing IMC phases.

The comparison continued between the Sn-Pb and SAC396 solder joints. The general sizes of the IMC phases were

similar between the two cases. Also, there was not any evidence of large-scale defects such as cracks in the SAC396 solder joint structures. On the other hand, the Cu_3Sn phase appeared as a distinct layer along the IMC/Cu pin interface in Fig. 12b; it was absent from Fig. 12a as well as all of the Sn-Pb solder joints. Also, small voids occurred intermittently *within* the (Cu-Au)-Sn IMC nearer to the IMC/Cu pin interface in the same specimen (Fig. 12b). The voids were not observed in Fig. 12a or in the Sn-Pb structures. In summary, the SAC396 solder joints developed microstructural characteristics that were generally, similar to those of the Sn-Pb samples, but differed noticeably with respect to many details. Those differences could potentially affect the SAC396 mechanical properties.

Pull strength data

The pull strength data are shown in Fig. 13. The bulk tensile strength of the SAC396 alloy is 50 – 70 MPa (10 mm/min, 25°C) [7]. The plain strain effect is clearly evident in the SAC396 solder joint strength. Interestingly, the data showed nearly identical strength values and trends as were observed with the Sn-Pb solder over the comparable process temperatures (Fig. 4). The strength values were statistically the same for the 60s and 120s process times. The 15s process time resulted in slightly higher strengths at 240°C and 260°C; however, that difference became negligible at 290°C for all three process times. Although the strength drop was significant, the joints retained more-than-enough robustness to perform an attachment function.

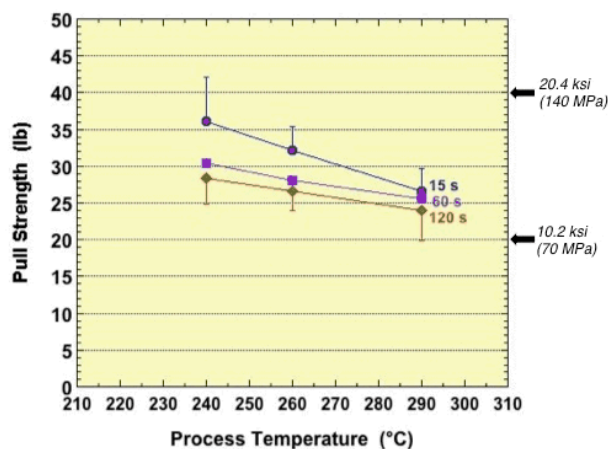


Fig. 13 Pull strength is shown as a function process temperature for the SAC396 solder joints made to the Ti-Cu-Pt-Au thin film. The error bars are one standard deviation.

Failure mode analysis

The same failure modes were observed with Pb-free solder joints as were reported upon for the Sn-Pb alloy. The test specimen is shown in Fig. 13 that was fabricated with the 240°C, 15s process conditions. The blue arrows indicated the *solder failure* mode sites; the yellow arrows point to the *thin film delamination* failure mode; and the magenta arrows identify the *LTCC divot* failure mode.

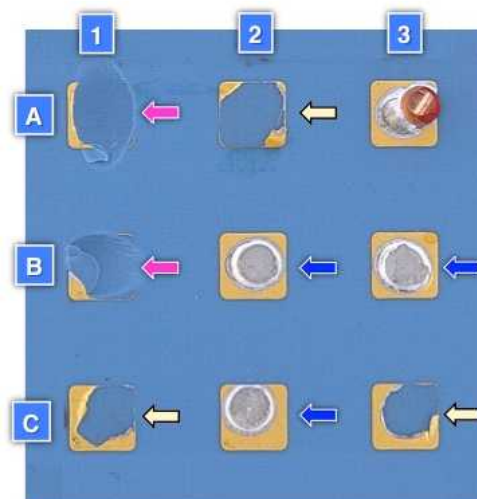


Fig. 14 Optical photograph shows the test specimen that was fabricated with the Ti-Cu-Pt-Au thin film and SAC396 solder using the 240°C, 15s process conditions. The blue, yellow, and magenta arrows indicate the *solder*; the *thin film delamination*; and the *LTCC divot* failure modes, respectively.

The occurrences of each of the failure modes as a function of process temperature were represented by the three stacked bar graphs in Fig. 15, one graph for each of the three process times. The graph in Fig. 15a (15s) shows a nearly equal presence of about 45% for both solder failure and thin film delamination modes at 240°C. The remaining failures were LTCC divots. The trend observed with the higher process temperatures of 260°C and 290°C was an increase in the solder failure mode that was accompanied by a decrease in the thin film delamination failure mode. This behavior was nearly the same as that observed for the Sn-Pb solder joints (Fig. 5a). The difference between Figs. 5a (Sn-Pb) and 15a (SAC396) was the persistence of the LTCC divot mode with the SAC396 solder. The LTCC divot mode dropped from 12% to 6% between 240°C and 260°C in Fig. 15a; it then increased to 18% at 290°C, replacing a portion of thin film delamination mode. The LTCC divot failure mode was absent from the Sn-Pb joints made at 260°C and 290°C.

The failure mode data are shown in Fig. 15b that were obtained for the 60s process time. The same general trend was observed here as was the case in Fig. 15a. There was an increased presence of solder failures at the expense of thin film delamination. This trend mimics that observed with the Sn-Pb solder and 60s (Fig. 5b), although the effect is more dramatic in Fig. 15b. Unlike the Sn-Pb case, the SAC396 solder joints retain a 6% occurrence of LTCC divots at the 290°C process temperature.

The failure mode data are shown in Fig. 15c for SAC396 joints made with the 120s soldering time. There was a consistent increase in the solder failure mode as well as an increase of the LTCC divot mode. Both behaviors came at

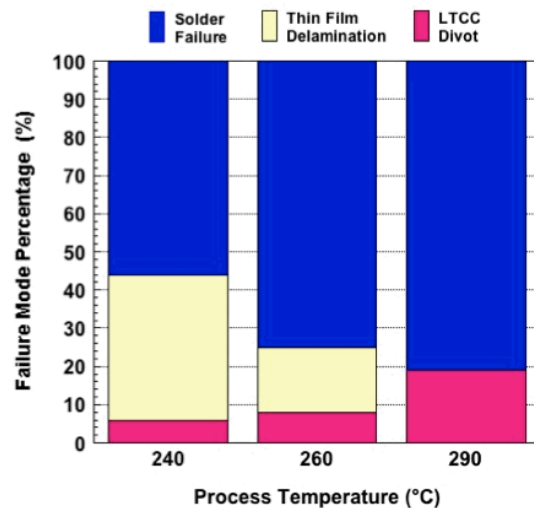
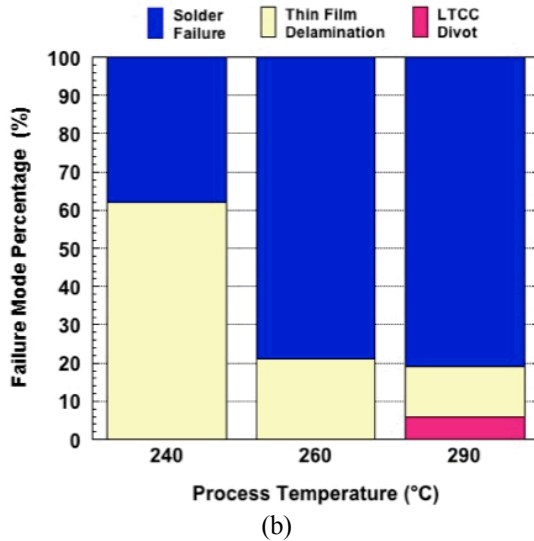
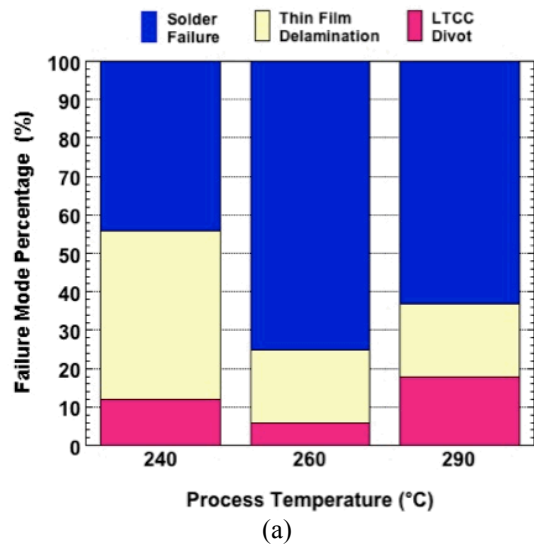


Fig. 15 Stacked bar charts show the percentages of the three failure modes as a function of process temperature for the soldering times: (a) 15s, (b) 60s, and (c) 120s. These data were obtained from the SAC396 solder joints made to the Ti-Cu-Pt-Au thin film.

the expense of the thin film delamination mode, which disappeared at the 290°C soldering temperature. The Sn-Pb solder joints did not exhibit this trend specifically between 240°C and 290°C (Fig. 5c). However, this behavior would represent the general course when the 215°C data are included in Sn-Pb analysis.)

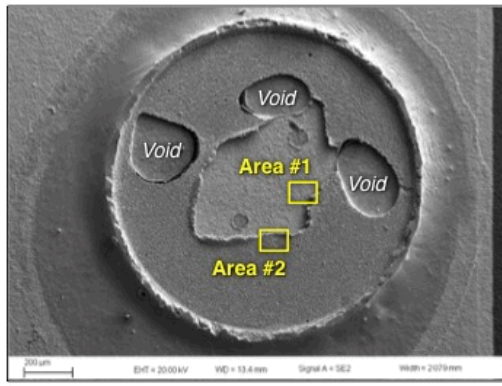
It appears that the presence of the small percentage of LTCC divot failures observed in Fig. 15b was not necessarily an isolated occurrence but, rather, evidence of a trend that became more prevalent in the test samples fabricated with the longer soldering time of 120s as shown in Fig. 15c. The LTCC divot failure mode increased from 6% to 19% across the temperatures. In the case of the Sn-Pb solder, the 120s data (Fig. 5c) likewise suggest an increased likelihood of LTCC divot failures to the higher soldering temperature (290°C).

The fracture surface morphology was examined as a function of the process conditions. The thin film delamination failure mode appeared very similar to that exhibited by the Sn-Pb solder (Figs. 6 and 7), regardless of process conditions. Also, the LTCC divot failures had a similar fracture morphology as the Sn-Pb solder joints across the process conditions.

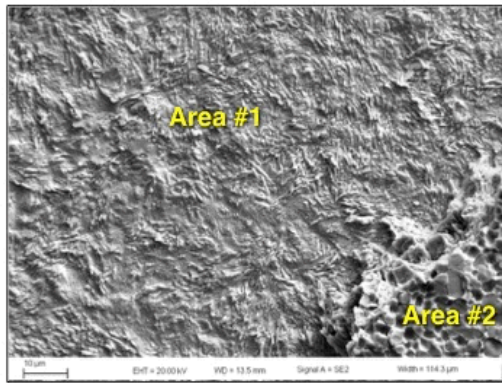
Therefore, attention was directed to differences that were particular to the solder failure mode. The fracture surface is shown in Fig. 16a that is representative of this mode on the test samples that were fabricated under the conditions of 240°C and 15s. Aside from the voids, there were two fracture morphologies denoted by Area #1 and Area #2. The Area #1 morphology, which is shown at higher magnification in Fig. 16b, exhibits the fracture surface morphology and EDX elemental distributions that are consistent with crack propagation through the Pt-Sn IMC layer and/or Pt/Pt-Sn interface. These characteristics were also similar to the Area #1 fractures of the Sn-Pb solder joints.

The Area #2 fracture surface, which dominated the morphology, is shown at higher magnification in Fig. 16c. The surface exhibits the faceted appearance of a brittle intergranular fracture that was similar to the Area #2 fracture of the Sn-Pb solder joints (Fig. 9). The EDX analysis and, in particular, the high Au signal, confirmed that the crack path had passed through the (Au-Cu)-Sn IMC layer that formed at the pin/solder interface. Crack propagation through the (Au-Cu)-Sn IMC layer was also established by EDX analysis for the Area #2 fracture surfaces of the Sn-Pb solder joints made at 215°C and 15s.

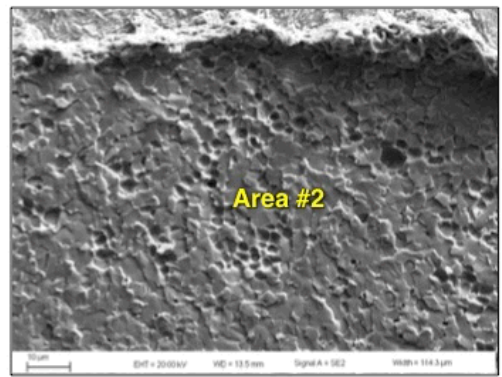
The solder failure mode fracture surfaces were also documented for the SAC396 solder joints that were formed under the harshest conditions of 290°C and 120s. The low magnification SEM/SE image is shown in Fig. 17a. The Area #1 and Area #2 morphologies are identified in the



(a)



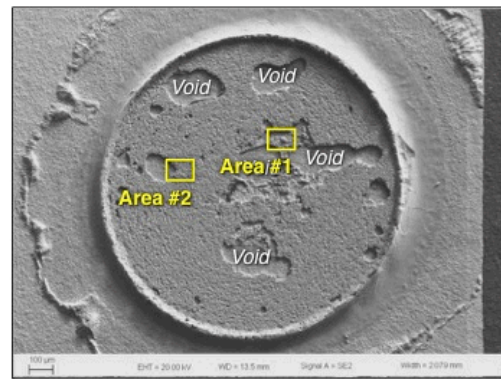
(b)



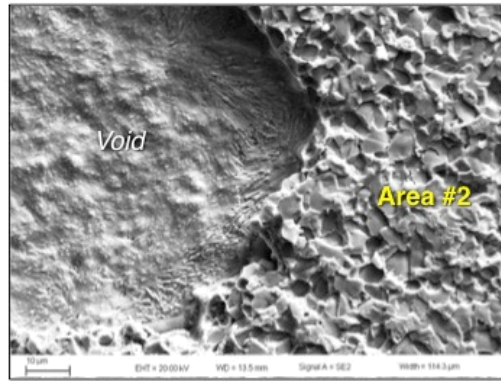
(c)

Fig. 16 (a) Low magnification, SEM/SE photograph shows the fracture surface on the LTCC substrate of the solder joint that was made to the Ti-Cu-Pt-Au thin film using the SAC396 alloy and process conditions of 240°C and 15s. The voids are identified as well as the two general fracture morphologies denoted by Area #1 and Area #2. (b) High magnification SEM/SE image illustrates the Area #1 fracture surface. (c) High magnification SEM/SE image highlights the Area #2 fracture surface.

photograph. The Area #1 morphology resembled the Area #1 surface in Fig. 16b that resulted from the Pt/Pt-Sn fracture mode. Area #2, which is shown at higher magnification in Fig. 17b, exhibited the brittle, intergranular surface morphology like that observed in Fig. 16c and the Sn-Pb solder (Fig. 9c).



(a)



(b)

Fig. 17 (a) Low magnification, SEM/SE photograph shows the fracture surface on the LTCC substrate of the solder joint that was made to the Ti-Cu-Pt-Au thin film using the SAC396 alloy process conditions of 290°C and 120s. The voids are identified as well as the two general fracture morphologies denoted by Area #1 and Area #2. (b) High magnification SEM/SE image illustrates the Area #2 fracture surface.

Referring to Figs. 16a and 17a, when the voids are removed from consideration, it was clear that the relative amount of Area #2 fracture surface was greater in Fig. 17a (290°C, 120s) than the fracture surface in Fig. 16a (240°C, 15s). This trend accompanied the reduced pull strength observed in Fig. 13 so that, overall, there was the same pull strength/failure mode correlation as was observed with the Sn-Pb solder joints.

A summary comparison was compiled between the pull strength and failure mode data of the SAC396 and Sn-Pb solder joints made to the Ti-Cu-Pt-Au thin film. Of particular interest were the *similarities*, which are listed, below:

- Comparable pull strength values over the range of process temperatures (240 – 290°C) and times (15 – 120s);
- Decrease of pull strength with increased process temperature;

- Higher pull strengths after the 15s soldering time versus the 60s and 120s soldering intervals, but that this difference diminished with increasing soldering temperature;
- Increased propensity for the solder failure mode with increased severity of the process conditions; and
- Having the solder failure mode include as significant contribution of crack propagation at pin/solder interface IMC structure.

In general, the solder failure mode and, in particular, the development of the (Cu-Au)-Sn IMC layer at the pin/solder interface appeared to control the pull strength of *both* Sn-Pb and SAC396 solder joints made to the Ti-Cu-Pt-Au thin film conductor. The point is reiterated that, although the pull strengths decreased with severity of the process conditions, the absolute values remained quite satisfactory vis-à-vis engineering applications.

A difference that did appear between the Sn-Pb and SAC396 data was the slightly greater occurrence of LTCC divots with the latter solder when comparing common processing temperatures (240 – 290°C) between the two alloys. It was concluded that the fact that, although the soldering conditions were similar, the SAC396 alloy solidified at a higher temperature (217°C) than did the Sn-Pb alloy (183°C). Therefore, there is a greater “temperature span” over which the mismatch of coefficients of thermal expansion (CTEs) between Cu, solder, and LTCC can generate *localized* residual tensile stresses in the latter. The slight increase of residual stresses was sufficient to drive an increased occurrence, albeit still limited, of the LTCC divot failures. The increased growth of the (Cu-Au)-Sn IMC layer with process temperature was a contributing factor to this scenario because the IMC phase further stiffened these joints.

In the case of the Sn-Pb solder, the residual stresses were sufficiently low that neither the CTE mismatch nor IMC “stiffening” effects could generate an appreciable frequency of LTCC divot failure modes.

The residual stress scenario cannot explain the minimum in LTCC divot formation with the 60s process time that was observed for both solder alloys (Fig. 5b, Sn-Pb and Fig. 15b, SAC396). The behavior was most evident for the SAC396 alloy due to the latter’s already heightened sensitivity to the LTCC divot failure mode. These soldering temperatures are too low to explicitly degrade the LTCC bulk material. Instead, it was concluded that the minimum in the LTCC divot failure mode at 60s was an effect of synergistic contribution in the solder joint. The change in LTCC divot frequency across soldering times was likely a secondary effect because the solder failure was the primary or failure mode. Although the solder failure mode similar predominated the 120s data, it cannot be entirely ruled out that the increased occurrence of LTCC divots introduced a

limited contribution to the lower pull strengths of the SAC396 as well as Sn-Pb solder joints.

Clearly, the above analysis is complex because the multiple materials *and* interfaces that comprise the solder joint construction contribute differently to the mechanical properties. Those interactions are not always intuitively obvious. Careful analysis of pull strengths and failure modes is required in order to identify that structure(s) that controls the mechanical performance of the solder joint. It is apparent from the above assessment that materials and interfaces *other than* those directly associated with the Ti-Cu-Pt-Au thin film controlled the mechanical properties – absolute strengths and failure modes – of both Sn-Pb or SAC396 solder joints.

Sn-Pb solder – solid-state aging

Solder joint microstructure

The analysis was omitted from this report that addresses the metallographic cross sections of the aged solder joints. An absence of evidence that there was a catastrophic loss of joint integrity under either process condition of 215°C, 15s or 290°C, 120s allowed the authors to proceed directly to the pull test analyses.

Pull strength data

The solid-state aging discussion will be limited to the Sn-Pb solder joints for brevity. The first case is that of the solder joints initially processed at 215°C and 15s. The pull strength values are shown in Fig. 18 as a function of aging time. Four traces reflect the aging temperatures.

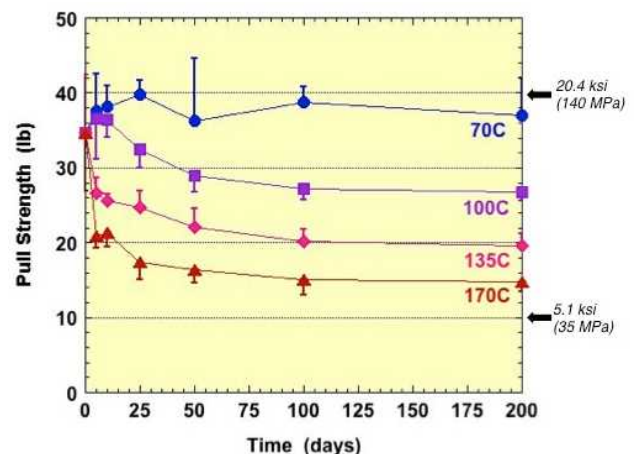


Fig. 18 Pull strength values are shown of Sn-Pb solder joints as a function of solid-state aging time. The plots of blue circles, purple squares, magenta diamonds, and red triangles represent the 70°C, 100°C, 135°C, and 170°C aging temperatures, respectively. The error bars are one standard deviation. Stress values represent, approximately, the lower and upper limits of pull strengths. The solder joints were processed at 215°C and 15s.

The stress values represent, approximately, the lower and upper limits of pull strengths. There was an absence of any significant change after aging at 70°C (blue circles) over the

entire time range of 5 – 200 days. Solid-state aging at 100°C caused a continuous decrease of pull strength with time. The pull strength of 27 ± 1 lb. at 200 days represented a 23% lower strength when compared to the 35 ± 8 lb. baseline value.

A very similar trend was observed for both the 135°C and 170°C aging temperature data in Fig. 18. However, the strength declines were clearly of a greater magnitude. After 200 days, the pull strengths had lost 43% (20 ± 2 lb.) and 57% (15 ± 1 lb.) when aging was performed at 135°C and 170°C, respectively. With only a couple of exceptions, the error bars ($\pm$ one standard deviation) remained relatively tight across the data, indicating that strength variability was not a consequence of the solid-state aging.

It is important to place the data in Fig. 18 into perspective vis-à-vis engineering applications. For example, although the joints aged at 170°C and 200 days lost more than 50% of their strength, their ability to still support 15 lb. of load (7.7 ksi, or 53 MPa of stress) represents a notable capability, especially for electronics applications.

The failure mode analysis was performed to correlate crack paths with the pull strengths. In order to avoid overly complicated plots, separate graphs of failure mode percentage versus aging time were created for each aging temperature. The graphs are shown in Fig. 19. Figure 19a shows the failure mode analysis for the 70°C data. The LTCC divot failure mode was not observed in these samples. Five days of aging resulted in primarily the thin film delamination failure mode (75%) and the remaining test sites showing the solder failure mode (25%). A similar trend was shown in Fig. 5a (215°C) if the LTCC divot failures were eliminated and the remaining failure mode scaled relative to each other. Then, the percentages calculated from Fig. 5a would be 62% and 38% for thin film delamination failures and solder failures, respectively.

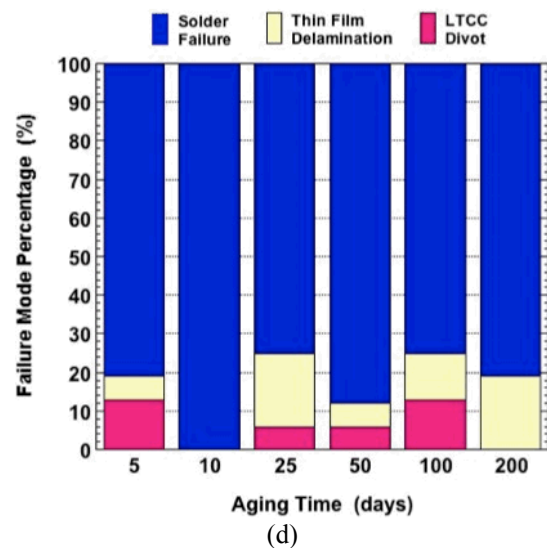
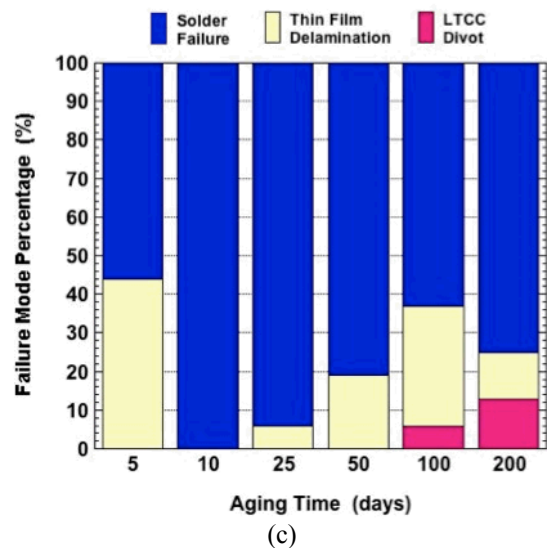
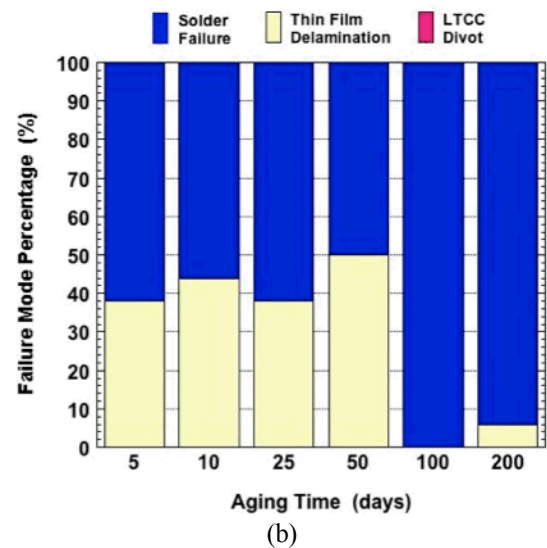
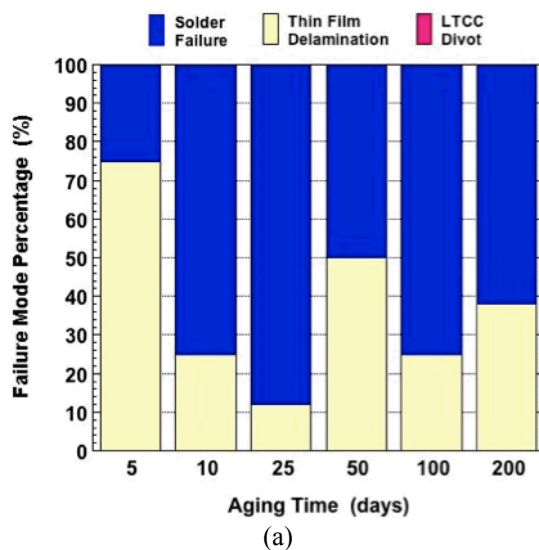


Fig. 19 Stacked bar charts show the percentages of the three failure modes as a function of solid-state aging time: (a) 70°C, (b) 100°C, (c) 135°C, and (d) 170°C. The solder was Sn-Pb and the process conditions were: 215°C, 15s.

An increase of aging time to 10 days caused a significant increase in solder failure modes at the expense thin film delamination in Fig. 19a. Further lengthening of the aging time resulted in, what appear to be, fluctuations between the two competing failure modes, although the solder failure mode remained at, or greater than, 50% of the pull test sites. A comparison was made between Fig. 19a and the 70°C plot in Fig. 18. The fluctuations in Fig. 18a matched those of the corresponding strength fluctuations in the latter plot. The higher the strength, greater was the percentage of solder failures (e.g., 25 days). This overall trend appears to be contrary to the analysis of the soldering process data whereby the prevalence of the solder failure mode was associated with a lower pull strength. Therefore, the impact of solid-state aging on joint strength differs from that of the severity of the soldering process parameters.

The chart in Fig. 19b shows the failure mode percentages for the 100°C aging temperature. The solder failure and thin film failure modes remained essentially constant at approximately 40 – 50% and 60 – 50%, respectively for aging times of 5 – 50 days. Then, the solder failure mode percentage sharply increased to over 95% after 100 and 200 days of aging. This drastic change in failure mode was not reflected in a correspondingly sharp transition in the “100°C” pull strength curve of Fig. 18. This comparison of failure mode versus pull strength indicated that, in the complex structure of these solder joints, there can be subtle changes to crack propagation behavior that do not necessarily lead to significant differences of pull strength capacity.

The 135°C aging temperature data are shown in Fig. 19c. The 45% presence of the thin film lamination after 5 days is higher than expected, given the 23% drop in pull strength versus the baseline value. At longer aging times, an unusual pattern developed in the failure mode behavior. After the solder failure mode reach a 100% maximum at 10 days of aging, it then decreased with longer aging time. First, it was replaced with small contributions of thin film delamination, 6% and 19% after 25 days and 50 days, respectively. This trend continued at 100 days with the exception that the LTCC divot failure mode appeared at 6%. After 200 days, the thin film delamination mode decreased by nearly two-thirds, being replaced with solder failures and, interestingly, a continued increase in divot failure modes.

Figure 19d shows the results of the failure mode analysis made to the samples aged at 170°C. The predominance of the solder failure mode is obvious; although it fluctuated, solder failures never fell below 65%. The remaining failure modes were mixtures of thin film delamination and a persistent presence of LTCC divots. The latter failure mode remained relatively small, being between 6% and 13%, and did not exhibit a particular trend as a function of aging time.

Referring to Fig. 18, the pull strength was compared to the failure mode data in Fig. 19d. The “170°C” curve in Fig. 18

exhibited a slight up-tick of pull strength between 5 days and 10 days, which was accompanied by an increase of the solder failure mode from 80% to 100%. This anomaly corroborates the earlier discussion of failure mode fluctuations in Fig. 19a (70°C) versus pull strength variations (Fig. 18, 70°C) and, therefore, does not appear to be simply a statistical variation. The pull strength exhibited a monotonic decrease with aging time of 25 – 200 days while the percentage of solder failures pulled back to between 75 – 88%, which was also in-keeping with the aforementioned trend.

In summary, correlations were investigated between pull strength and failure mode as a function solid-state aging time and temperature for the Sn-Pb solder joints. In the case of aging *time*, there were measurable changes of pull strength as shown in Fig. 18; but, those changes at 70°C and 100°C, although significant from an absolute value perspective, appeared to be too small to develop a significant correlation with the corresponding failure mode results in Fig. 19. In a few cases, a reduction of the solder failure mode was associated with decreased pull strength, which is contrary to the behavior recorded from the process parameter experiments. Again, the statistical significance of the data trend is relatively weak.

On the other hand, the more significant changes of pull strength with solid-state aging temperature could be correlated with the failure mode. The large drops in strength at early aging times for 135°C and 170°C were accompanied by an increase in the solder failure mode. A similar correlation was observed across aging temperature when the strength curves in Fig. 18 were compared to Fig. 19. These trends were commensurate with the earlier test data that addressed the effects of soldering time and temperature. That is, it is the solder microstructure – bulk solder and accompanying IMC layers – that control the solder joint strength, including after solid-state aging.

Test specimens were made with the Sn-Pb solder using the more severe process conditions of 290°C and 120s. The pull strength data are shown in Fig. 20. Recall from Fig. 4 that the baseline strength is relatively low: 22±2 lb. The pull strength data exhibited a measureable decrease with increasing aging temperature. However, there was not a statistically significant difference of pull strength as a function of aging time for any of the temperatures. The strength magnitudes, while low, would still provide a suitable attachment capability for electronics applications.

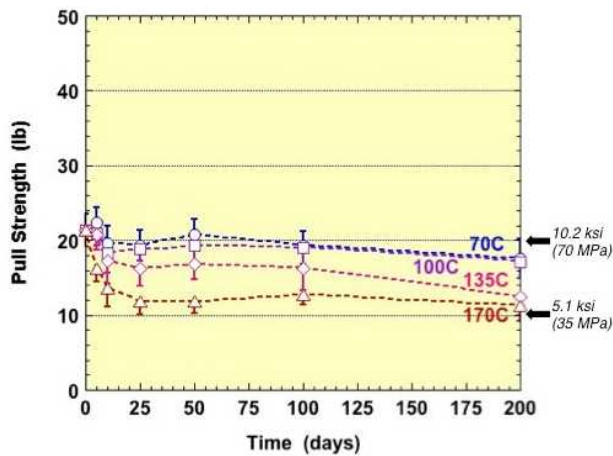


Fig. 20 Pull strength values are shown for Sn-Pb solder joints as a function of solid-state aging time. The plots of blue circles, purple squares, magenta diamonds, and red triangles represent the 70°C, 100°C, 135°C, and 170°C aging temperatures, respectively. The error bars are one standard deviation. Stress values were calculated at the upper and lower limits of pull strengths. The solder joints were processed at 290°C and 120s.

A comparison was drawn between the pull strength data in Fig. 18 (215°C, 15s) and Fig. 20 (290°C, 120s). The change in strength as a function of aging time and more so, aging temperature, was much more substantial in Fig. 18. Yet, the temperature curves in Fig. 20 appeared to “collapse” down to a similar, lower limit represented by the 170°C data in both Figs. 18 and 20. This comparison suggests that a similar mechanism is responsible for the strength loss due to either an increased severity of process conditions (290°C, 120s) or solid-state aging. The two contributions are additive towards a total effect of minimum strength represented by the 170°C curves. Harsher soldering parameters are simply more “effective” at reducing joint strength than solid-state aging exposure.

The failure mode analysis was performed on the solid-state aged, pull test sites. The failure mode data are shown in Fig. 21 for those samples aged at 70°C. One-hundred percent solder failure mode occurred across all aging times. *Except for an isolated occurrence of thin film delamination or an LTCC divot, the failure mode charts representing 100°C, 135°C, and 170°C aging temperatures were the same as that in Fig. 21.*

Certainly, the prevalence of the solder failure mode is commensurate with the reduced pull strengths observed in Fig. 20. Nevertheless, additional insight can be gained into the aging behavior of the Sn-Pb solder joints by referring back to the baseline data in Fig. 5c. In that graph, the “290°C” bar shows failure mode percentages of 49%, 38%, and 13% for solder failures, thin film delamination, and LTCC divots, respectively. Clearly, Fig. 21 (and like plots for the other aging temperatures) indicates a significant change to the fracture behavior as a result of even the mildest solid-state aging conditions of 70°C and 100°C over

5 – 10 days. Figure 20 shows only a very small change to pull strength. Moreover, these conditions cause negligible growth of the IMC layers [8]. Therefore, the failure mode analysis indicated that significant activity had taken place in the solder microstructure, but had yet to impact joint strength.

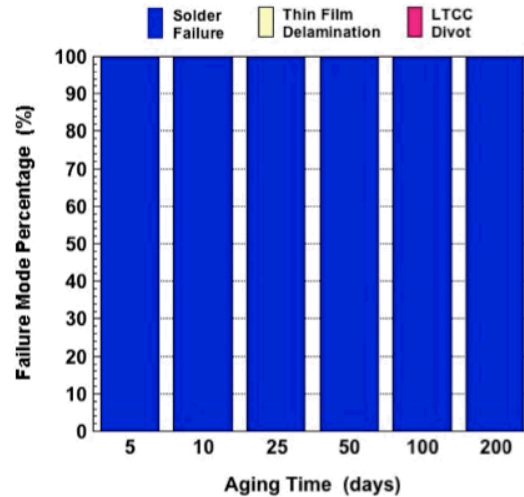


Fig. 21 Stacked bar chart show the percentages of the three failure modes as a function of solid-state aging time for a 70°C aging temperature. These data were obtained from the Sn-Pb solder joints made to the Ti-Cu-Pt-Au thin film using the process conditions: 290°C, 120s.

The fracture surfaces were investigated in order to correlate those morphologies with the failure mode exemplified by Fig. 21. Shown in Fig. 22 are SEM/BSE images that were taken from the LTCC sides of the fracture surfaces generated by pin pulls on samples fabricated with the 290°C, 120s process. The solid-state aging temperature was 100°C and the time periods were 10, 100, and 200 days. The respective failure mode charts were similar to that in Fig. 21. These images can be compared to the baseline case that is represented by the bottom SEM/BSE image in Fig. 11. The solid-state aging treatments appear to have caused an increase to the Area #1 failure mode. Recall that the Area #1 failure mode has crack propagation in the Pt-Sn IMC or at the Pt/Pt-Sn IMC interface.

There were not any noticeable changes to the fracture surface details that would suggest a reason for the preference of the Area #1 crack path versus the Area #2 path after solid-state aging. Because solid-state reactions are slow between Sn-based solders and Pt, it was surmised that, rather than there having been a slight weakening of the solder/Pt interface microstructure having caused the preference for Area #1 fracture, aging at 100°C caused a slight strengthening of the solder/Cu pin interface microstructure that “forced” the crack path to the other interface. Again, the pull strength remained essentially unchanged vis-à-vis the baseline condition. These observations indicate that the fracture surface morphology

was more sensitive to small aging effects in the Sn-Pb solder joint microstructure than was the pull strength.

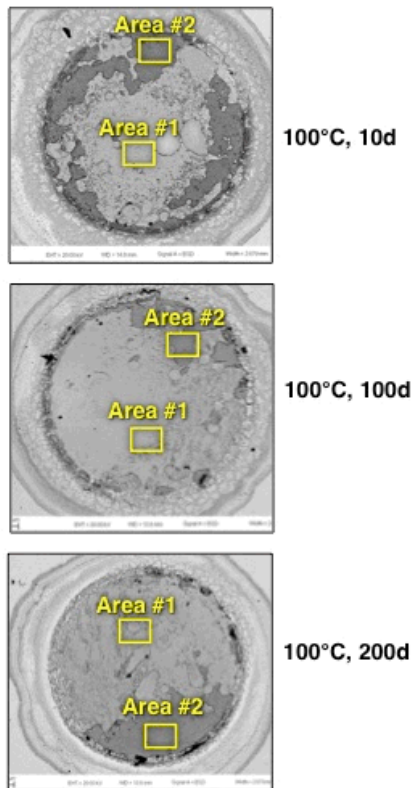


Fig. 22 SEM/BSE images show the fracture surfaces left on the LTCC side of pull tested samples that were soldered with Sn-Pb alloy at 290°C for 120s and then aged at 100°C for 10 days (top), 100 days (middle), and 200 days (bottom). The yellow boxes highlight the Area #1 and Area #2 fracture surface morphologies.

In order to assess the consistency of this trend, a second set of fracture surfaces were examined, which had also been processed at 290°C for 120s, but aged at 170°C for 10, 100, and 200 days. The respective SEM/BSE images are shown at the top, middle, and bottom positions in Fig. 23. Again, the baseline condition can be found in the bottom SEM/BSE image of Fig. 11. The failure mode chart was almost identical to that in Fig. 21.

The fracture surface exhibited the same two basic Area #1 and Area #2 morphologies. The solid-state aging caused generally an increased presence of the Area #1 morphology former morphology versus the baseline case. However, a similar trend was not consistently observed as a function of solid-state aging time in Fig. 23. This seeming inconsistency is rooted in the fact that solid-state aging at 170°C caused a greater mixture of smaller Areas #1 and #2 distributed across the surfaces. This behavior was not observed in Fig. 11 or in Fig. 22.

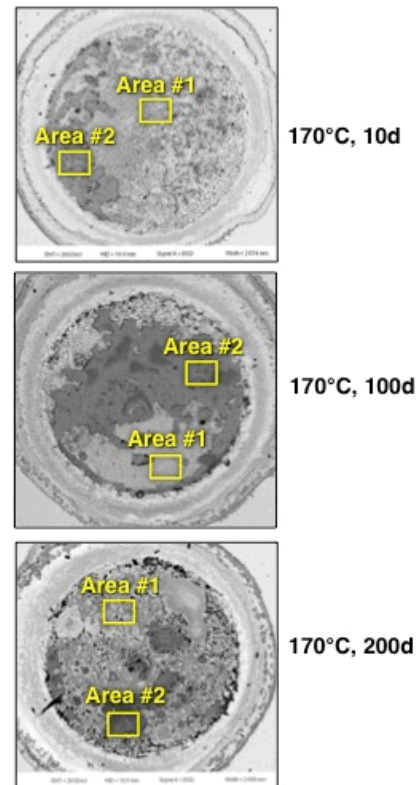


Fig. 23 SEM/BSE images show the fracture surfaces left on the LTCC side of pull tested samples that were soldered with Sn-Pb alloy at 290°C for 120s and then aged at 170°C for 10 days (top), 100 days (middle), and 200 days (bottom). The yellow boxes highlight the Area #1 and Area #2 fracture surface morphologies.

A summary analysis was made by compiling together the fracture surface morphology observations; the failure mode data; and the pull strength results as a function of solid-state aging. The following generalizations were developed:

- Solid-state aging decreased the pull strength of the Sn-Pb solder joints, but not so in a catastrophic manner that would render them inadequate to function in an electronics application
- The strength loss was accelerated by harsher, initial solder conditions.
- Reduced strengths were accompanied by an increased preference for the *solder failure* mode.
- The fracture surface morphology (crack path) was the most sensitive metric to either soldering process and/or solid-state aging effects on the Sn-Pb solder joints.
- Aside from the role of the Pt-Sn IMC layer in the fracture surface morphology (Area #1), the adhesion and integrity of the Ti-Cu-Pt-Au thin film did not control the mechanical performance of the Sn-Pb solder joints.

CONCLUSIONS

1. A study was performed to evaluate the mechanical properties of solder of solder joints made to a 0.200Ti-4.0Cu-2.0Pt-0.25Au (μm) thin film conductor on low-temperature co-fired ceramic (LTCC) substrates.
2. The solder joints were made with 63Sn-37Pb (wt.%, abbreviated Sn-Pb) or the 95.5Sn-3.9Ag-0.6Cu (SAC396) alloys; although the majority of the analysis targeted the Sn-Pb solder joint.
3. Pull strength and failure modes were analyzed as a function of soldering temperature (215 – 290°C) and soldering time (15 – 120s). The effects of solid-state aging (70 – 170°C; 5 – 200 days) were assessed for the Sn-Pb solder joints.
4. Both Sn-Pb and SAC396 solder joints exhibited similar pull strength magnitudes as well as a nominal loss of such strength with increased severity of the process conditions. The decrease of strength, which was accompanied by an increased occurrence of the solder failure mode, was sensitive to the soldering temperature and time.
5. Solid-state aging of Sn-Pb solder joints caused a general decrease of pull strength. The strength change was greatest between aging temperatures and was more dramatic for samples fabricated under the 215°C, 15s conditions due to the higher, initial strength. The strength loss with solid-state aging was accompanied by the same increased preference for the solder failure mode as observed as a function of process parameters.
6. The fracture surface morphology (crack path) was more sensitive to the effects of both soldering process and solid-state aging than was the more generalized failure mode metric or the pull strength performance.
7. Aside from the role of the Pt-Sn IMC layer in the fracture surface morphology (Area #1), the adhesion and integrity of the Ti-Cu-Pt-Au thin film did not control the mechanical performance of the Sn-Pb solder joints.
8. This report clearly illustrates that the complexity of solder joint requires that a careful analysis be made of (a) pull strength, (b) failure mode, and (c) fracture morphology (crack propagation) in order to thoroughly understand the structure(s) that control mechanical properties in an effort to optimize the performance of electronic interconnections.

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