# Thermal Conductivity Manipulation in Lithographically Patterned Single Crystal Silicon Phononic Crystal Structures

Bongsang Kim, Janet Nguyen, Charles Reinke, Eric Shaner, Charles Harris, Ihab El-Kady, and Roy Olsson III
Advanced MEMS Department
Sandia National Laboratories
Albuquerque, NM USA
bonkim@sandia.gov

*Abstract*— **Thermal conductivity of single crystal silicon was engineered using lithographically formed phononic crystals. Specifically sub-micron periodic through-holes were patterned in 500nm-thick silicon membranes to construct phononic crystals, and through phonon scattering enhancement, heat transfer could be significantly reduced. The thermal conductivity of silicon phononic crystals was measured as low as 32.6W/mK, which is ~75% reduction compared to bulk silicon thermal conductivity [1]. This corresponds to 37% reduction even after taking the contributions of the thin-film and volume reduction effects, while its electrical conductivity reduces as much as volume reduction effect. The demonstrated method uses conventional lithography-based technologies that are directly applicable to diverse micro/nano-scale devices, leading toward huge performance improvements where heat management is important.**

*Index Terms*—**phononic crystals, phonon scattering, boundary scattering, thermal conductivity, heat transfer, thermal model**

## I. Introduction

Heat management is becoming more and more important in many MEMS/NEMS devices. For example, thermal actuator is one of the most widely used transducer mechanisms in MEMS devices where large displacement and large actuation forces are needed [2]. Recently demonstrated ovenized micromechanical resonators use localized heating to compensate the temperature induced frequency drift [3]. Micromachined thermoelectric converters are being noticed as the next generation energy harvesters generating electrical power from wasted heat [4]. In such applications, dealing with the heat transfer is one of the critical for the best performance.

However, in many cases, the issues of thermal management are often coupled with the electrical conductivity issues, making the problem more complicated. For example, in ovenized resonators, high thermal isolation of the device from the surroundings is required to improve energy efficiency, however at the same time, high electrical conductivity is desired for better signal processing. In thermoelectric energy harvesters, their figure of merit is determined by the ratio between thermal conductivity and electrical conductivities. To maximize the amount of harvesting energy, low thermal conductivity and simultaneously high electrical conductivity are needed. In general, however, these two conductivities move in the same direction; if thermal conductivity increases, electrical conductivity also increases, and vice versa, therefore, heat management coupled with electrical transfer issue is not a trivial problem.

Indeed, manipulation of phonons, or lattice vibrations, is an effective way to deal with heat transfer problems in micro/nano-machined structures. Unlike metals where both heat and electricity is transferred through electrons, in many semiconductor materials, thermal conduction is dominated by phonon while electrical conduction is through electron. In semiconductors, the contained thermal energy is transferred through the vibration of the adjacent lattices. For example, in silicon, phonons of frequencies ranging from GHz to THz take charge of heat transfer. Therefore, if only phonons can be manipulated in such materials, it is possible to control thermal conductivity while leaving electrical conductivity intact.

Reduction in thermal conductivity has been frequently observed in micro/nano machined structures such as thin-film deposited silicon and nanowires [5, 6].This is because as critical dimensions of heat pathways (thickness of thin film or width of nanowires) become comparable to the phonon mean-free-path, phonon scattering increases, resulting in reduction in thermal conductivity. This is also applicable by patterning features. For instance, through nano-holes patterned in a silicon membrane, significant reduction in thermal conductivity has been demonstrated [7]. Despite such promising results, however, due to complexity of the fabrication processes and lack of effective integration methods, very few examples of application could be found among the demonstrated structures.

Alternately, a much simpler way of phonon manipulation has been demonstrated with the recent advances in lithographic technologies [8]. For example, phononic crystals were fabricated by lithographically defined sub-micron holes in a silicon layer to construct waveguides successfully achieving 30dB

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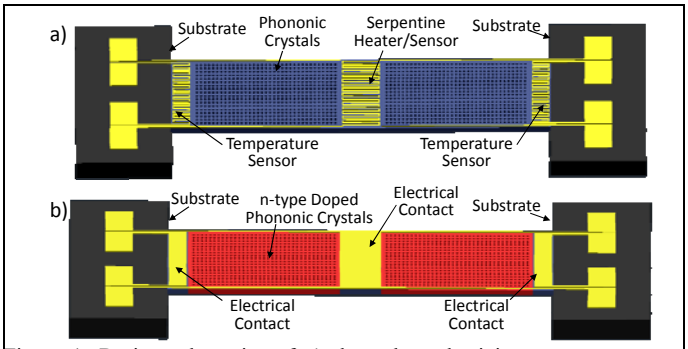


Figure 1. Design schematics of a) thermal conductivity measurement test structure and b) electrical conductivity measurement test structure.

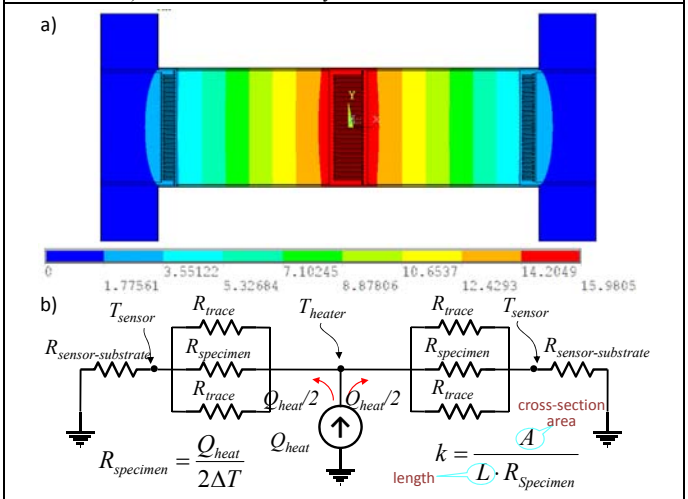


Figure 2. a) ANSYS FEM simulation model of thermal conductivity test structure and b) the equivalent thermal circuit model.

acoustic rejection at 67MHz for RF communication applications. Lithography-based phononic crystals have much more flexibility and controllability allowing much broader and direct applications into many existing micro/nano-machined devices.

In this work, we have investigated heat and electrical transfer in lithographically defined single crystal silicon phononic crystals. Conductivity measurement test structures were designed, modeled, and fabricated using conventional micro/nano-machining technologies. Both thermal and electrical conductivities of phononic crystal test structures were measured and compared together with ANSYS FE modeling of volume reduction effects. Then, the discussion about the impact of phonon manipulation on heat transfer is followed.

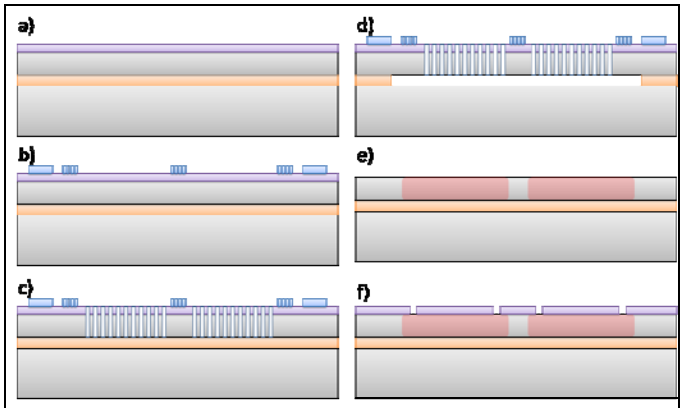


Figure 3. Cross-section view of fabrication process. Step e and f are needed only for the electrical conductivity measurement test structure fabrication.

## II. Test Structure

### *A. Test Structure Design*

Figure 1a illustrates the test structure design for thermal conductivity measurement. The structure is symmetric bridge shaped. A 250um-wide serpentine trace functioning both as a heater and temperature sensor, is placed in the middle. Two more serpentine-shaped temperature sensors are installed at both bridge ends. Between these serpentine traces, phononic crystals were patterned by punching periodic holes. While heat is supplied at the center, by measuring the temperature difference across the bridge, the device thermal characteristics can be extracted. Figure 2 shows the equivalent thermal circuit model of the designed thermal conductivity test structure. Since all measurement was conducted in vacuum, convectional heat leak can be ignored. Also radiation heat transfer was estimated maximum 0.4% compared to conductive heat transfer, therefore, also was ignored in these models.

In Figure 1b, the test structure design for the electrical conductivity measurement is illustrated. The structure design is very similar to the thermal conductivity test structure. However, the bridge membrane is n-type, and electrical via contacts are installed instead of serpentine traces at the bridge center and the bridge ends.

The complete design sets of hole pitches (lattice constants) and hole diameters as well as corresponding limiting dimensions for both test structures are summarized in Table 1.

### *B. Device Fabrication*

Table 1. Summary of device design parameters and measured thermal conductivities and electrical conductivities. For each device design, total 6 devices were measured. Device ID-1 is the control device which doesn't have any holes in the membrane.

| **Device ID** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** | **16** | **17** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A, lattice constant (nm) | N/A | 500 | 500 | 600 | 600 | 600 | 700 | 700 | 700 | 700 | 700 | 800 | 800 | 800 | 800 | 800 | 900 |
| D, diameter (nm) | N/A | 213 | 303 | 204 | 295 | 365 | 209 | 294 | 360 | 424 | 486 | 290 | 357 | 419 | 479 | 535 | 532 |
| L, limiting dimensions(nm) | N/A | 286 | 196 | 395 | 304 | 234 | 491 | 405 | 339 | 275 | 213 | 509 | 442 | 380 | 320 | 265 | 367 |
| mean $k_m$ (W/mK) | 104 | 63.3 | 42.4 | 73.7 | 56.3 | 42.8 | 79.4 | 65.7 | 54.1 | 43.3 | 32.6 | 72.2 | 63.4 | 53.5 | 44.4 | 35.8 | 45.1 |
| standard dev. $k_m$ (W/mK) | 1.4 | 1.3 | 1.6 | 1.5 | 1.3 | 1.4 | 1.0 | 1.4 | 1.2 | 1.4 | 1.3 | 1.1 | 1.1 | 1.1 | 1.2 | 1.2 | 1.0 |
| $\sigma_m$ (S/cm) | 0.541 | 0.726 | 1.017 | 0.657 | 0.810 | 1.010 | 0.626 | 0.724 | 0.836 | 0.996 | 1.246 | 0.674 | 0.745 | 0.843 | 0.972 | 1.143 | 0.952 |
| $k_m / k_{m,control}$ | 1 | 0.608 | 0.408 | 0.708 | 0.541 | 0.412 | 0.763 | 0.632 | 0.520 | 0.416 | 0.313 | 0.694 | 0.609 | 0.514 | 0.427 | 0.344 | 0.434 |
| $\sigma_m / \sigma_{m,control}$ | 1 | 0.744 | 0.532 | 0.823 | 0.668 | 0.535 | 0.864 | 0.747 | 0.647 | 0.543 | 0.434 | 0.802 | 0.726 | 0.641 | 0.556 | 0.473 | 568 |
| $F_{FEM}$ | 1 | 0.750 | 0.551 | 0.834 | 0.679 | 0.547 | 0.871 | 0.757 | 0.655 | 0.551 | 0.447 | 0.813 | 0.729 | 0.645 | 0.558 | 0.478 | 0.568 |
| mean $k_n$ | 1 | 0.805 | 0.736 | 0.844 | 0.790 | 0.747 | 0.871 | 0.829 | 0.787 | 0.750 | 0.696 | 0.847 | 0.83 | 0.792 | 0.759 | 0.714 | 0.759 |
| standard dev0. $k_n$ | 0 | 0.006 | 0.017 | 0.008 | 0.007 | 0.013 | 0.008 | 0.009 | 0.007 | 0.013 | 0.017 | 0.007 | 0.003 | 0.005 | 0.009 | 0.013 | 0.007 |

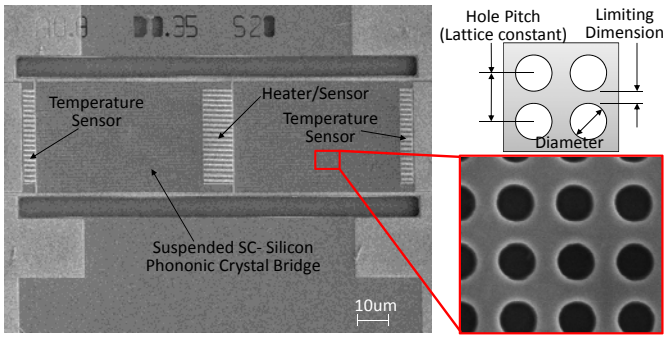

Figure 4. SEM images of the fabricated phononic crystal test structure.

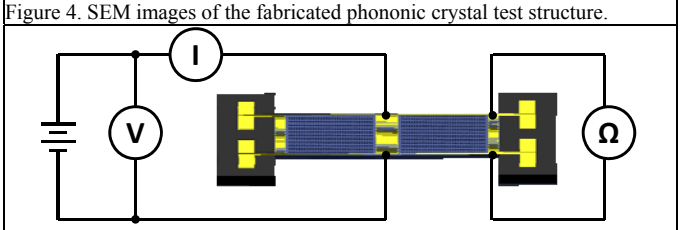

Figure 5. Test setup diagram for thermal conductivity measurement

Figure 3 shows the schematics of thermal conductivity test structure fabrication process0. The fabrication starts with 6-inch SOI wafers0. The device layer is 500nm-thick lightly p-type doped (boron $10^{16}$) single crystal silicon0. On top of the SOI wafers, 100nm of undoped amorphous silicon is blanket deposited as an electrical isolation layer between the underlying device layer and the following metal contact layer (Figure 3a). Via high temperature annealing, the high stress in the amorphous silicon layer is released. Then, aluminum is deposited and patterned as heaters, temperature sensors, interconnects, and bondpads (Figure 3b). Using plasma etching, phononic crystals and release trenches were defined in the silicon layers (Figure 3c). As the final step, the buried oxide ($SiO_2$) underneath the test structure is removed by timed HF vapor etch to release the bridge (Figure 3d). Figure 4 shows SEM images of a fabricated thermal conductivity test structure.

Electrical conductivity test structures were fabricated in 250nm-thick single crystal silicon device layer. Two more extra steps were added for these devices: 1) before depositing amorphous silicon, phosphorous implantation was conducted for the localized n-type doping (target concentration: $10^{20}/cm^3$) of the bridge membrane (Figure 3e), and 2) after the amorphous silicon deposition, electrical via contacts were etched penetrating insulation layer (Figure 3f).

## III. Measurement

First, the temperature dependence of resistances of both the heater serpentine trace at the bridge center and temperature sensor traces at the bridge ends were calibrated. In a separate heated chuck measurement, both traces exhibited almost identical relative resistance change due to temperature change, with the measured TCR (temperature coefficient of resistance) of 0.0027.

Figure 5 shows the thermal resistance measurement setup diagram. Heat is supplied at the center of the test structure by applying power across the serpentine heater. By measuring the voltage across the heater and the current through it, both the supplied heat and resistance change can be simultaneously monitored. At the same time, the resistance change of the sensor traces at the bridge ends is also measured. Using the above TCR=0.0027, the temperature changes of the heater and sensors are calculated. All measurements were conducted in vacuum (< 1mTorr) while sweeping the heating power from 0 to 1 mW and back to 0 again. Figure 6 shows an example plot of the measured temperature vs. heating power. From measured data, using the thermal models shown in Figure 2, the thermal resistances across the phononic crystals were extracted and by multiplying cross section areas and dividing by the length, thermal conductivities, $k_m$, were calculated for each measured points. All the measured thermal conductivity data are summarized in Figure 7a and Table 1.

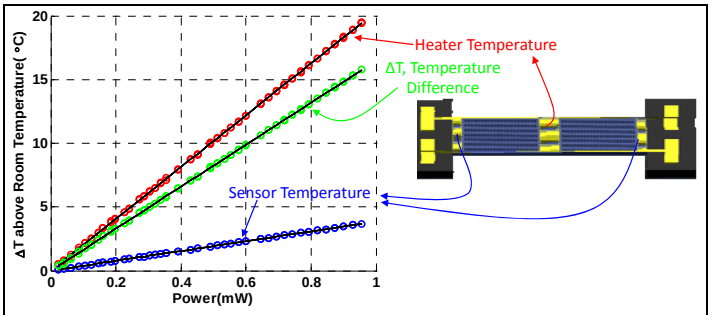

Figure 6. An example plot of measured temperature vs. heating power plot (Device ID-7). Temperature difference across the phononic crystal bridge was measured using calibrated serpentine traces while heating power supplied at the bridge center was sweeping between 0 to 1mW.

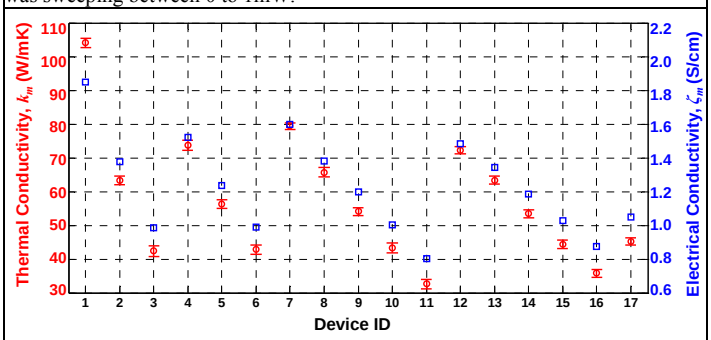

Figure 7. Measured thermal conductivities (red) and electrical conductivities (best) of phononic crystal test structures.

Electrical conductivity across the phononic crystal bridges was also measured. While power was supplied across the half of the bridge, its current and voltage were measured and the corresponding resistance was calculated. Extracted electrical conductivity values, $\sigma_m$, are summarized in Figure 7b and Table 1 as well.

## IV. Result

As can be seen in Figure 7, all the samples containing holes (phononic crystals) showed significant reduction in both thermal and electrical conductivity compared to the control device (Device ID-1), which didn't have any holes.

To understand real phononic effect, how much of a portion of the reduction in conductivity came from the volume reduction by introducing the through holes was evaluated using ANSYS FE simulation as shown in Figure 8a. Since this ANSYS simulation models only continuum effect (Fourier's

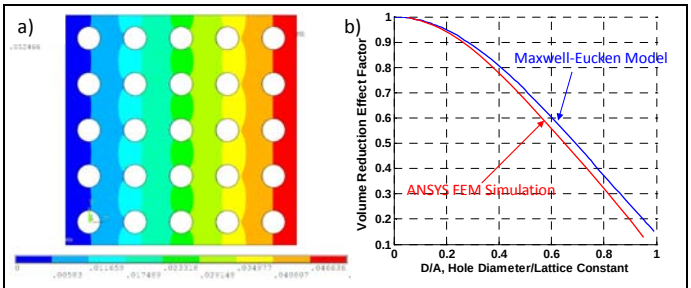


Figure 8. a) ANSYS FEM simulation for the effective conductivity reduction by introducing periodic holes. This model captures only classical volume reduction effect, not any phononic effect. b) Volume reduction effect factors, $\zeta_{FEM}$ , vs. hole diameter/lattice constant.

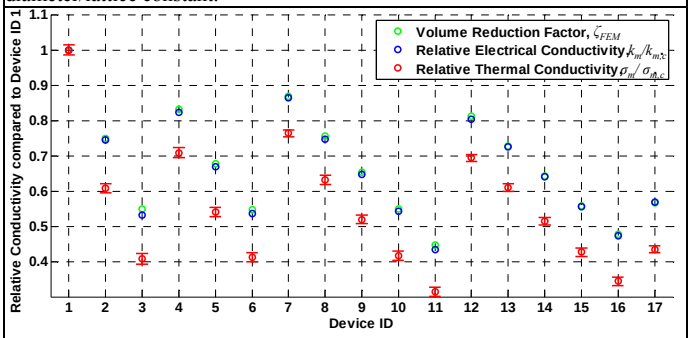


Figure 9. Comparison between $k_m/k_{m,control}$, $\sigma_m/\sigma_{m,control}$, and $\zeta_{FEM}$. The measured $\sigma_m/\sigma_{m,control}$ match very well with $\zeta_{FEM}$ for all Device IDs. Some data points it is not easy to tell the difference because they exactly overlap with each other. However, the $k_m/k_{m,control}$ ratios are much smaller than $\zeta_{FEM}$ for all cases, inferring a reduction in the thermal conductivity is beyond the contribution from the volume reduction effect.

law for the thermal conductivity and Ohm's law for the electrical conductivity), not any phononic effect, the absolute dimension doesn't matter, only the relative ratio between hole sizes and pitches matters. Figure 8 plots the volume reduction effect factor, $\zeta_{FEM}$ , as a function of the material porosity.

Table 1 and Figure 9 compare the relative thermal and electrical conductivity compared to the control sample for each device design as well as their corresponding volume reduction effect factor, $\zeta_{FEM}$, modeled in Figure 8. As can be seen, for all samples, the ratio of the thermal conductivities, $k_m/k_{m,control}$, (relative thermal conductivity with respect to the control device), were much lower than that predicted from ANSYS FE simulation. In contrast, the ratio of the electrical conductivities, $\sigma_m/\sigma_{m,control}$ (relative electrical conductivity with respect to the control device), measured from n-type doped samples with the same hole pitches and diameters, match very well with the simulated volume reduction effect. These results suggest that inclusion of sub-micron periodic holes reduced the thermal conductivity much beyond the contribution from the volume reduction effect, whereas the electrical conductivities are reduced simply by the amount of volume reduction.

To evaluate phononic impact on thermal conductivity, all measured relative thermal conductivity values are normalized by the simulated volume reduction effect, i.e.,

$$k_n = \frac{k_m / k_{m,control}}{\zeta_{FEM}} \quad (1)$$

Figure 10 compares these normalized thermal conductivities, $k_n$, versus limiting dimension (spacings between holes) with the same lattice constant. This $k_n$ indicates how much the thermal

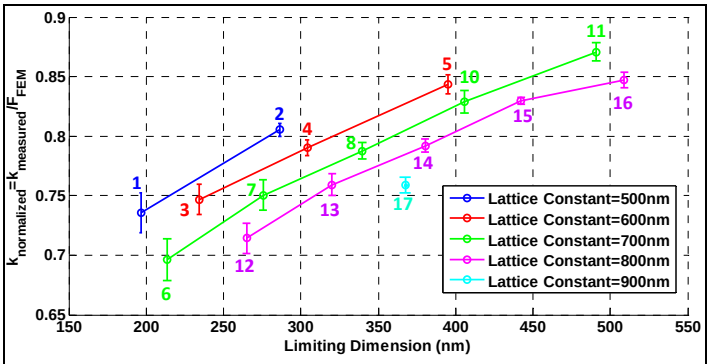


Figure 10. Comparison of $k_n$ versus limiting dimension with the same lattice constant. As the limiting dimension decreases, the $k_n$ decreases, which indicates that incoherent scattering plays a significant role to reduce thermal conductivity of phononic crystals. Numbers adjacent the data points are the Device ID. Each data is from 6 measured devices.

conductivity is reduced beyond the contribution from the volume reduction effect. For example, Device ID-11 measured $k_n$=0.696 in Figure 10, which means thermal conductivity is reduced 30.4% additionally, even after taking the volume reduction effect account. For all measured devices, $k_n$, consistently decreases as the limiting dimension decreases, inferring phonon scattering plays a significant role in the thermal conductivity reduction.

## V. Conclusions

It has demonstrated that thermal conductivity of single crystal silicon can be effectively engineered using lithographically patterned phononic crystals. By introducing sub-micron diameter periodic through holes, electrical conductivities of the phononic crystal membranes were changed only by the amount of volume reduction effect, while their thermal conductivities much further due to the enhanced phonon scattering. The demonstrate approach has huge potentials. Phononic crystals could be constructed by using only conversional lithography techniques, which not only opens direct applications to many micromachined devices without much modification in the original fabrication process but also allows their repeatable mass production.

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