SAND2011-1007C

Micro-fabricated surface ion traps with arbitrary lateral geometries

D. Stick, F. Benito, M.G. Blain, R. Cook, M. Descour, A.R. Ellis, K.M. Fortier, R.A. Haltli, C. Highstrete, S.A. Kemme, D.L. Moehring, B.P. Tabakov, C.P. Tigges

Sandia National Laboratories

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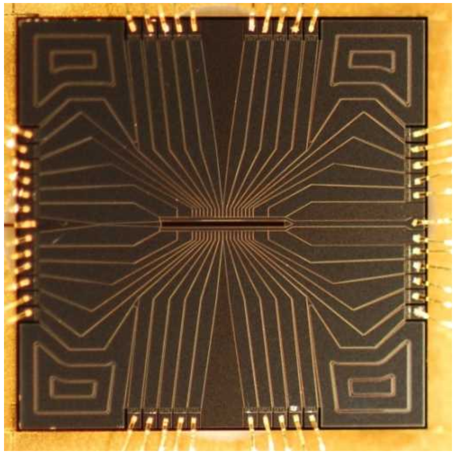
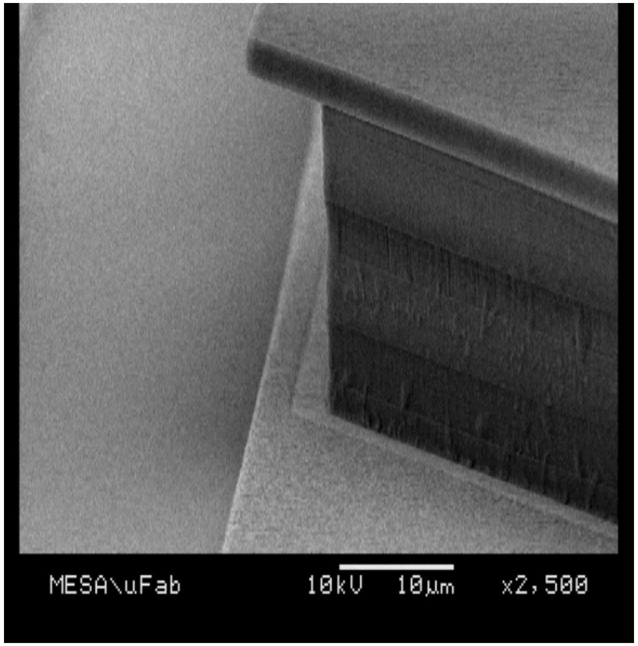
Outline

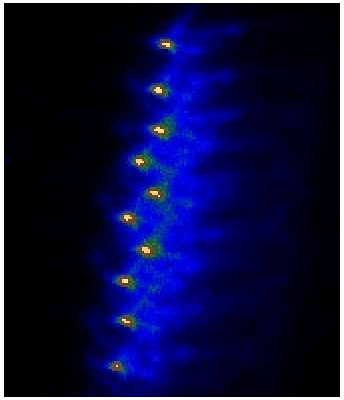
- Status of current devices
  - Linear trap, Y trap
- Current fabrication techniques
  - Loading holes, 2 level metallization
- Future fabrication techniques
  - 4 level metallization, trench capacitors
- Future devices
- Conclusion

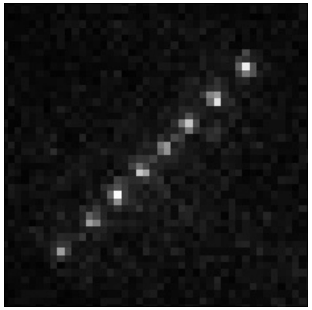
Status of current devices::Linear trap

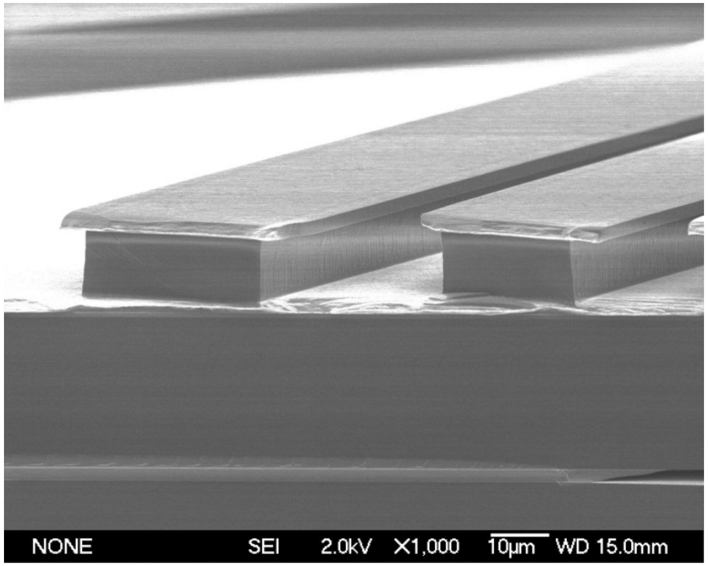


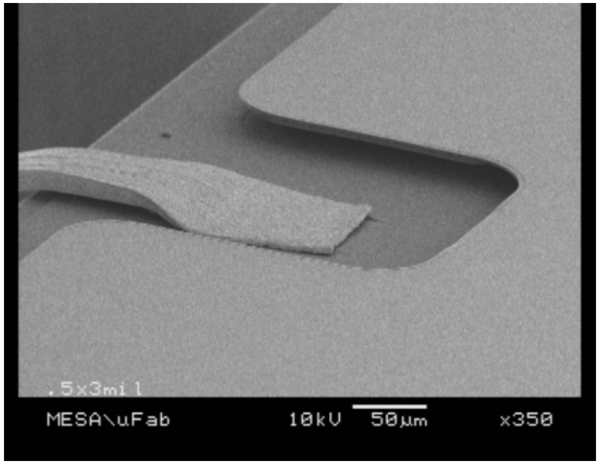
- Devices successfully demonstrated by multiple groups: SNL, Oxford, Maryland, MPQ,
  - used same control voltages
- Un-cooled lifetime: 15 – 120s







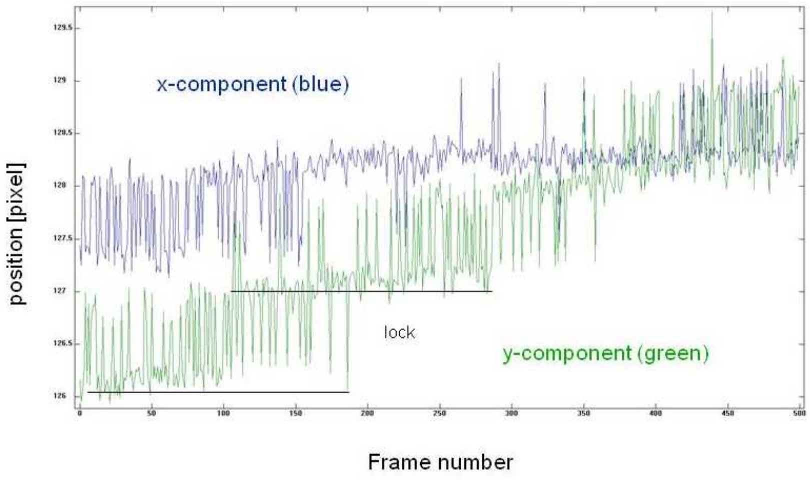


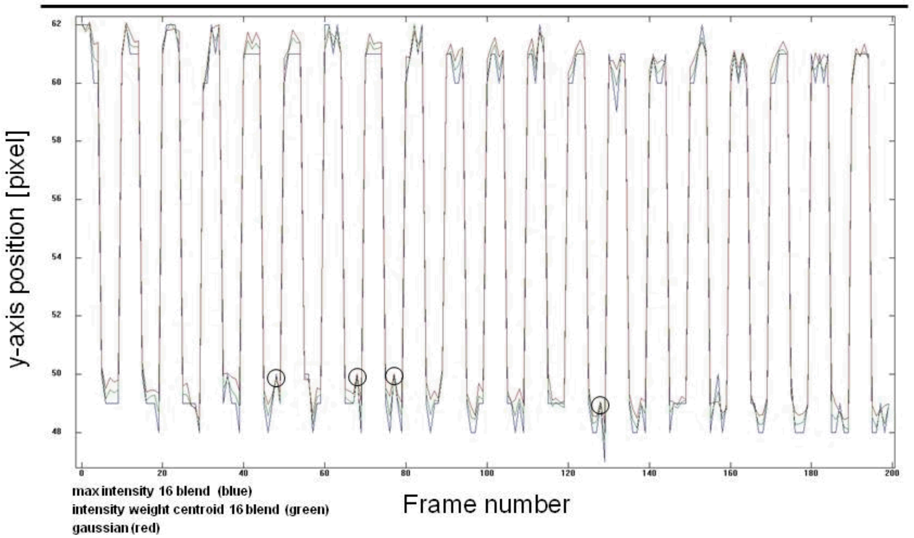


Status of current devices::Linear trap

- Micromotion compensation:
  - No capacitors: unable to compensate micromotion
  - Capacitors only on inside DC rails: compensates micromotion in plane, uncompensated out of plane
  - Capacitors on all electrodes: compensated: 1 – 10 V/m compensation

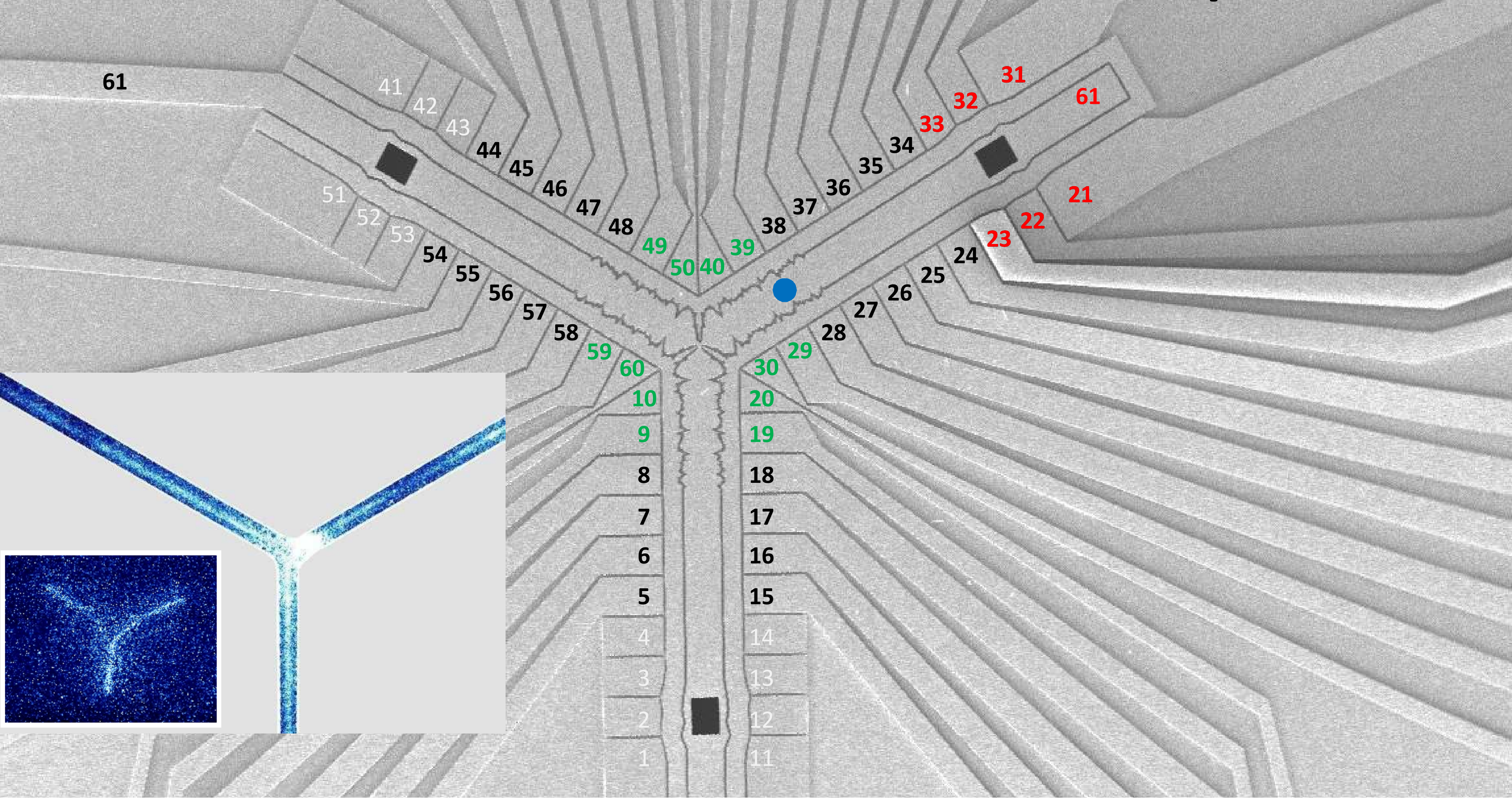
- Drift: over 5 hours (with repeated loading), compensation drifted by 10 – 40 V/m





- Heating rate:
  - $S_E(\omega)$ = 5 x 10^{-11} $(V/m)^2$/Hz for one trap, 5 x 10^{-10} for another

Status of current devices::Y trap



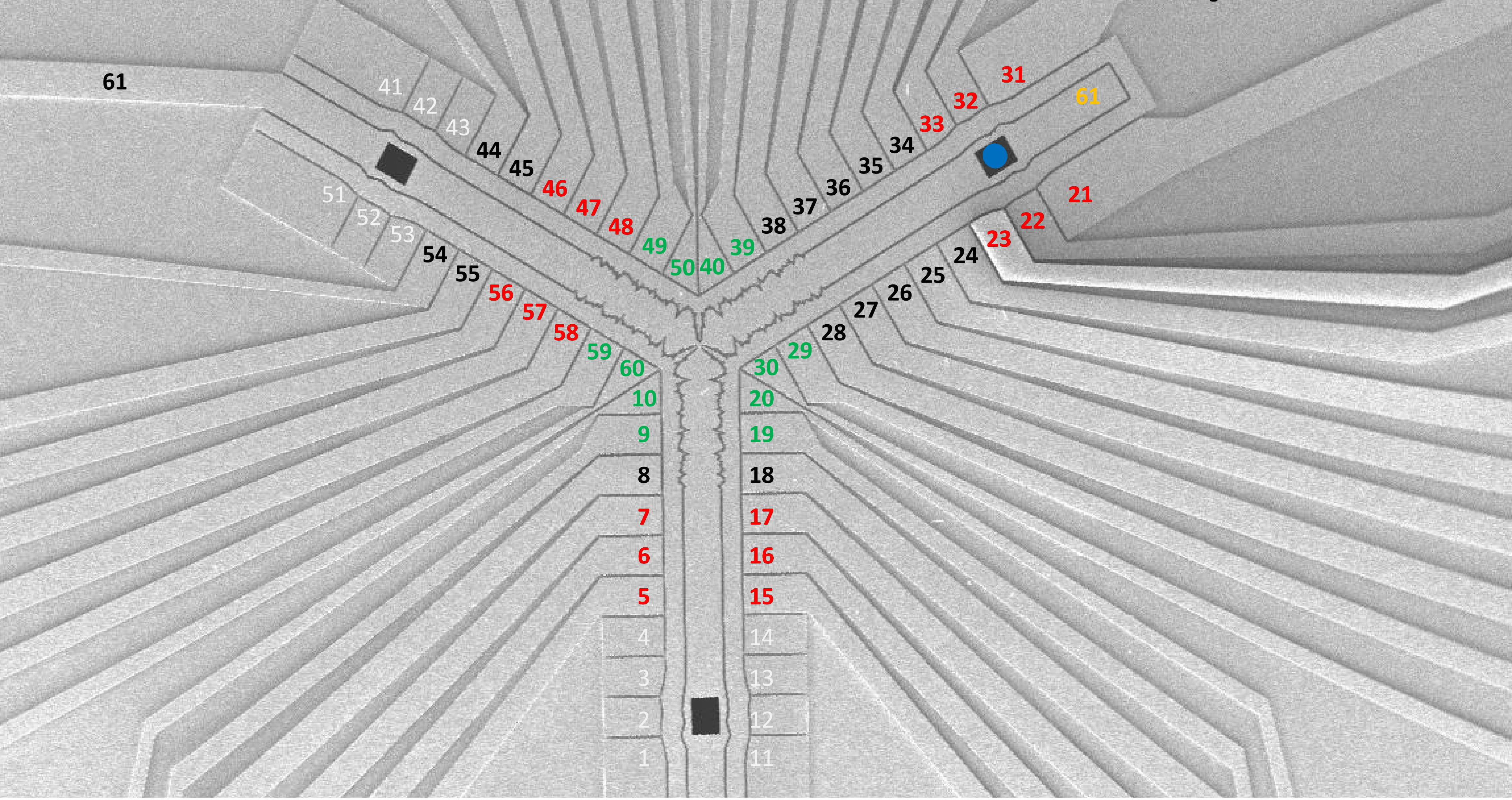
1 Million junction shuttles without ion loss

Including 250 microns up each arm

Linear shuttling uses only 7 closest electrodes at any given times (example shown in red).

Junction shuttling uses only 13 electrodes (shown in green + e61).

Status of current devices::Y trap

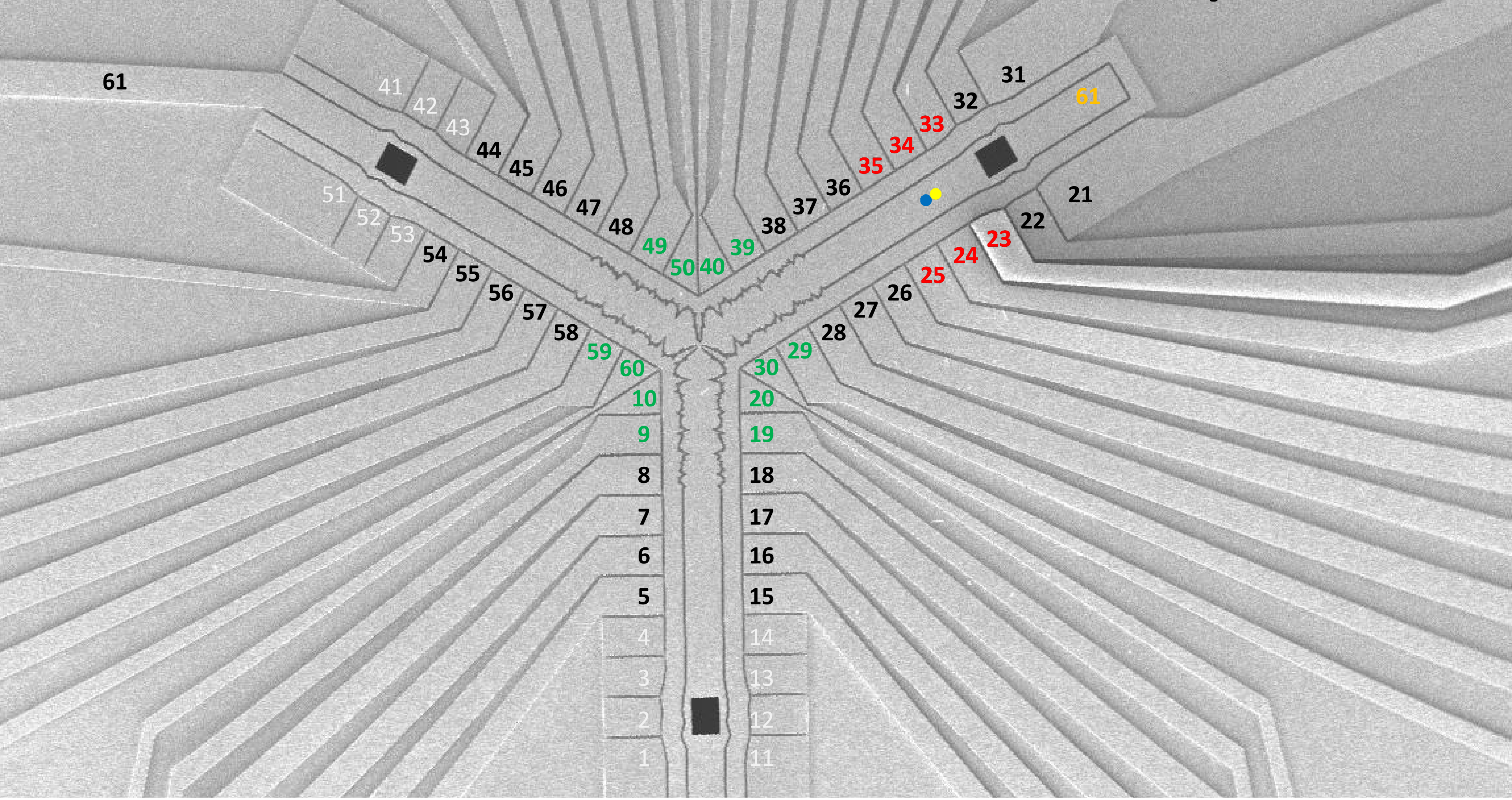


Shuttling to all regions of trap with ions in multiple wells

1 ion trapped in each arm for over an hour

Linear shuttling varying only 6 closest electrodes at any given time (examples shown in red).
Junction shuttling uses only 12 electrodes (shown in green). e61 constant at all times (orange).

Status of current devices::Y trap

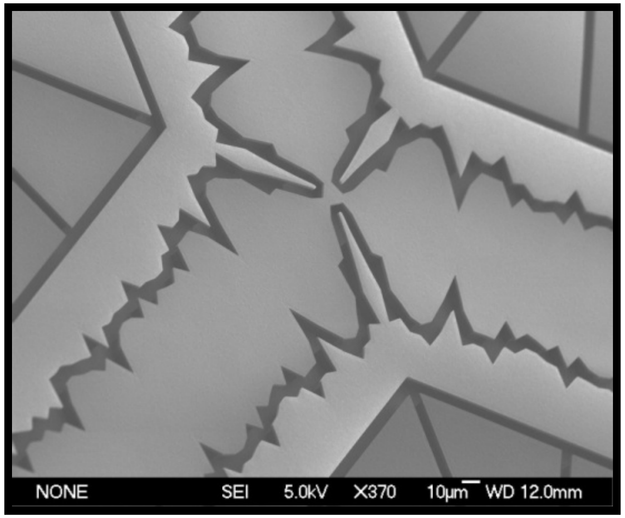


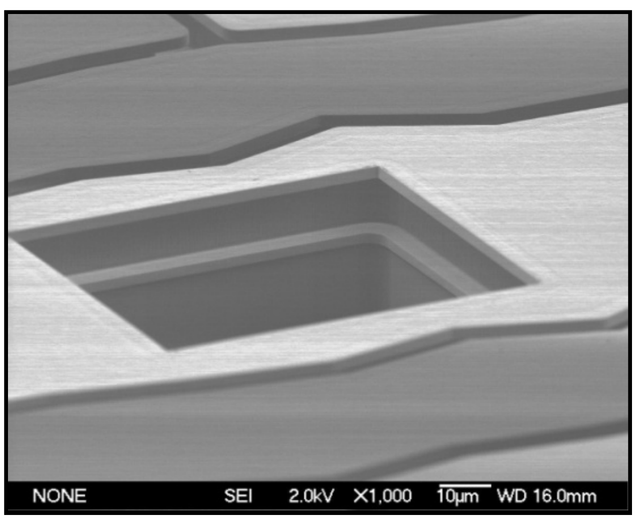
Ion reordering routine

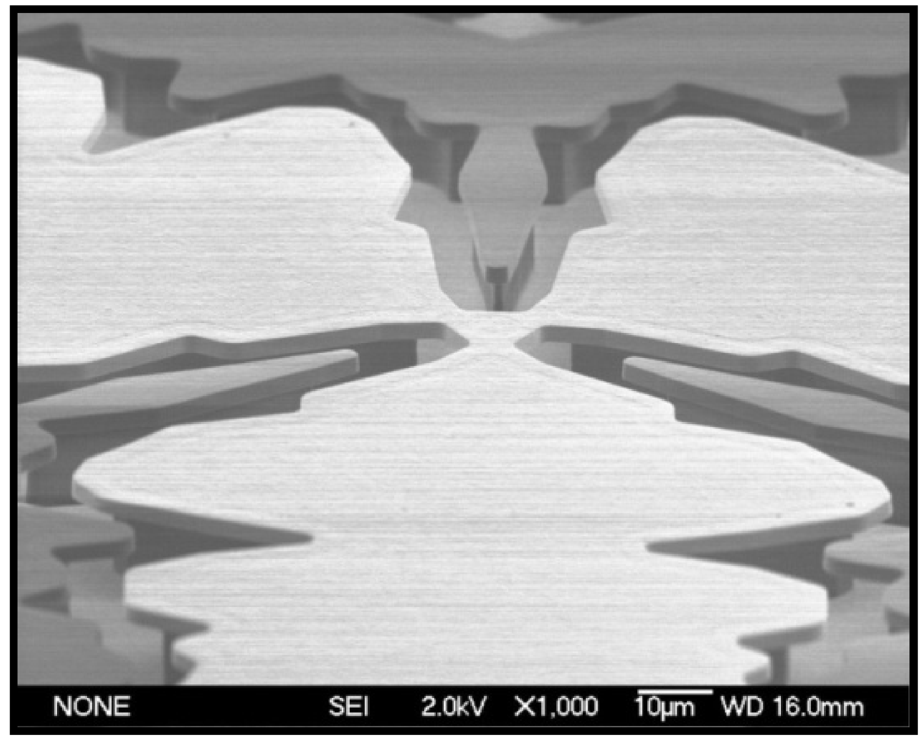
Split; multiple linear and junction shuttles; recombination

Linear shuttling varying only 6 closest electrodes at any given time (example shown in red).
Junction shuttling uses only 12 electrodes (shown in green). e61 constant at all times (orange).

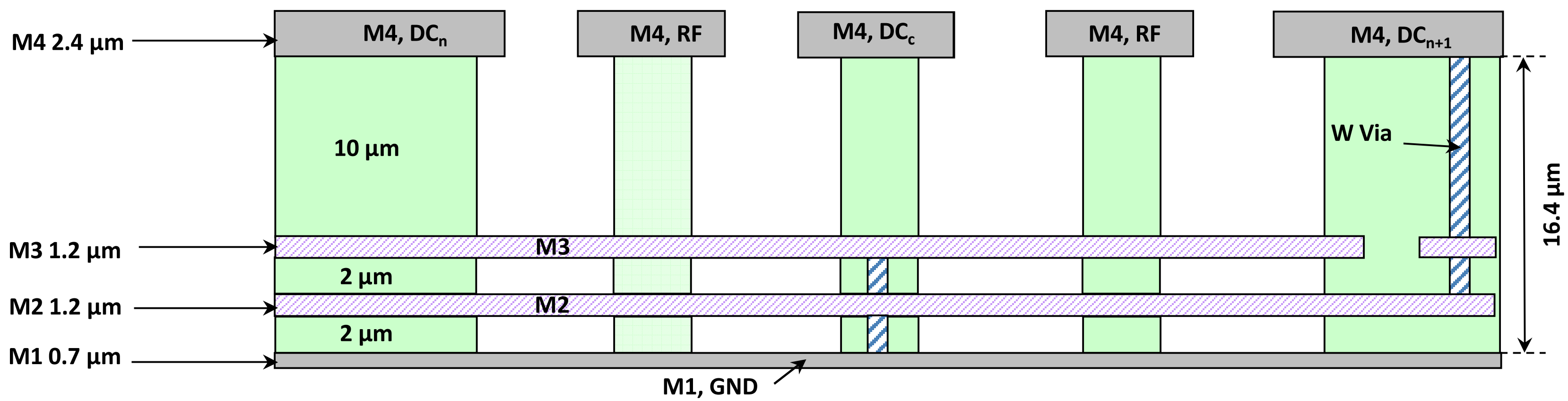
Current capabilities:: 2-level metal & Loading holes

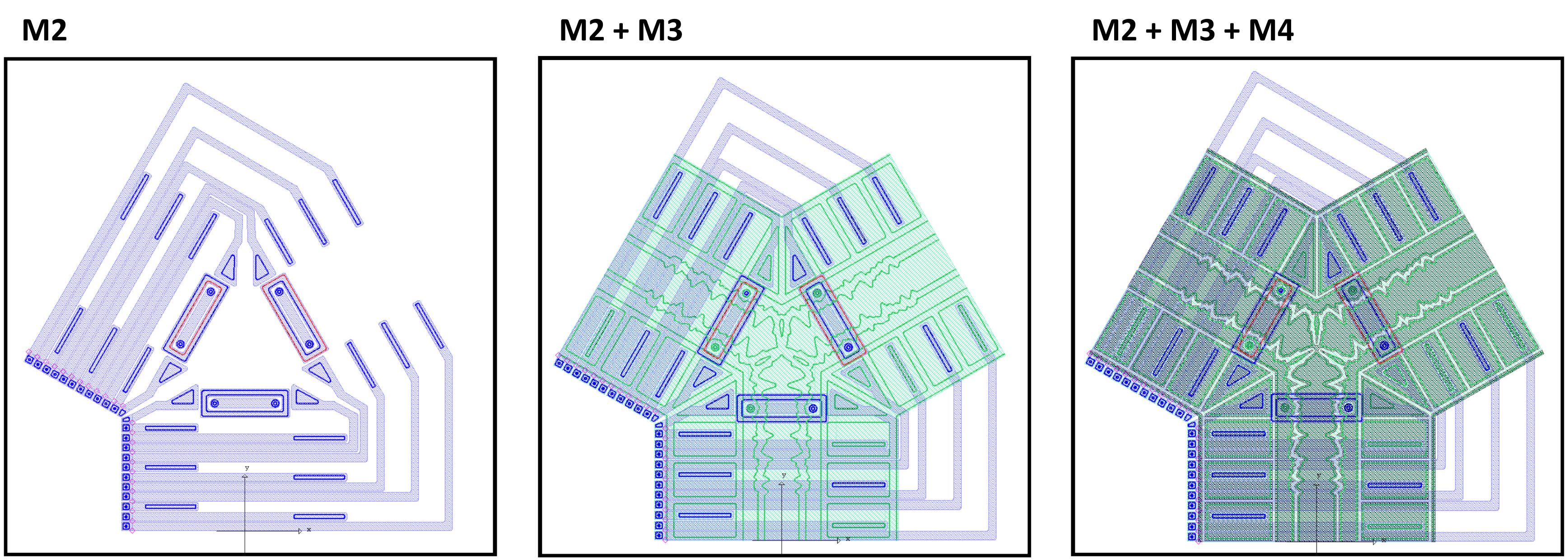






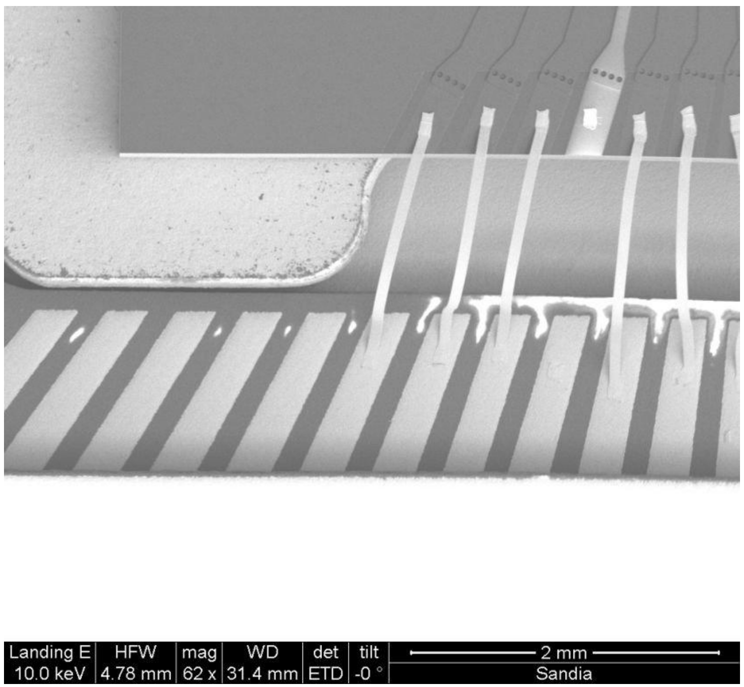
Future capabilities::4-level metal

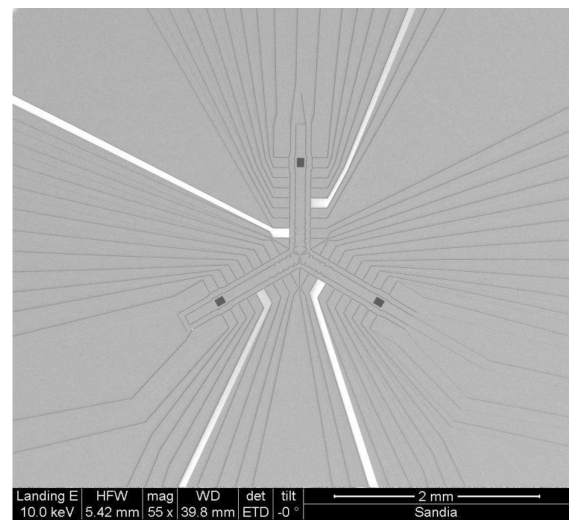




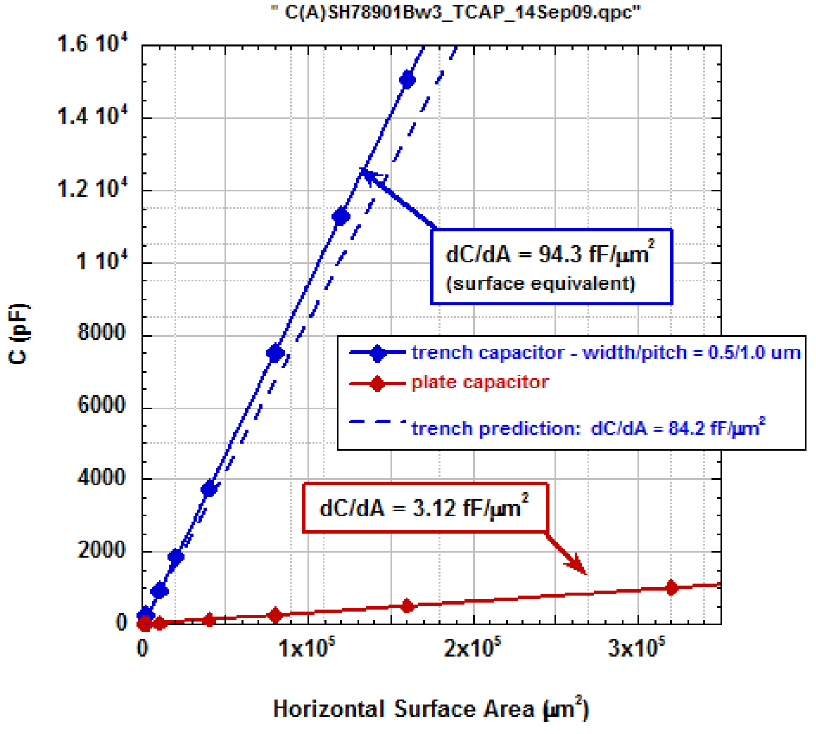
Future capabilities::4-level metal

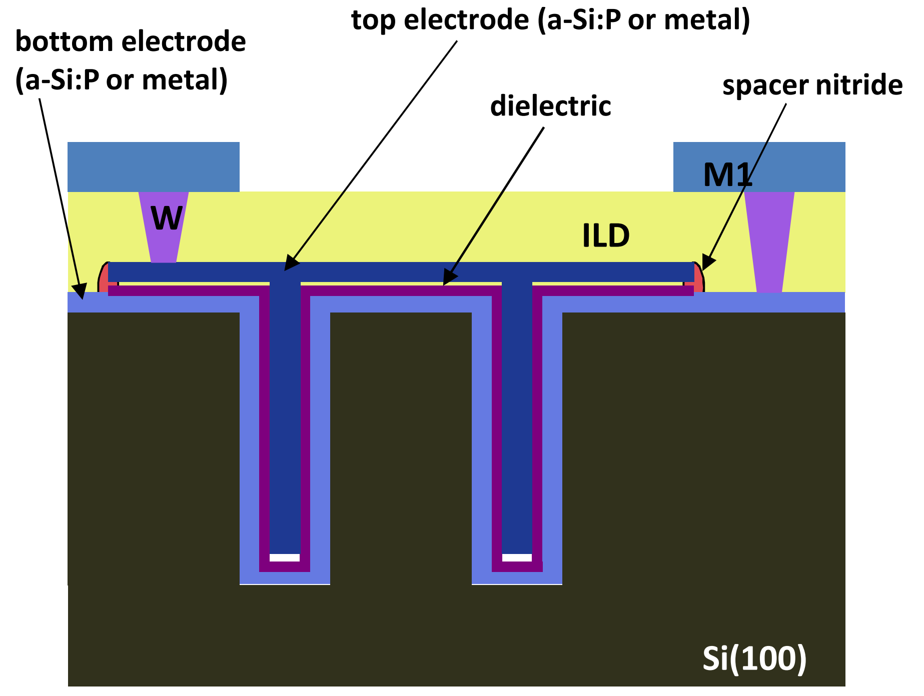
Image of 4 level metal device



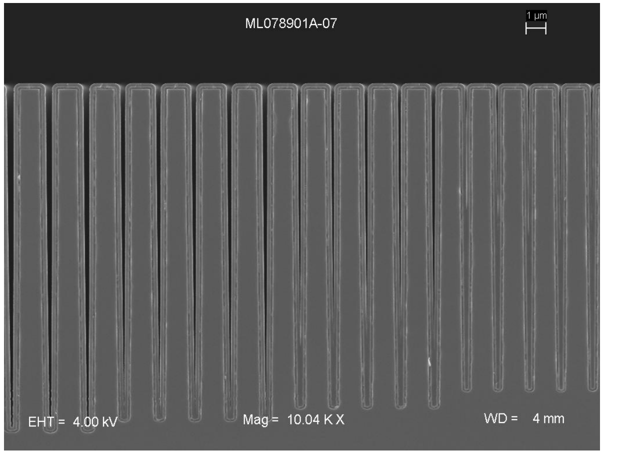


Future capabilities::Trench capacitors

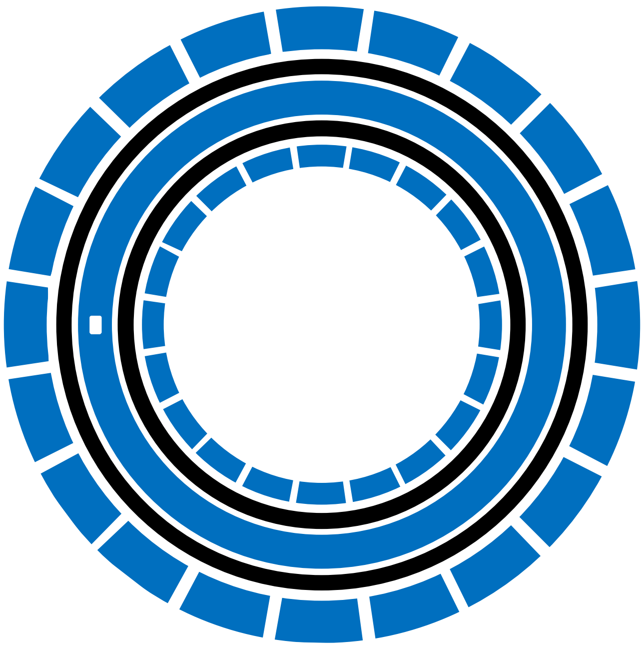


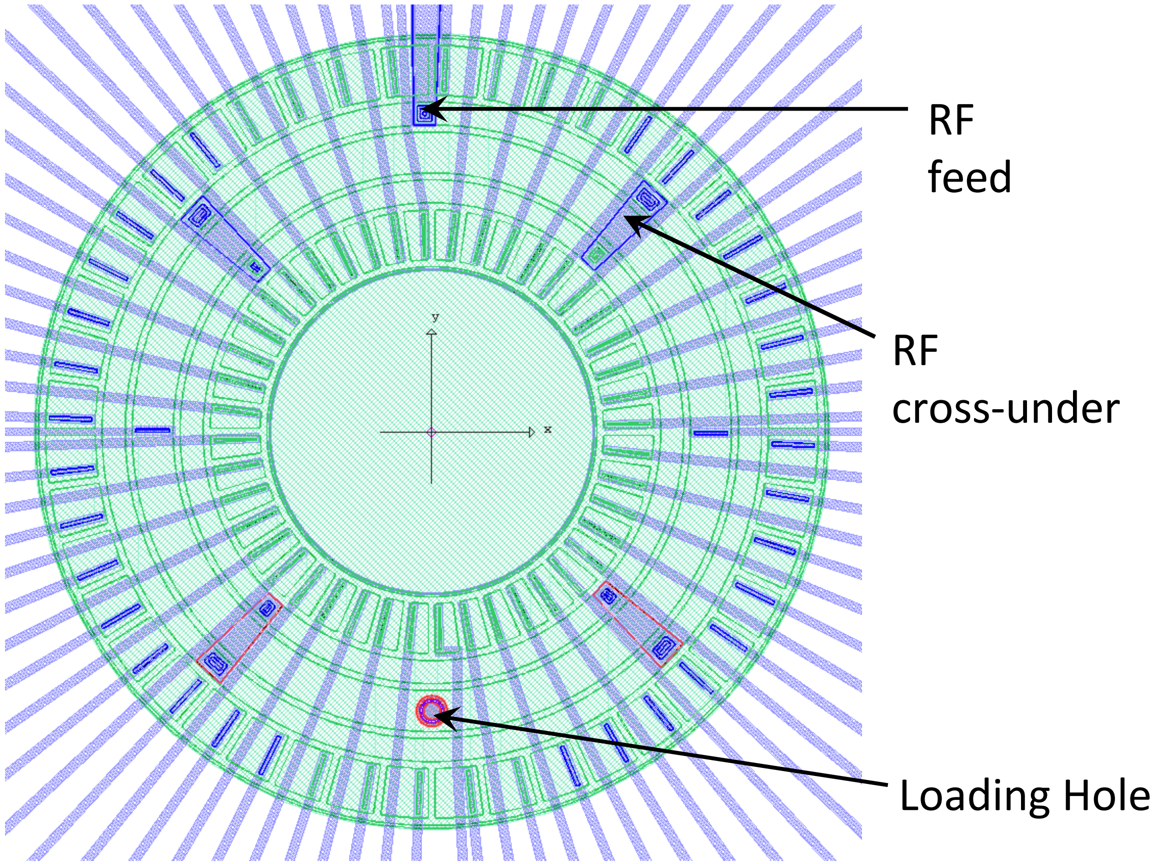


- Higher capacitance density for trench capacitors (94.3 fF/µm² vs. 1.3 fF/µm²).
- 13 µm deep trench; width/pitch = 0.5/1.0 µm
- Capacitors are located within microns of DC electrode.
- 1nF trench capacitor is about the size of an electrode



Future devices::Ring trap



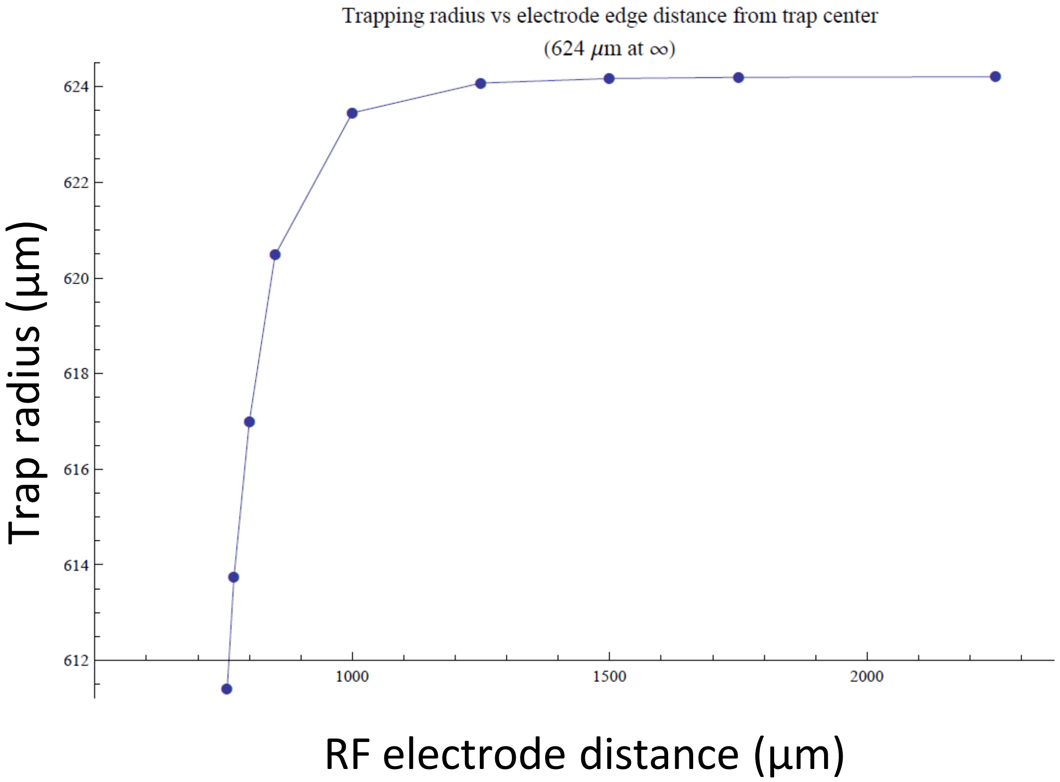


Future devices::Ring trap

- 127 kHz frequency for n=200 ions
  - $n^{1.5}$ dependence
  - 1 MHz for 800 ions

- Loading hole
  - 25 micron radius hole
    - deforms tangential pseudo-potential by 155 kHz, ~500 μeV deep
  - 5 micron radius hole
    - deforms tangential pseudo-potential by 9 kHz, ~5 μeV deep

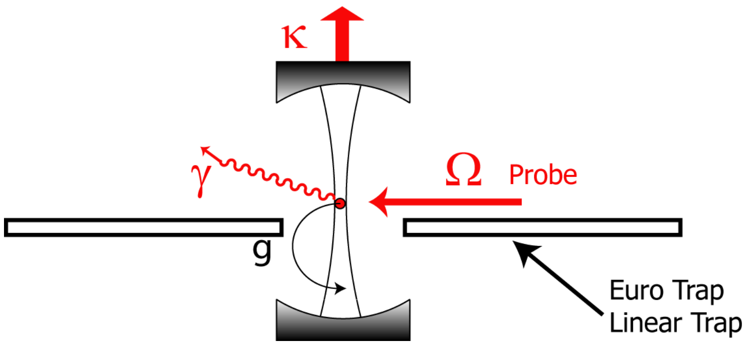
- Radial force of Coulomb repulsion pushes ring out by 0.023 microns (for 200 ions)



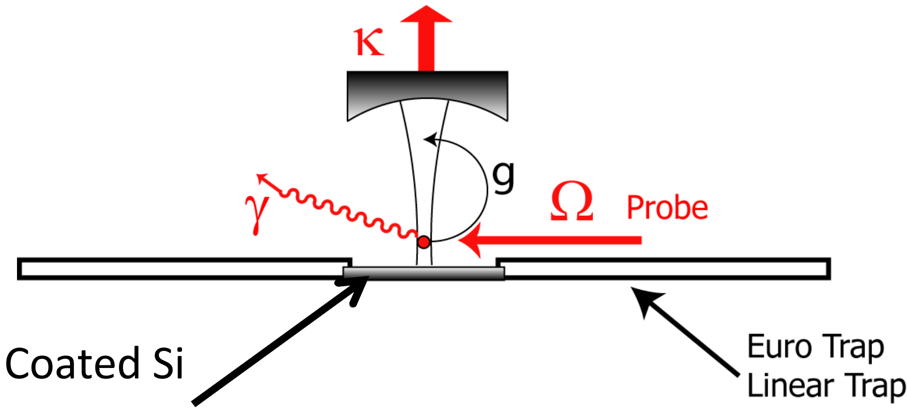
Future devices::Cavity trap

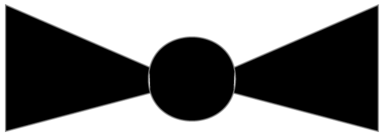
Two Basic Cavity Designs

Symmetric Cavity Design



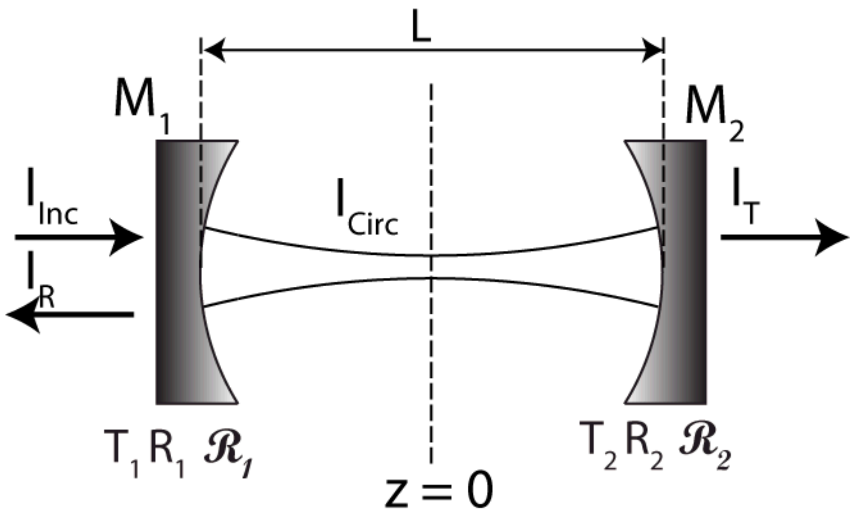
Hybrid Integrated cavity





The second mirror will be a "hand-able" piece of Si that is coated by ATF and then glued into the linear trap

Cavity QED Geometry



Using mirror geometry and reflectance we can compute the relevant CQED parameters:

- Finesse = 2 π/Loss
- w_0 – Beam Waist
- V_m – Mode Volume
- κ – Cavity Line Width
- g – Coherent Coupling Rate
- C – Single Atom Cooperativity

Purcell Enhancement

$$P=\frac{2C}{C+\kappa}$$

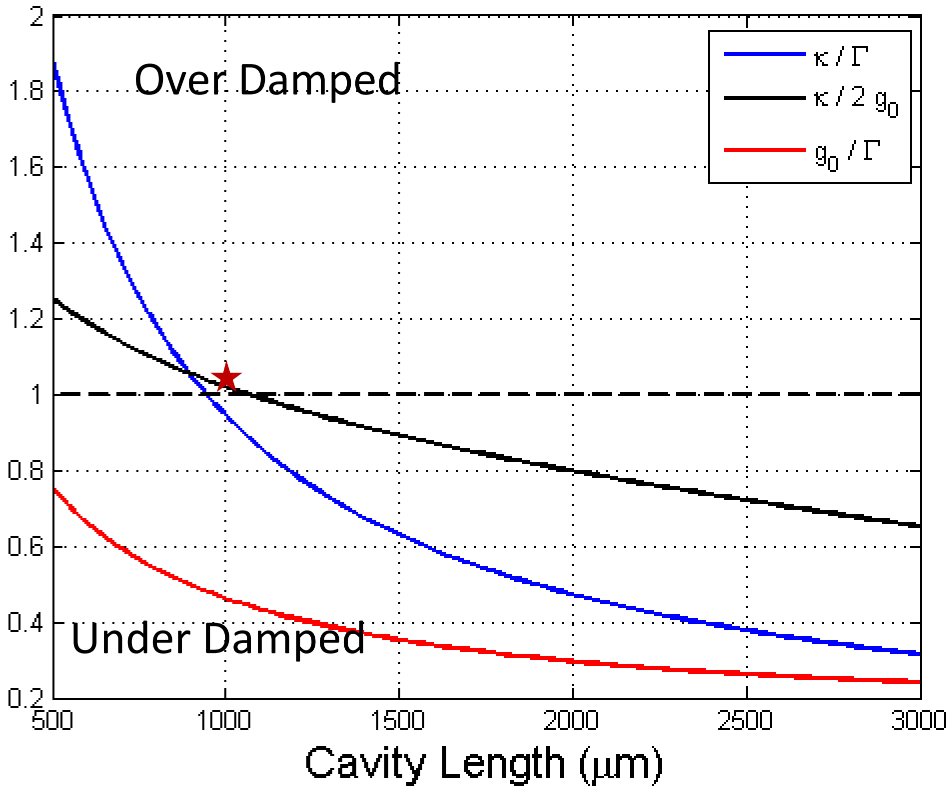
$$g \propto \frac{1}{\sqrt{V_M}}$$

$$C=\frac{g^2}{\kappa\,\gamma}$$

Hybrid Integrated Cavity

$$\mathrm{RoC}_1 = \infty$$
$$T_1 = 200 \text{ ppm}$$
$$\mathrm{RoC}_2 = 5 \text{ mm}$$
$$T_2 = 1000 \text{ ppm}$$

Assume that the ion is trapped 150 microns from Si flat mirror

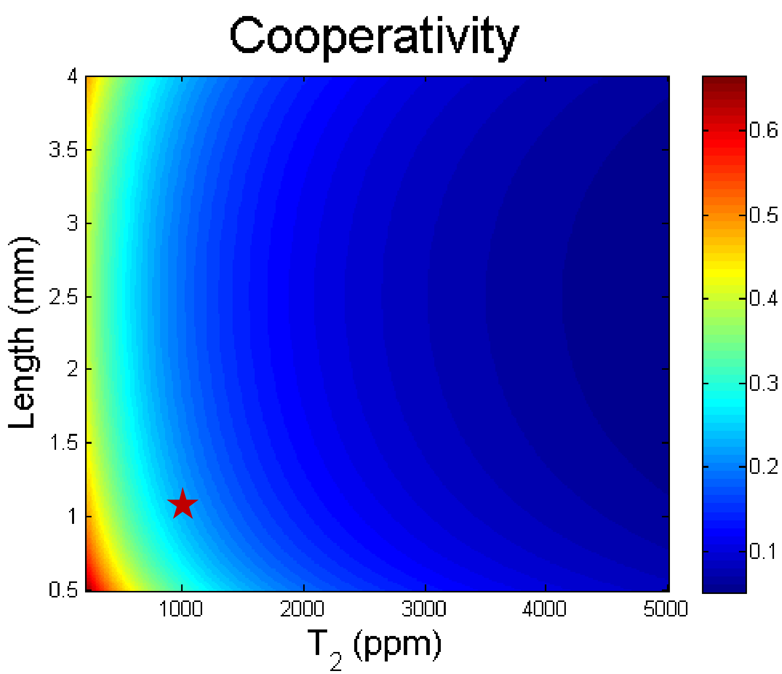


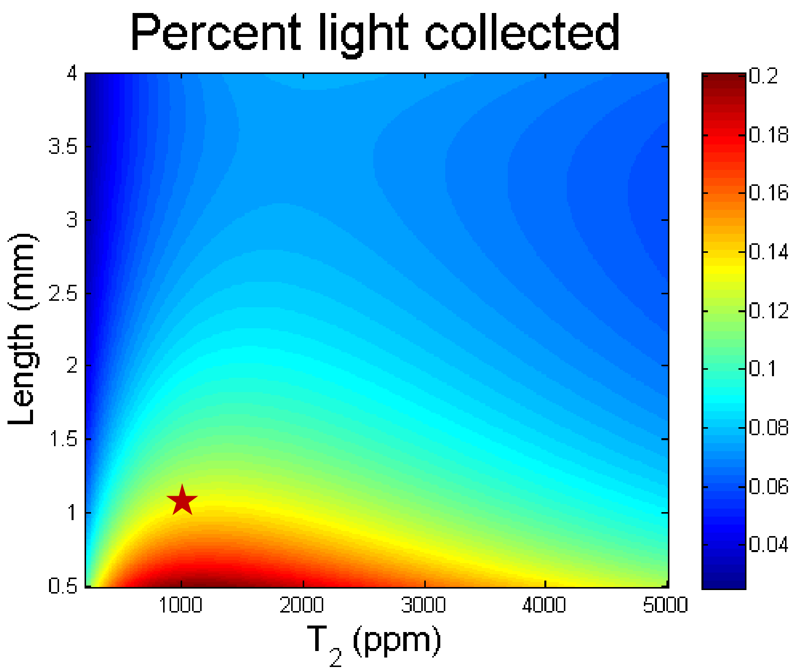
For good photon extraction
We ideally want:

$$\kappa >> g, \Gamma$$
$$g >> \Gamma$$

★ Design Cavity

Plots of C and %light collection





★ Design Cavity

$$\mathrm{RoC}_1 = \infty$$

$$T_1 = 200\ \mathrm{ppm}$$

$$\mathrm{RoC}_2 = 5\ \mathrm{mm}$$

$$P_{col} = \frac{T_2}{\mathcal{L}}\left(\frac{2\kappa}{2\kappa + \Gamma}\right)\left(\frac{2C}{1+2C}\right)$$

Where $\frac{T_2}{\mathcal{L}}$ Is the ratio of the output coupler's transmission losses to the total losses of the cavity system

Hybrid Integrated Cavity Design

$L = 1\ \text{mm}$

$\text{RoC}_1 = \infty$

$T_1 = 200\ \text{ppm}$

$\text{RoC}_2 = 5\ \text{mm}$

$T_2 = 1000\ \text{ppm}$

$\frac{\kappa}{2\pi} = 17.905\ \text{MHz}$

$\frac{g_0}{2\pi} = 9.061\ \text{MHz}$

$\frac{\gamma_{Yb}}{2\pi} = 19.600\ \text{MHz}$

$C = 0.2339$

$P_{col} = 13.73\%$

$\mathfrak{I} = 4188$

$\text{scatter loss per mirror} = 150\ \text{ppm}$

Mirror Surface Roughness

Si = 2 Ǻ RMS

$w(z_1) = 15.34\ \mu\text{m}$

$w(z_{\text{ion}}) = 15.38\ \mu\text{m}$

$w(z_{\text{chip}}) = 15.35\ \mu\text{m}$

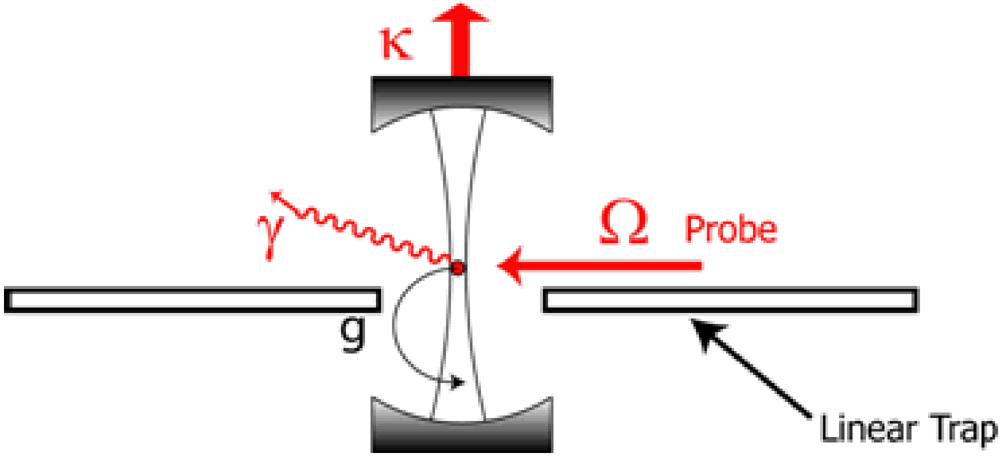
$w(z_2) = 17.15\ \mu\text{m}$

$g_1 g_2 = 0.8$

stability

$0 \le g_1 g_2 \le 1$

Traditional Integrated cavity



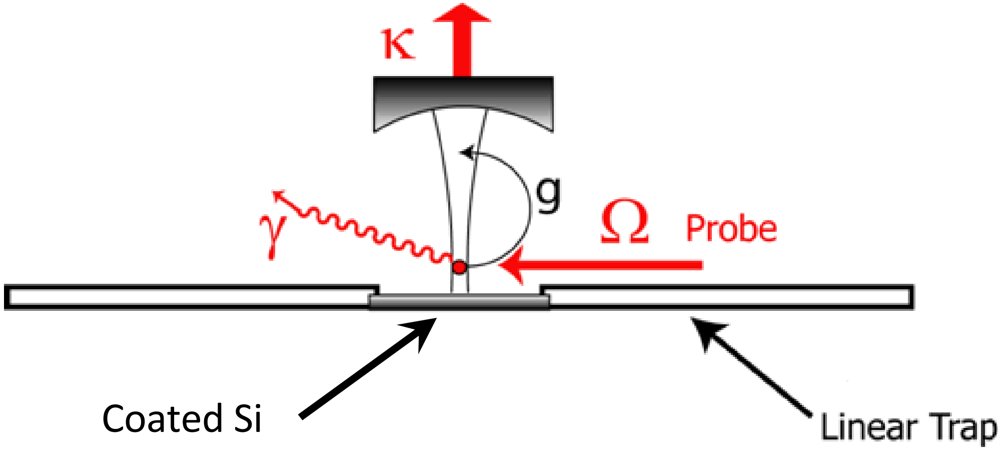
Requirements

- $C > 0.2$ for Yb^+
- $F > 1000$; desired $F > 3000$ @ 369 nm

Additionally, the cavity parameters should be tuned to maximize photon output.

New criteria: 10% photon output

Hybrid Integrated cavity



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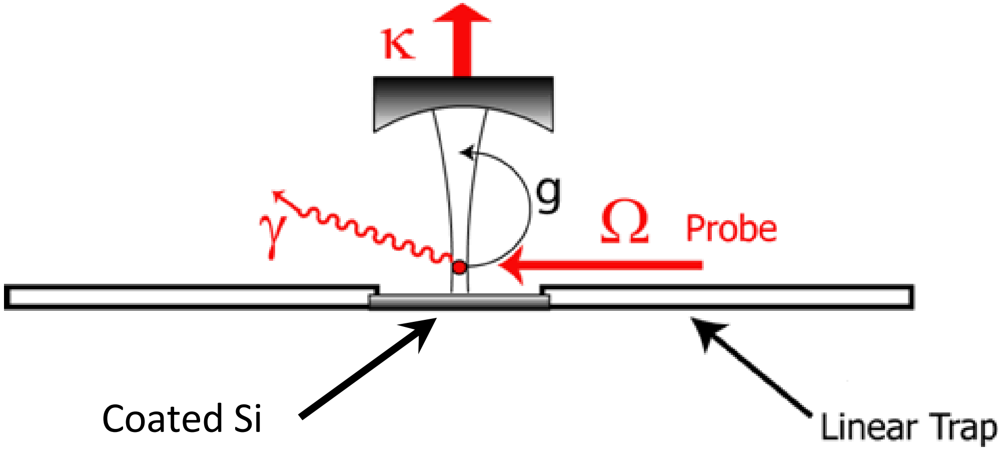

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For good photon extraction
We ideally want:

$$\kappa >> g, \Gamma$$

$$g >> \Gamma$$

$$C = g^2 / \kappa \Gamma$$

$$P_{col} = \frac{T_2}{\mathcal{L}} \left(\frac{2\kappa}{2\kappa + \Gamma} \right) \left(\frac{2C}{1 + 2C} \right)$$

$$\text{RoC}_1 = \infty$$

$$T_1 = 200 \text{ ppm}$$

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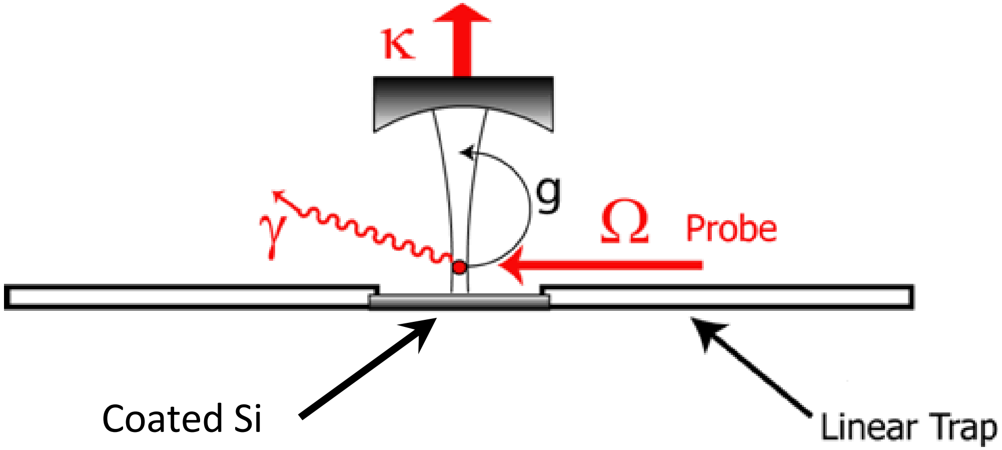

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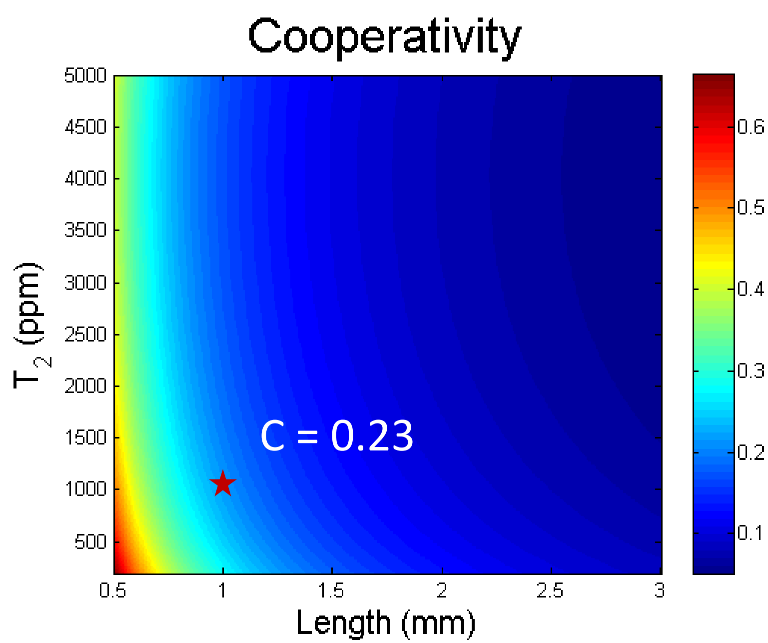
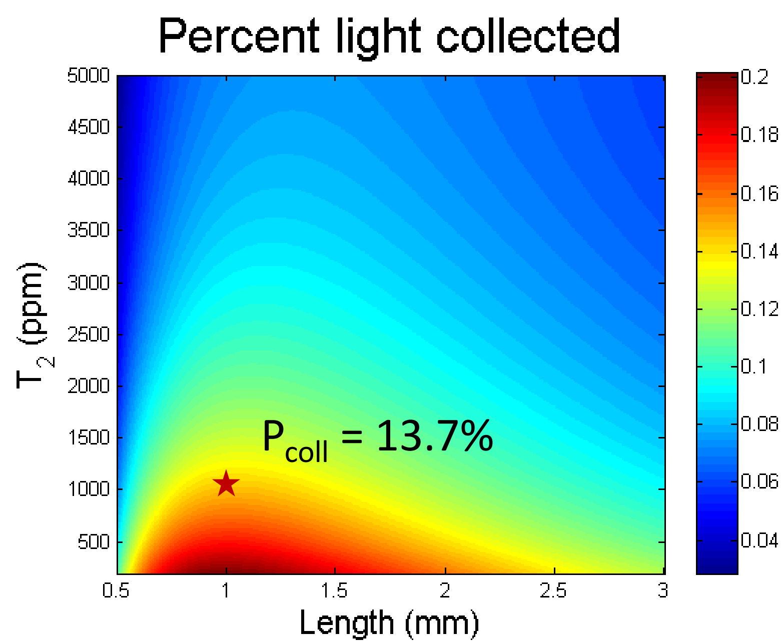
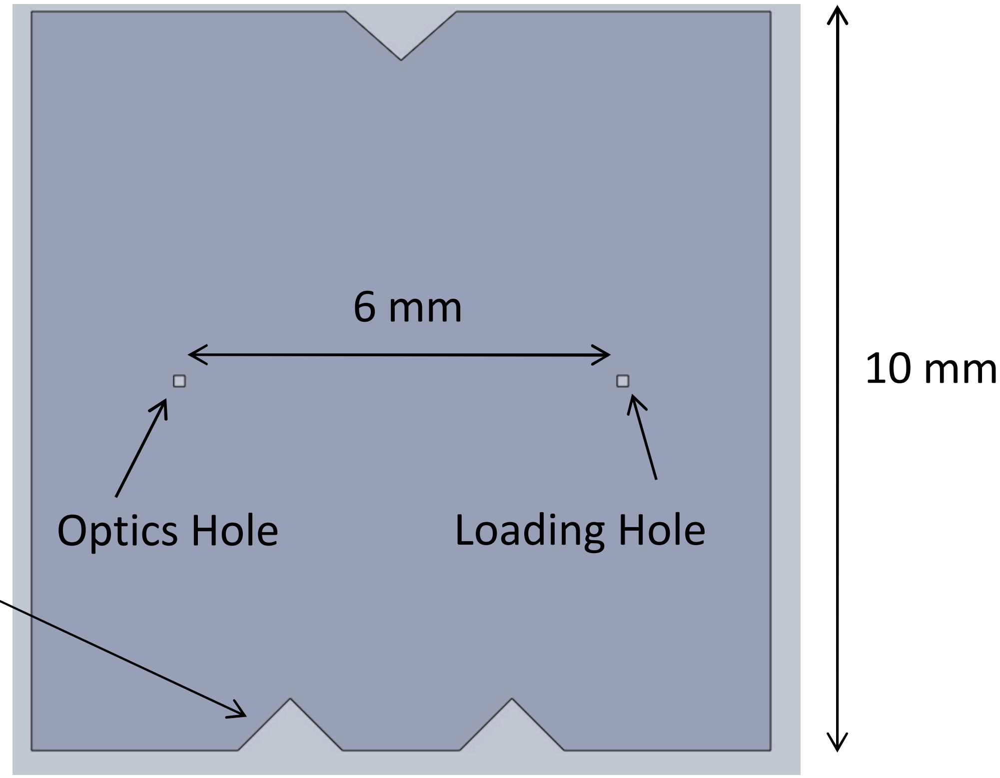
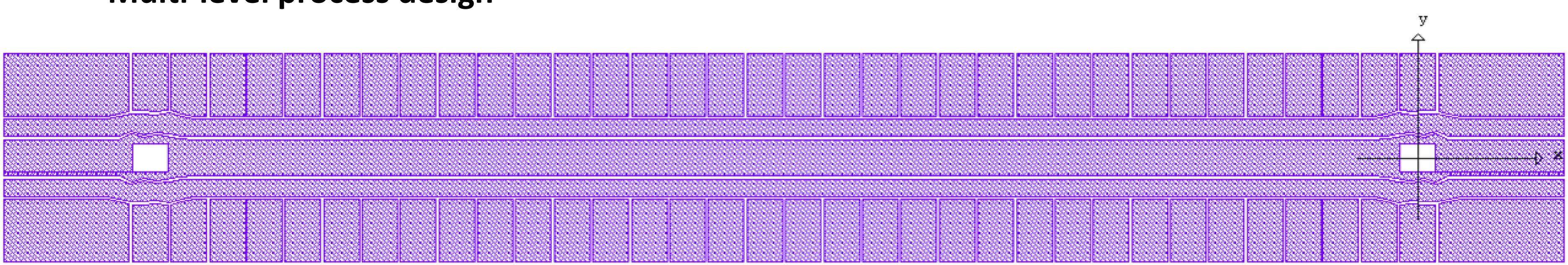




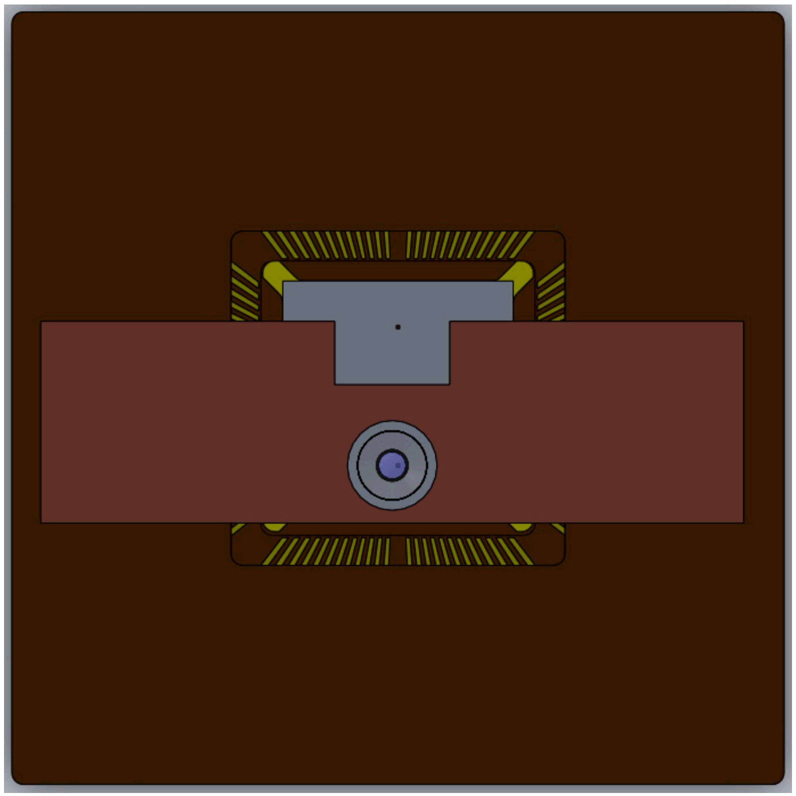
- Change loading slot into two distinct access holes: optical and loading
    - Protects mirrors from neutral atom contamination
    - Allows for normal imaging at loading hole
- Add registration features to register cavity mount to chip
- Optical hole is 100 x 120 microns
- Ion height ≈ 110 microns

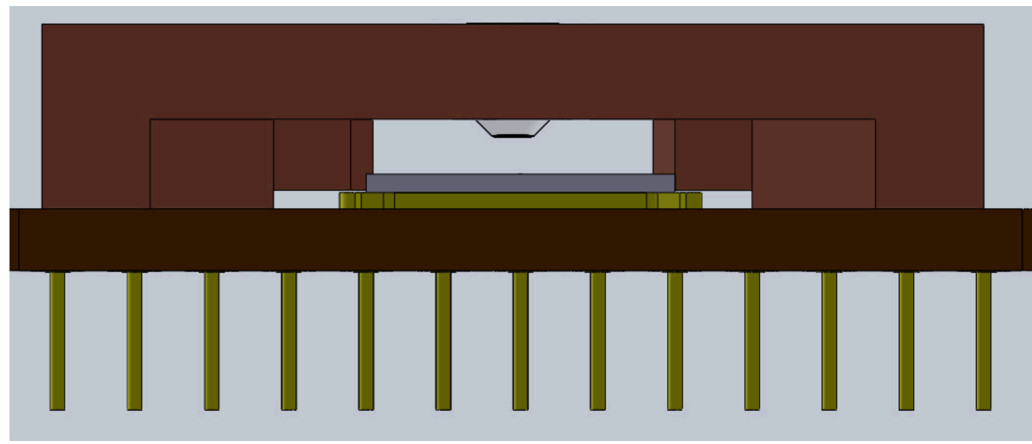


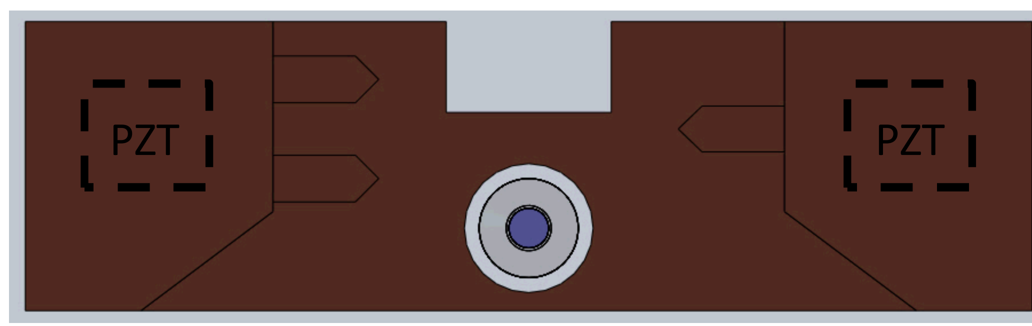
- New linear trap design
    - 73 DC electrodes
    - Multi-level process design



- Mount epoxied to CPGA Socket
- Mount made from dense material, oxygen-free copper
- Cut away allows for imaging of ions at the loading hole
- Mount is registered to linear trap via registration points





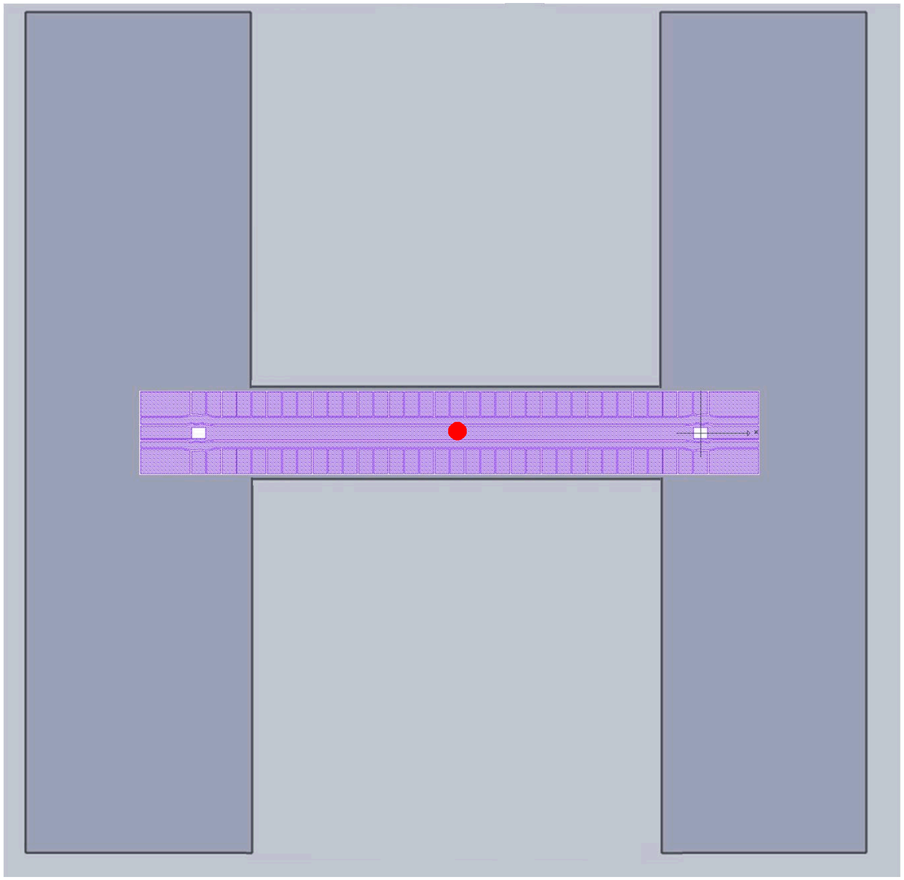


- Delivery of packaged system to UMD and Duke by February 1, 2012.

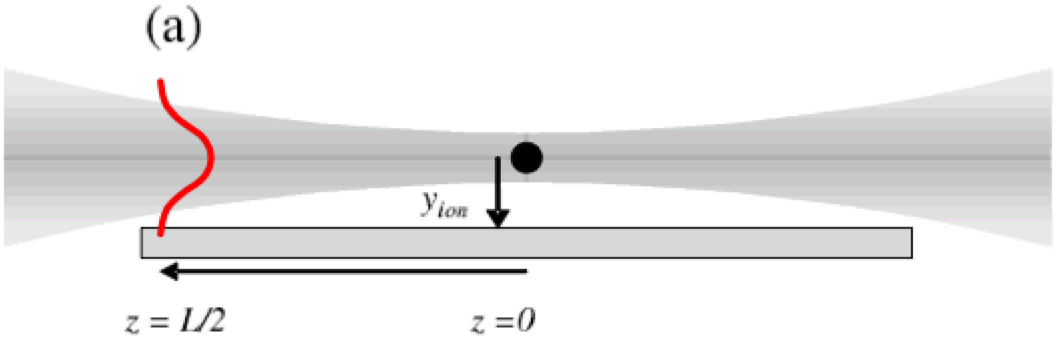
Using the same fabrication techniques that are used for:

- precise placement thru-holes &
- multi-level processing,

we can design the chip itself to any desired shape.



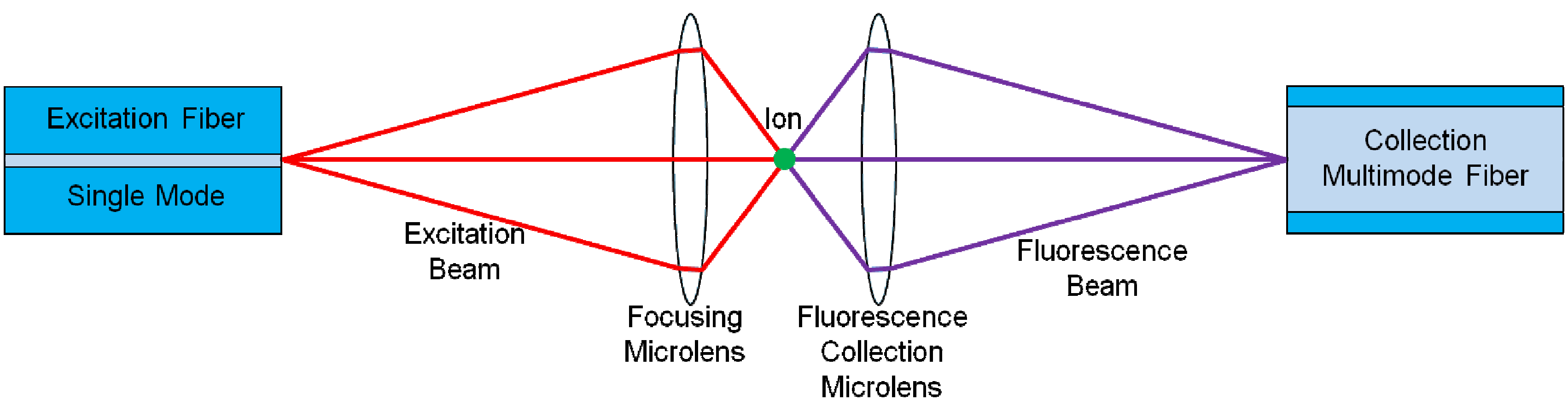
This can allow for tighter focusing of laser light onto the ions.



Integrated Micro-Optics for Ion-Trap Chips

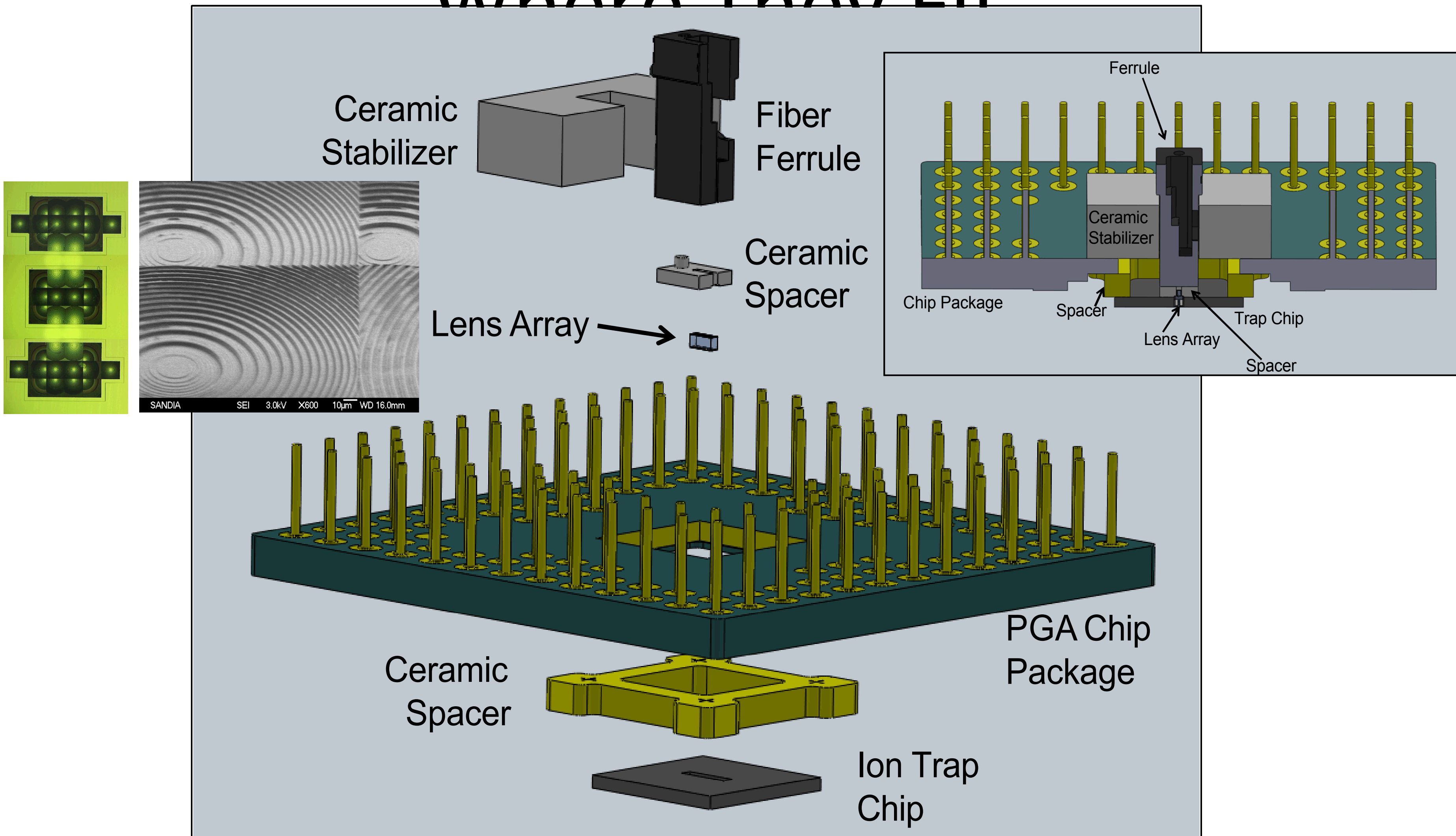
Integrated Micro-Optics for Ion-Trap Chips

- Our successes in making and integrating DOEs for Ion-Trap Chips benefit this neutrals effort directly
- Quantum computers function by manipulating the states of isolated, trapped ions, which can be manipulated and read out optically
- Micro-optics needed to excite and detect fluorescence from trapped ions
- Optical solutions must support high vacuum (10^{-11} Torr) and ~150C bake-out
- Layout for exciting a trapped ion and collecting the resulting fluorescence

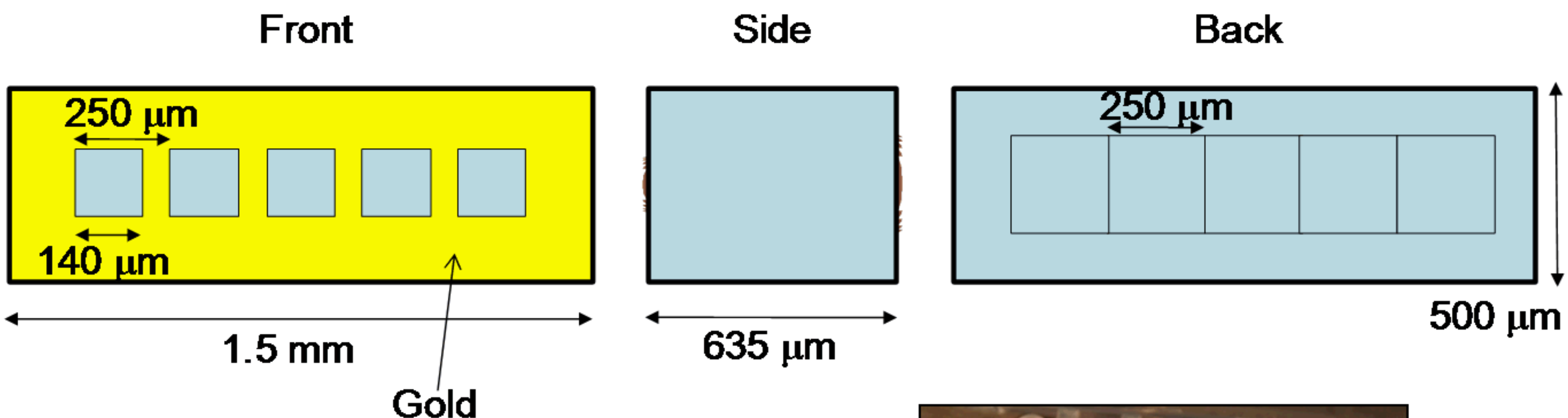


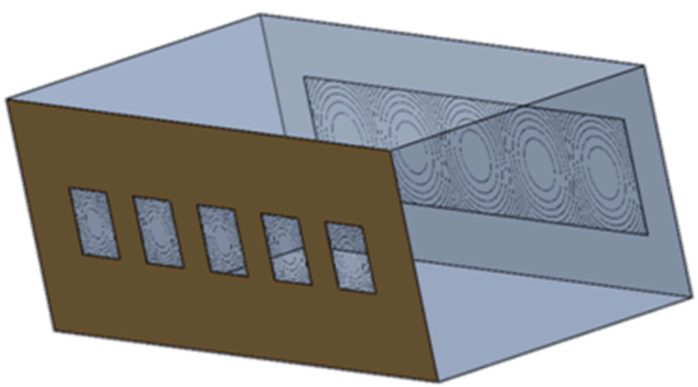
Integration with Ion-Trap Chip: 8-Level DOEs and Where They Fit

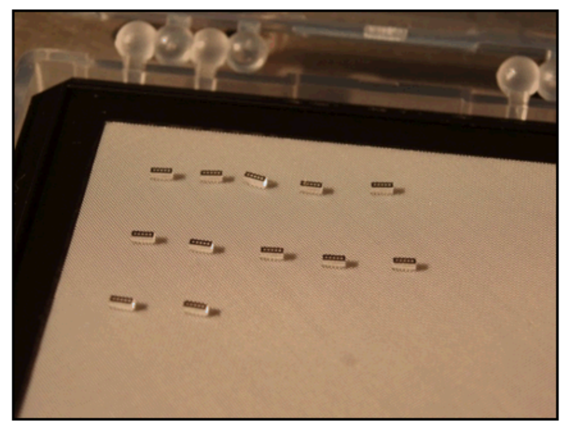
Successes for Micro-Optics in Ion Trapping



Micro-Optic Chip 5-Lens Array 1.5mm X 0.5mm X 0.635mm

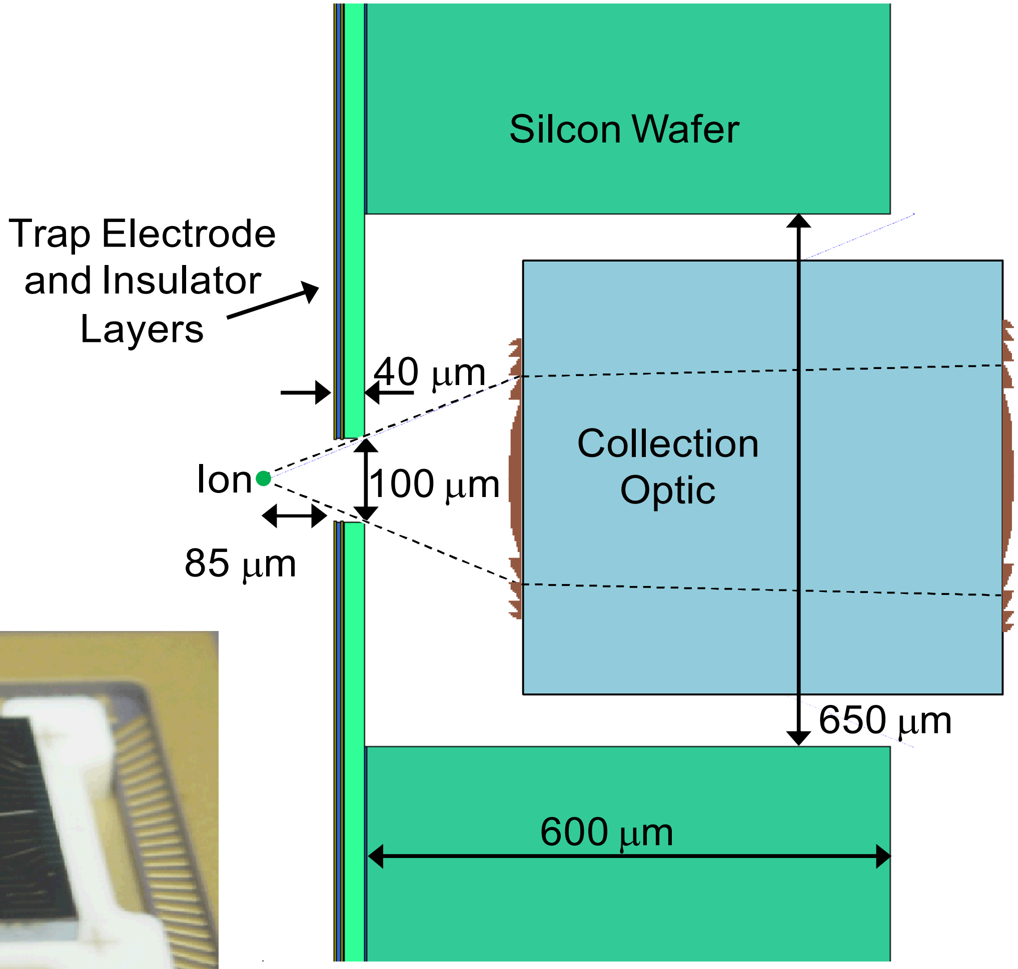


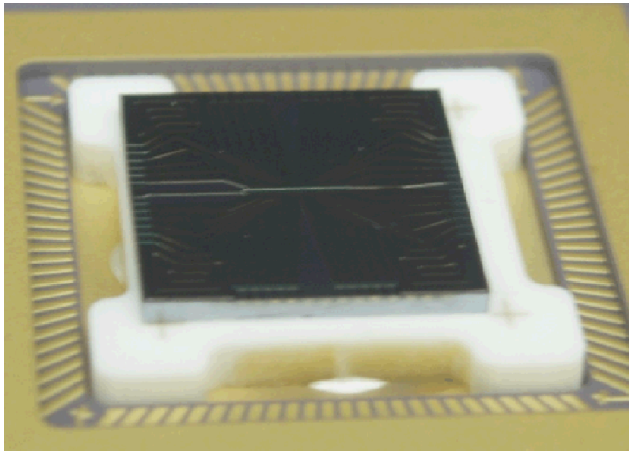




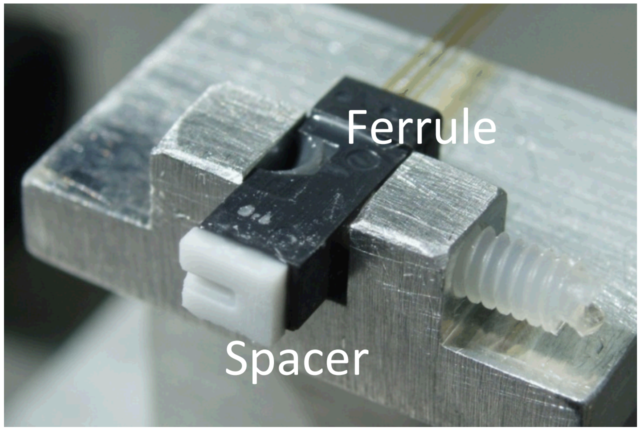
DOEs Embedded into Ion-Trap Chip

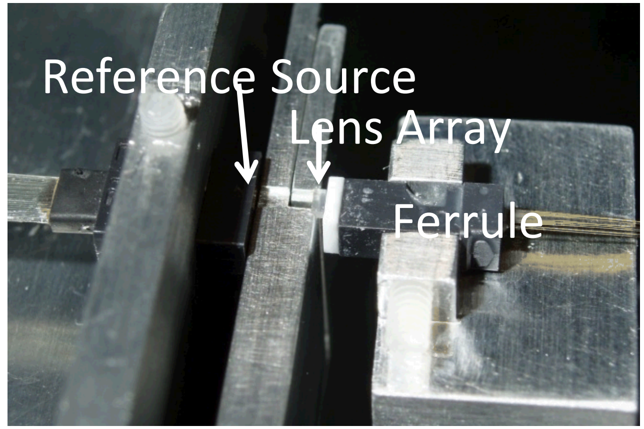
- Section through the ion trap chip, showing representative dimensions
- Dotted lines indicate the marginal rays from the ion passing through the trap slot, which is the aperture stop for the collection optics

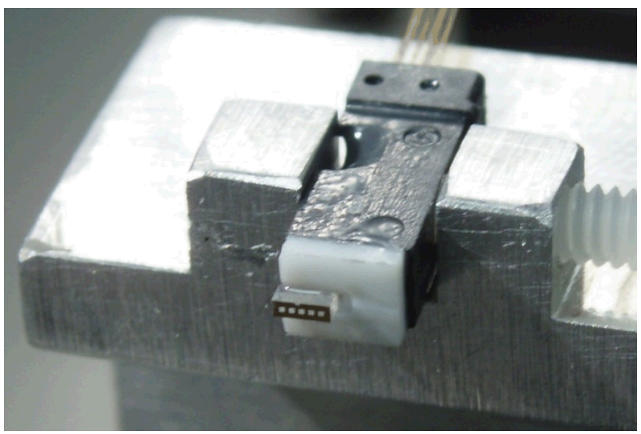


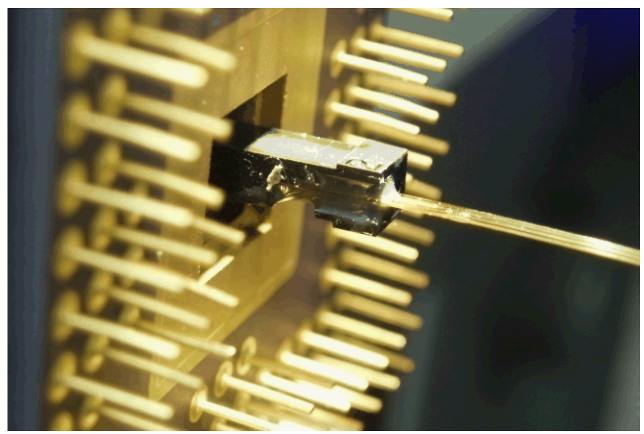


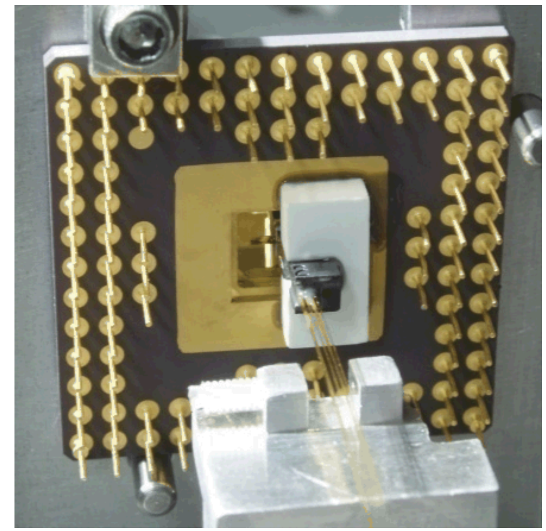
Alignment and Assembly



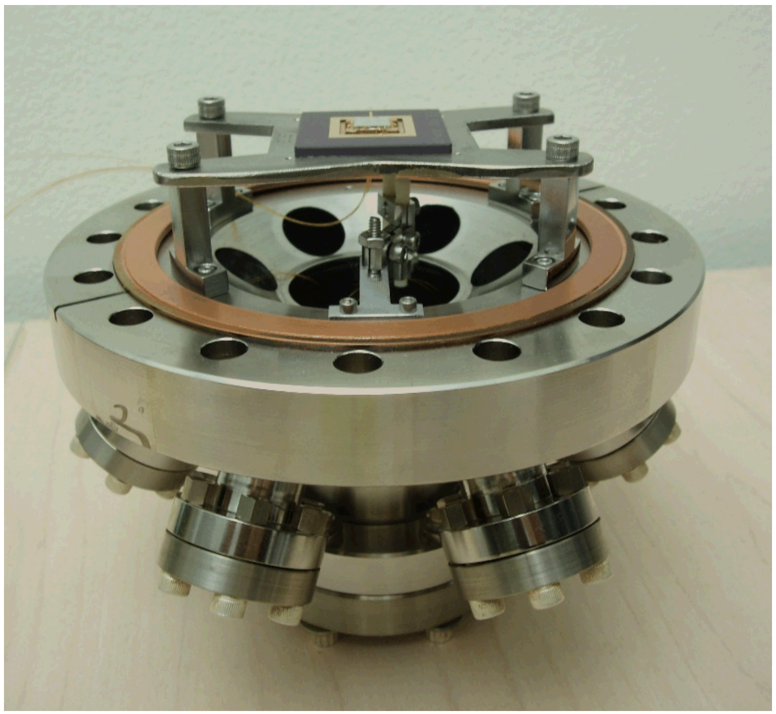


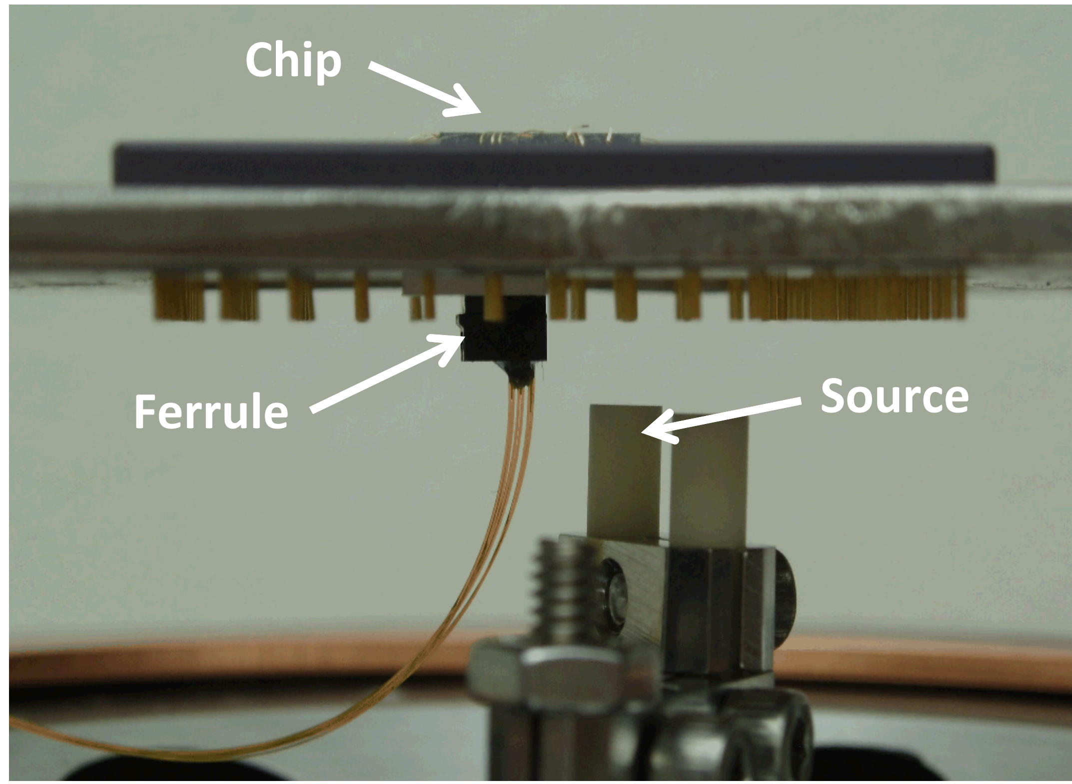






Ion-Trap Chamber Detail





Successes for DOEs in Ion Trapping

- Over the past 5 years: designed, fabricated, and integrated arrays of fluorescence-collecting and excitation DOEs into ion traps
- No degradation of the high-vacuum environment or bake-out process
- Ion-trap chip has been used to successfully trap ions, performed 30000 shuttling operations with no modifications to the control voltages
- Accepted into Applied Physics B
- Reassembling optimized lens set for collection efficiency

Image of NIST quantum sim trap