

SANDIA LAB NEWS • April 14, 2006 • Page 6

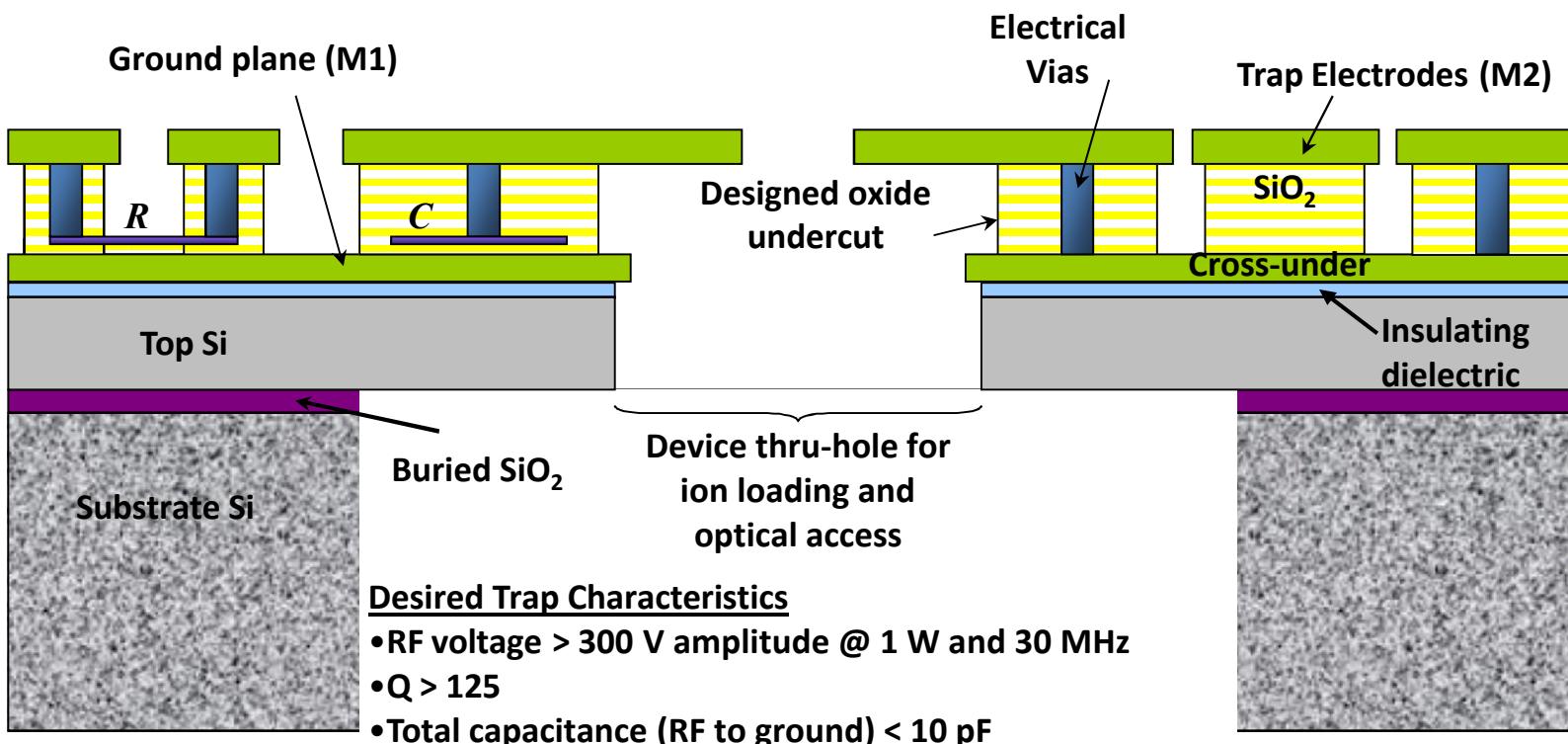


G. Biedermann, M. Blain, R. Boye, T. Carter, A. Cruz-Cabrera, R. Cook, K. Fortier, J. Gallegos, R. Haltli, C. Highstrete, J. Hudgens, R. Jarecki, S. Kemme, D. Moehring, C. Nakakura, J. Stevens, S. Samora, D. Stick, C. Tigges, D. Udoni

■ Objectives/Status

- **Fabrication:** fabricate Si/SiO₂ based surface traps
 - Demonstrated controlled, user definable (e.g. 5 μm) set-back of dielectric underneath trap electrodes for shielding stray charge from the ions
 - Demonstrated on chip passive RF filter components (resistors, capacitors) integrated with ion traps
 - Demonstrated feasibility of sub-trap-electrode-plane wire bond technology preventing laser light scatter from chip-to-package wires
- **Hybridized Trap Optics:** Improve optical signal collection and field of view for ion trapping by integrating optics on the trap chip. Increase packing density by utilizing flexible, off-axis optical design.
 - Fabricated 8-level F/1 lenses with focused spot diameters <1micron.
 - Multi-fiber feed-thrus and in-vacuum connectors survive bake-out and maintain ultra-high vacuum.
- **Trap Diagnostics:** Quantify and improve the performance of ion traps wrt metrics important to QC. Test simulations.
 - Trapped single and multiple ion crystals in macro-trap.
 - Trapped and shuttled single ions/multiple ions in micro-trap.
 - Verified simulations with trapping/shuttling/perturbation measurements
 - Trapped and shuttled ions in Y junction surface trap.

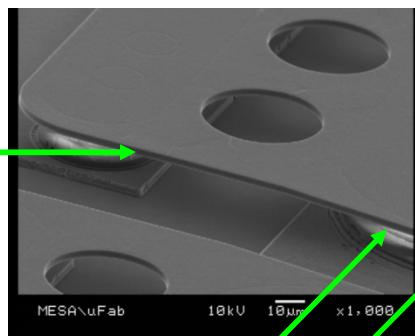
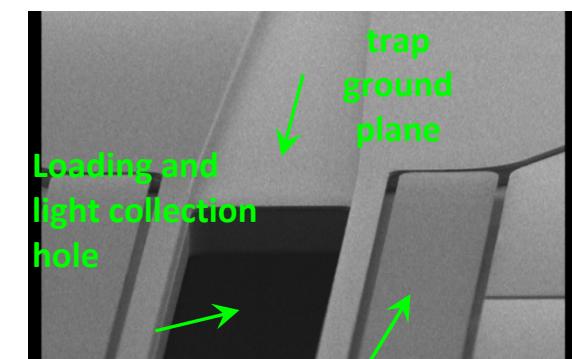
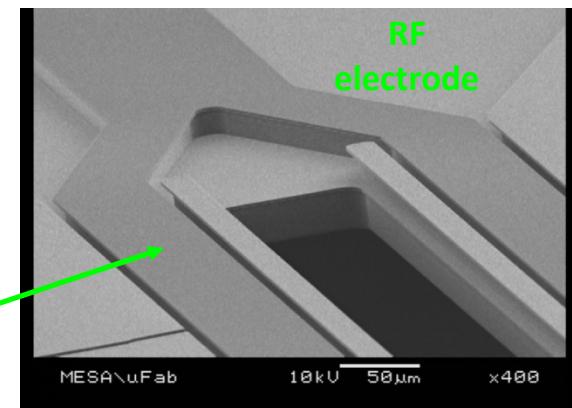
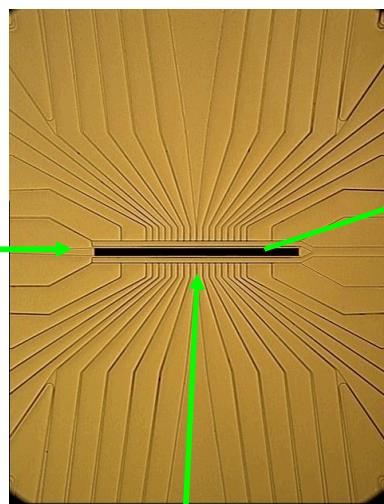
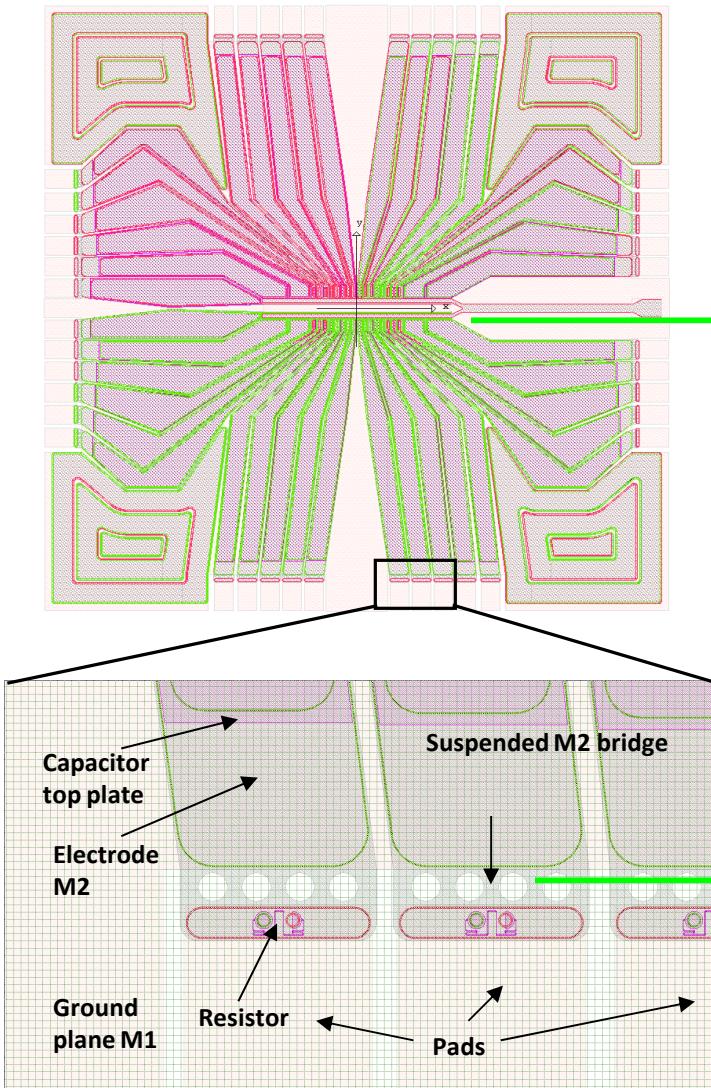
Schematic Cross-Section of Sandia Surface Micro-trap Technology



Demonstrated:

- Precision sidewalls and thick dielectric separation of trap electrodes and ground plane.
- 2.7 μ m inter-metal via technology allows electrode crossing and perfectly vertical oxide support sidewalls that are controllably recessed from the edge of the electrode.
- Accurate and precise electrode overhang fabrication is controllable and repeatable and allows vertical evaporation of metal of choice.

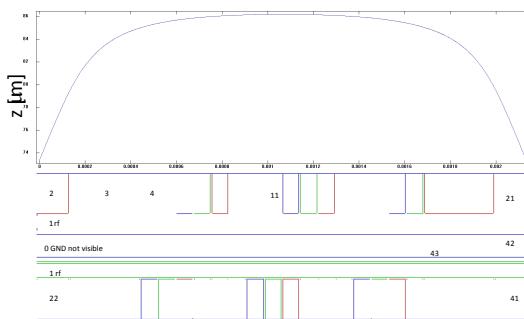
“Thunderbird 1”



Precision
dielectric set-back

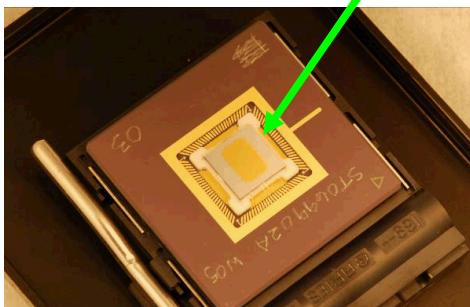
Low profile wire bonding of traps avoid interference with lasers

RF Null heights for surface microtraps are small, e.g. 25-100 μm

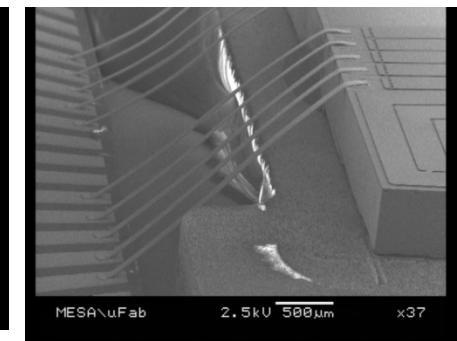
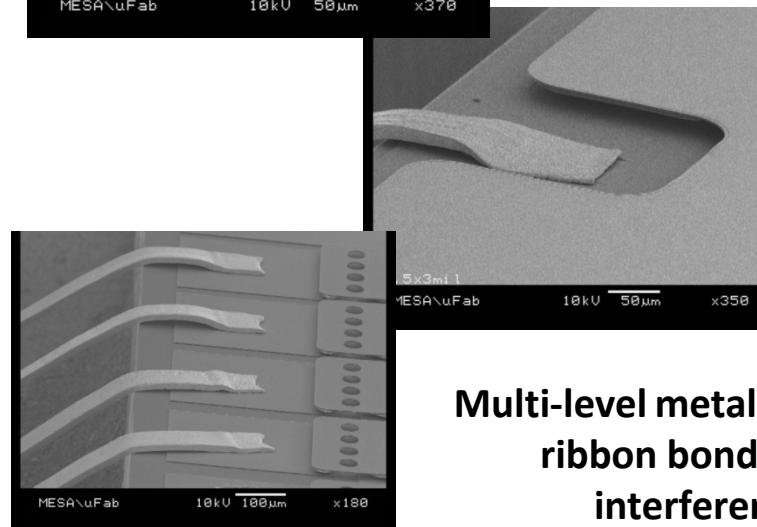
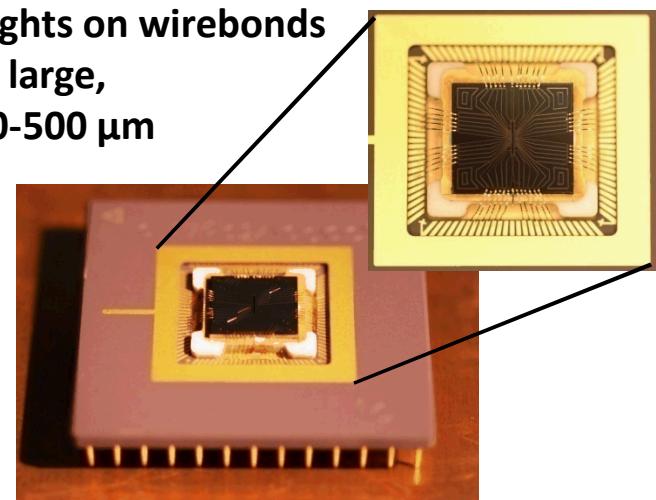
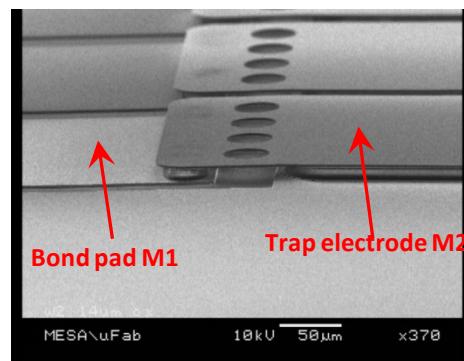


Overhung Trap electrodes allow post packaging evaporation of alternative metals on trap

Au coated trap electrodes



Typical loop heights on wirebonds are large, e.g. 50-500 μm



Multi-level metalization and low profile ribbon bonding of traps avoid interference with lasers

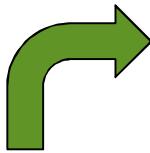
Sandia rendered, NIST surface micro-trap design

Date	Trap	SiO ₂ thickness (μm)	C (pF)	f (MHz, .4W)	Q @ .4 W	Q @ 1 W	V @ 1 W
1/6/08	ST069905A W02 #03	16	7	31.56	150	175	357
	ST069905A W02 #04	16	7	31.58	158	150	331
	ST069905A W03 #01	24	6	32.75	182	172	354
	ST069905A W03 #02	24	6	32.50	190	171	353
	ST069905A W03 #03	24	6	32.88	183	183	365
1/12/09	ST069905A W02 #05	16	7	31.60	158	186	368
	ST069905A W04 #01	16	7	31.64	176	186	368
1/13/09	ST069905A W04 #04	16	7	31.65	176	167	349
	ST069905A W02 #08	16	7	31.61	151	158	339
	ST069905A W02 #07	16	7	31.60	176	158	339
	ST069905A W04 #03	16	7	31.62	176	166	348
1/20/09	ST069905A W02 #07	16	7	31.62	166	170	
	ST069905A W04 #01	16	7	31.63	176	169	
	ST069905A W04 #03	16	7	31.63	167	171	
	ST069905A W02 #03	16	7	31.62	176	172	

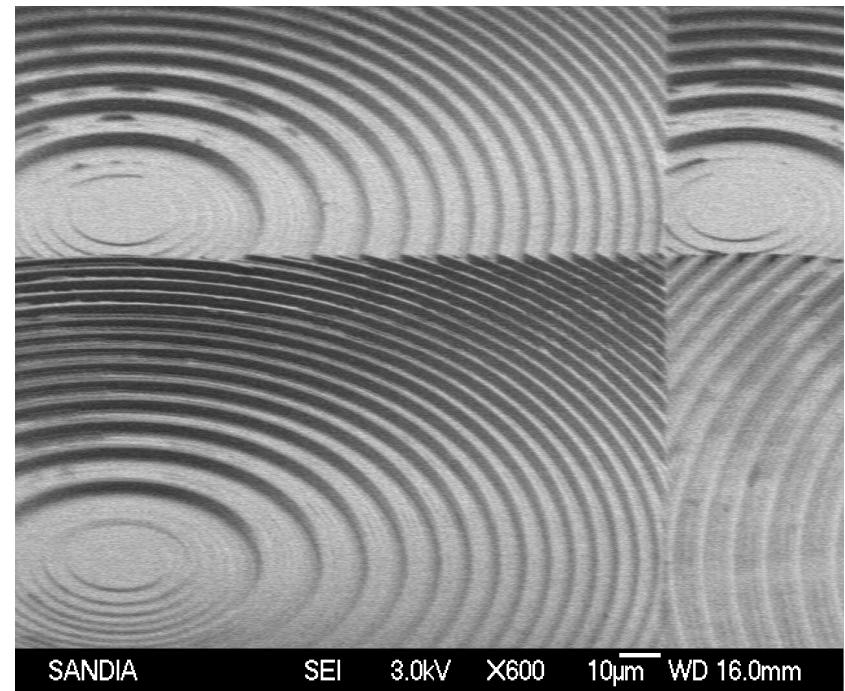
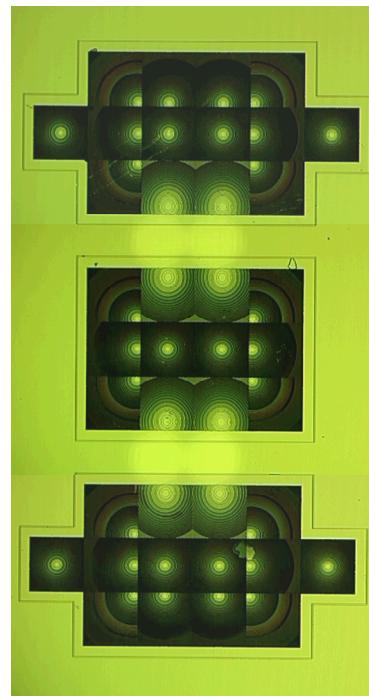
Q's are limited by the chip socket,
not the trap chip

Why integrate optics?

- Can realize transmissive and/or reflective integrated optics
- Because of off-axis capability, can pack lenses densely and with 100% fill factor
- Lens focus need not be a point, can be a volume to accommodate ion motion or integration tolerance



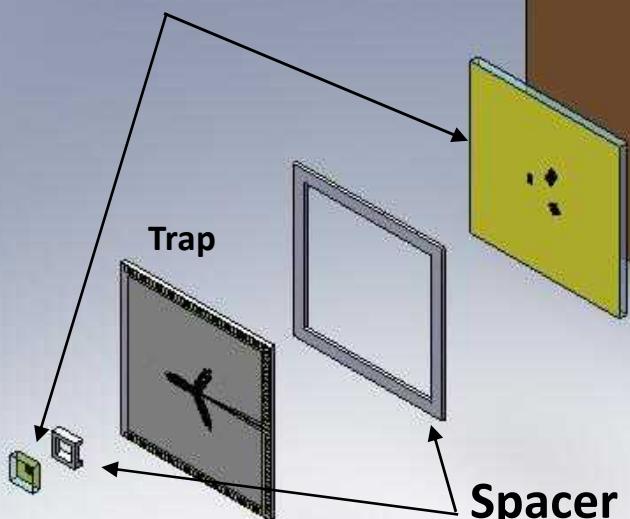
Optical microscope bird's-eye view of a DOE array that Sandia designed and fabricated for cascaded optical computing.



Scanning electron micrograph (SEM) of a portion of the 100% fill-factor optical interconnect array in fused silica, fabricated at Sandia.

Gray scale lenses

- Gray scale increases efficiency, decreases scatter
- Fabricated in reflective metal or UV transparent substrate

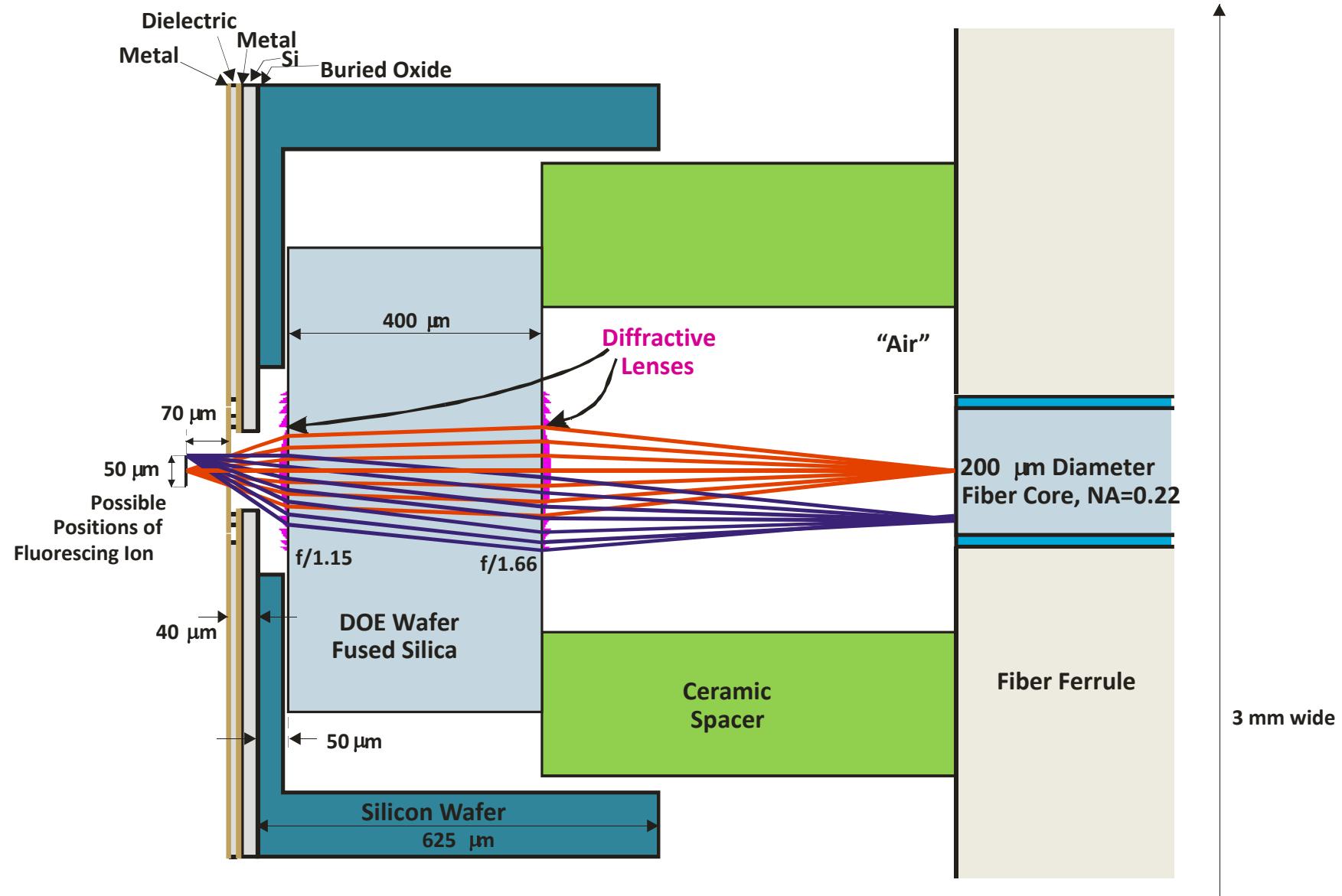


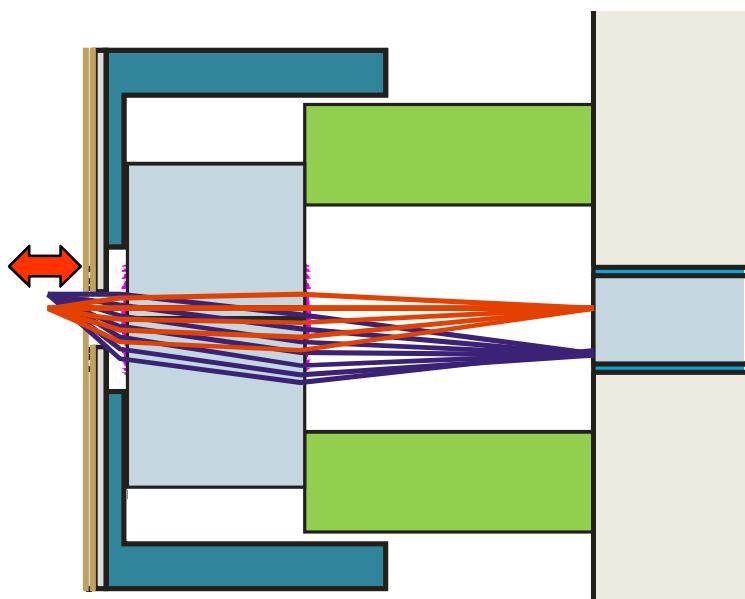
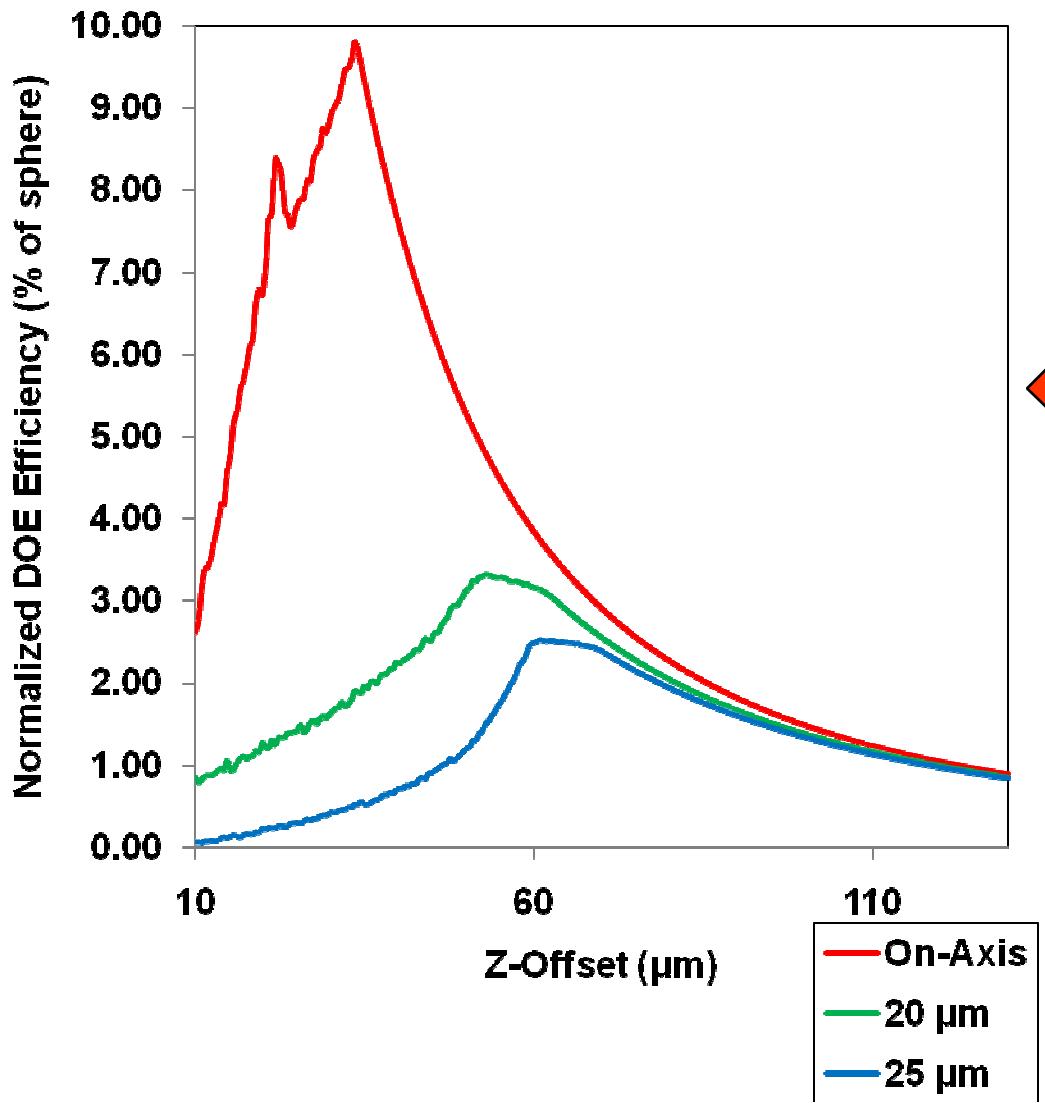
Spacer

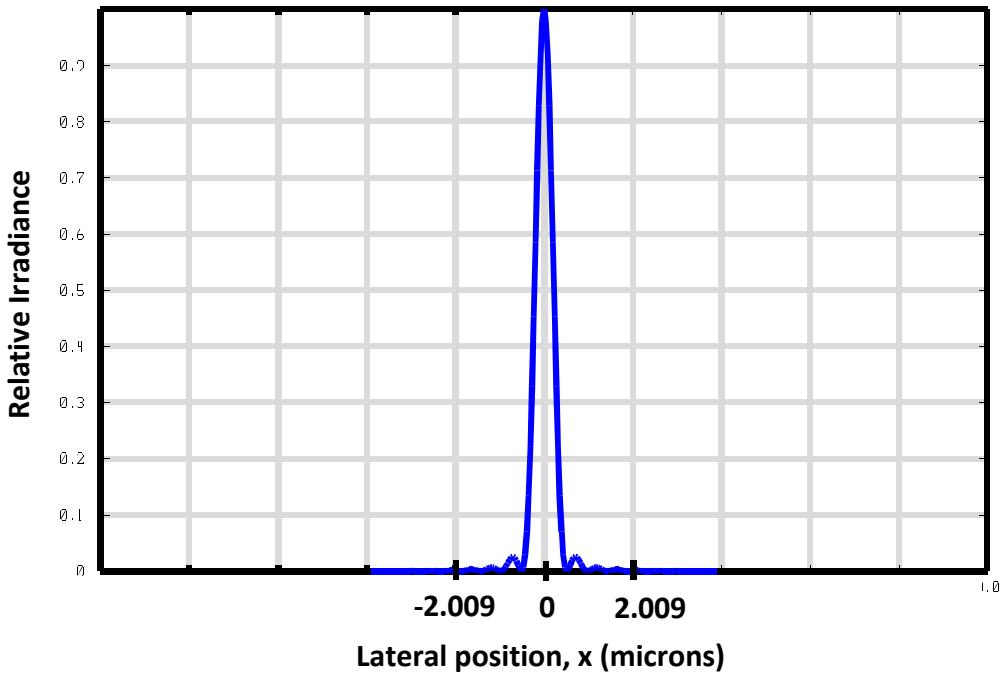
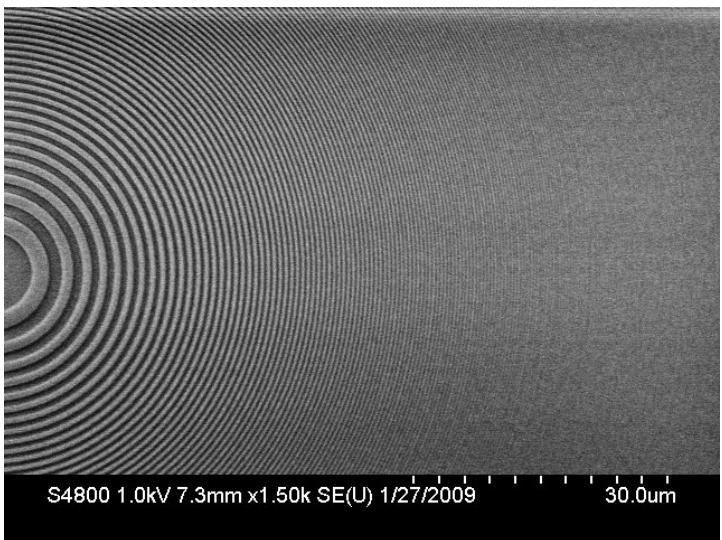
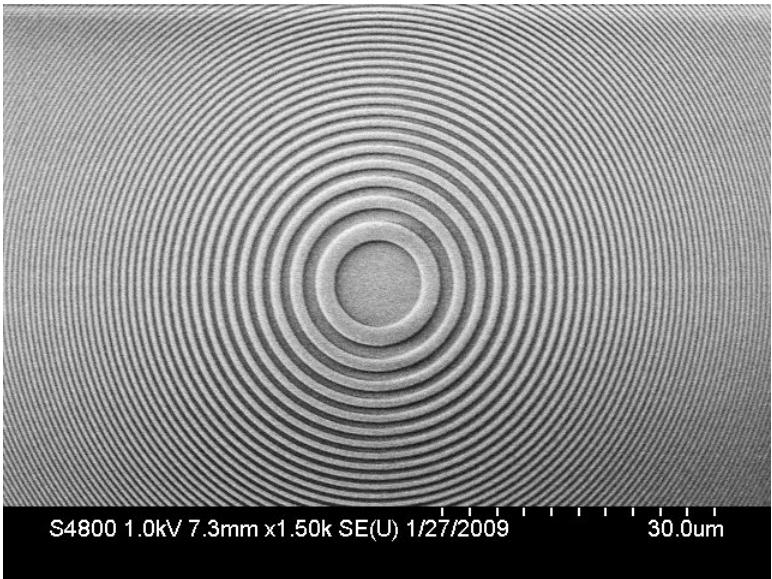
- Defines working distance
- Silicon

Fibers

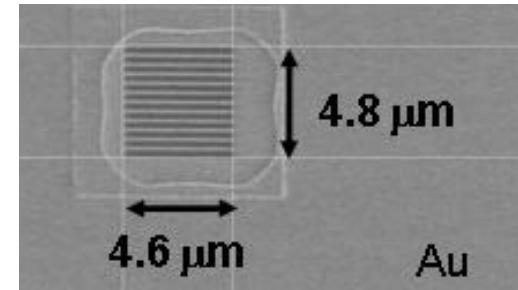
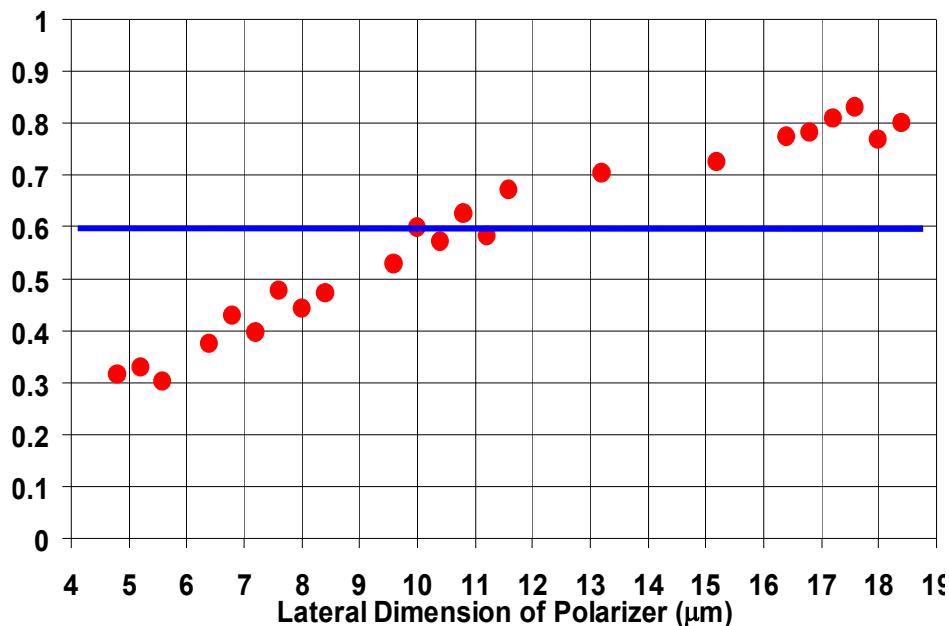
- Ferrule not shown
- 250 micron spacing
- Only 2 fibers shown, more can be utilized



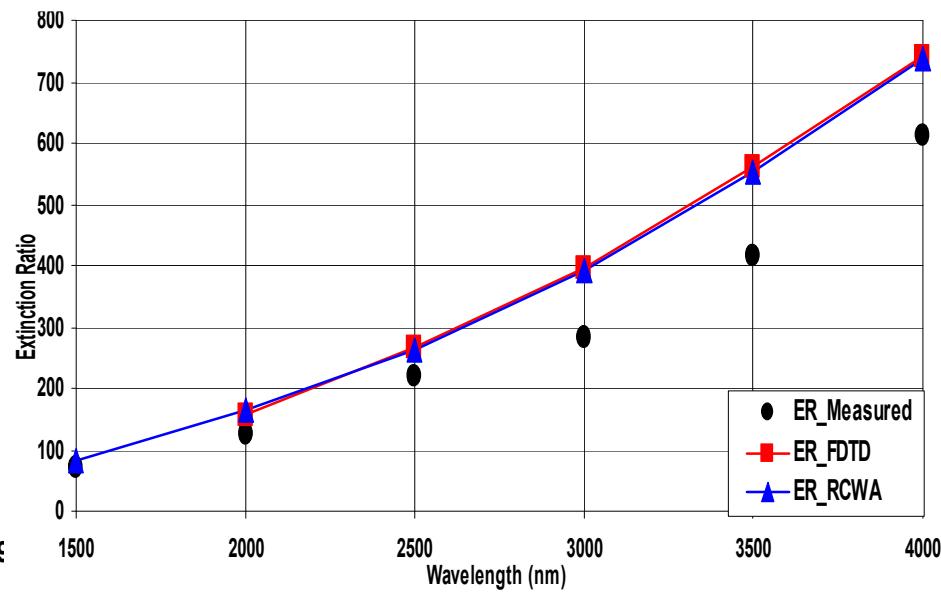


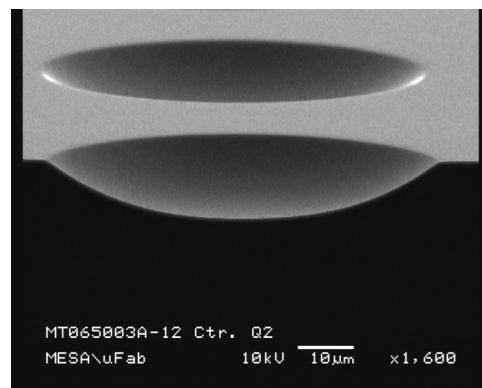
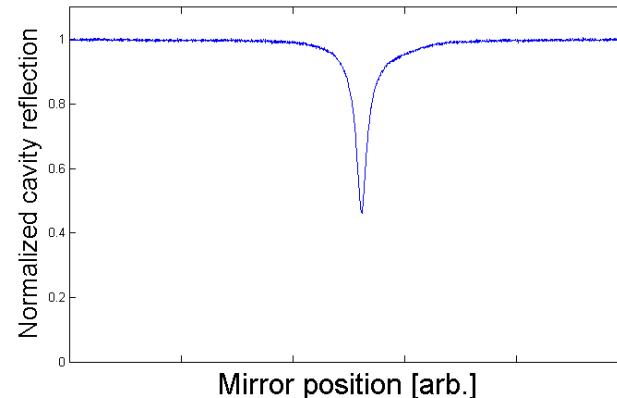
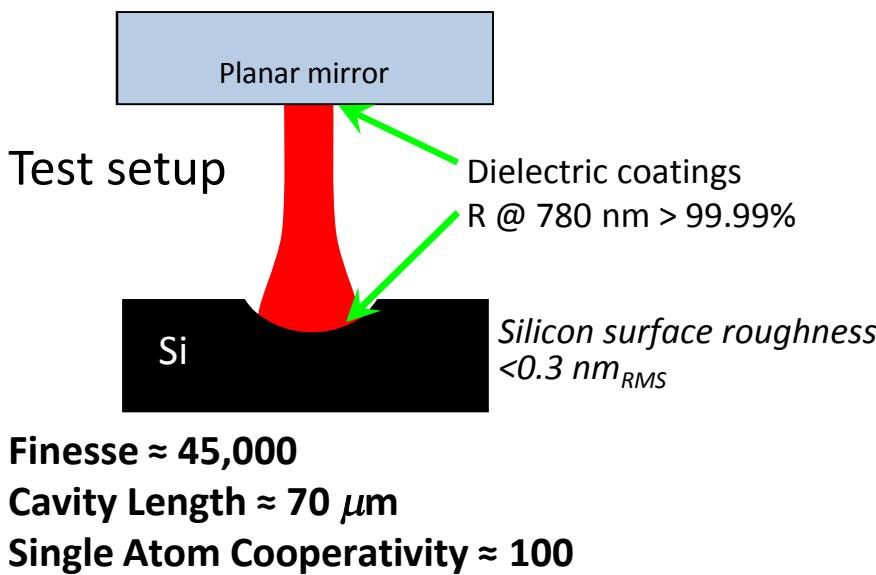


- Fabricated and tested fused silica and lithium fluoride polarizers with **extinction ratios > 100:1**
- Measured **transmitted signal (TM) >80%**
- Fabricated and tested **microwaveplates** with **9.4° rms** variation across broad MWIR band.

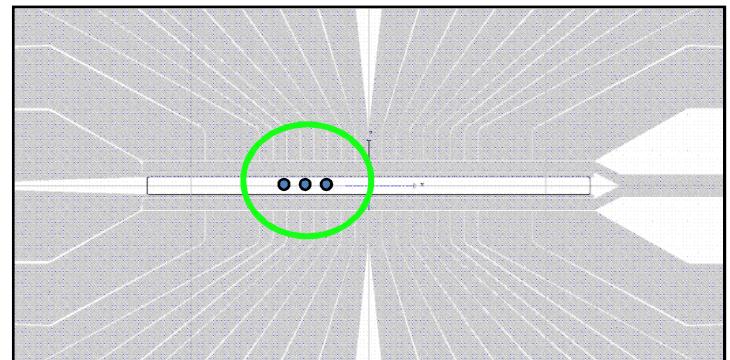
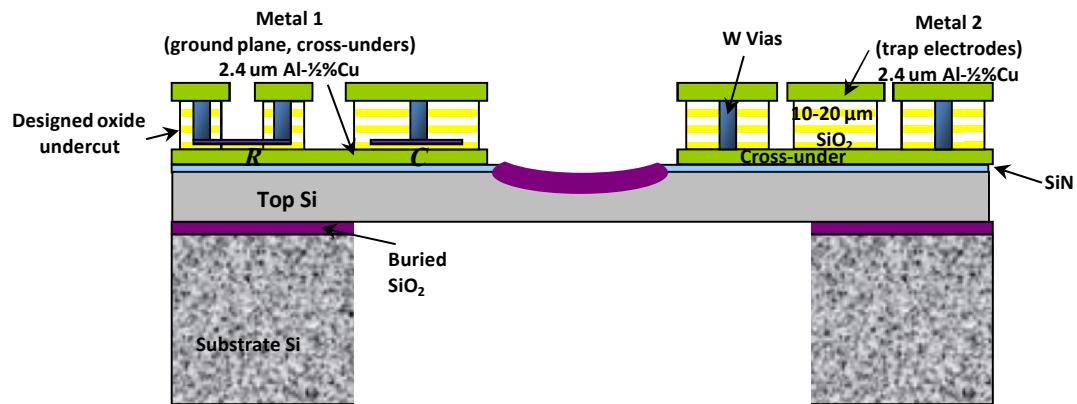

 Measured Transmission @ $\lambda = 3.39 \mu\text{m}$


Measured Broadband Extinction Ratio

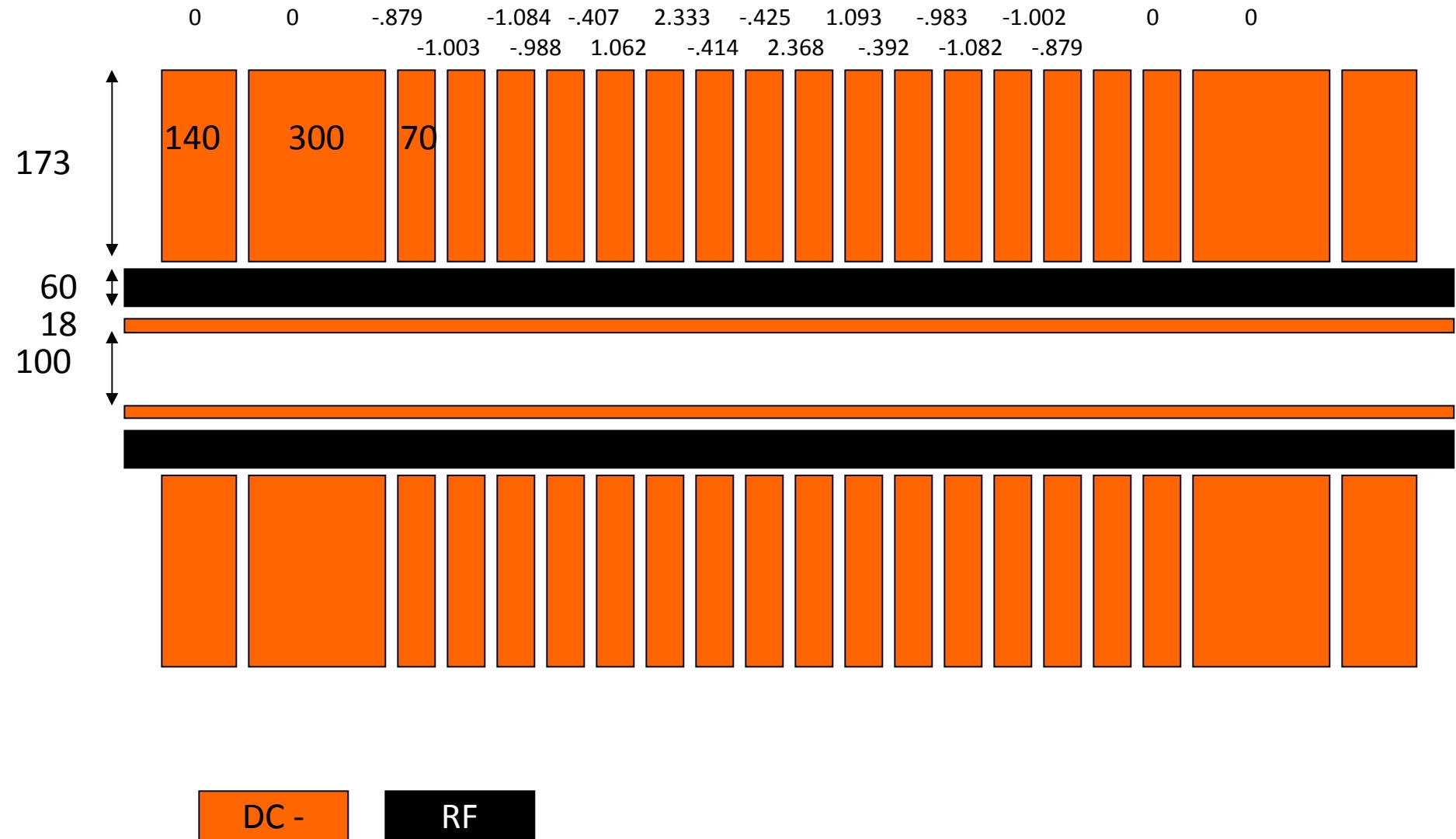


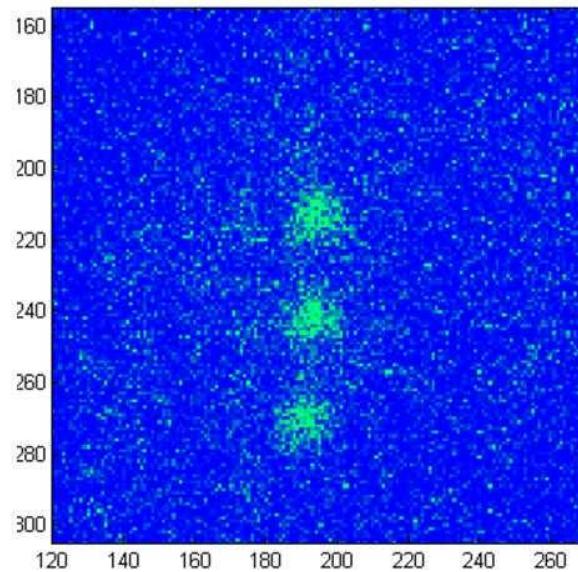
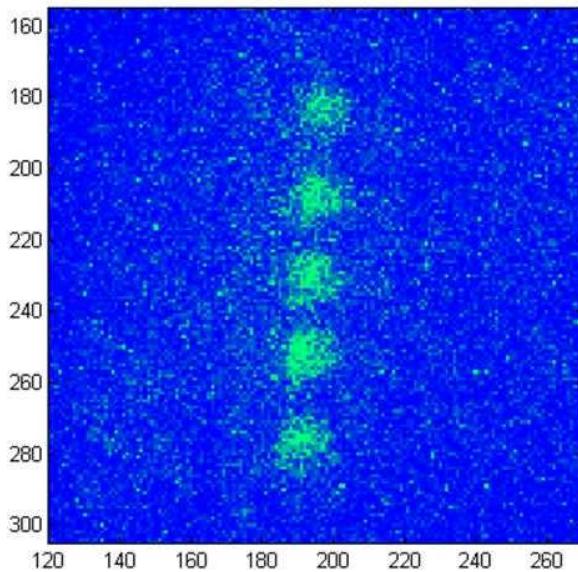


Microcavity mirrors may be placed in the top-Si of the microtrap chip

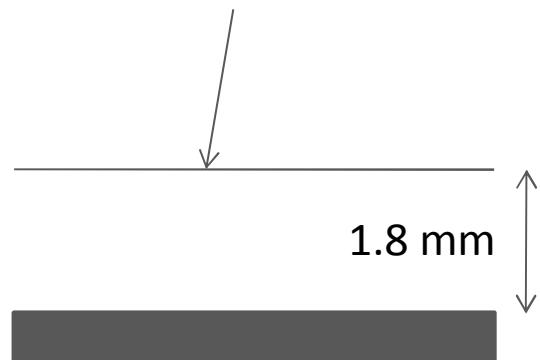


All gaps 7 microns





80% transparent
wire mesh



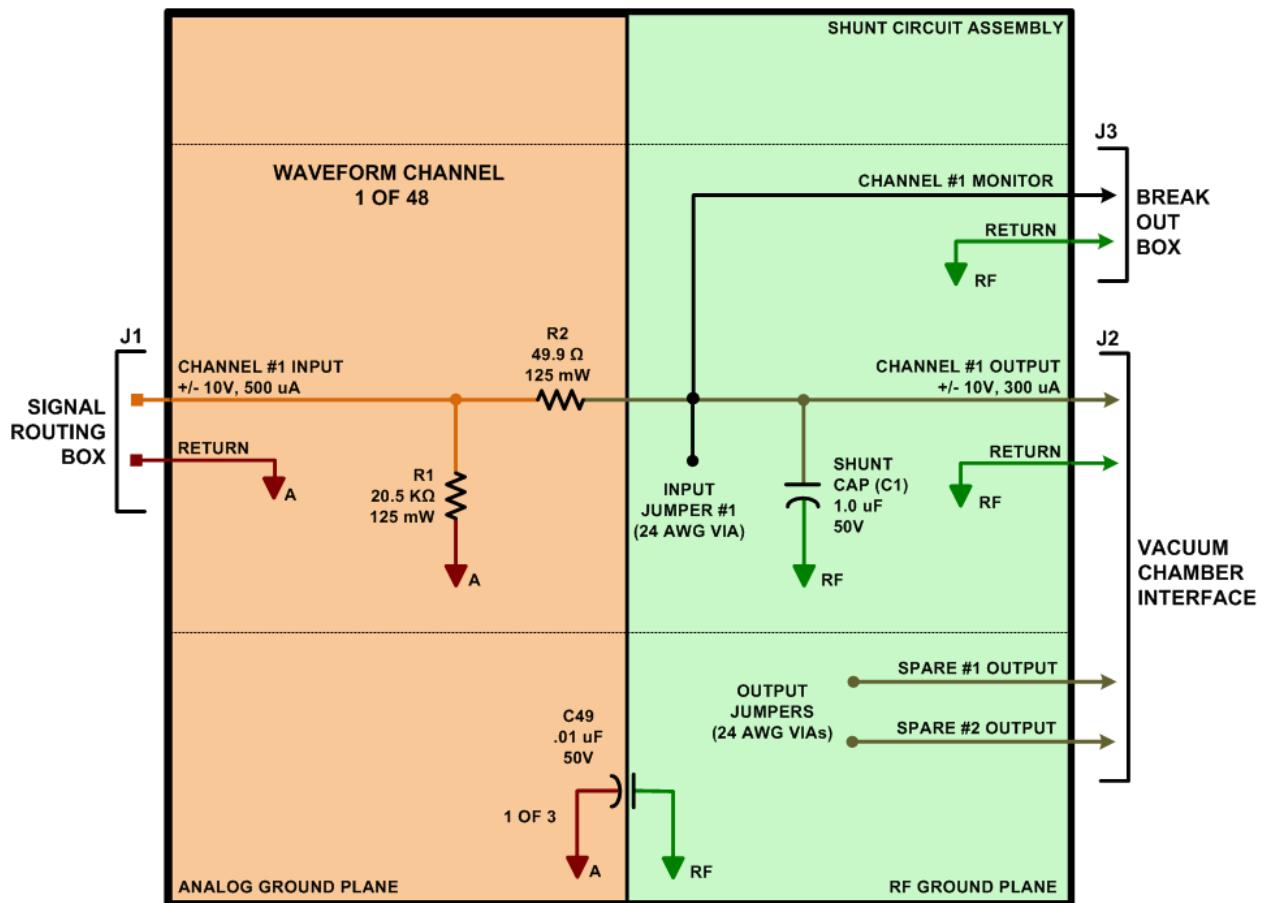
- RF: 150 V amplitude at 30 - 44 MHz
- RF null: 80 microns above surface, principal axes rotated 36°, 750 kHz axial frequency, 5.5 MHz radial frequency
- DC control: 42 independent control electrodes, controlled by NI DAC cards
 - +10 volts, 500 kHz max rep rate

- Doppler broadened linewidth of neutral ^{40}Ca is ~ 75 MHz (compared to natural linewidth of 34 MHz)
 - photoionization beams at 45 degrees to trap axis, so neutral atom flux aperture is 140 microns, vs 1 cm distance from trap to oven exit
- Loading rate at 1×10^{-10} torr (base pressure of 1.5×10^{-10} torr), 100 μw of 423 nm light, 1 mW of 375 nm light
 - ~ 1 ion per second
- 423 nm light has no affect on ion position, 375 nm light moves ion 2 microns longitudinally, with ~ 3 s settling time

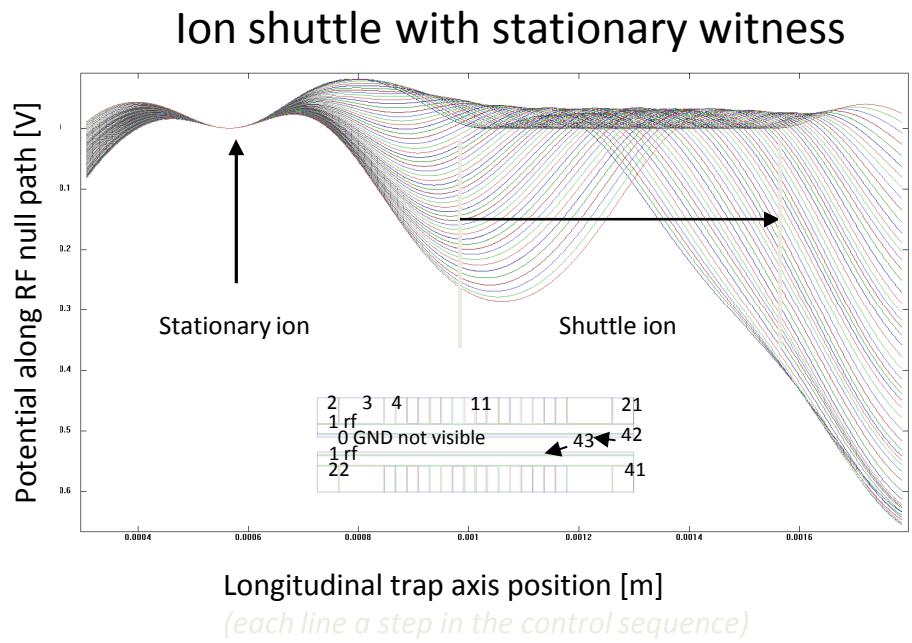
- Lifetime, for constant laser cooling: demonstrated 3 hours
- Lifetime, un-cooled: demonstrated 5 minutes, typical 3 minutes, now down to 20 seconds
- To Do: set up re-crystallization time measurement
- Measure heating rate in traps with different metal over coatings (evaporated or electroplated)

Shuttling/Splitting

- Successfully shuttled to neighboring electrode
 - Repeated round trip 10^6 times at 1 kHz, 10 kHz, 50 kHz
- Successfully shuttled 10 electrode widths (770 microns) 10^6 without loss
- Demonstrated splitting ions

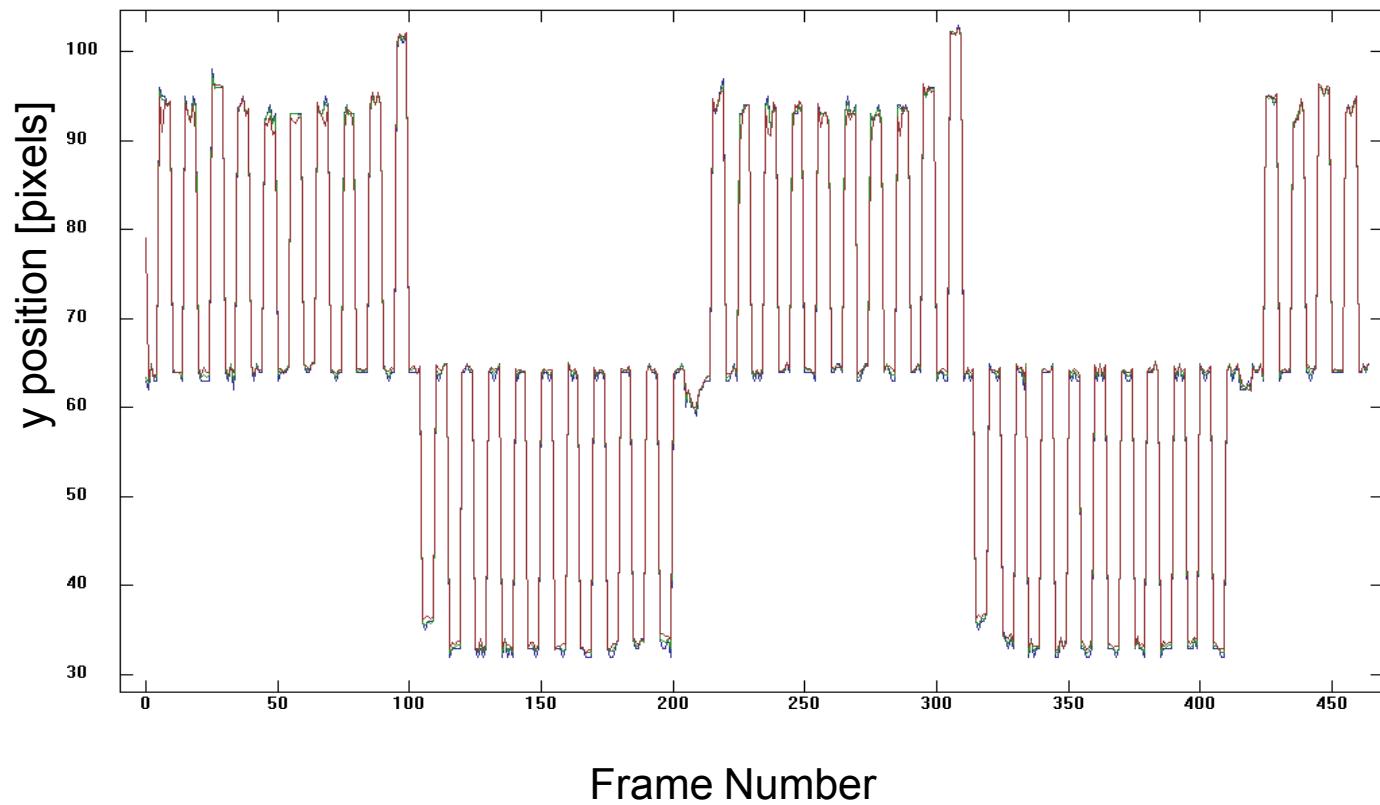
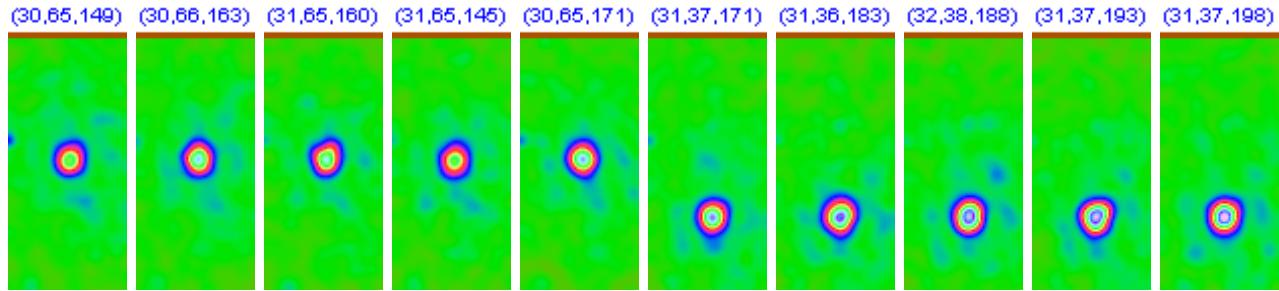


- Electrostatic potential determined numerically e.g.
 - Boundary element method coupled with
 - Interpolation of result
- At each desired step (location) the control solution is cast as a constrained optimization problem
 - The voltage budget is minimized by a proxy function (sum of the squared free electrode potentials)
 - The constraints for each ion typically
 - The potential at the ion is zero (1 constraint)
 - The electric field at the ion is zero (3 constraints)
 - The longitudinal confinement frequency (1 constraint)
- In this case the resulting linear system of equations is solved directly
 - In other cases, a non-linear system might be iterated

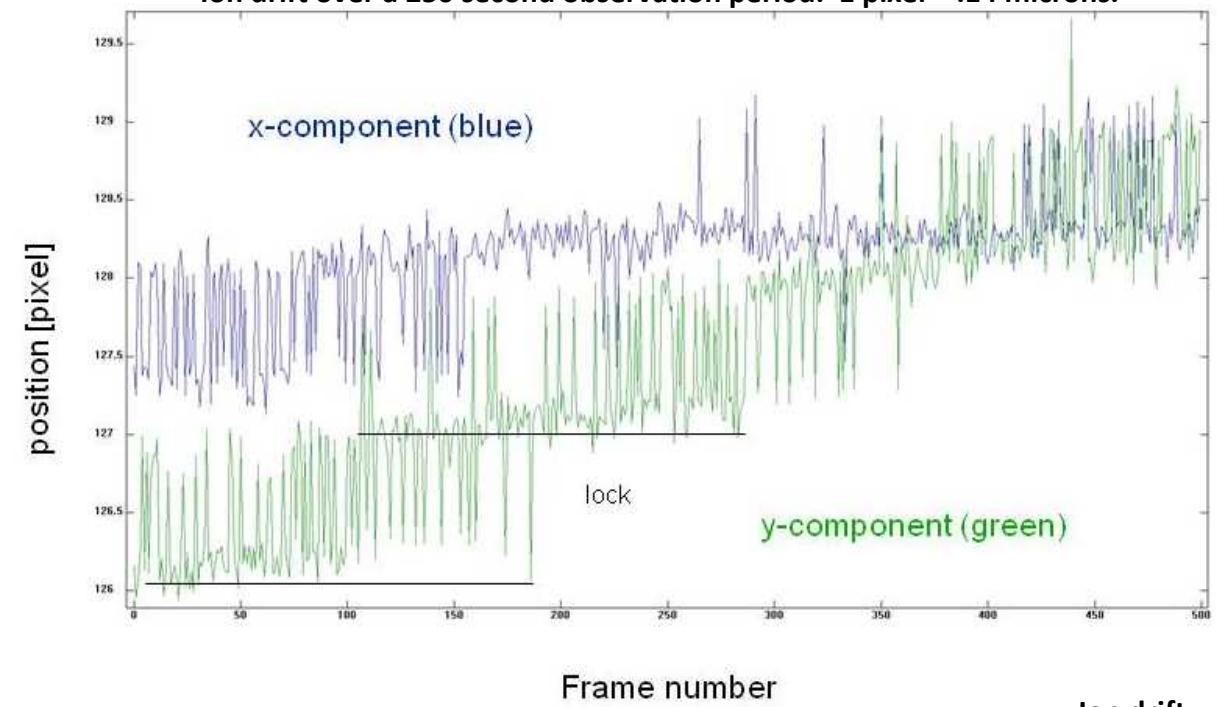


- Example shuttle ion from station 11 to 18 (with stationary witness at station 5)
 - 10 constraints: $2 \times (V, V_x, V_y, V_z, V_{xx})$
 - Sum of control voltages squared minimized
 - Required voltage budget 6.53V

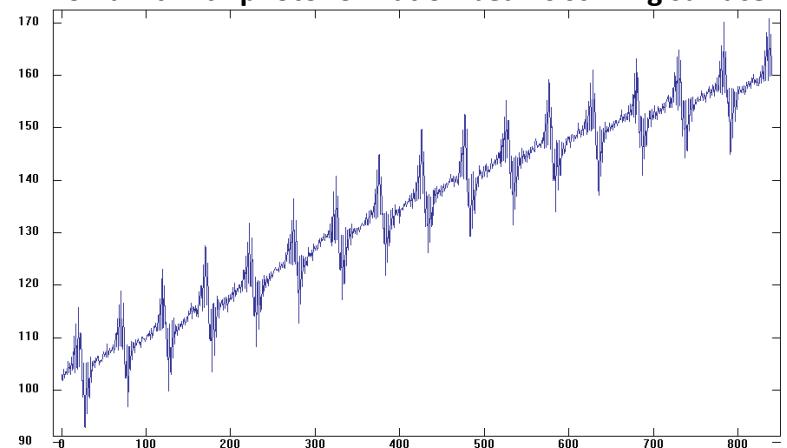
Simulations agree to within 5% of experiment

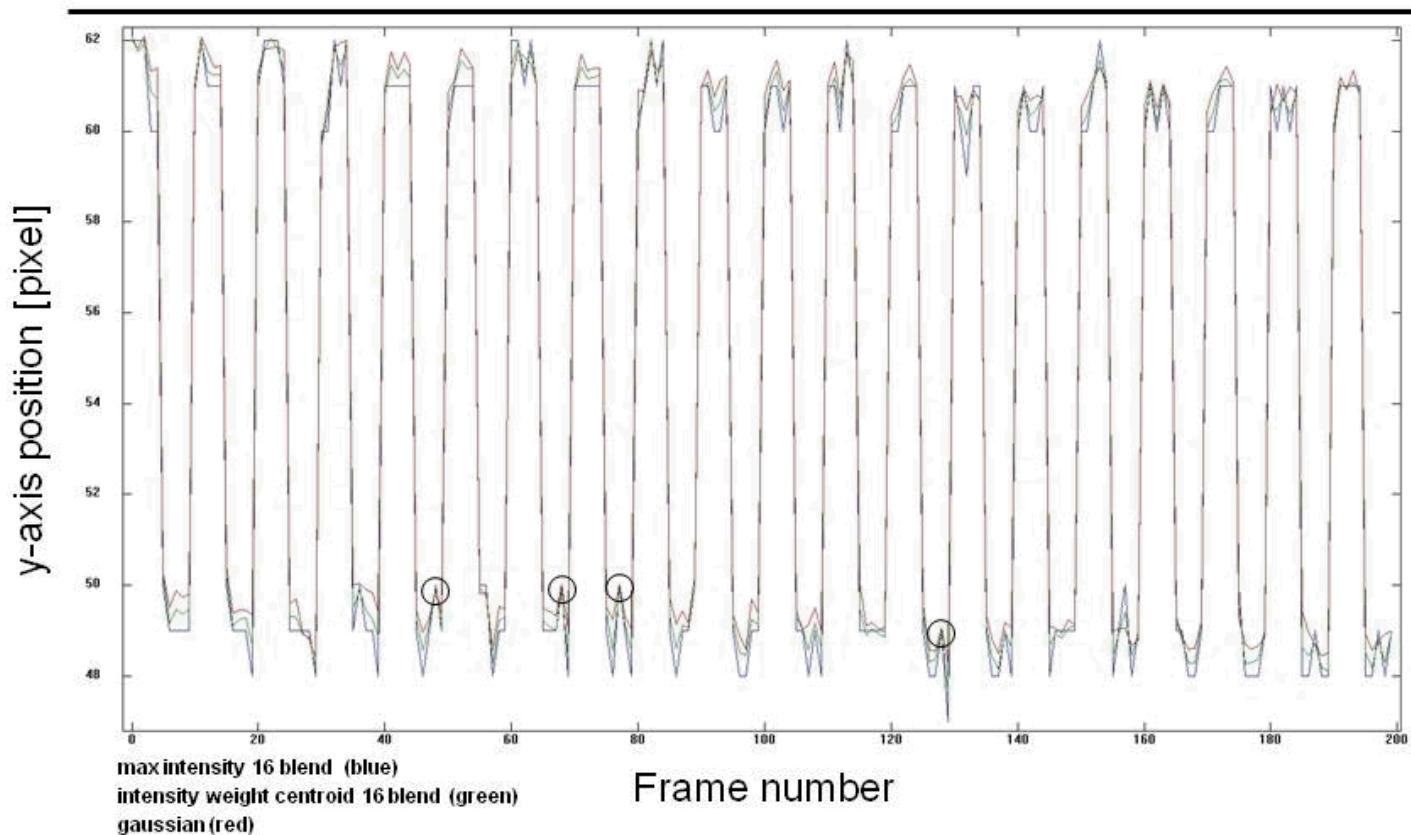


Ion drift over a 250 second observation period. 1 pixel = .14 microns.



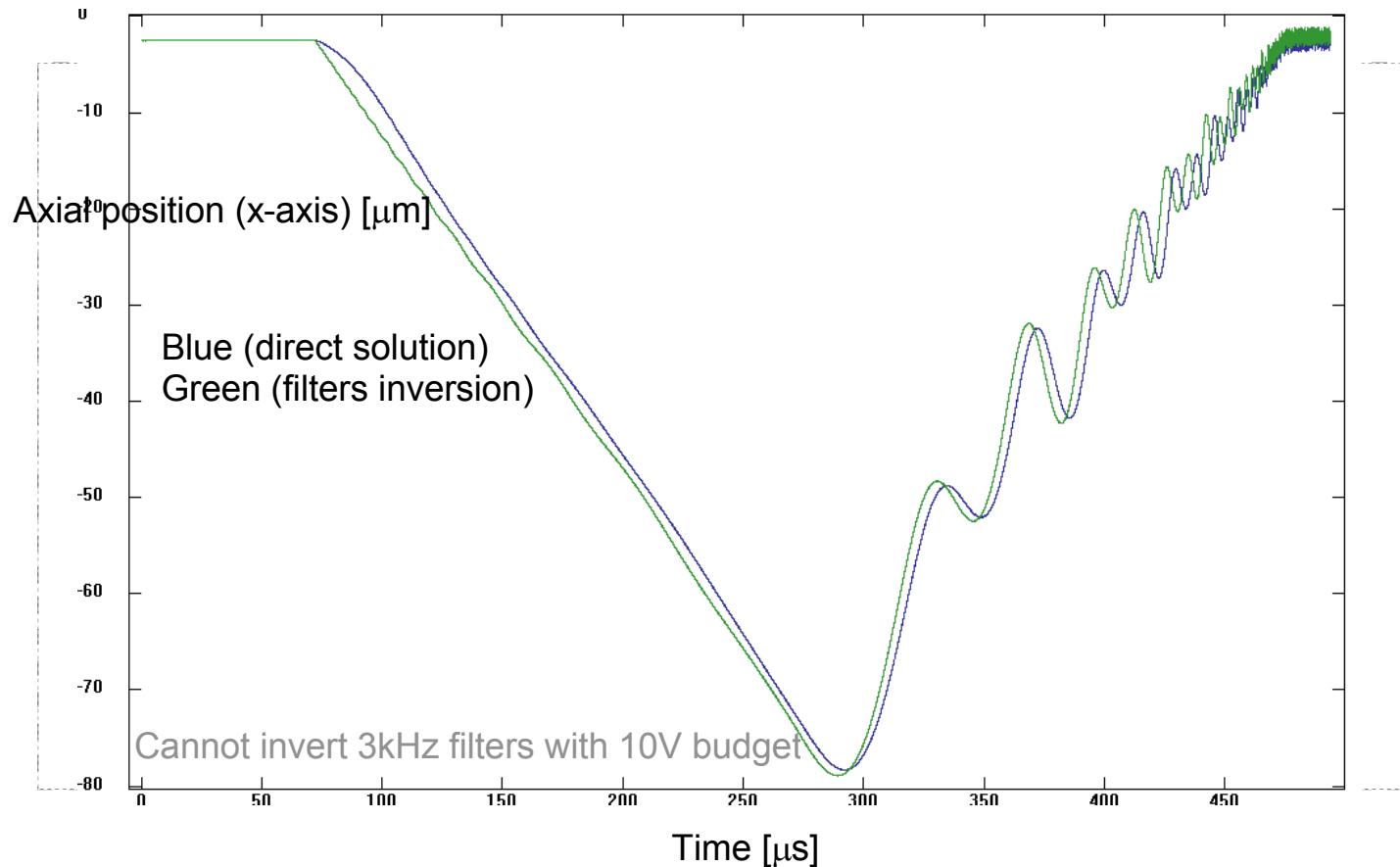
Ion drift with photo-ionization beams striking surface

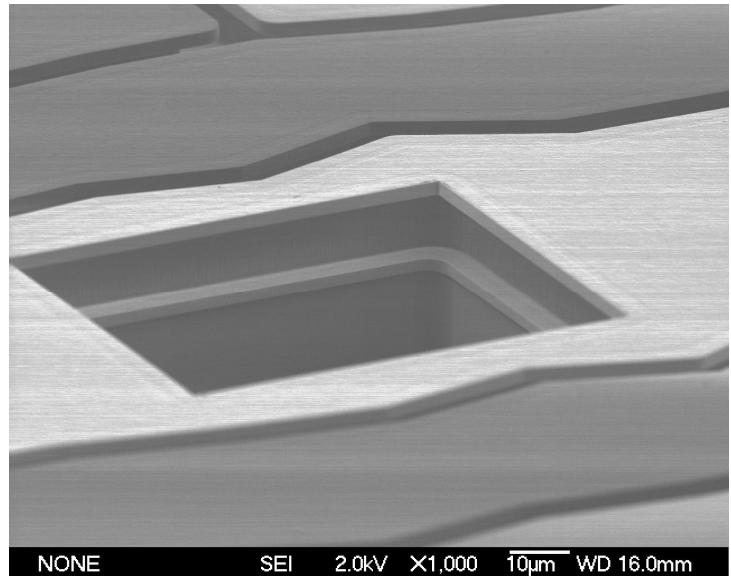
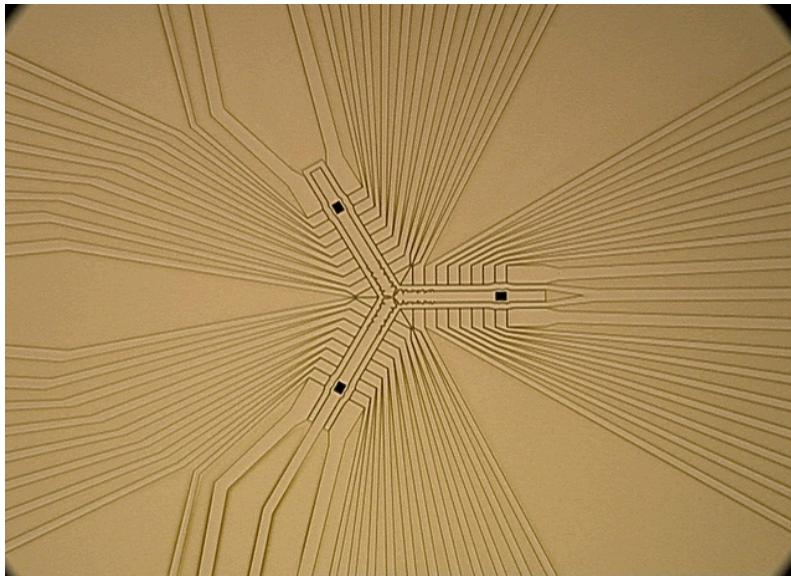




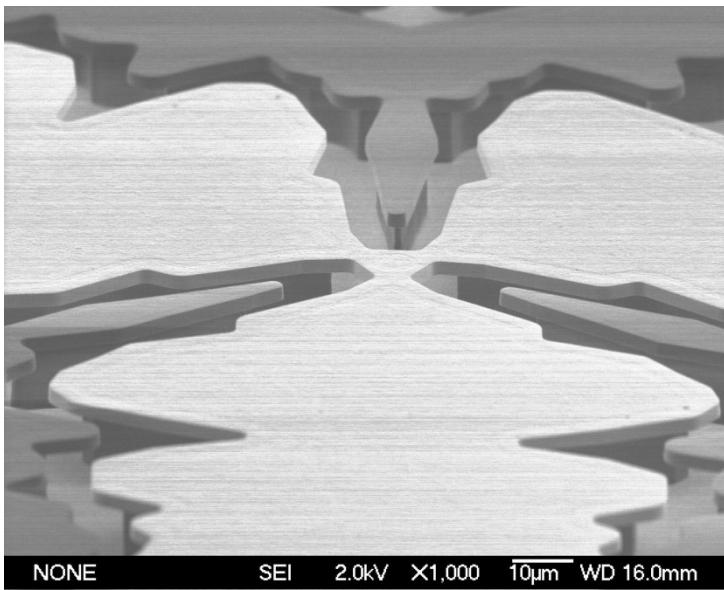
Ion switching between two positions to see if there is drift inducing charging. Each frame is 1 second.

Shuttling simulation incorporating filters

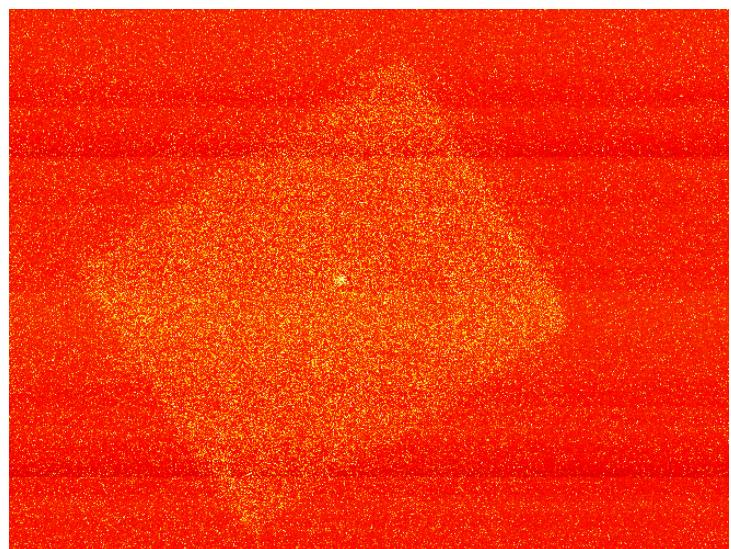


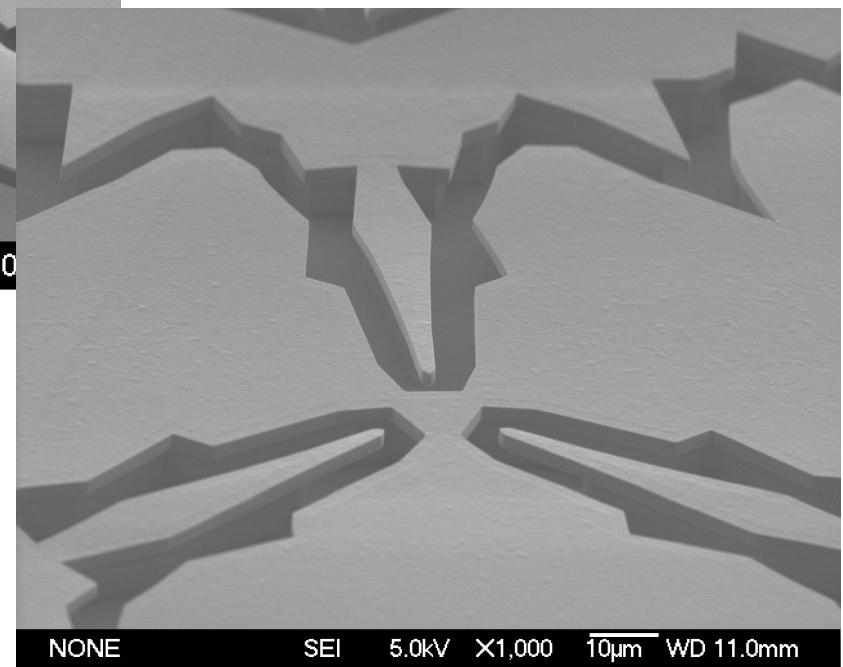
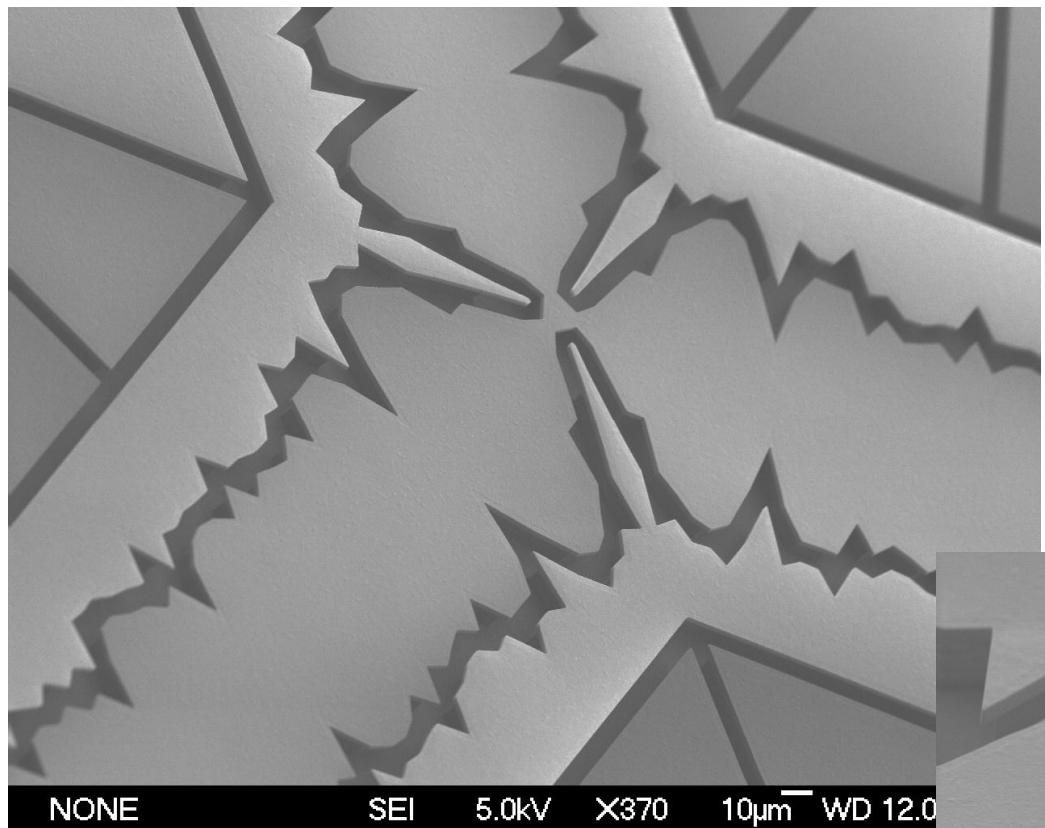


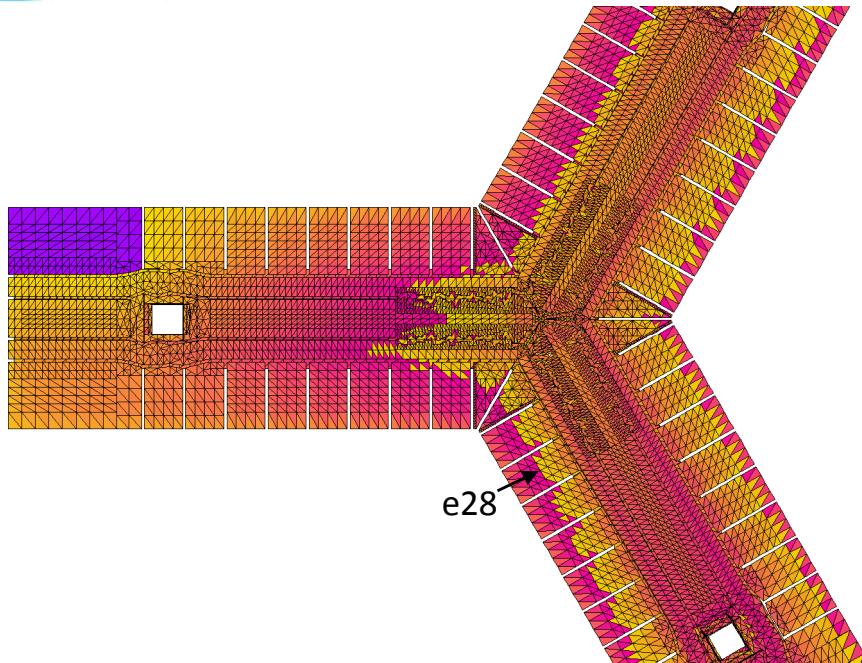
NONE SEI 2.0kV $\times 1,000$ 10 μm WP 16.0mm



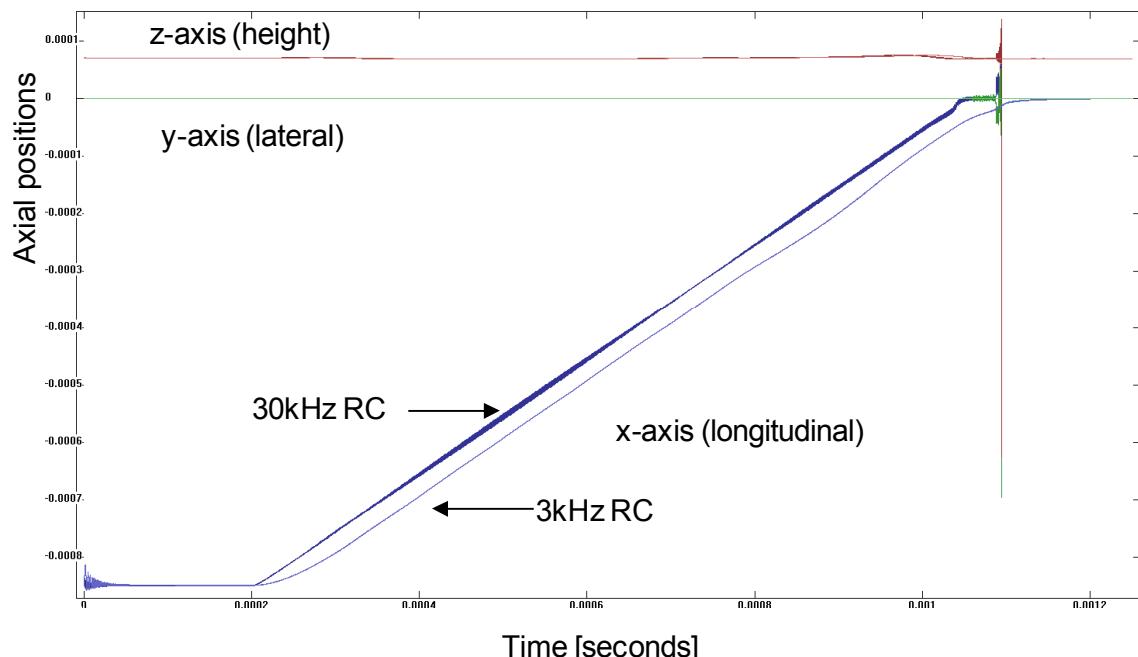
NONE SEI 2.0kV X1,000 10µm WD 16.0mm





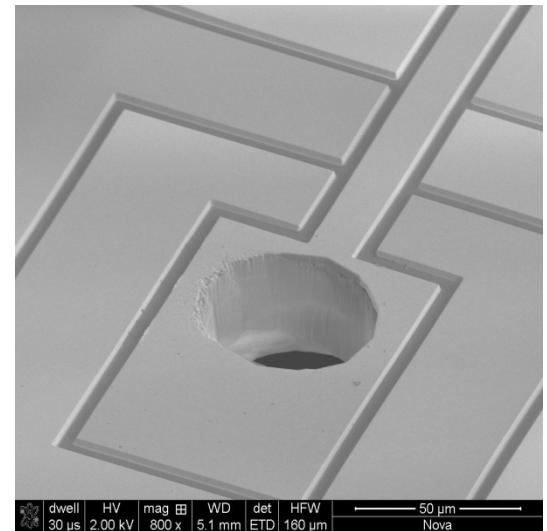
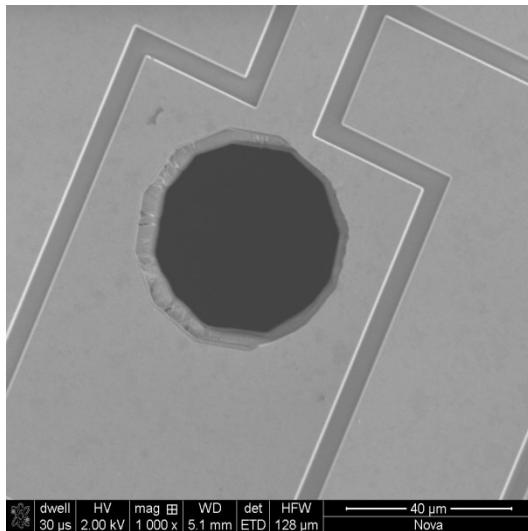
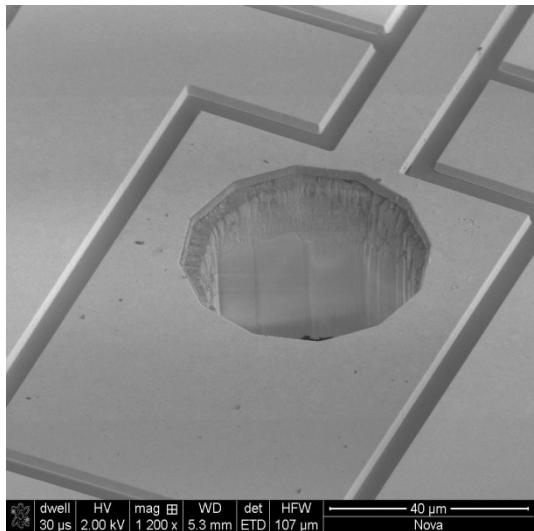


RS816 Y-Junction ion shuttle simulation



End

Top row: images of holes after normal incident FIB milling of quartz



Top row: (unfortunately not oblique) images of holes after 90-22 = 68 deg tilt FIB milling of quartz

