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Evaluation of Soft-Core Processors on a Xilinx Virtex-5 Field Programmable Gate Array

XRTC Conference

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Outline

- Rationale
- Background
- Test Setup
- Performance Results
- Utilization Results
- Beam Testing Experiments
- Conclusion

Rationale

- **Evaluate soft-core processors within a Xilinx Virtex-5 FPGA to possibly provide a more flexible and capable processing solution for the DOE/NNSA's Joint Architecture Standard (JAS).**
  - **Results can help architect a hardware design for a particular application:**
    - **Trade-offs between using FPGA resources.**
    - **On-chip vs. external memories.**
    - **What types of memories to use.**
    - **Etc.**

Background

- **Goal:**
  - **Use performance metrics and resource utilization to evaluate the soft-core processors.**
- **ML507 Development board used for evaluation:**
  - **XC5VFX70T – ff1136 -1 FPGA**
- **Two soft-core processors were evaluated:**
  - **MicroBlaze (MB) v7.10.d - Xilinx**
  - **Leon3 (SPARC v8) - Gaisler**
    - **Non-fault tolerant (FT) version.**
    - **Fault tolerant (FT) version:**
      - **FT integer unit (IU)**
      - **FT floating point unit (FPU) – 8-bit EDACing**
      - **FT cache – 4-bit parity detection**
      - **FT external memory controller for SRAM – 7-bit EDACing**

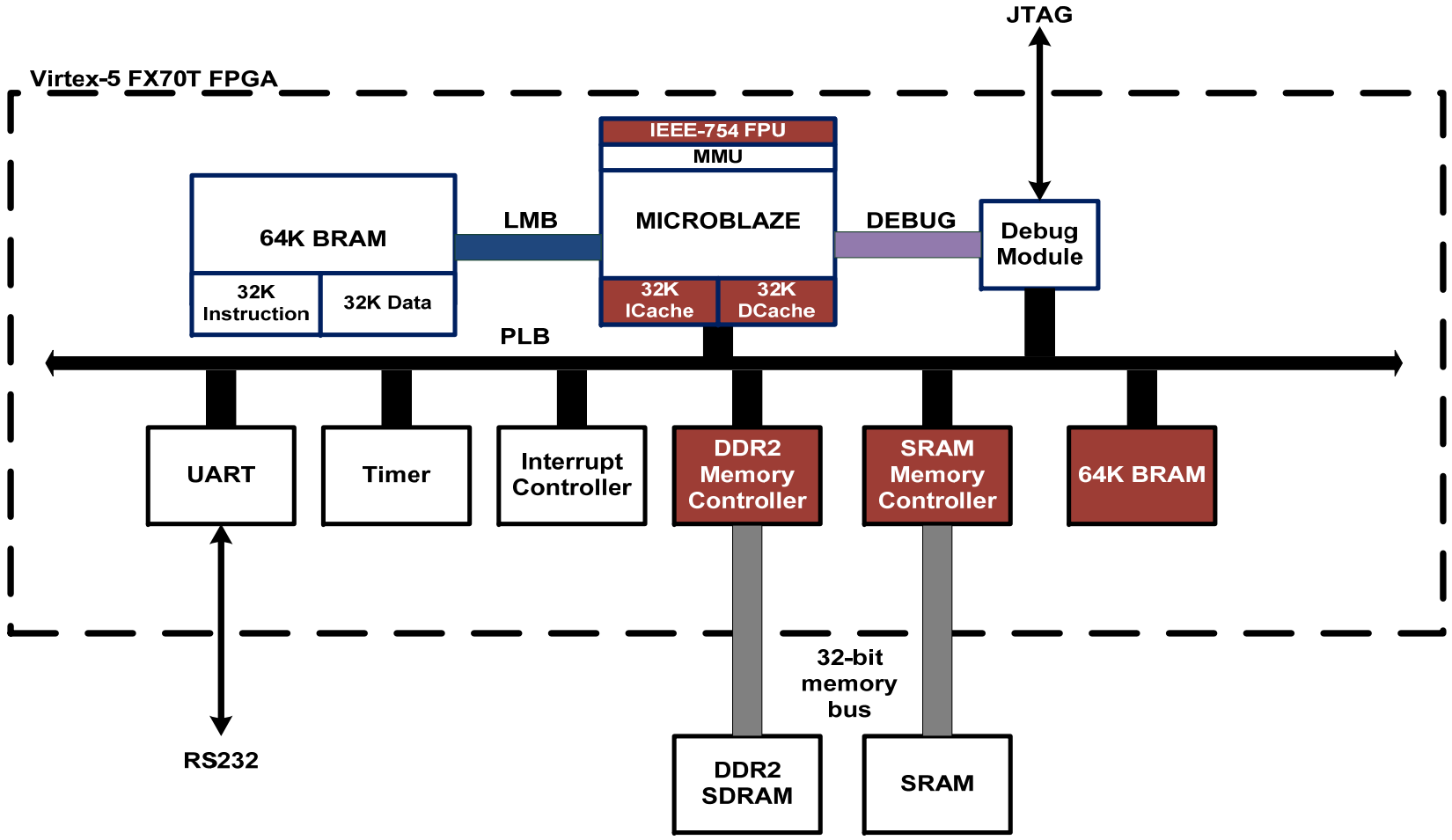
Hardware Test Setup

- Various configurations were used in hardware to test performance:
  - Cache enabled/disabled
  - FPU enabled/disabled
  - Memory Management Unit (MMU) disabled when available.
  - Various frequencies:
    - MicroBlaze – 25, 50, 75, 100, 125, 133, 150 MHz.
    - Leon3 – 50, 80, 100 MHz.
      - Limited by the use of the DCM for timing.

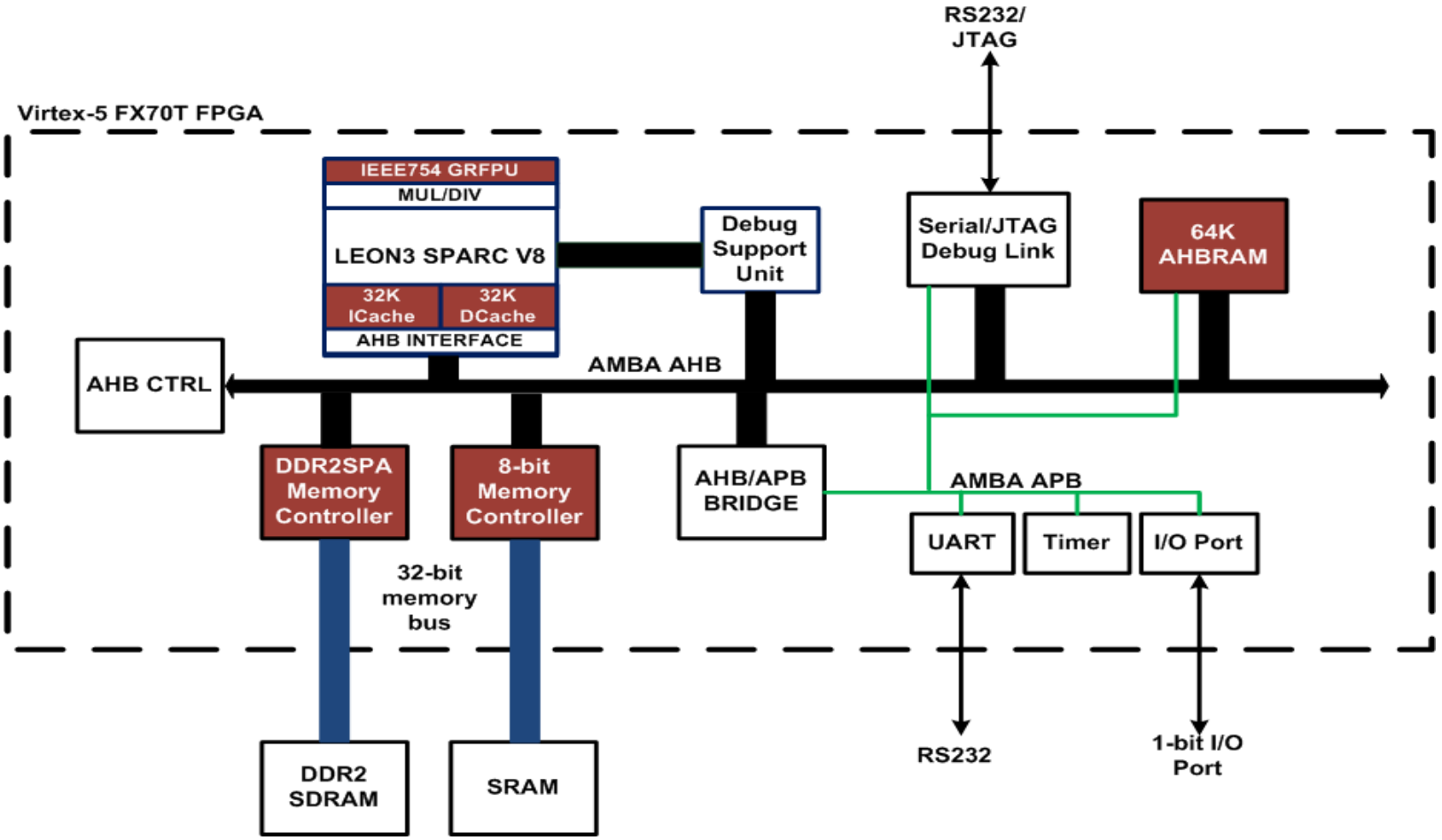
Software Test Setup

- To evaluate performance:
  - Dhrystone – fixed-point operation metrics.
  - Whetstone – floating-point operation metrics.
- Code location in memory:
  - On-chip memory using the LMB, PLB, AHB RAM
  - External memory using SRAM, DDR2 SDRAM
- Compiler optimizations for both processors:
  - Level 1 : Jump and pop optimizations.
  - Level 2 : Standard optimization level.
  - Level 3 : Adds more expensive options which can increase code and create less efficient code.

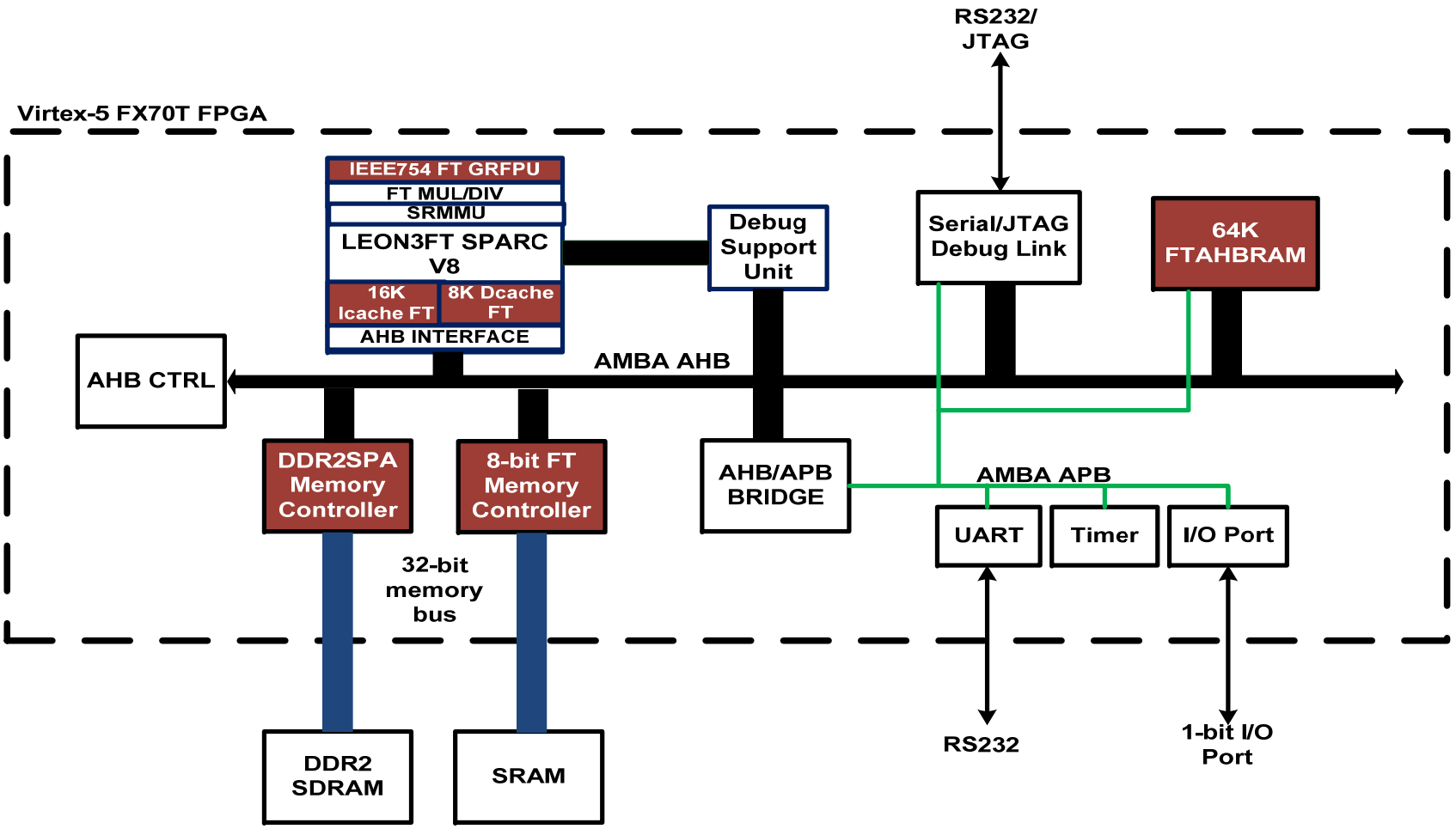
MicroBlaze Block Diagram



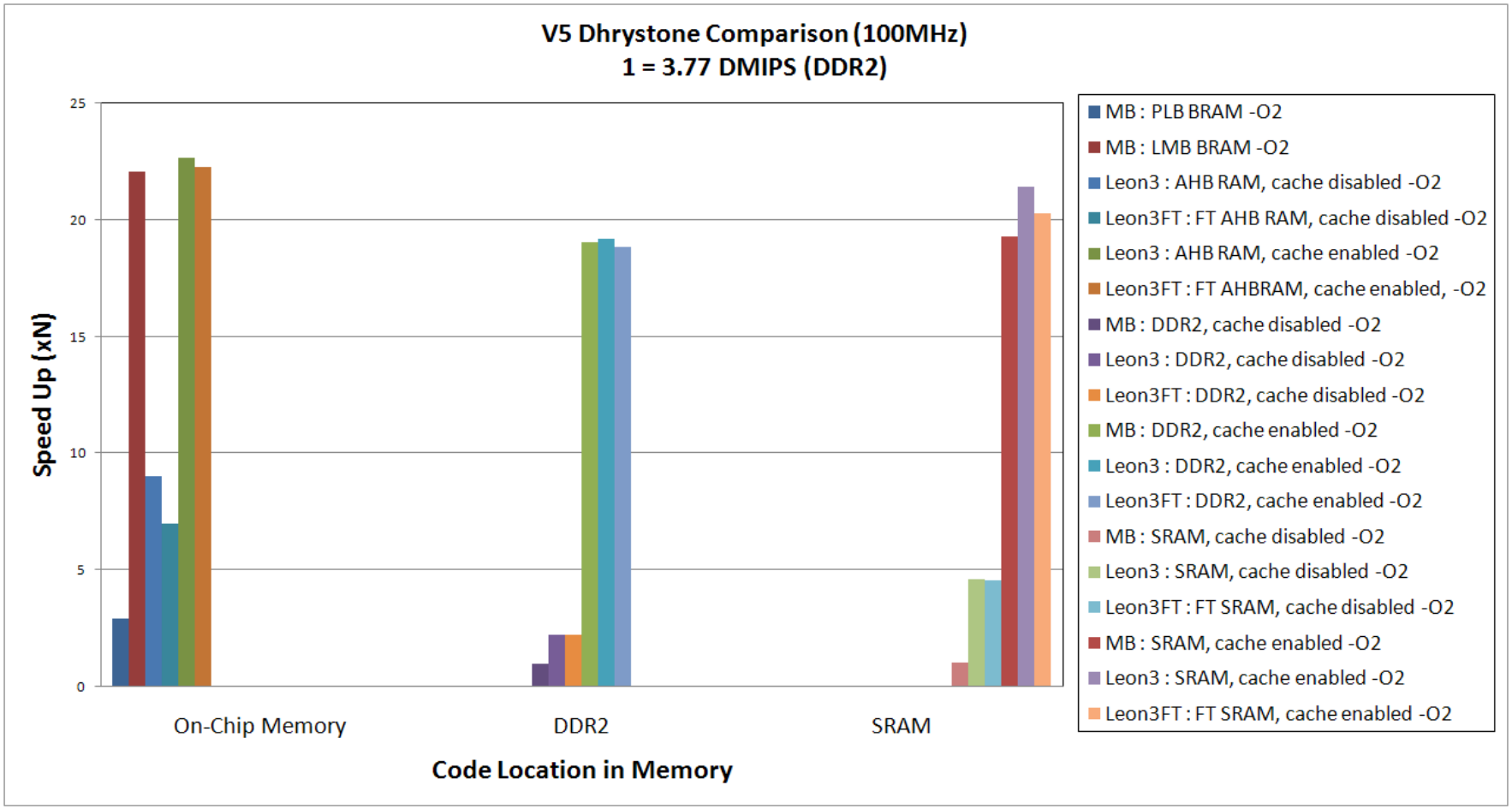
Leon3 Block Diagram



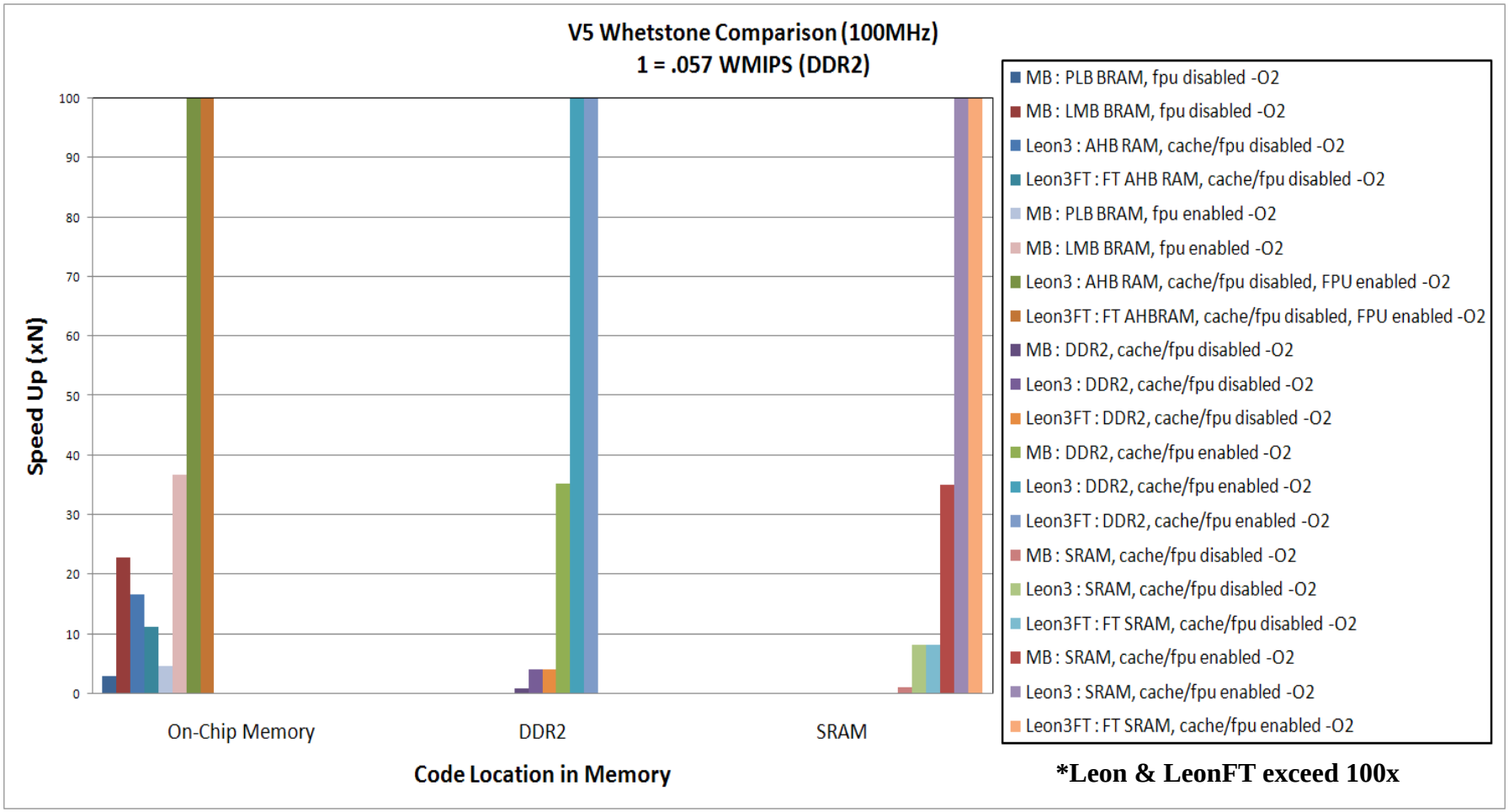
Leon3FT Block Diagram



Dhrystone Results

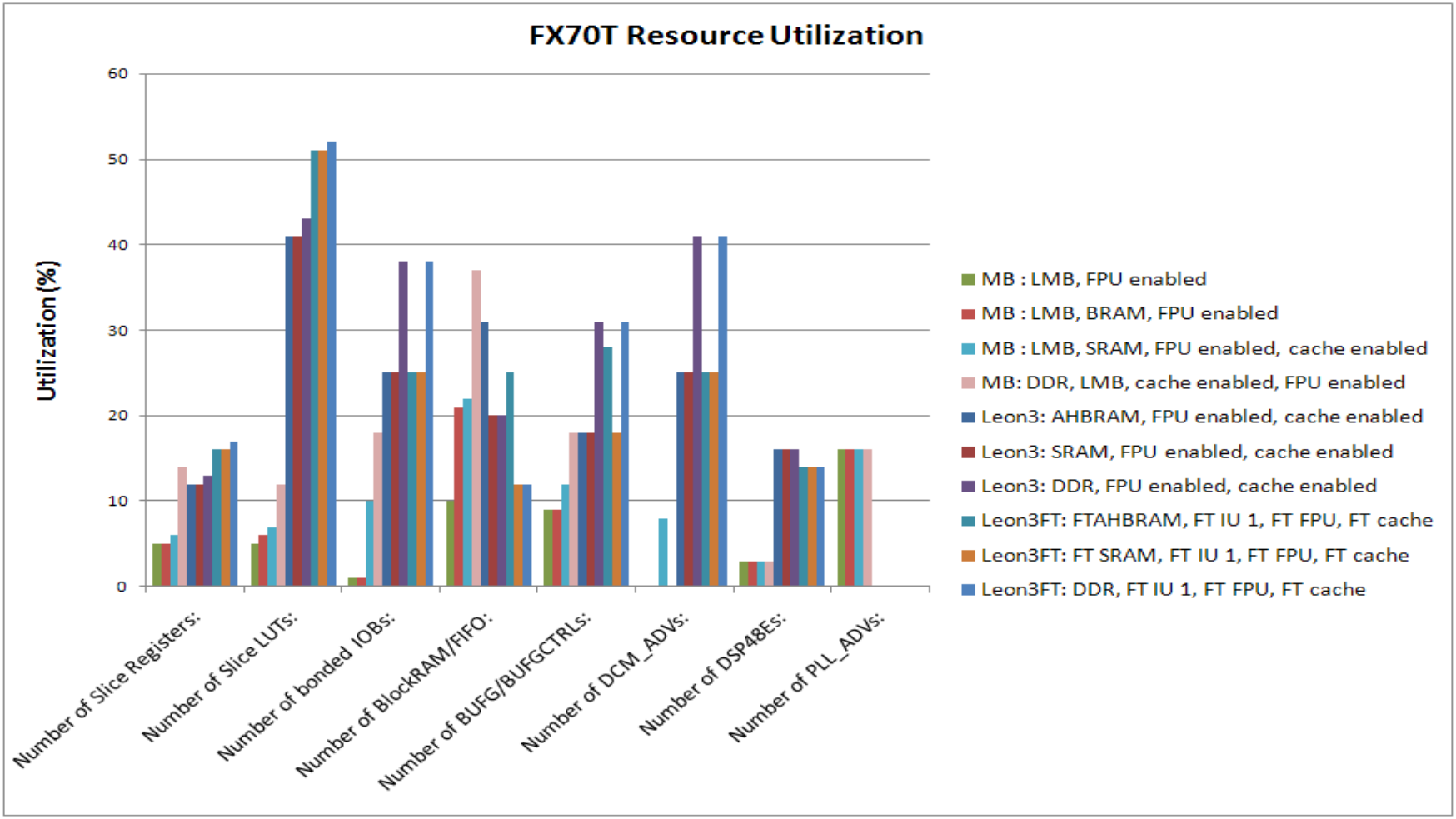


Whetstone Results



***Leon & LeonFT exceed 100x**

Resource Utilization



Where Do We Go From Here?

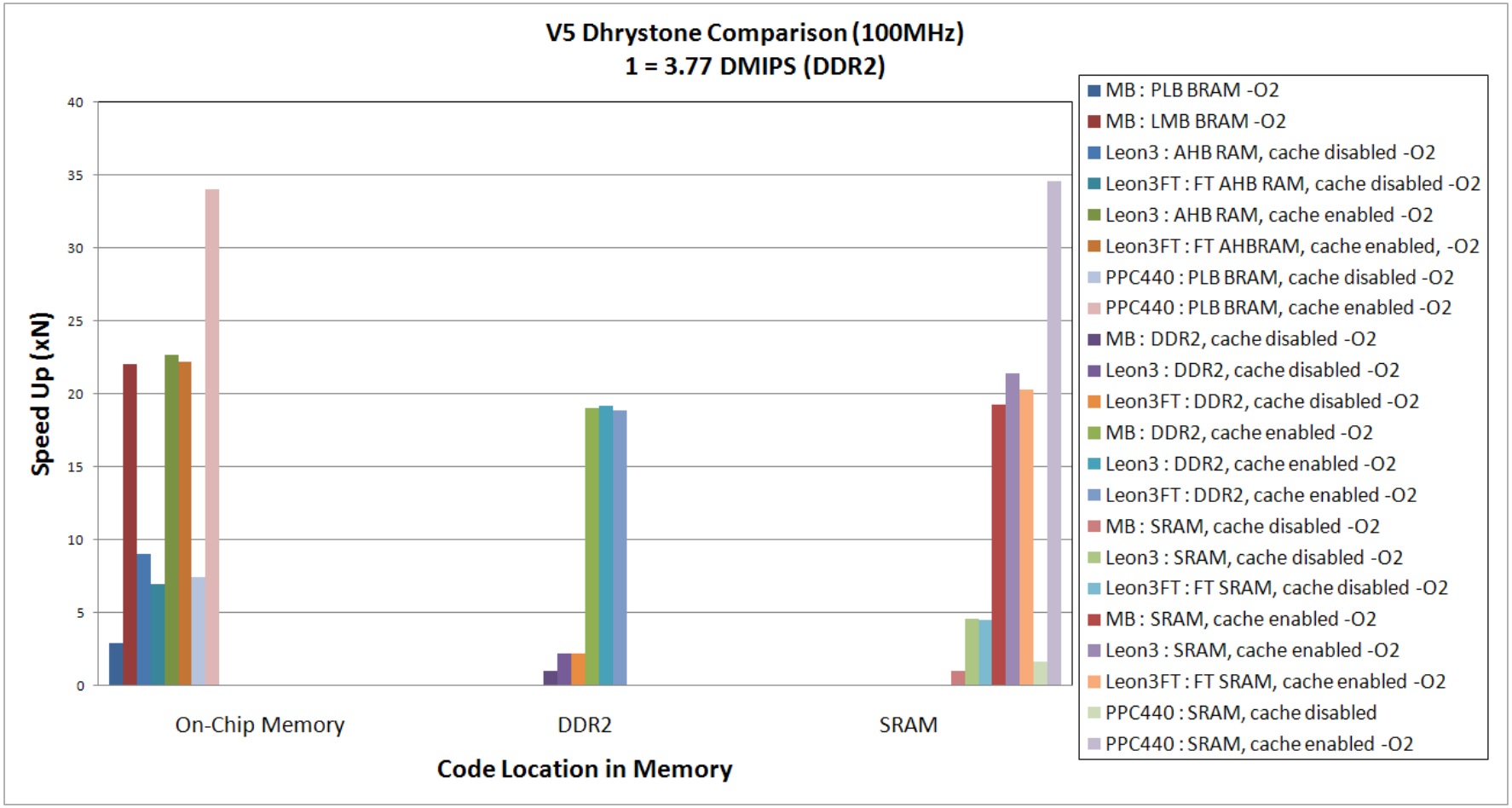
- **Beam testing the Leon3 and Leon3FT.**
  - **Simple Leon3 design –**
    - **“Wiggle” a pin and count the number of resets.**
    - **Test Write Enable (WE) issue seen in the MB.**
  - **Leon3 and Leon3FT on commercial FX130T.**
    - **FPU/FT FPU enabled/disabled.**
    - **FT IU enabled**
    - **On-chip memory with FT enabled/disabled.**
    - **External memory with FT enabled/disabled.**
  - **Leon3 and Leon3FT on radiation hardened V5QV.**

Conclusion

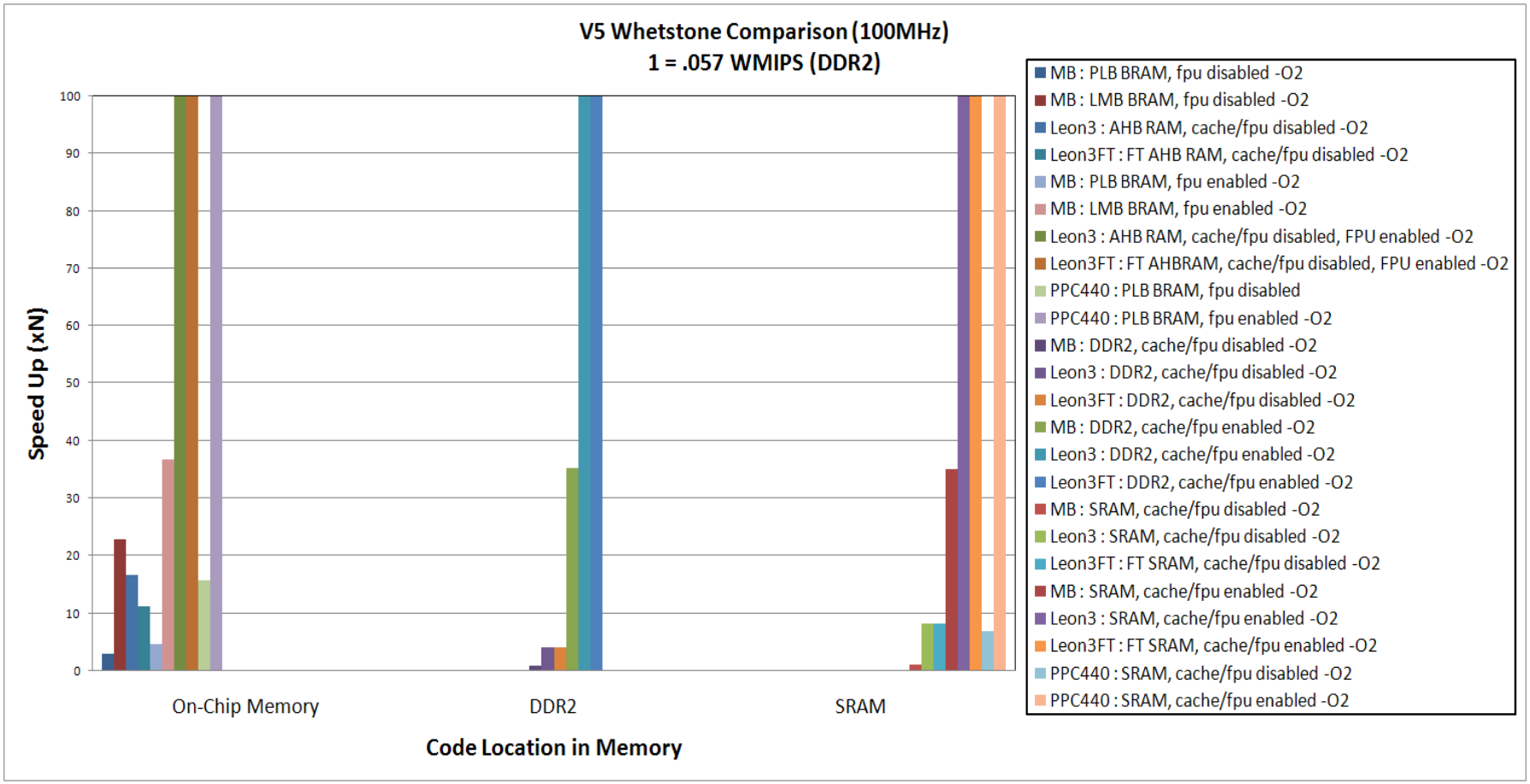
- **Enabling the cache and FPU greatly improves the processor's performance:**
  - **Leon3/Leon3FT:**
    - **More efficient than MB with cache disabled while running out of external memory.**
      - **With cache enabled, the performance is similar.**
    - **With FPU enabled Leon/LeonFT is much more efficient.**
  - **MB:**
    - **With FPU disabled, MB is more efficient, but performance is still low.**
- **Resource Utilization:**
  - **Cost vs. Performance:**
    - **Leon performs better than MB, but requires more resources.**

Bonus Slides

Dhrystone – PPC440



Whetstone – PPC440



Resource Utilization – PPC440