

Applications and Processing: Full-Tape-Thickness Features in LTCC

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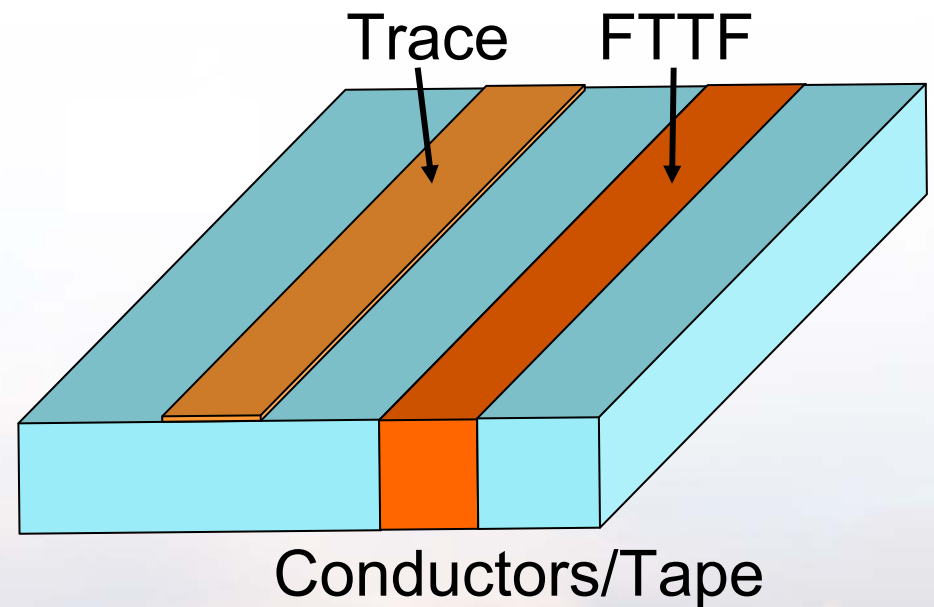
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Outline

- Sandia Overview (3 slides)
- Technical Introduction
 - Processing for low temperature cofired ceramic (LTCC)
 - Motivation
 - Review of FTTF
- Feature Construction
 - Staggered FTTF
 - Solid FTTF
 - Sidewall Metallization
- Summary



Sandia's Sites

**Albuquerque,
New Mexico**



**Livermore,
California**



**Kauai,
Hawaii**



**Yucca Mountain,
Nevada**



**WIPP,
New Mexico**



Pantex, Texas



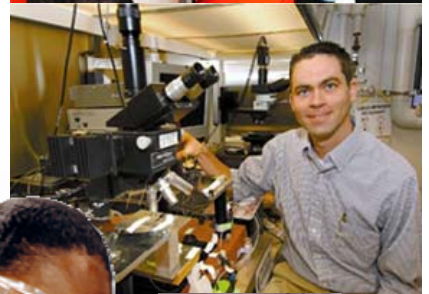
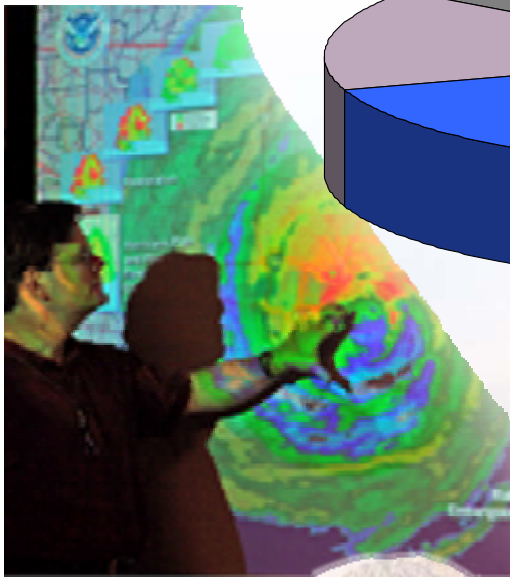
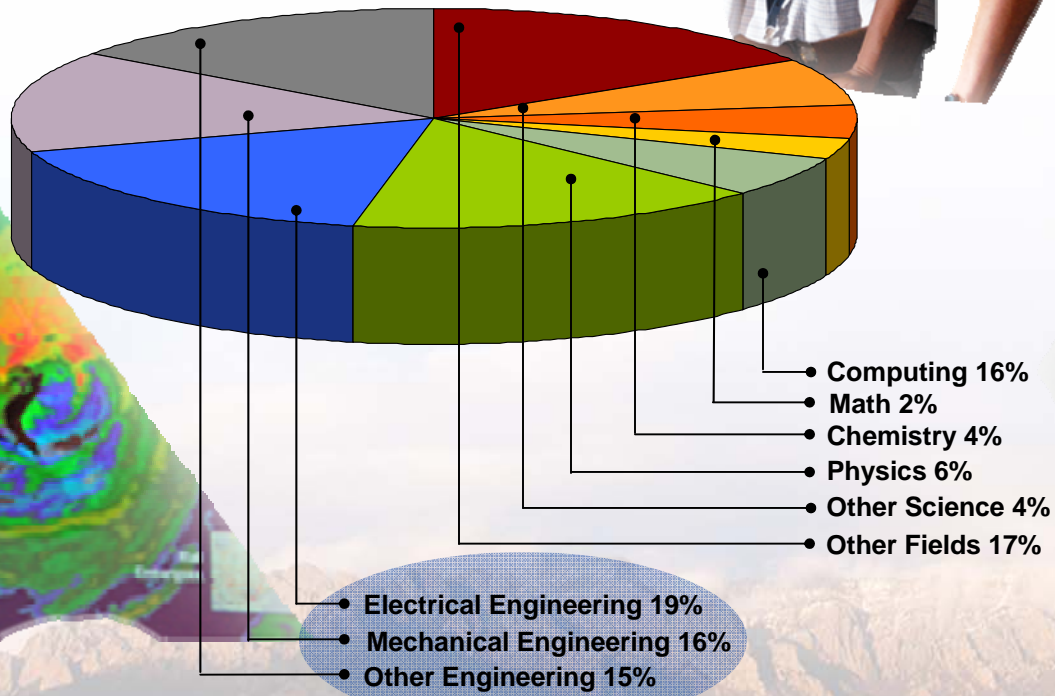
Tonopah, Nevada



Sandia's People

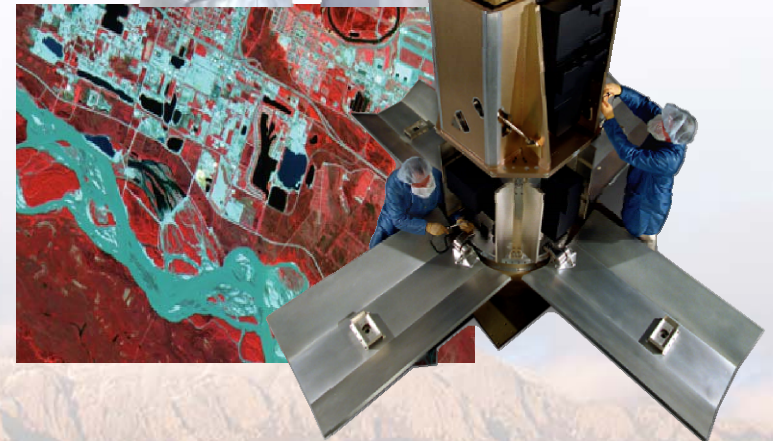
- On-site workforce: 11,200
- FY08 permanent workforce: 8,400
- FY08 gross payroll: \$886.1M
- FY08 budget: \$2.3B

Technical Staff (3,844) by Degree
(End of FY08)

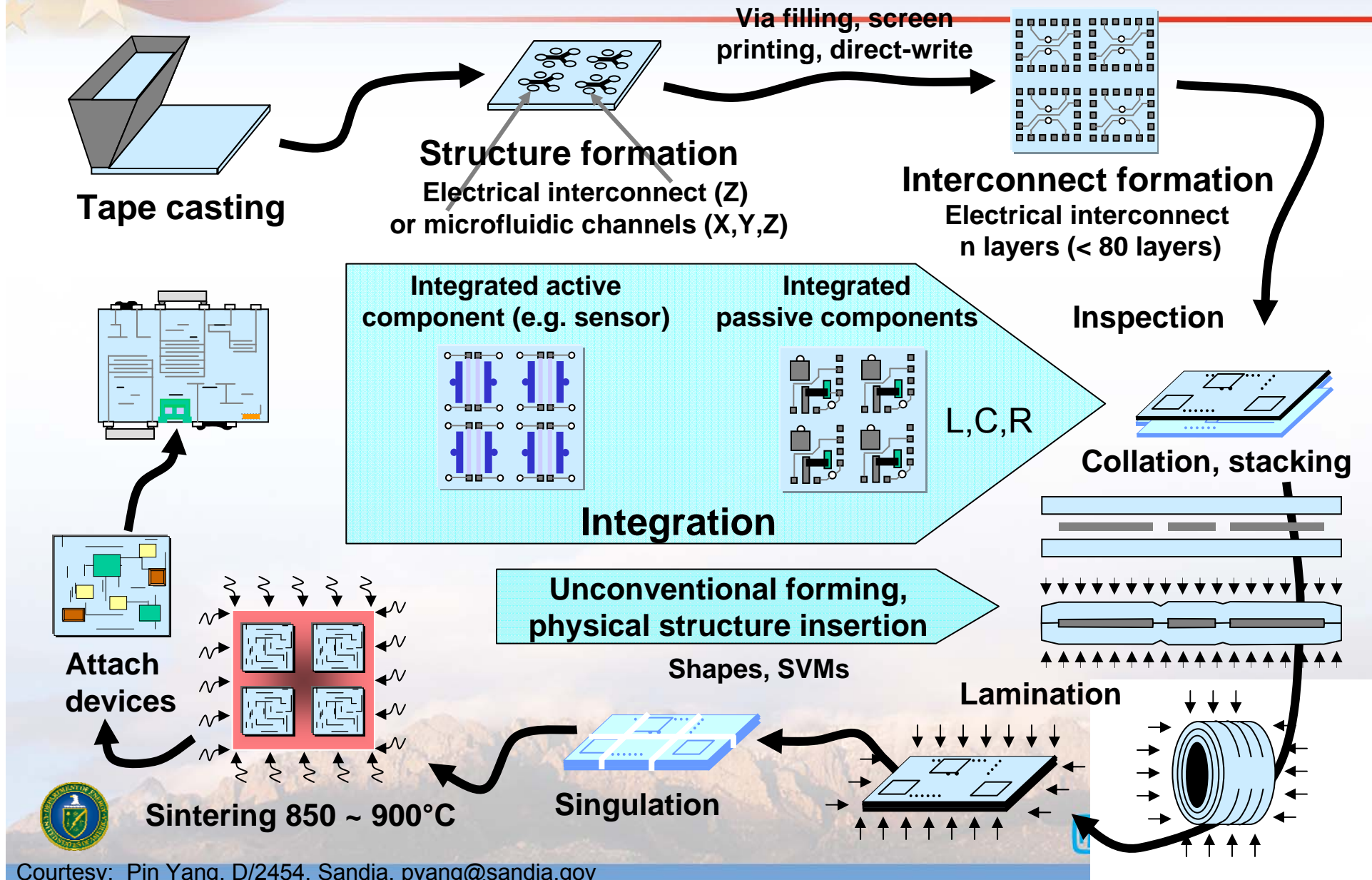


Technologies for National Security

- We develop technologies to:
 - Sustain, modernize and protect our nuclear arsenal
 - Prevent the spread of weapons of mass destruction
 - Provide new capabilities to our armed forces
 - Protect our national infrastructures
 - Ensure the stability of our nation's energy and water supplies.
 - Defend our nation against terrorist threats

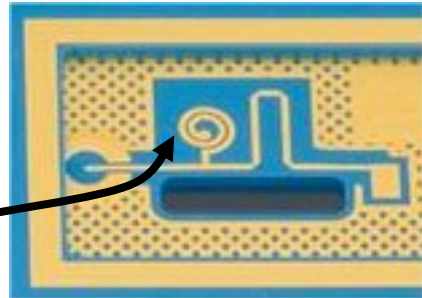


LTCC Processing

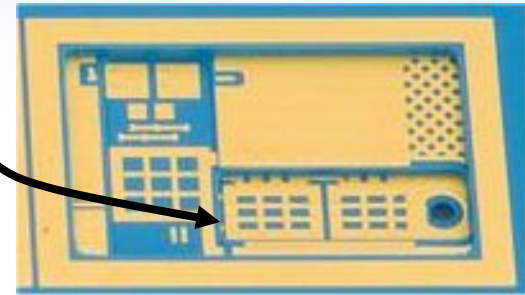


Planar MCM Features

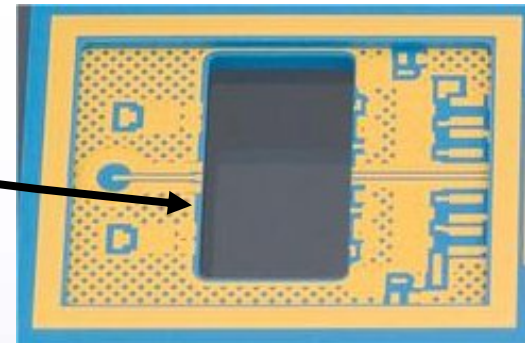
Integral
limiter



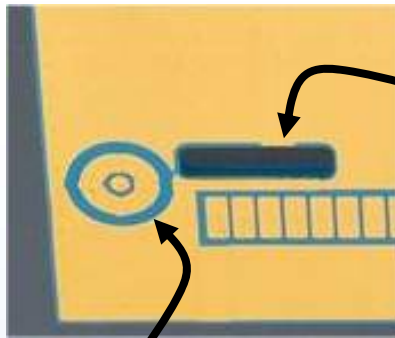
Multiple
cavity
levels



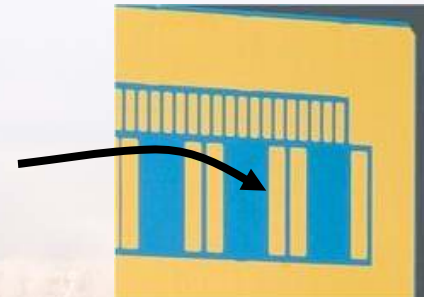
Cutouts for
high-power
devices



Connectors



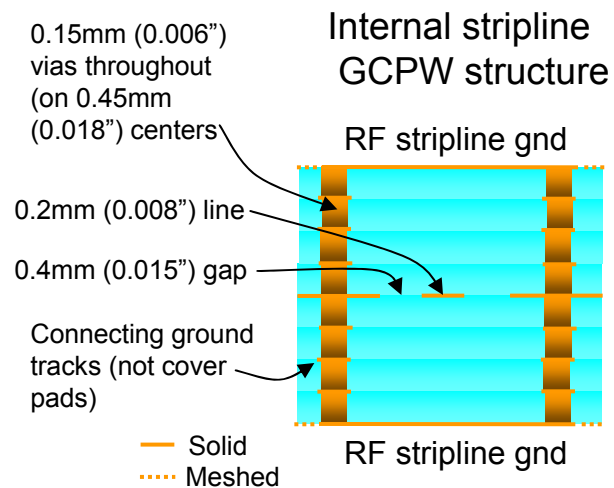
Discrete
component
pads



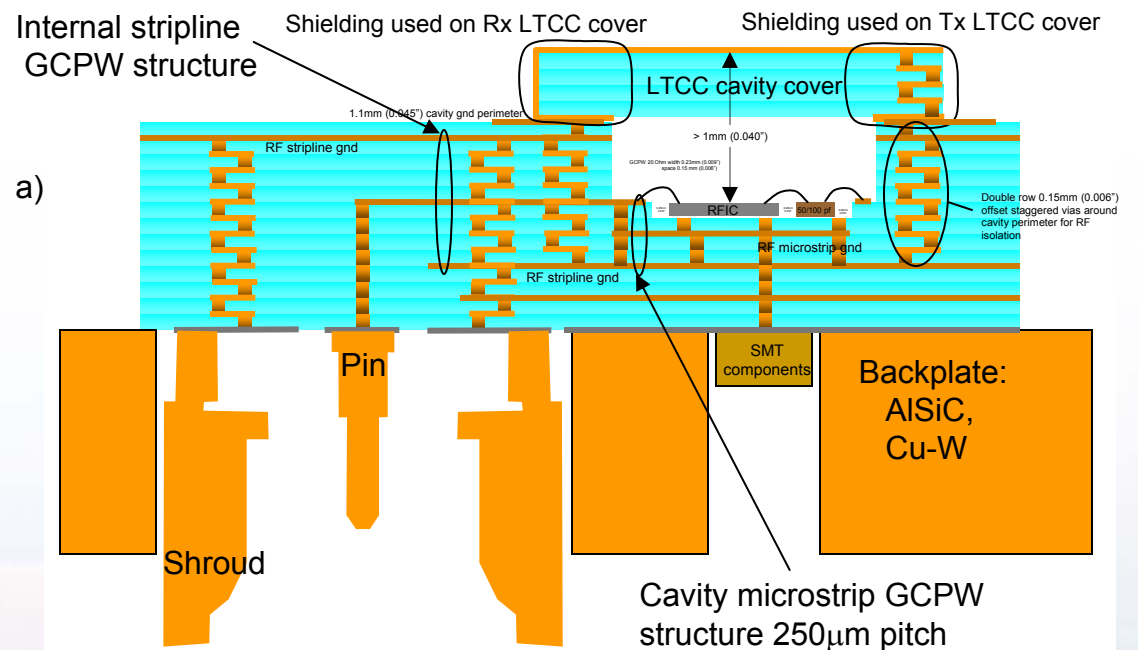
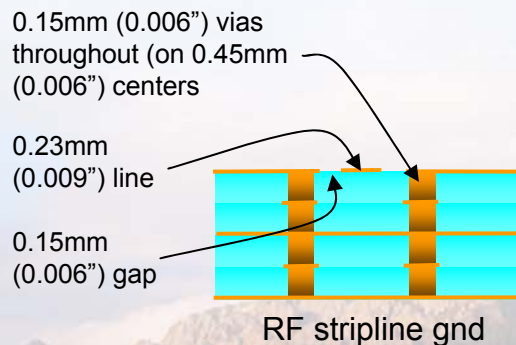
1 cm



MCM: Sectional View



Cavity microstrip GCPW
structure 250μm pitch



Well-suited to RF features; stripline, microstrip.



FTTF Background

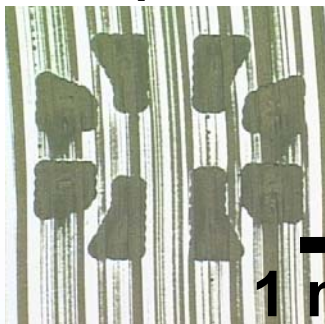
- Via-fill technology
- Commercial materials
 - LTCC tapes (DuPont 951)
 - Thick film pastes (DuPont 5738, 6141)
- Many standard practices
 - Tape punching
 - Screen printing
 - Stencil via-fill
 - Lamination (20.7 MPa (3000 psi), 70°C)
 - Cofiring cycle (450°C dwell, 850°C peak)



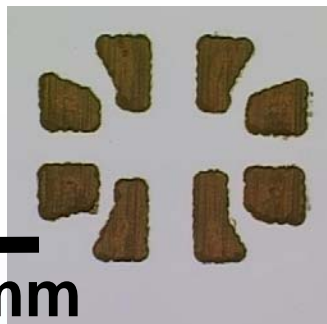


Paste Screeding

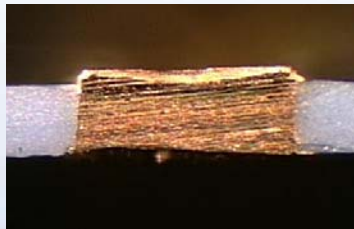
Backing
in-place



Backing
removed



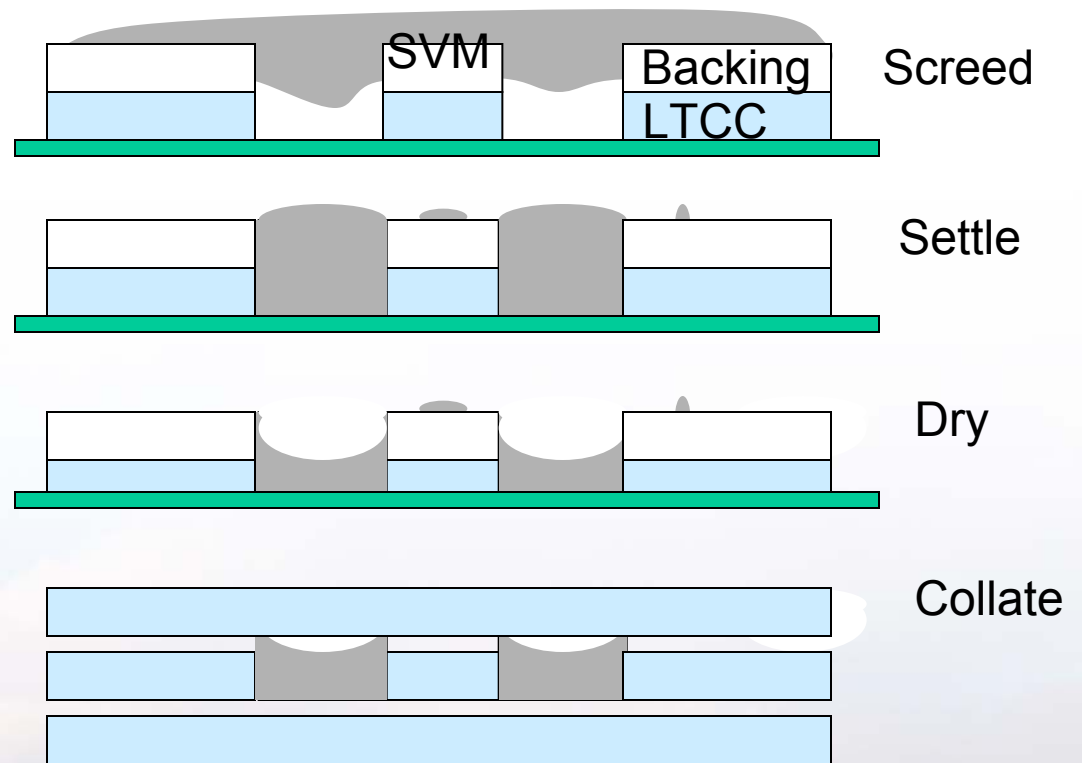
Screeded conductors



1 mm



1 mm



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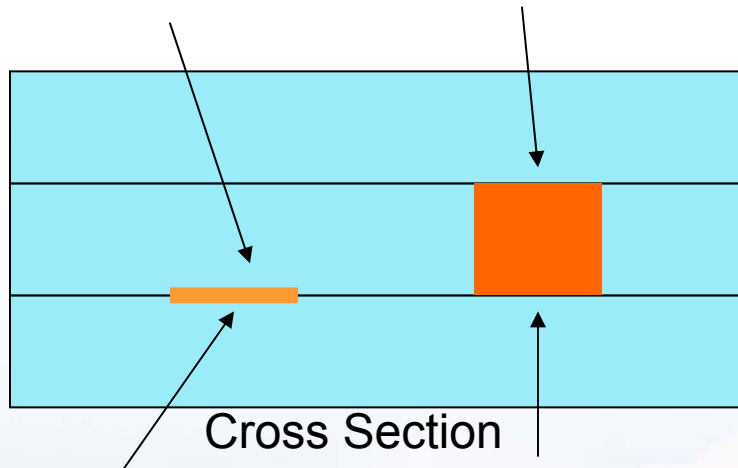
Screeding without artwork or stencils saves time, \$.

FTTF Reduces Resistance

Trace material vs. via fill material

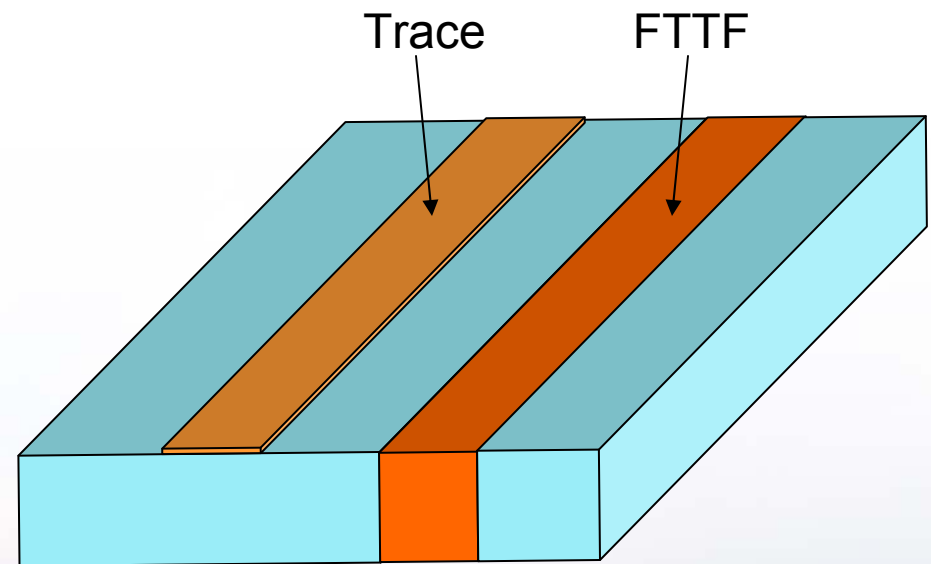
5 m Ω /sq. at
9 μ m thickness

5 m Ω /sq. at
25 μ m thickness



5 m Ω /sq. for
thick film line at
9 μ m thickness

0.6 m Ω /sq. for
FTTF at 216 μ m
thickness



Total sheet resistance

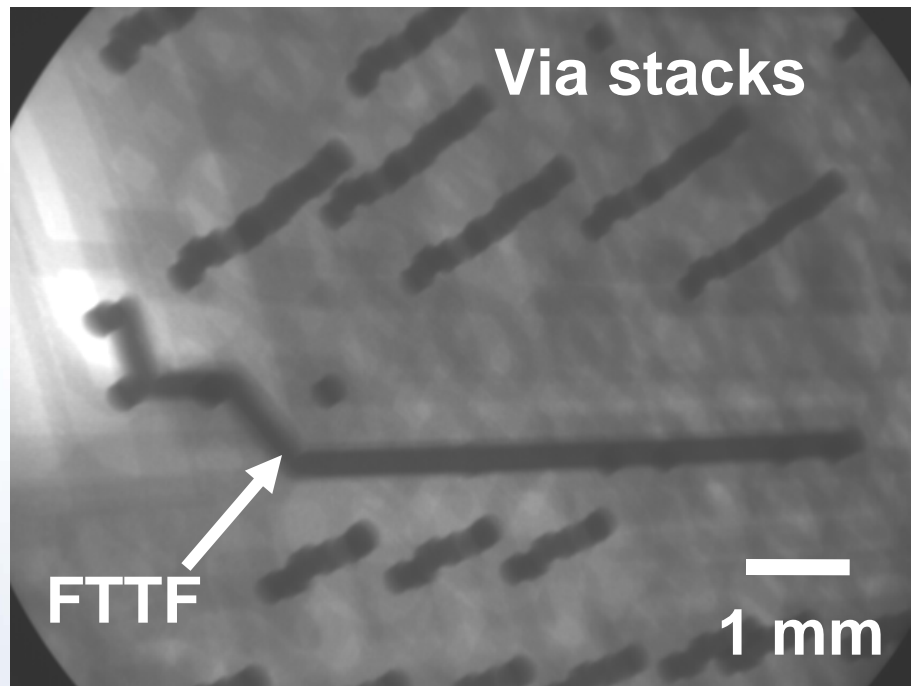


A 'via' shaped like a slot.

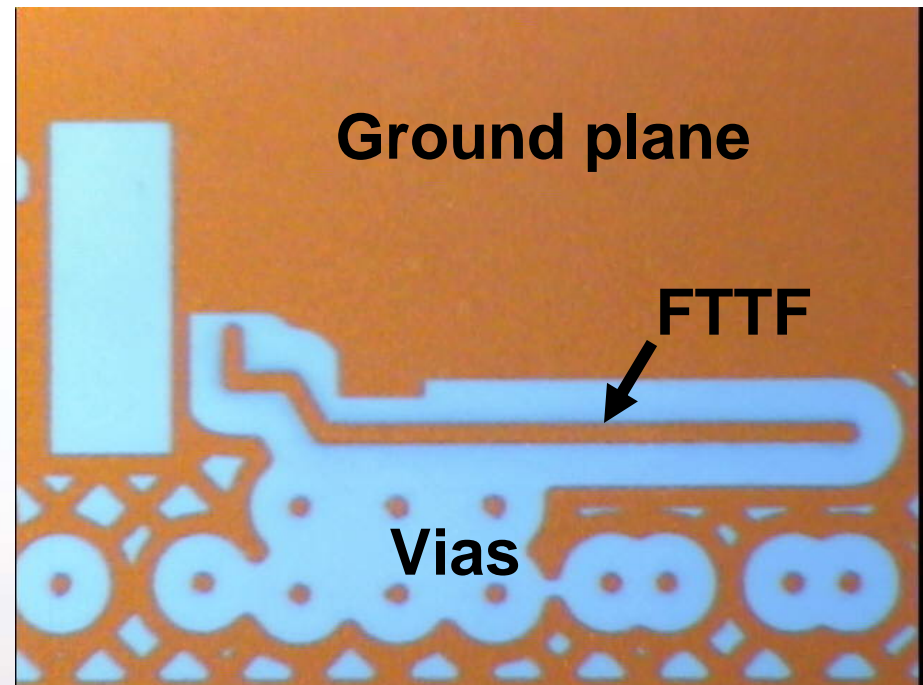


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FTTF Conductor Trace



X-ray: fired board



Optical Image: Unfired layer

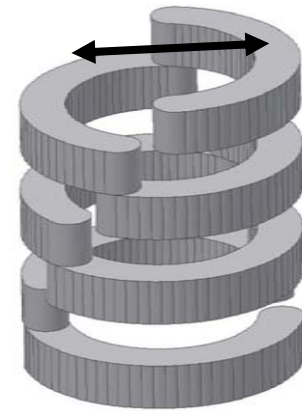
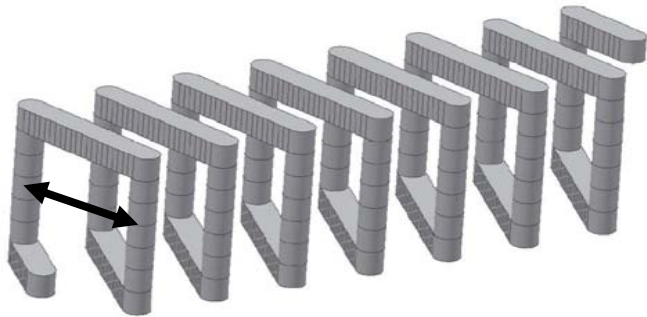
Feeds DC bias to 4W high efficiency PA
Maximize drain voltage to FET



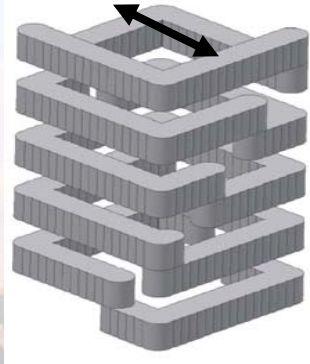
Full Tape Thickness Features (FTTF)

$$Q = \frac{\omega L}{R}$$

Q Quality factor
 ω Frequency
L Inductance
R Resistance



Diameters: 1mm and 2mm



10 Layers

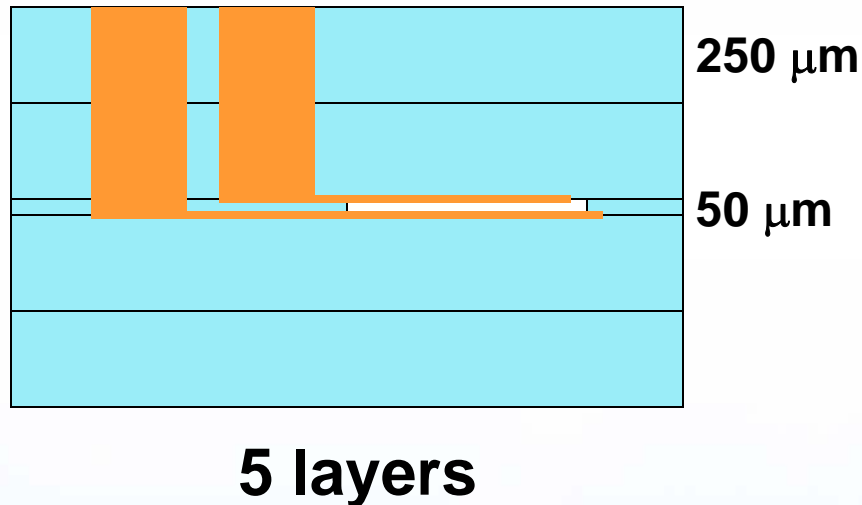


High-Q inductors result from lower resistance.

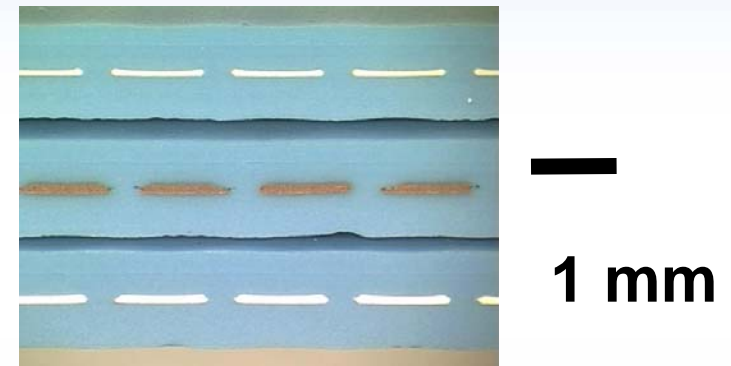


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FTTF Capacitors



Replace 2-3 dielectric prints
Eliminate pinholes
Laminate, then screed technique
Electrodes on facing layers



Cross section



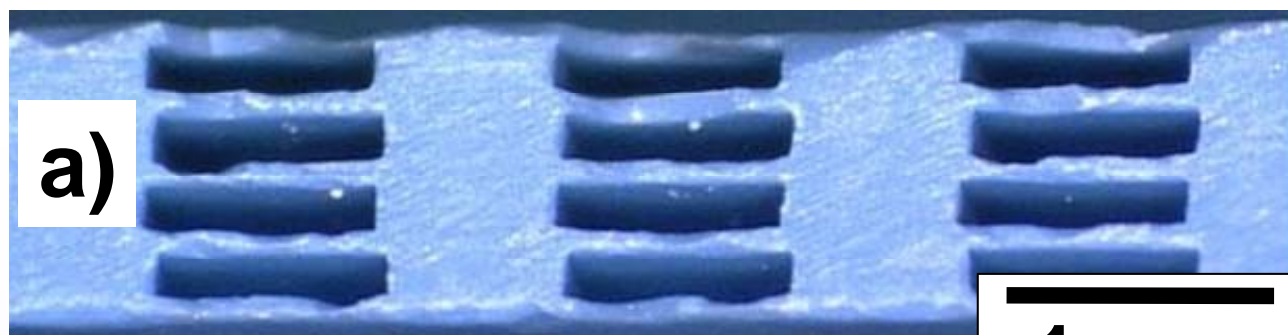
500 μm



Functional capacitors result.

FTTF Channels

Walls predefined



1 mm

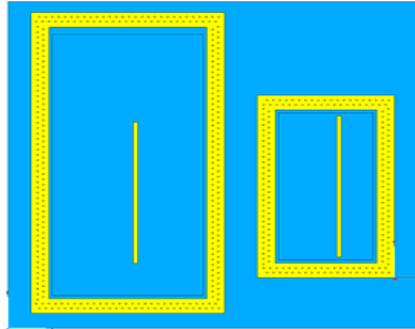
Walls defined
upon lamination



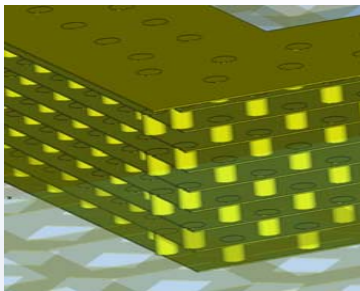
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Complex channels are compatible with LTCC.

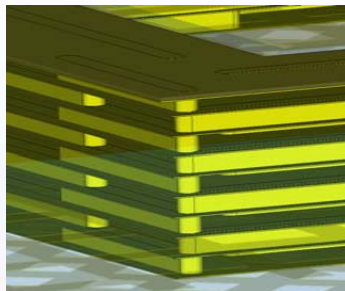
Dense E-M Shields with FTTF



3D-EM simulator antenna radiator & receiver

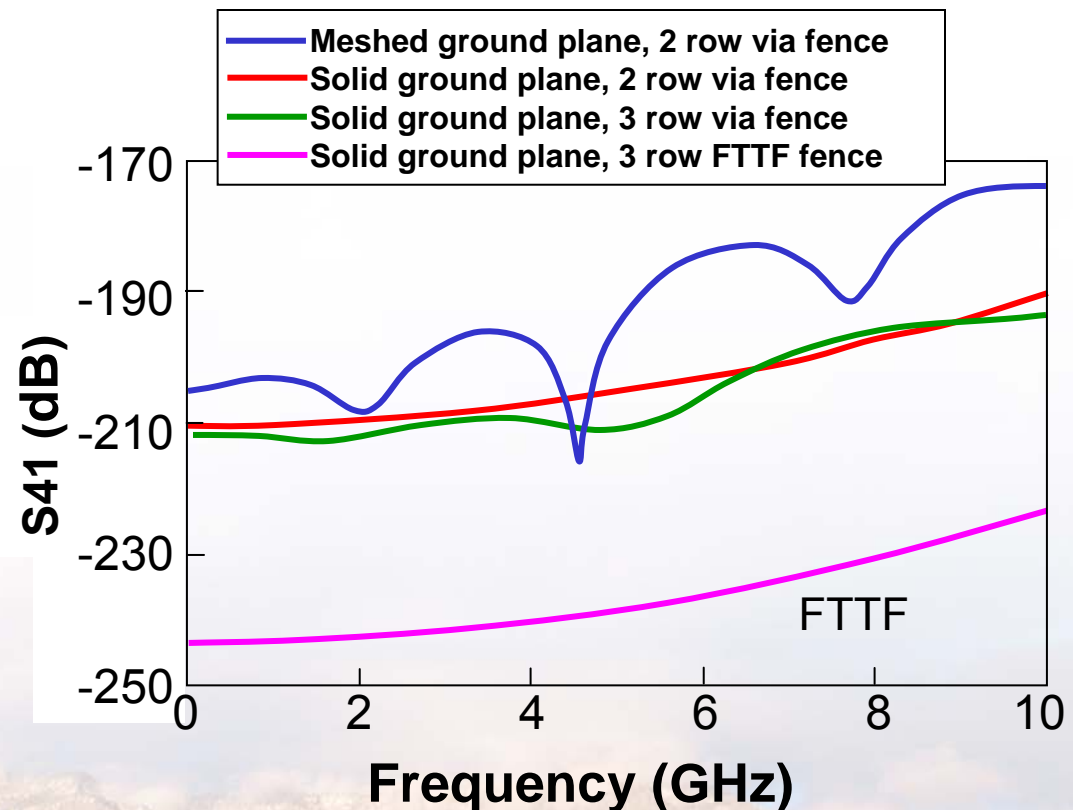


Conventional 2X staggered via fence



New 2 row FTTF segment fence isolation

Comparison of cavity isolation (model)

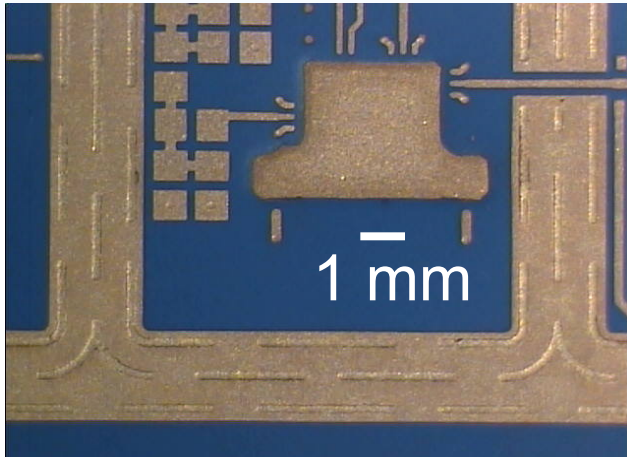


Superior isolation for the FTTF segment fence.

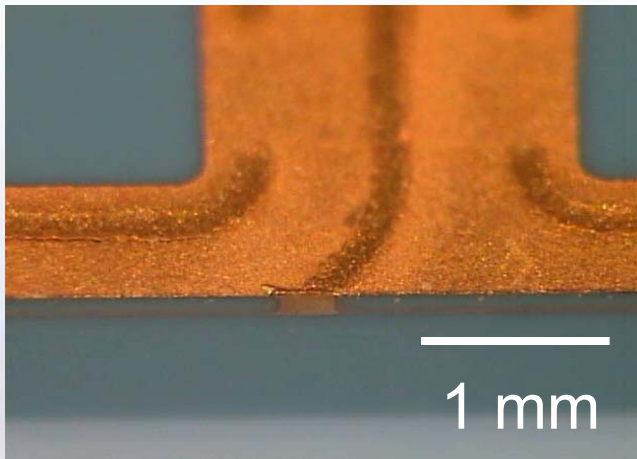


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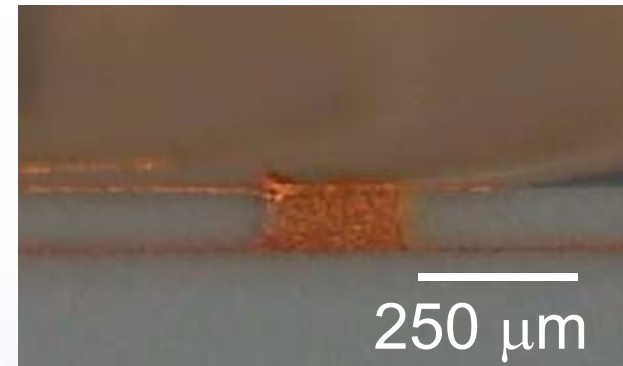
FTTF Segment Fence Isolation Structures



Structures beneath Seal Ring—3 Rows



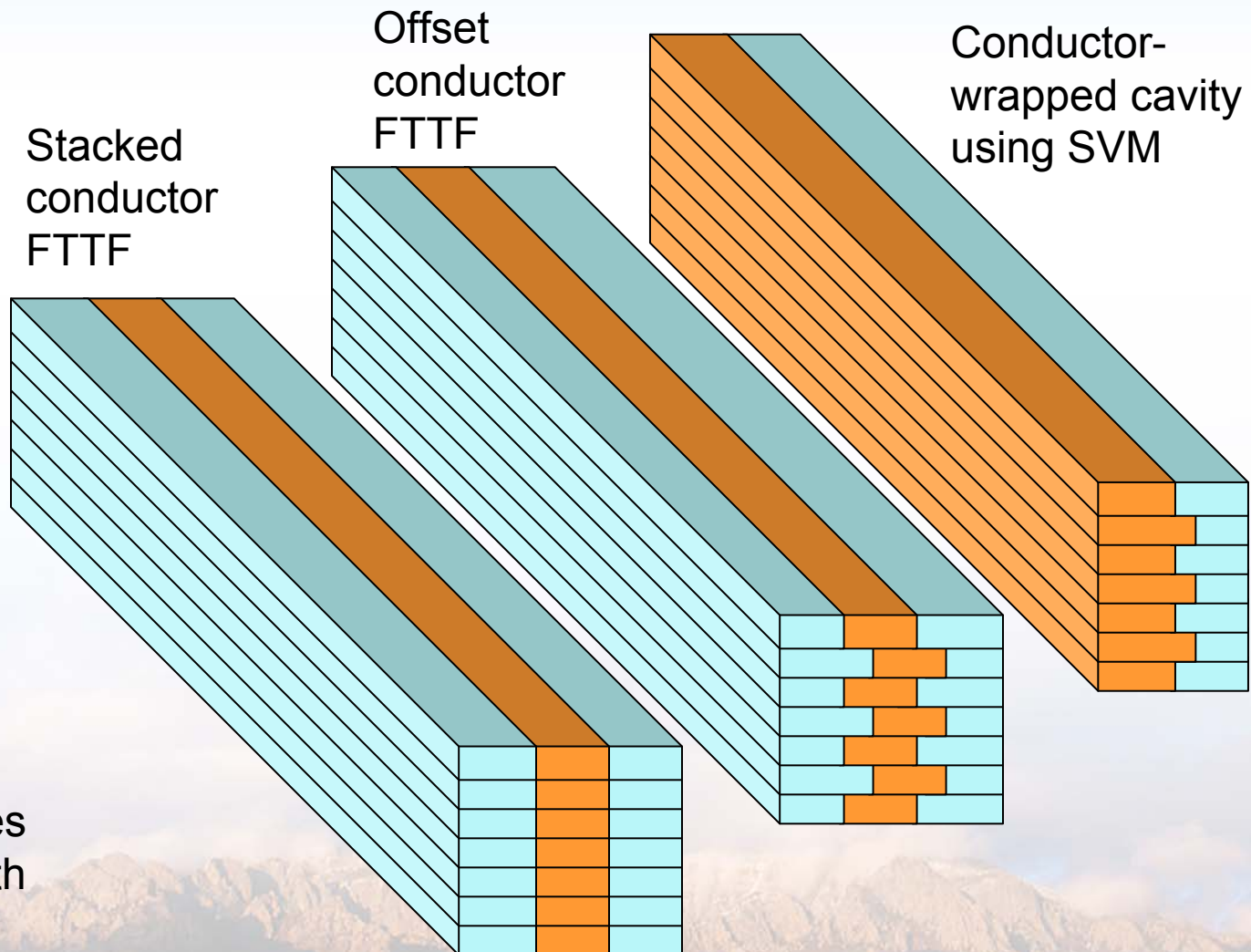
Cross Section



Magnified Cross Section



Solid Conductor Wall E-M Shield



- Provides complete shielding.
- Uses less material than slots.
- More compact than staggered vias or slots.
- Overlapping features for additional strength in handling.

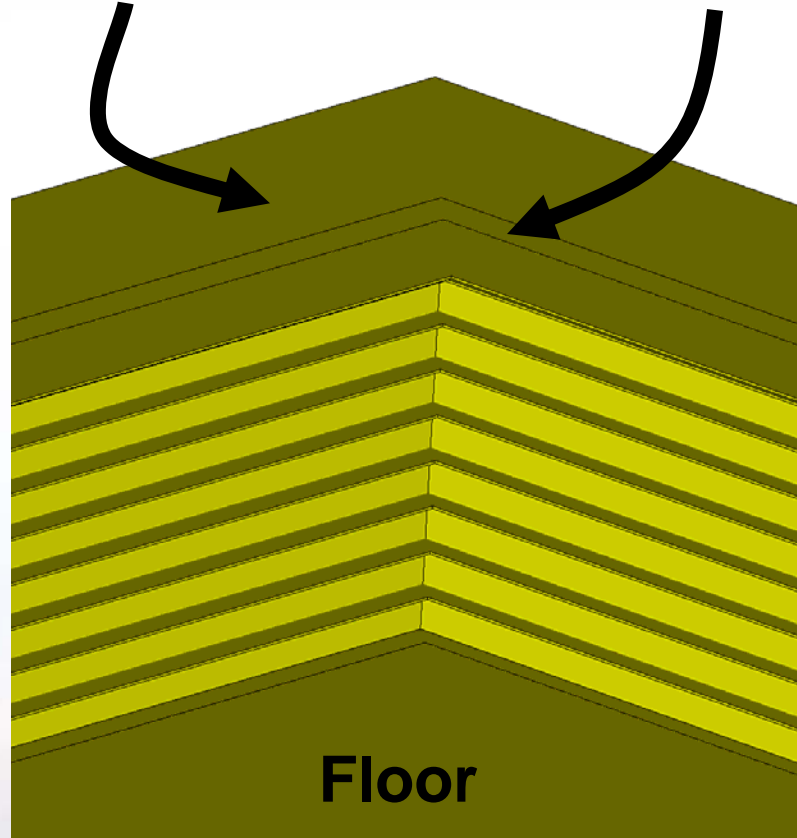


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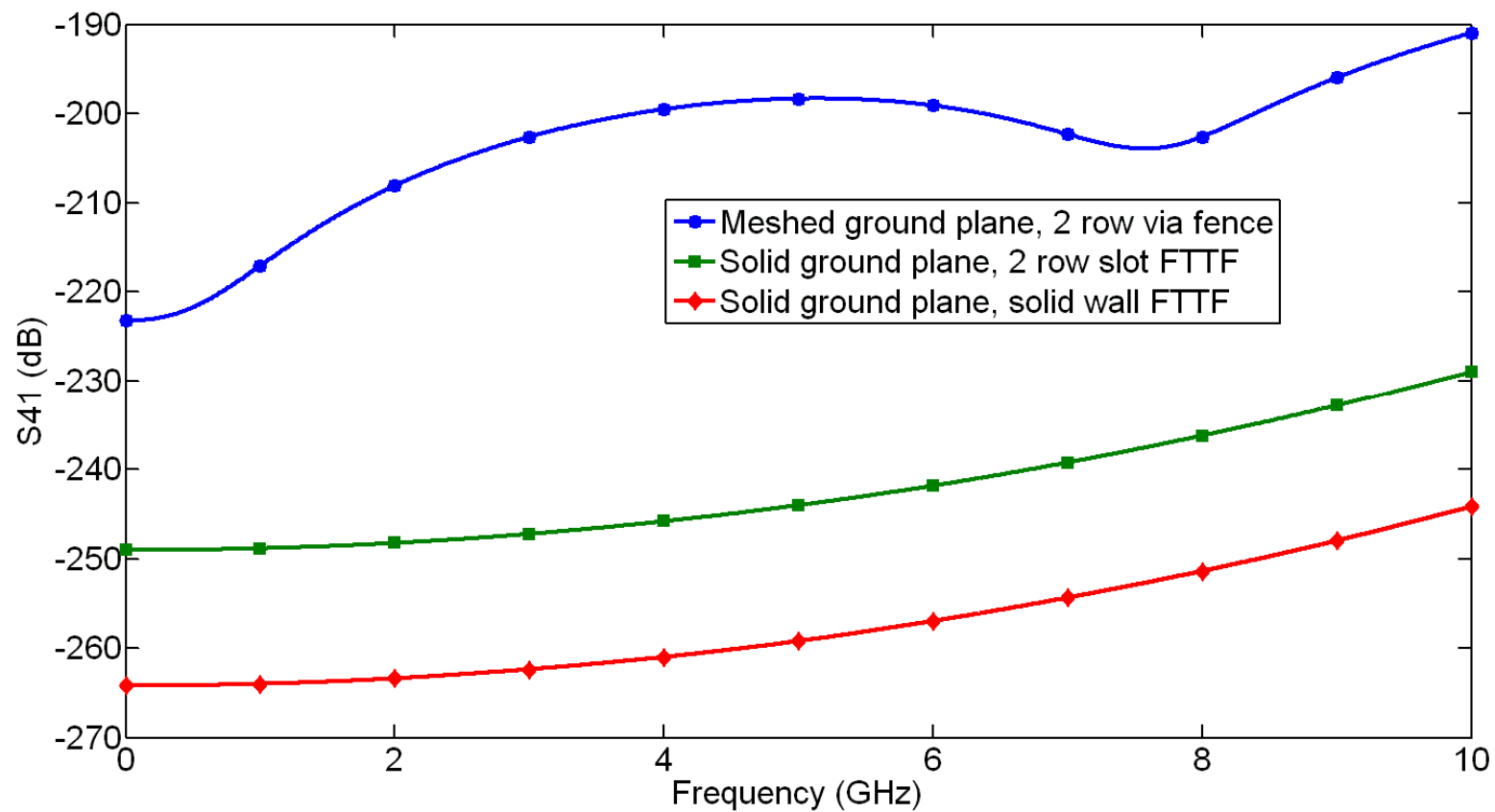
Solid wall E-M shield shows feasibility.

Seal ring:
top layer

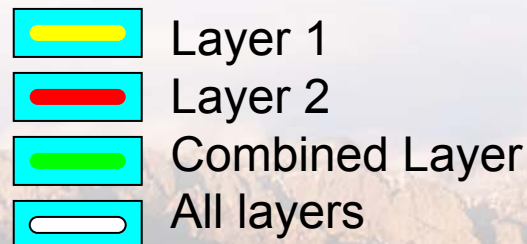
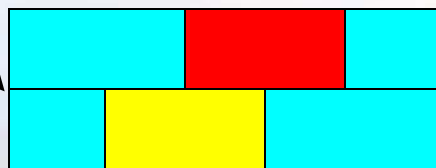
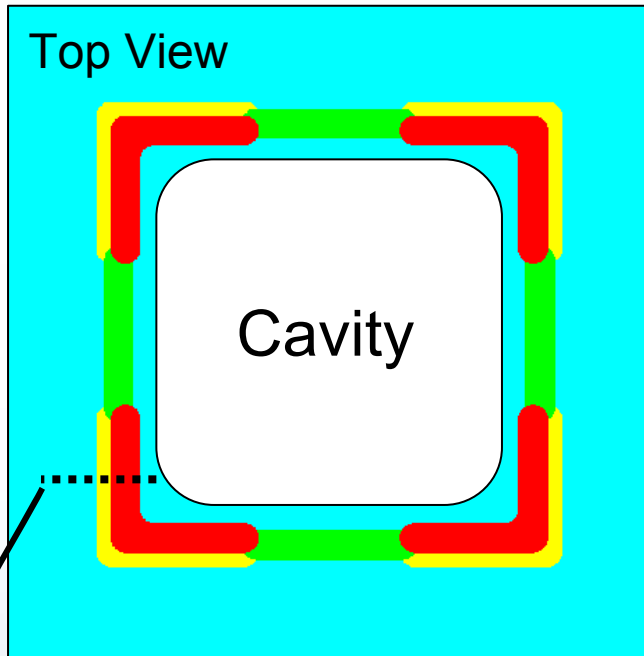
Image of wall
at top surface



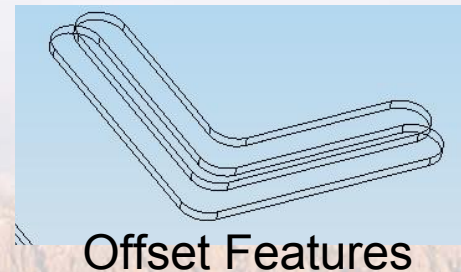
Simulation of Solid Wall Performance



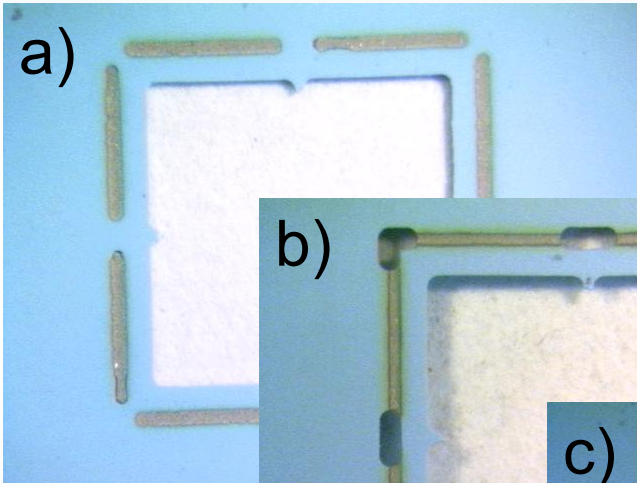
Process Sequence



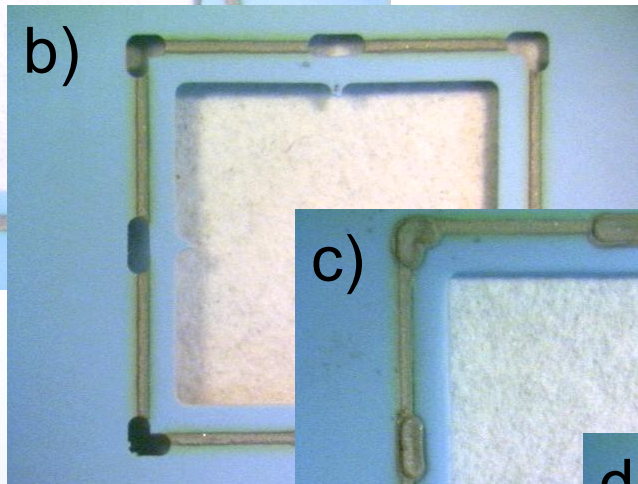
- 1) Punch and fill layer 1 (yellow)
- 2) Punch and fill layer 2 (red)
- 3) Laminate 1 to 2 (lamination and offset are optional)
- 4) Punch and fill layers 1+2 (green)
- 5) Note: inner track of tape completely supported by dried thick film.
- 6) Repeat for other layers
- 7) Collate and laminate all layers



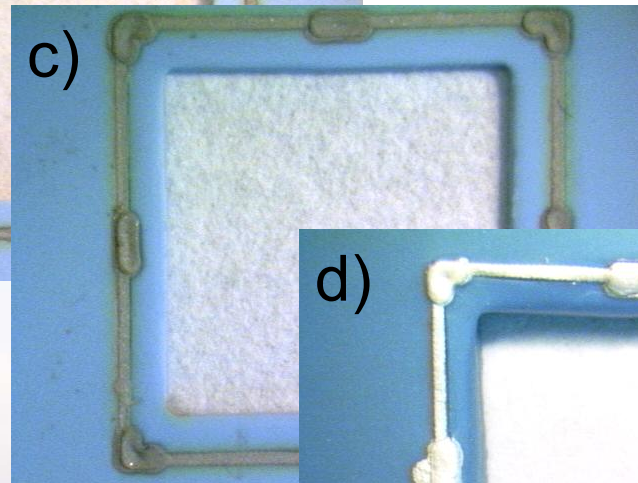
Cavity Isolation Construction Sequence



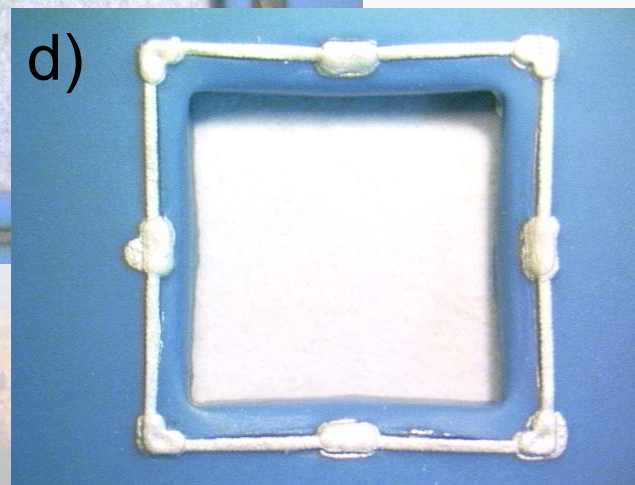
a) 254 μm (0.010") track punched and screeded in 254 μm (0.010") tape



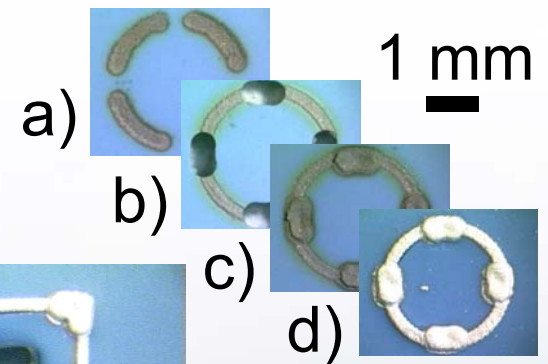
b) 2 ea laminated, 508 μm (0.020") dia. tethers punched



c) Tether region screeded and dried



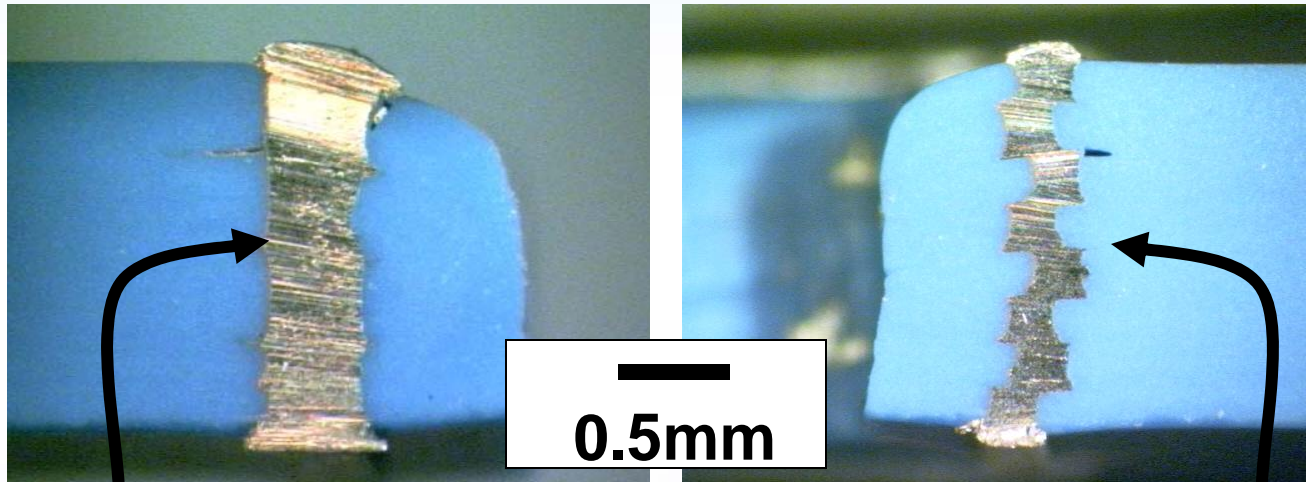
d) 8 layer tall solid wall surrounding cavity as-fired



Connector

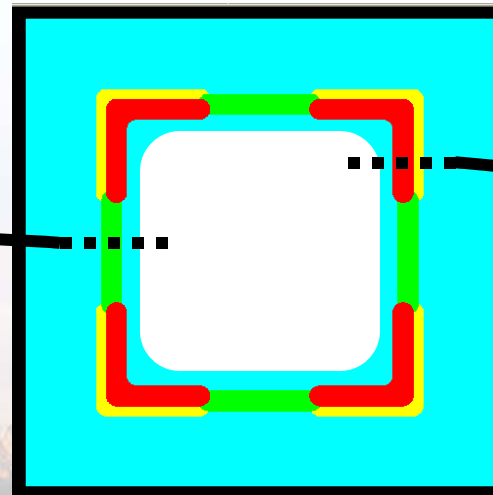


Fired Cross Section (Sawed)



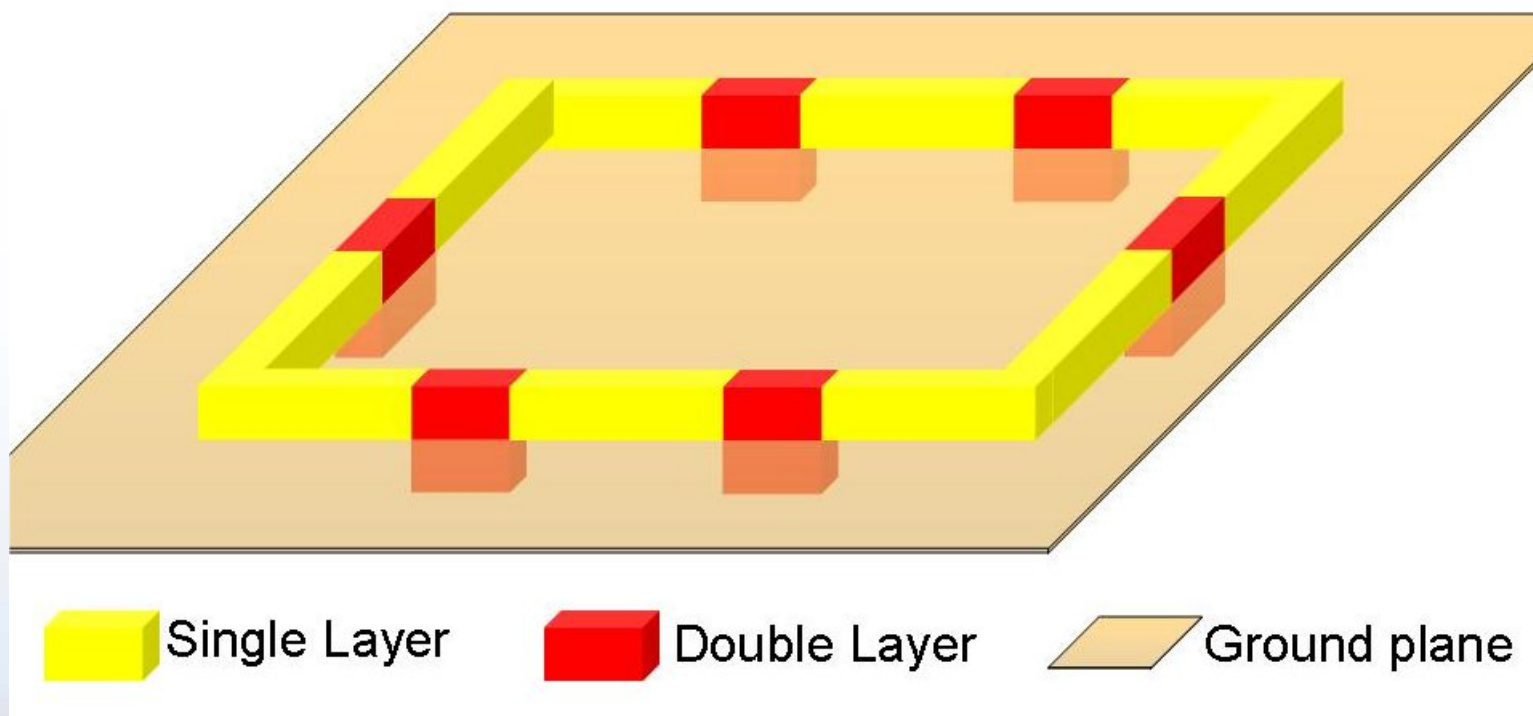
Stacked section,
0.020" wide

Staggered section,
0.010" wide



 Solid wall E-M shield shows feasibility.

Solid Wall Sequence



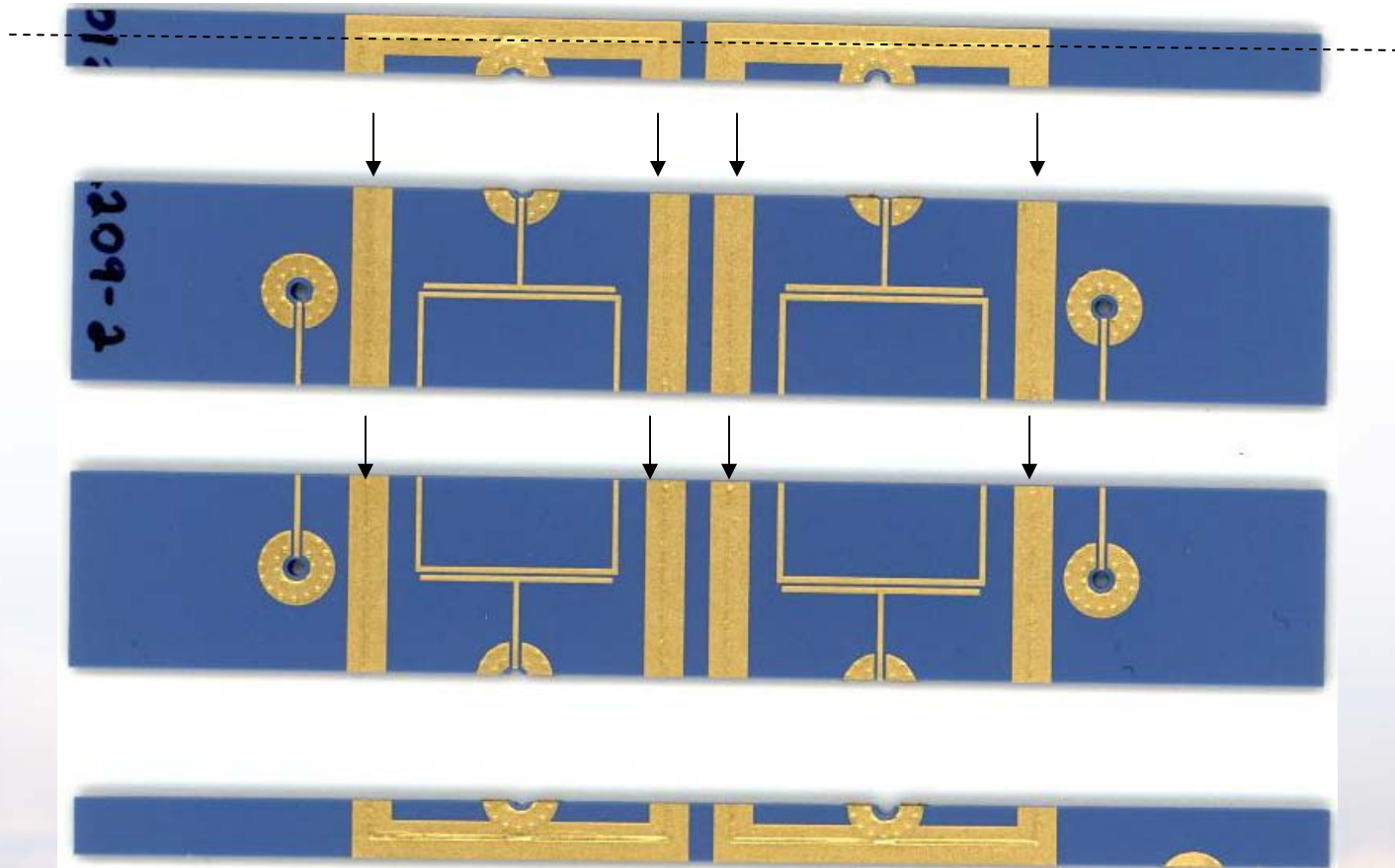
Single Layer Solid Wall Isolation



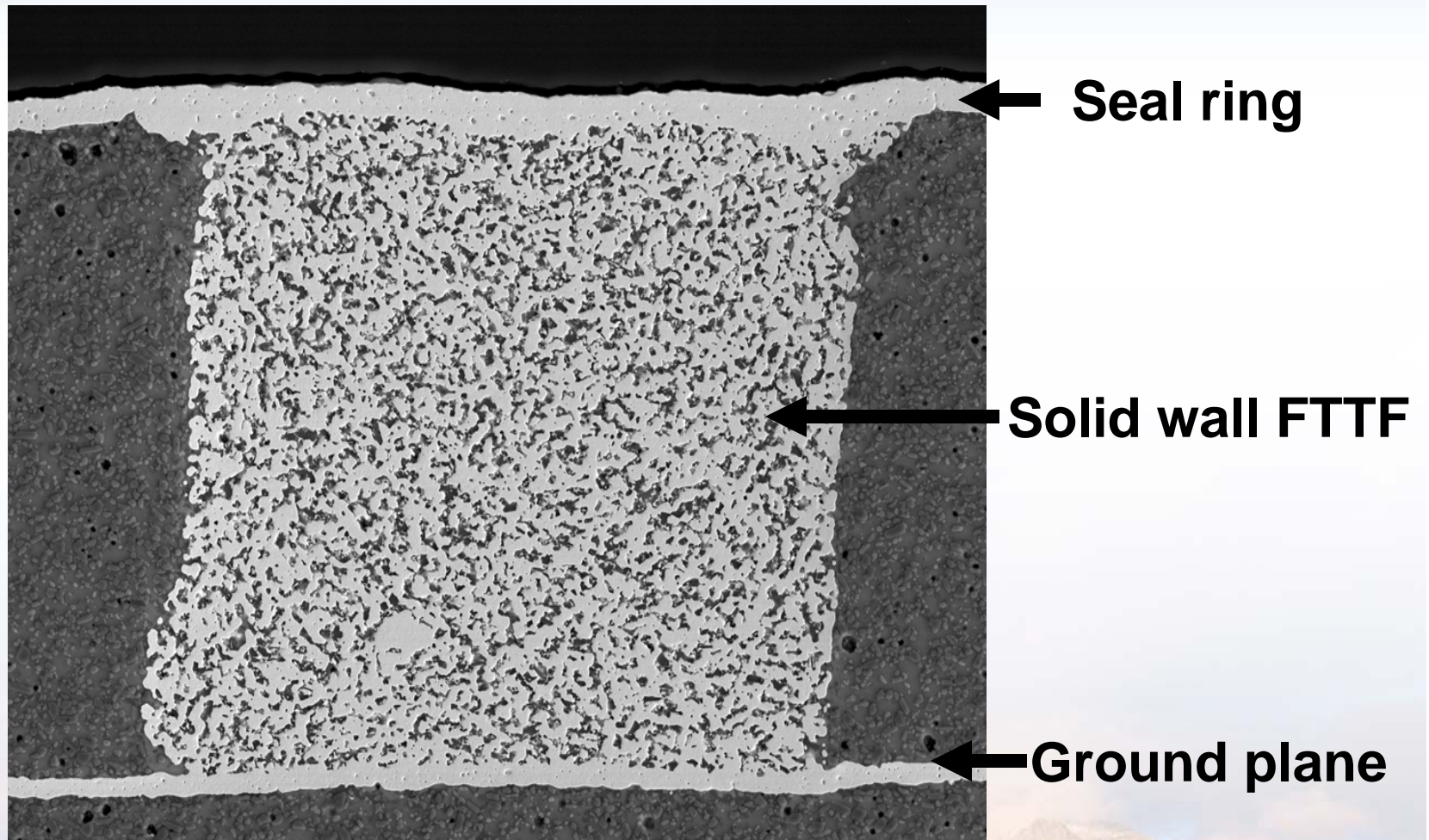
4 'room' design
Punched in 0.010" tape
Punched in laminated tape



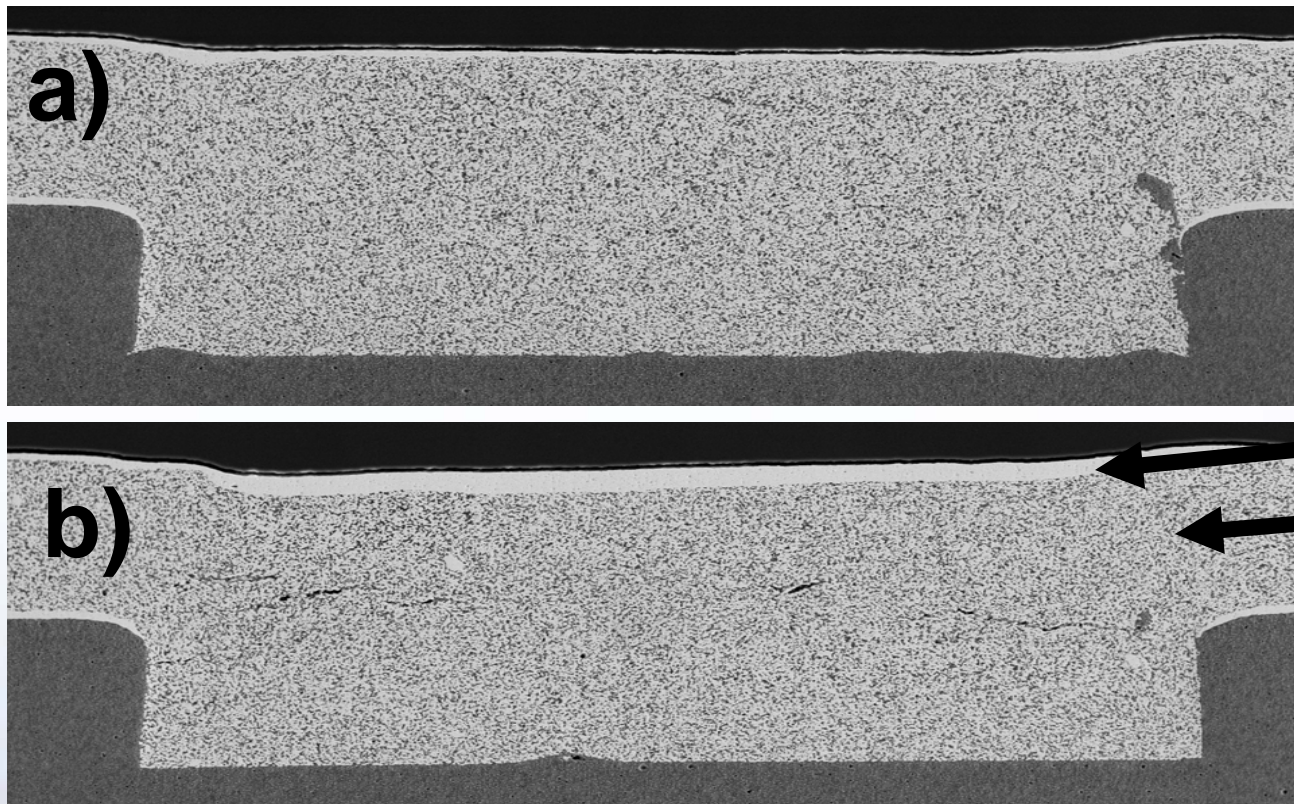
Single Layer Solid Wall Isolation



Single Layer FTTF Cross-Section



Cross-Section Along Length



Seal ring

Solid wall FTTF

Ground plane

100 μm



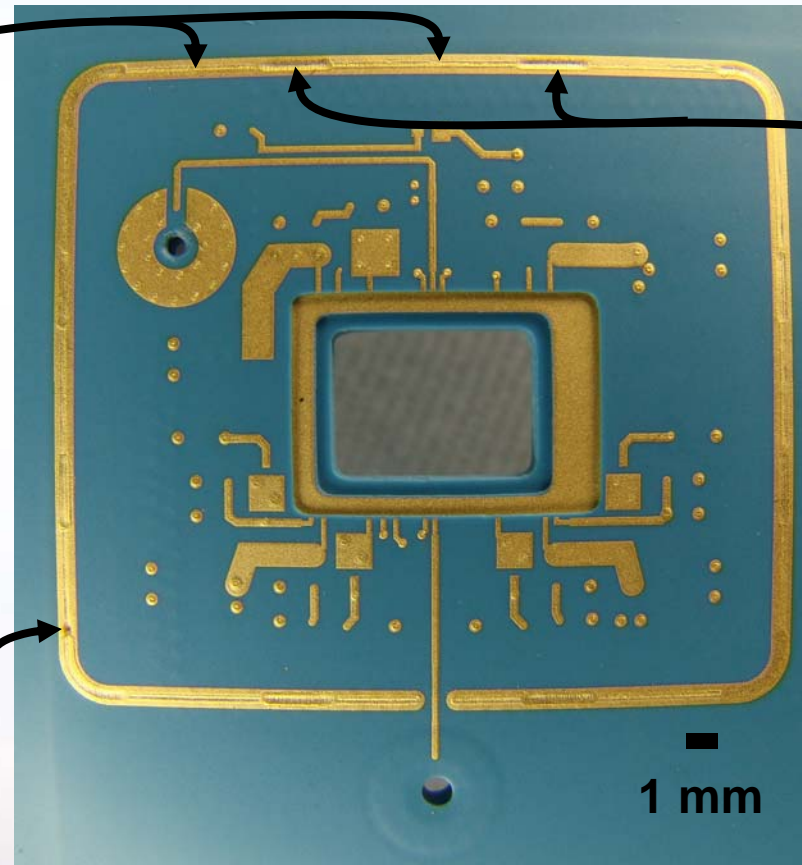
Fired Solid Wall

(eight layer test fixture)

Primary
punching of
top layer

Defect: missing
via-fill material

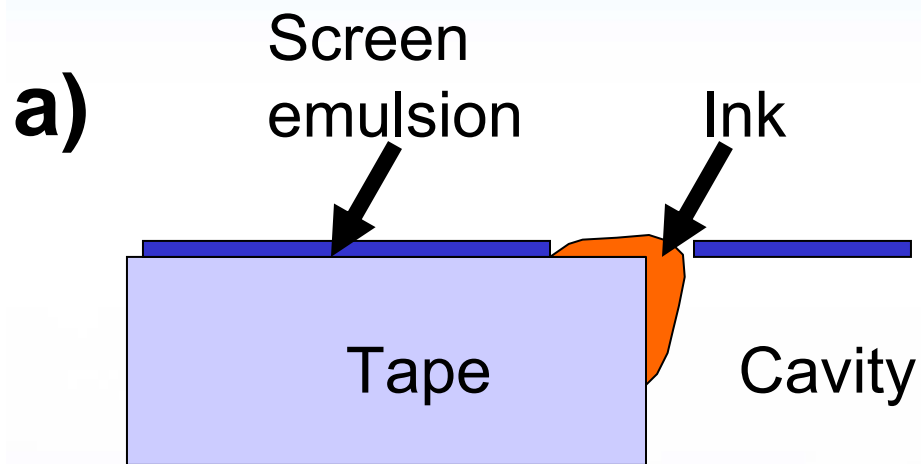
Secondary
punching of
top two layers



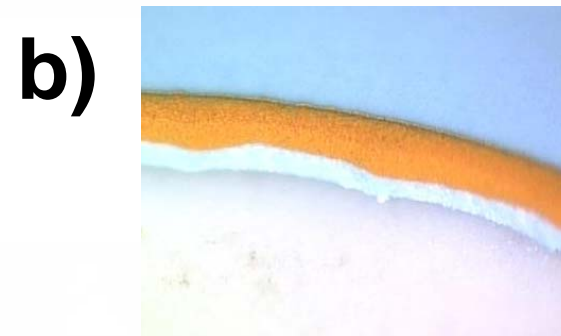
Solid wall covered by cofired barrier layer; No cracks.



Aside: Sidewall Metallization

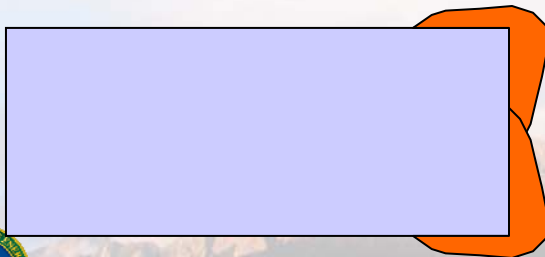


Single screen print

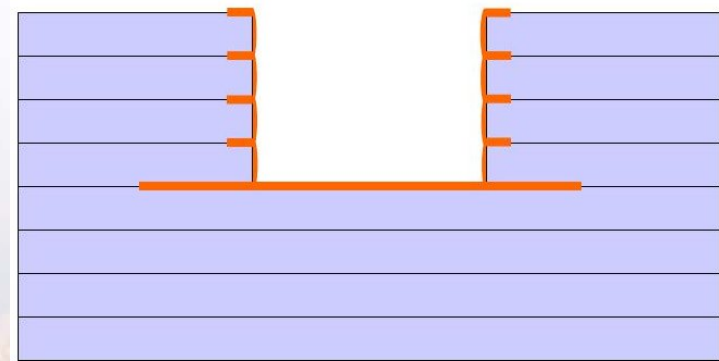


c)

Invert and print second side

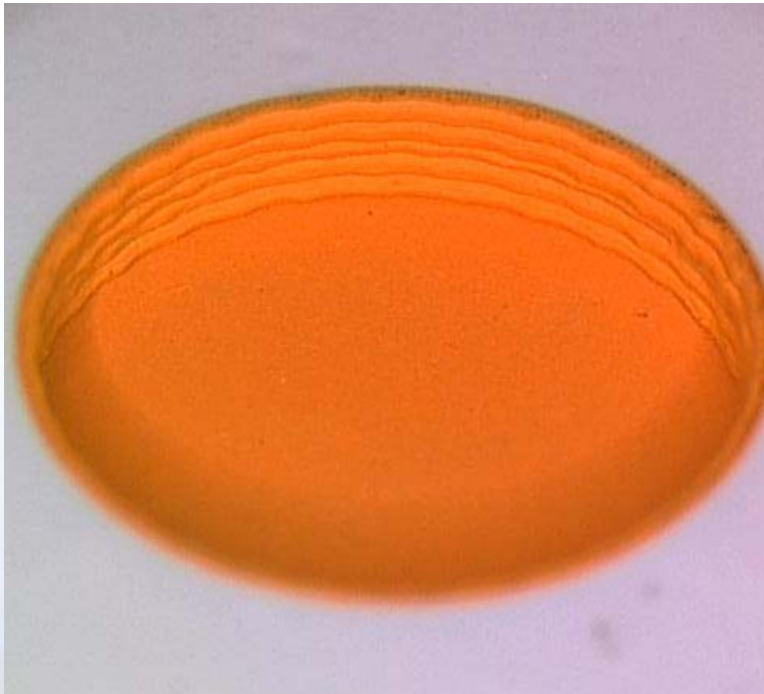


d) Stacked, laminated



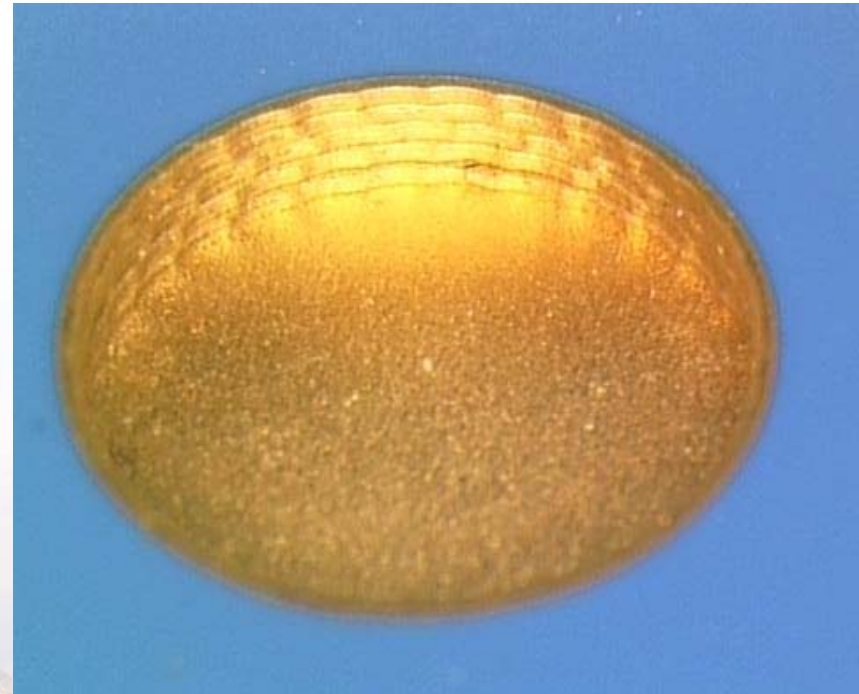
Metallized Cavity Sidewall

Unfired



1 mm

Cofired



1 mm





FTTF Summary

- Useful features
 - Critical lines
 - High Q inductors
 - Thermal spreaders
 - Capacitors
 - Channels
 - Interleaved E-M shielding—Superior to via fences
 - Solid E-M shielding—Superior to interleaved FTTF
- Future work
 - RF performance
 - Material compatibility





Acknowledgements

- Marcelino Armendariz, Damien Brandenburg, Kirk Buckholz, Adrian Casias, Rajen Chanchani, Dennis De Smet, Jeff Dimsdle, Brian Duverneay, John Dokos, Mike Girardi, Steve Goldammer, Randy Hamm, Brooke Hillis, Matt Johnson, Jesse Lai, Cristie Lopez, Ken Reaves, David Saiz, Tom Swiler, Tim Turner, Paul Vianco, Ambrose Wolf, Roger Woodrum, Pin Yang, and Gary Zender for technical contributions that made this work possible.
- DuPont Microcircuit & Component Materials
- Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.
- The Kansas City Plant is operated and managed by Honeywell Federal Manufacturing and Technologies for the United States Department of Energy under contract No. DE-AC04-01AL66850.

