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SOI-Enabled MEMS Processes Lead to Novel Mechanical, Optical, and Atomic Physics Devices

G. V. Herrera, Todd Bauer, M. G. Blain, P. E. Dodd, R. Dondero, E. J. Garcia, P. C. Galambos, D. L. Hetherington, J. J. Hudgens, F. B. McCormick, David R. Myers, G. N. Nielson, C. D. Nordquist, M. Okandan, R. H. Olsson, K. Ortiz, M. R. Platzbecker, P.J. Resnick, R. J. Shul, M. J. Shaw, David J. Stein, C. T. Sullivan, M. R. Watts

Sandia National Laboratories,[1] Albuquerque NM

[1.] **Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.**

National Nuclear Security Administration

Sandia National Laboratories

Outline of Presentation

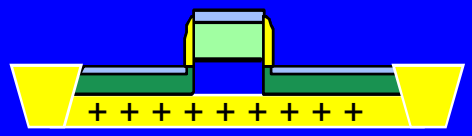
- Sandia's history with rad-hard SOI
- Extensions beyond CMOS SOI
  - Radio-Frequency Devices
  - High-Voltage Devices
  - Optical Devices
  - Atomic/Ion Trapping Quantum Devices
  - Lift-off Devices
- Conclusions

Sandia's CMOS Radiation Hardening

- Eliminating upset in >0.5μm bulk silicon CMOS introduced prohibitive performance delays for resistive feedback approaches.
- SOI wafers reduced collected charge by reducing collection volume.
- Switching to SOI required Sandia to develop:
  - qualification techniques for sufficient yield of high-density CMOS circuits (material science and process expertise)
  - alternative hardening approaches to meet total-dose radiation requirements (transistor and circuit design).

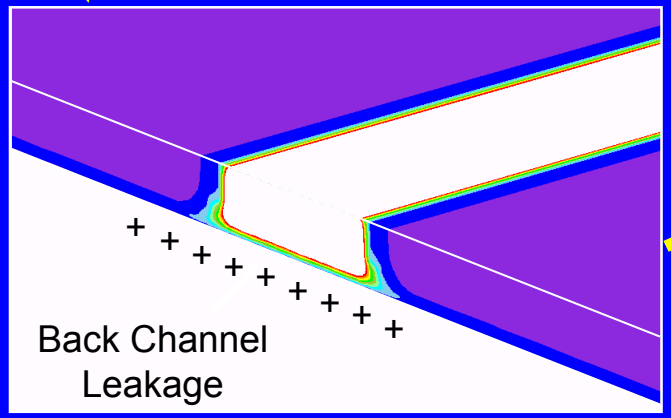
SOI excels at dose-rate and single-event immunity but can suffer from total-dose effects for larger (0.35μm) analog transistors.

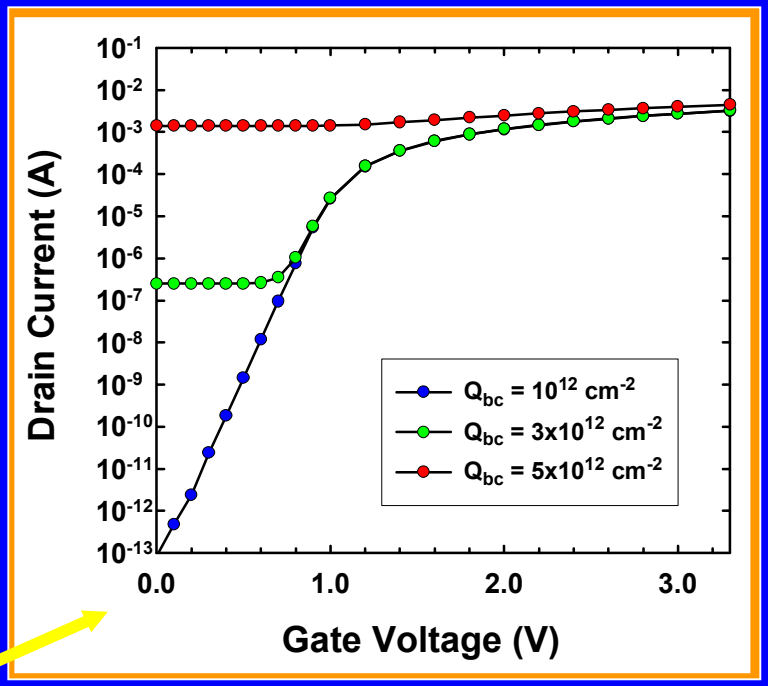
SOI Transistor



Charge trapped in the buried oxide leads to leakage currents

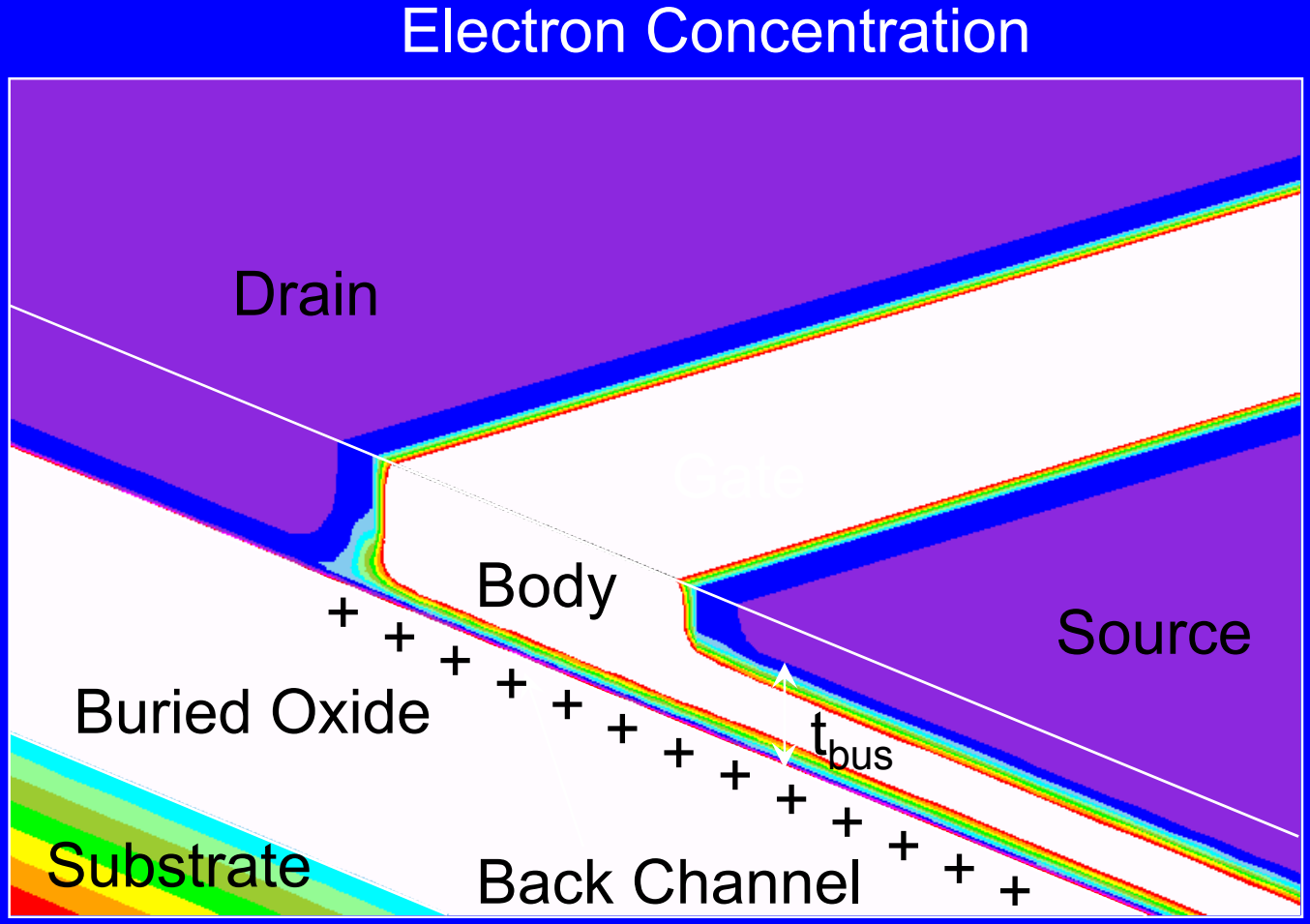
Electron Concentration





3D simulations predict leakage as a function of trapped radiation-induced charge at the transistors back-channel.

The BUSFET[1] eliminates rad-induced back channels for total-dose immunity.



1. n-channel Body-Under-Source FET:
0.35 x 10 μm
3.3 V
10^{18} cm^{-3} retrograde doping profile

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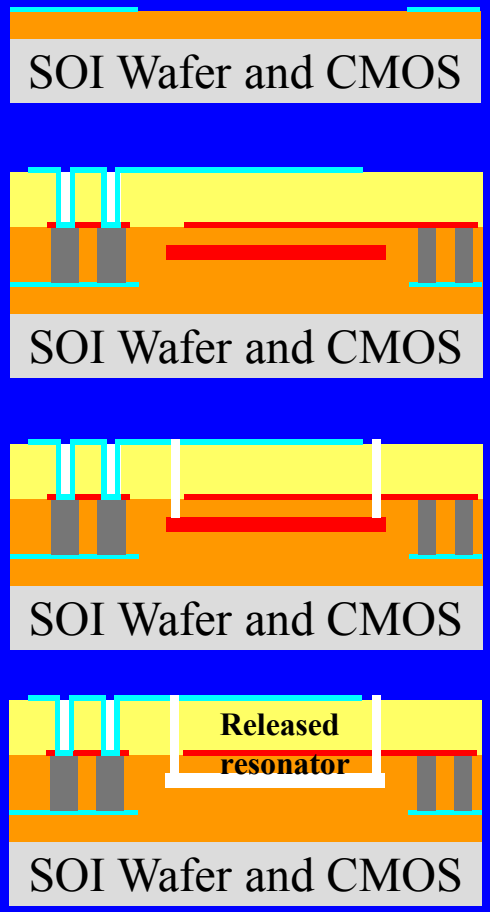
SOI Add-ons: Post-CMOS RF Filter and Oscillator Fabrication

- 6 mask levels
- AlN sputter deposited at 350°C (Post-CMOS compatible)
- All CMOS compatible metals/materials
- Highly c-axis oriented with a rocking curve full width half maximum = 1° (strong piezoelectric coupling)
- Dry Si release (no stiction issues, simple and cheap)
- Integration directly over SOI CMOS



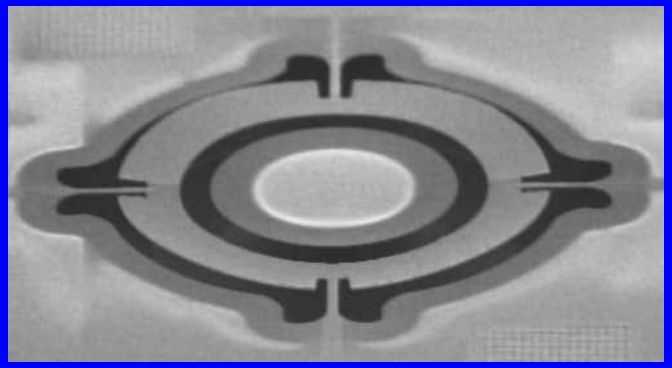
Post SOI CMOS Process Flow

Al
Si Release Layer
Ti/TiN/Al
Oxide
W
AlN

SOI CMOS Add-ons: Piezoelectric Post-CMOS MEMS

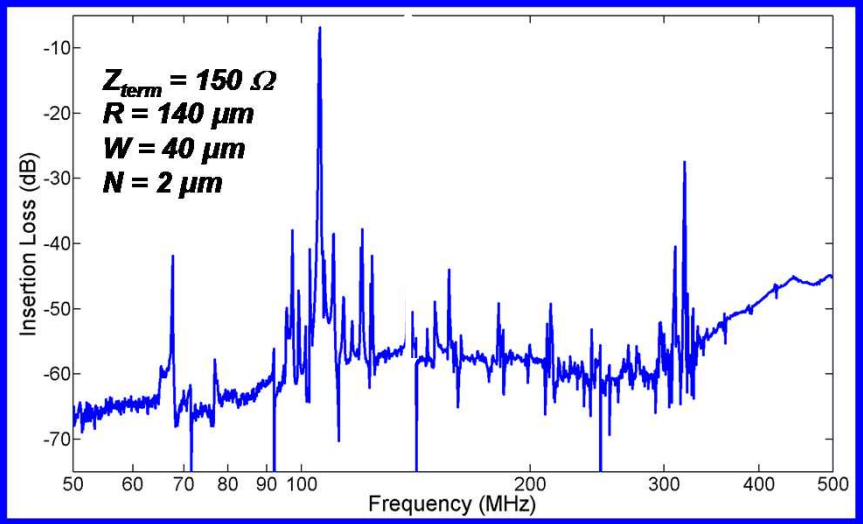
Properties

- Lithographically Defined Mechanical Resonance (Any Resonance Frequency Between 1 MHz – 10 GHz on the Same Wafer)
- Post-CMOS Compatible
- High Q, High Frequency, Low Impedance



Motivation

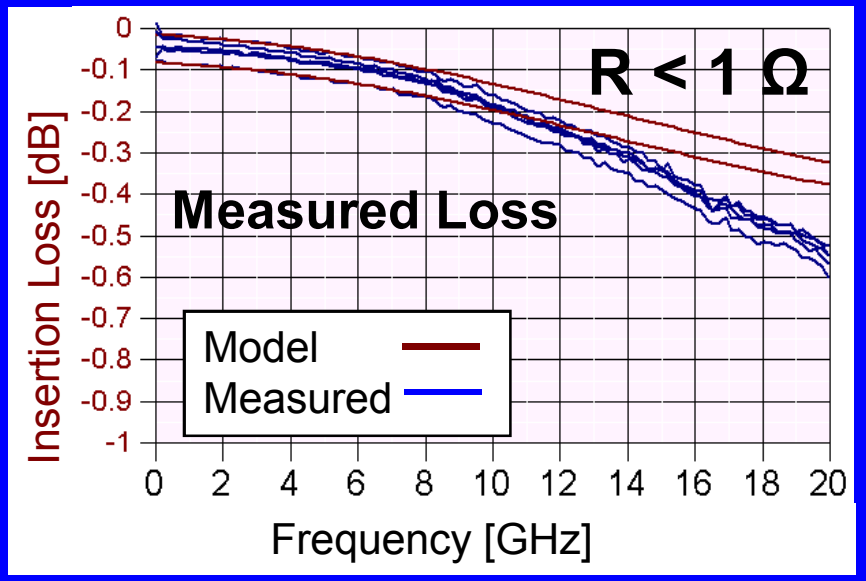
- Single-Chip Frequency References and Low-Phase-Noise Voltage-Controlled Oscillators
- Miniature High-Selectivity Filters and Filter Banks not otherwise available
  - RF Filters in Non-Commercial Bands
  - Miniature SAW IF Filter Replacement
  - Filter Banks for Spectrum Analysis and Advanced Radios
  - Super High Frequency Acoustic Filters with Previously Unachievable Selectivity

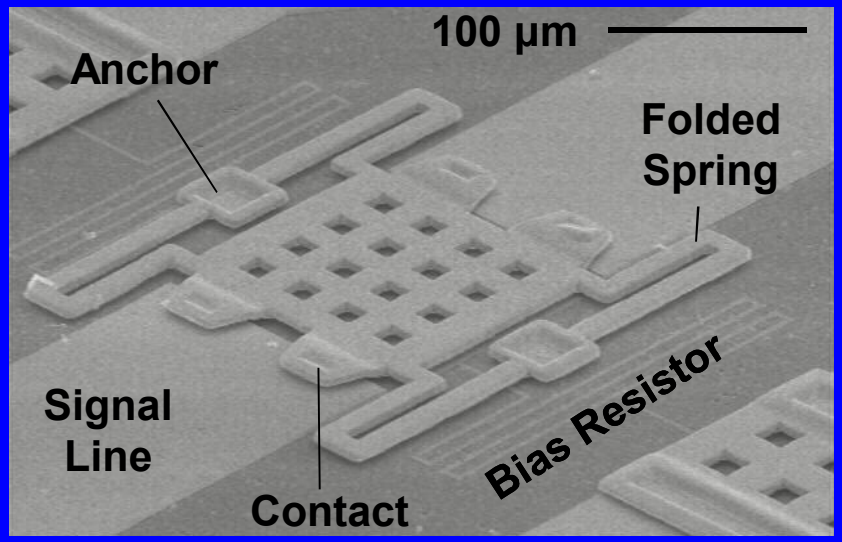


AlN Dual Mode Filter and Wideband Response

SOI CMOS Add-ons: RF MEMS switches

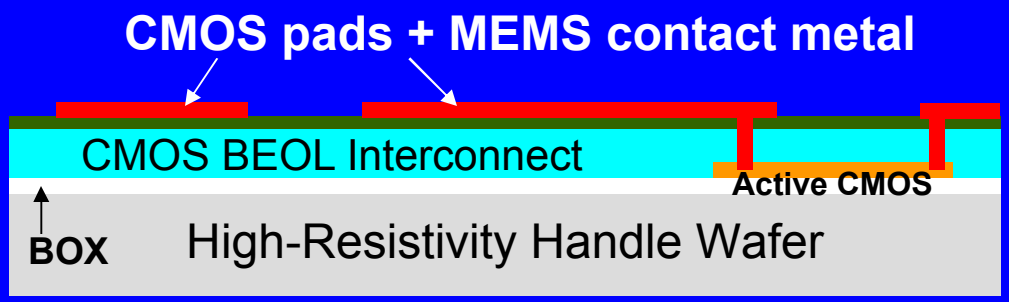
- Low-insertion-loss, high linearity technology complements CMOS
- Enables RF circuits integrated with control or active RF electronics
- CMOS compatible post-processing for integration on active circuits
- SOI allows high-resistivity handle substrates for low-loss transmission lines



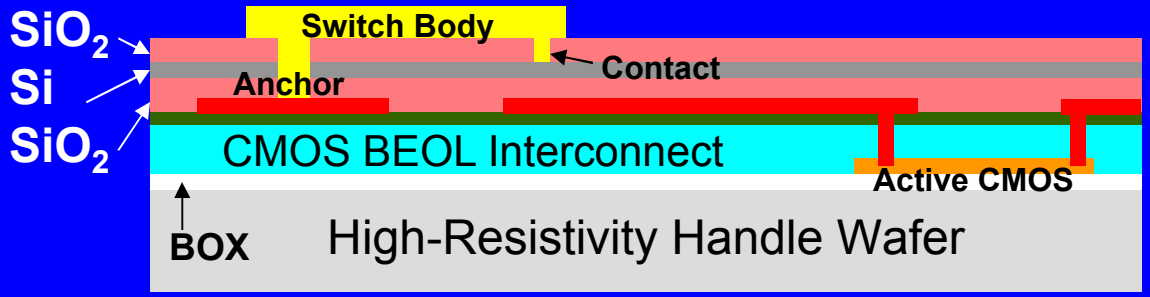


RF MEMS Switch Process

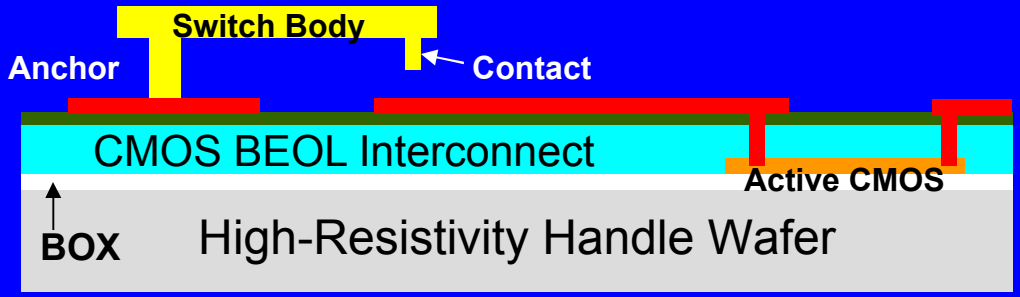
- Low-temperature process for post-processing on CMOS circuits
- Exploit SiO_2/Si selectivity for controlled contact depth
- Sandia MicroFab allows low-loss metals and contacts unavailable in high-volume CMOS facilities



Sacrificial Layer Deposition and Etch followed by Mechanical Layer Patterning and Deposition



MEMS Release



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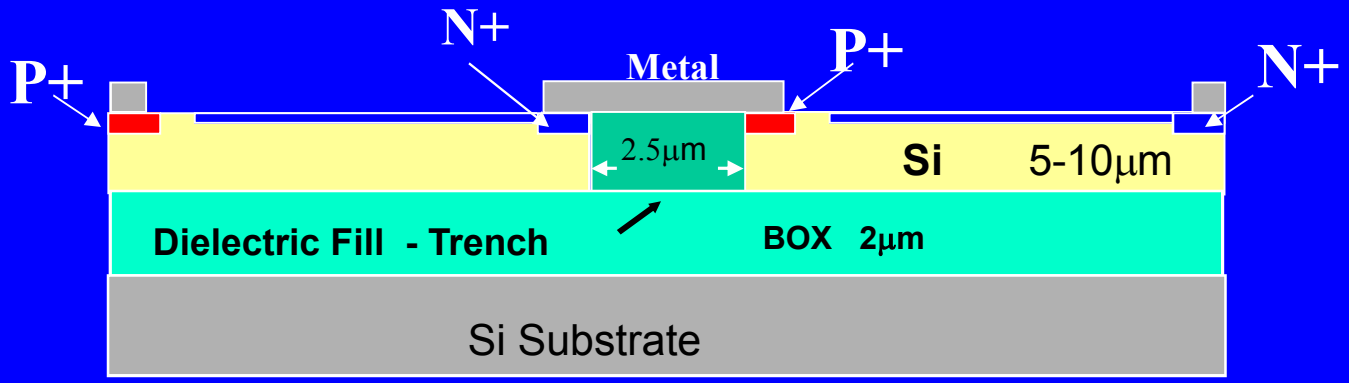
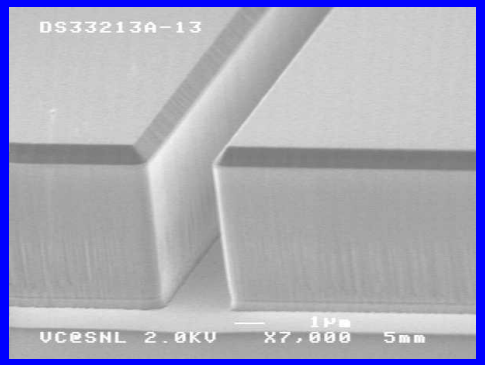
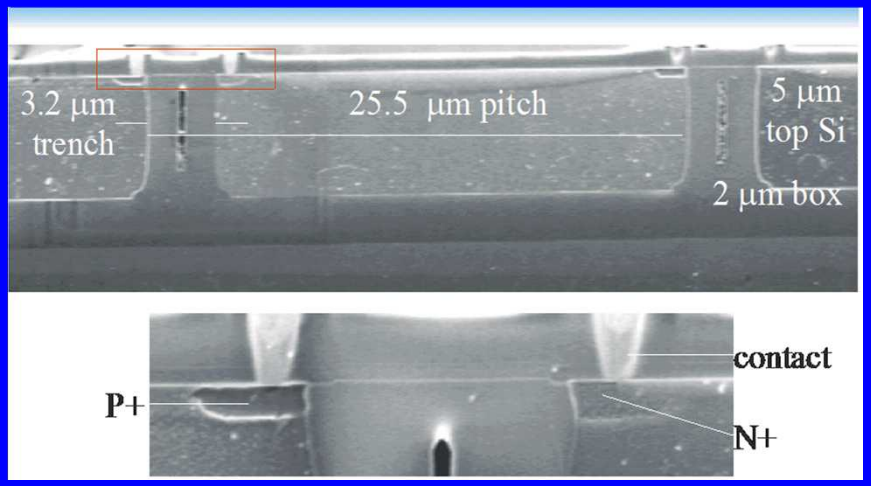
Series connected High-Voltage Photovoltaics



SOI with buried oxide layer and trench with dielectric fill provide cell electrical isolation



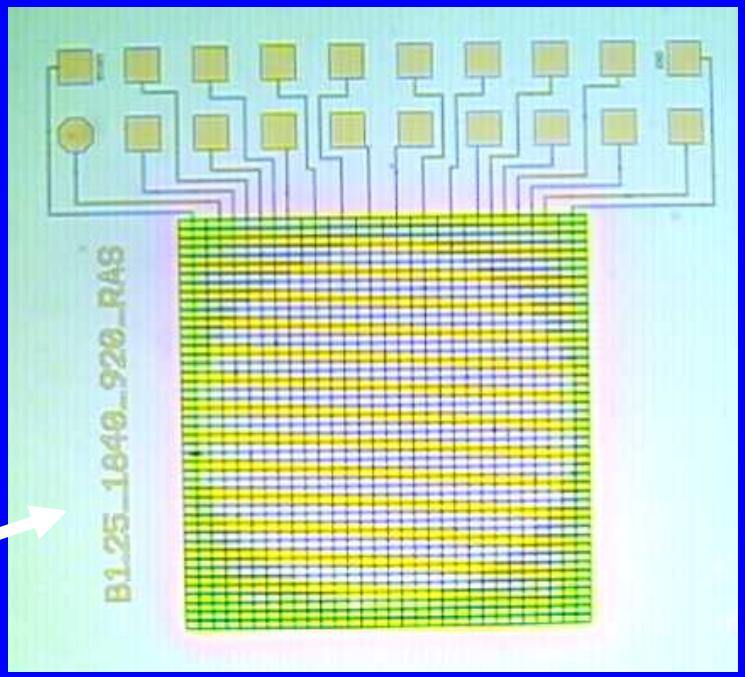
Trench prior to fill

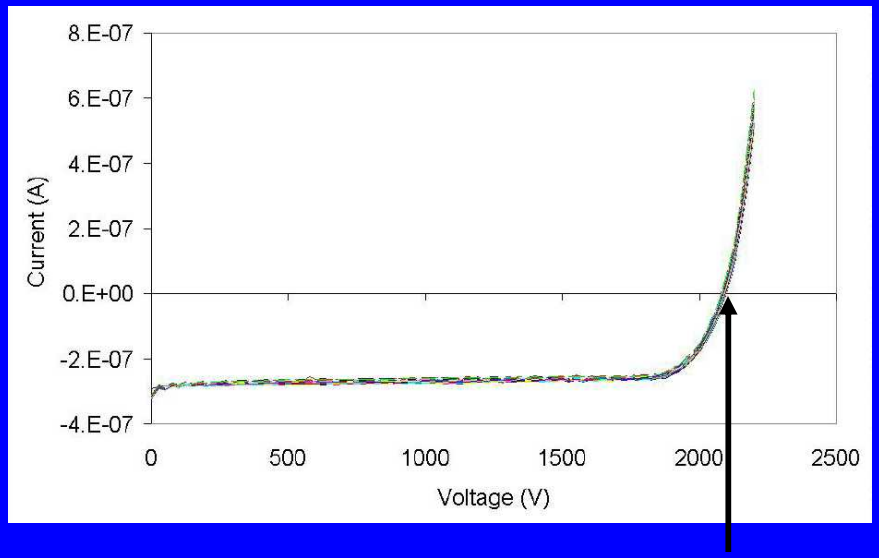


Filled trench with series connections

High-Voltage Photovoltaics from series-connected arrays.

Series Si Cells, 1.25 mm diameter, Multiple Taps





>2,000 V breakdown

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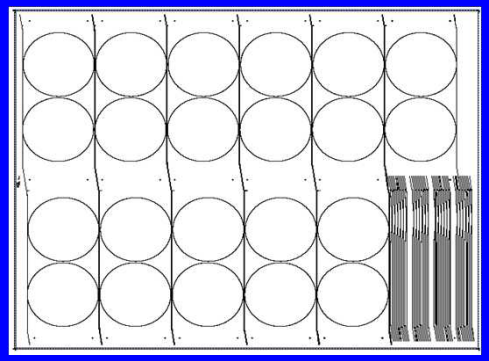
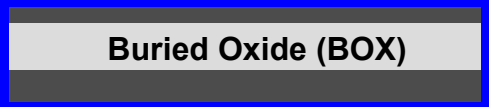
Ultra-Low-Loss SOI Silicon Rib Waveguide



Design test mask with ring resonators and varying coupler gap sizes



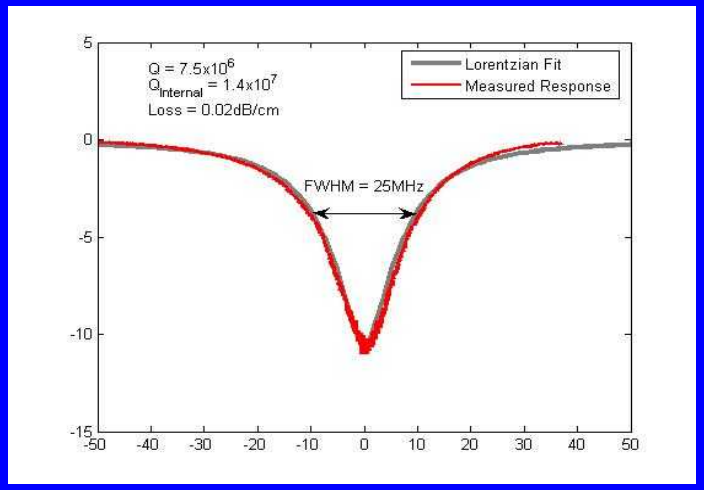
1.34 um n-type 38-63 Ohms – Silicon (100) device layer
1.0 um buried oxide (BOX)
675 um silicon n-type substrate

Pattern with Photo Resist

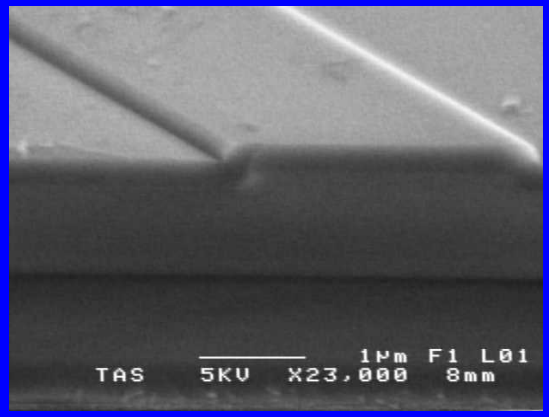
Reflow Photo Resist

Etch 0.2 um Rib into Silicon Surface

Oxidize Silicon
Final thickness is 1.0 um Si with 0.2 um Rib

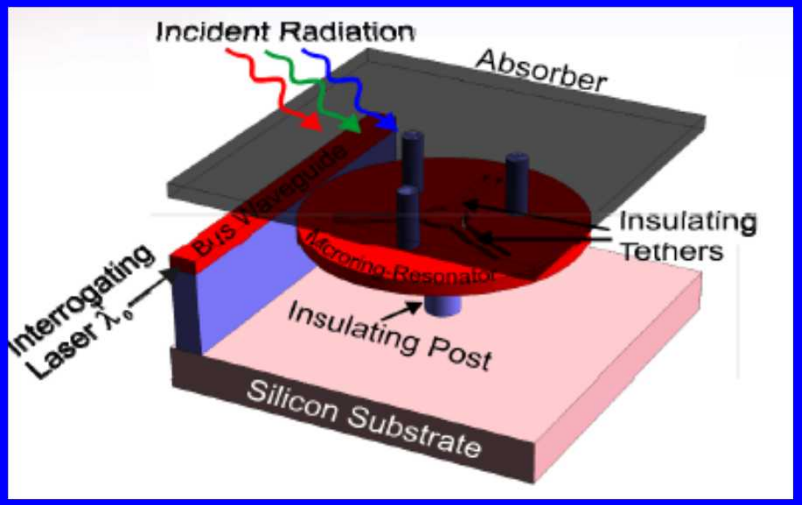


Results
$Q = 7.5 \times 10^6$
Internal $Q = 1.4 \times 10^7$
Loss = 0.02 dB/cm

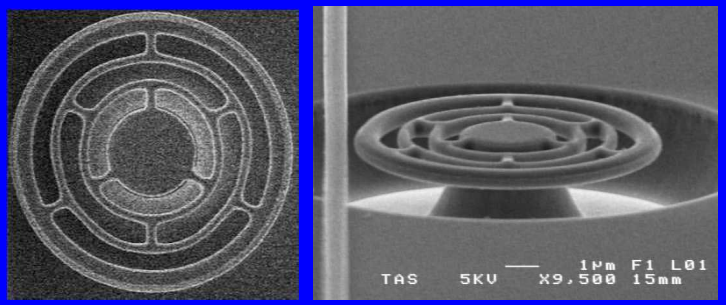


Fabricated Waveguide

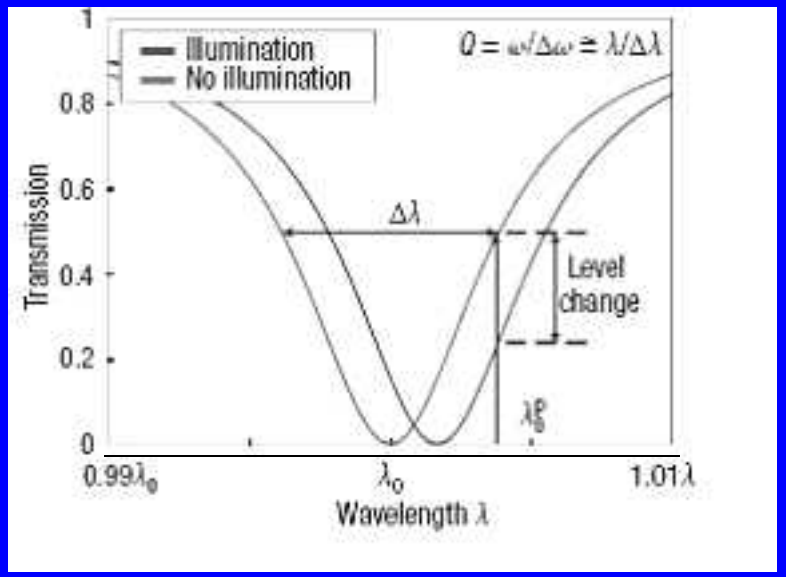
SOI for optical thermal sensors



Single Pixel

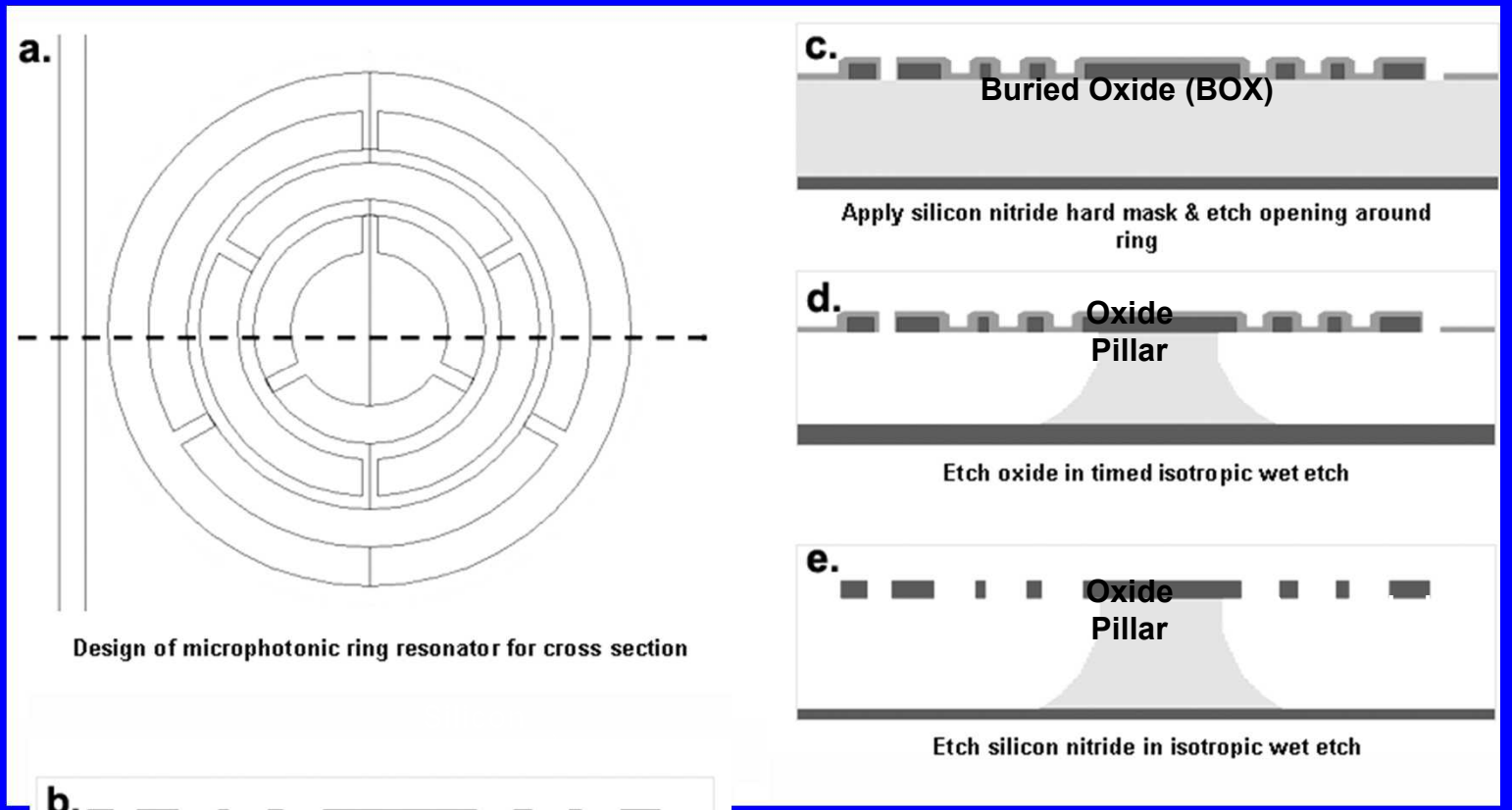


Fabricated and Oxidized SOI Rings



- Low thermal conductivity of BOx provides maximizes impact of temperature excursions.
- Theoretical uncooled IR sensitivity within ~20x of cooled HgCdTe!

Fabrication of Thermally Isolated SOI Ring Resonators



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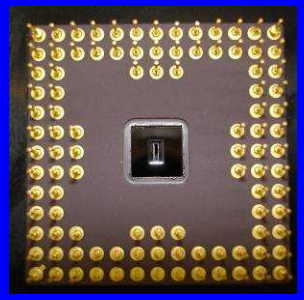
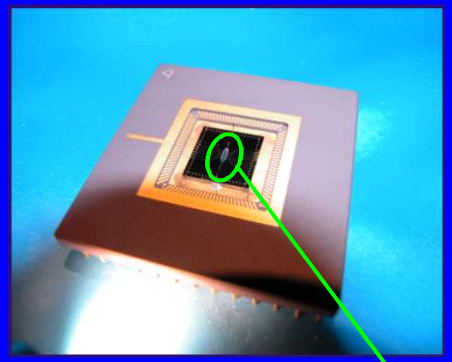
3-D Ion Trap Chip (ITC) with through-chip and through-package optical access.

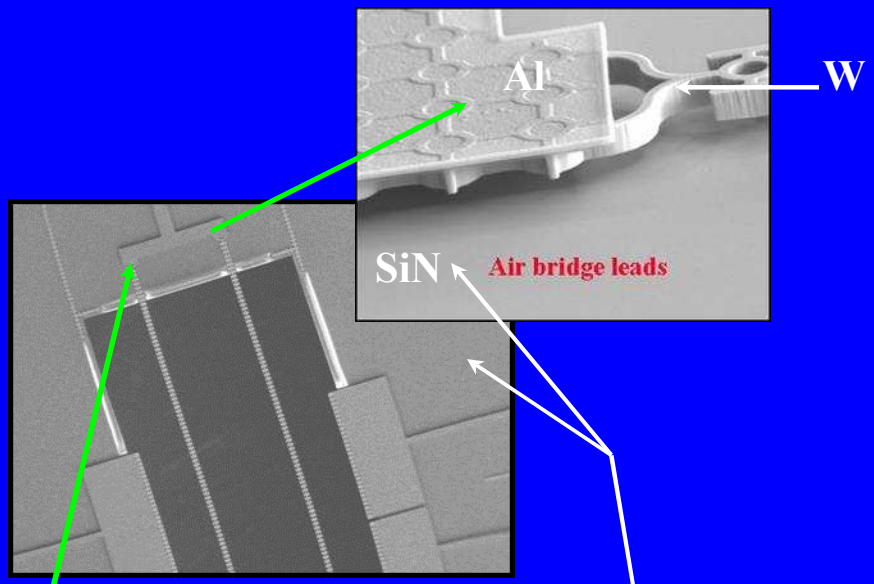
Packaged 3D ion trap chip

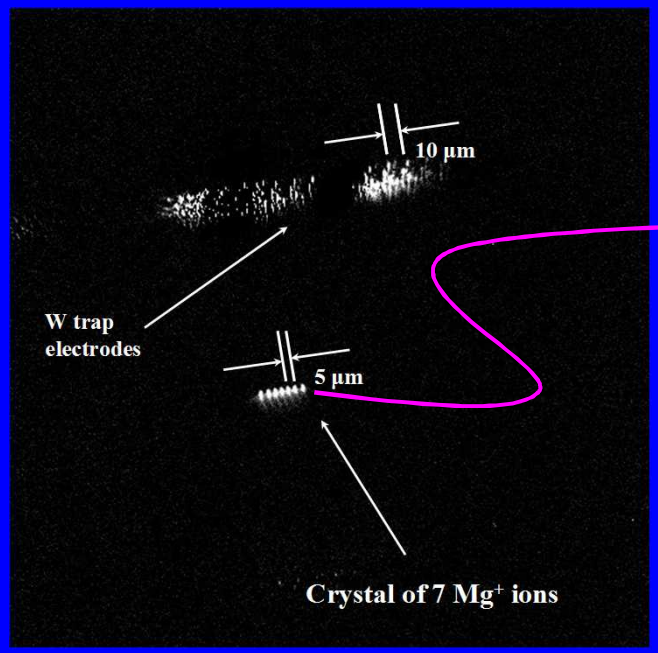


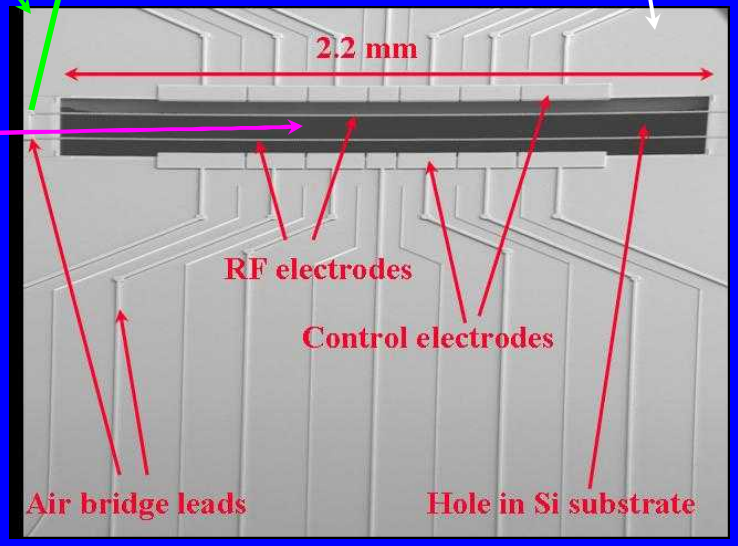
Back



Front



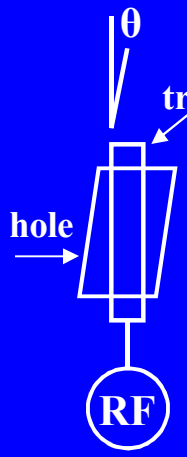


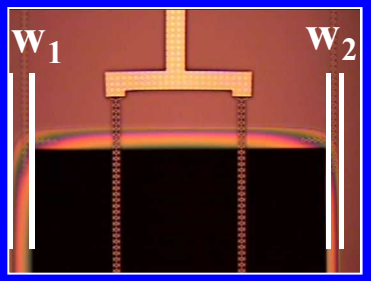


heating rate w/ SiN surfaces 7.2E5 quanta/sec

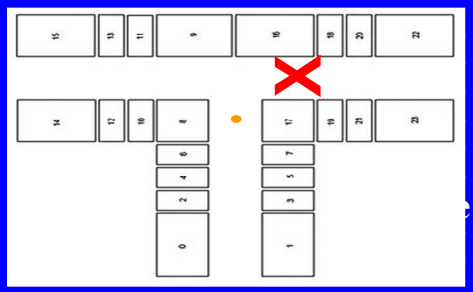
Courtesy of NIST Boulder – Wineland group

SOI for substrate through-hole engineering





Misalignment and rotation of via to electrodes could affect ion transport and heating rates

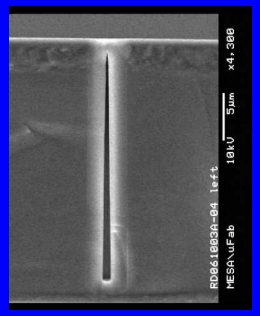


group

Silicon on Insulator (SOI) technology allows for precise, front-side alignment of the through hole to ion trap electrode features

Top Si plug defining through hole is precisely aligned to trap electrodes and can be very small

Oxide release seam in top Si allows later removal of Si plug



Hole etched in handle Si after trap electrode definition on top of substrate

Top Si

Buried SiO_2 (BOx)

The handle Si is etched away from the trap chip backside (stopping on the BOx).

Handle Si

Handle Si

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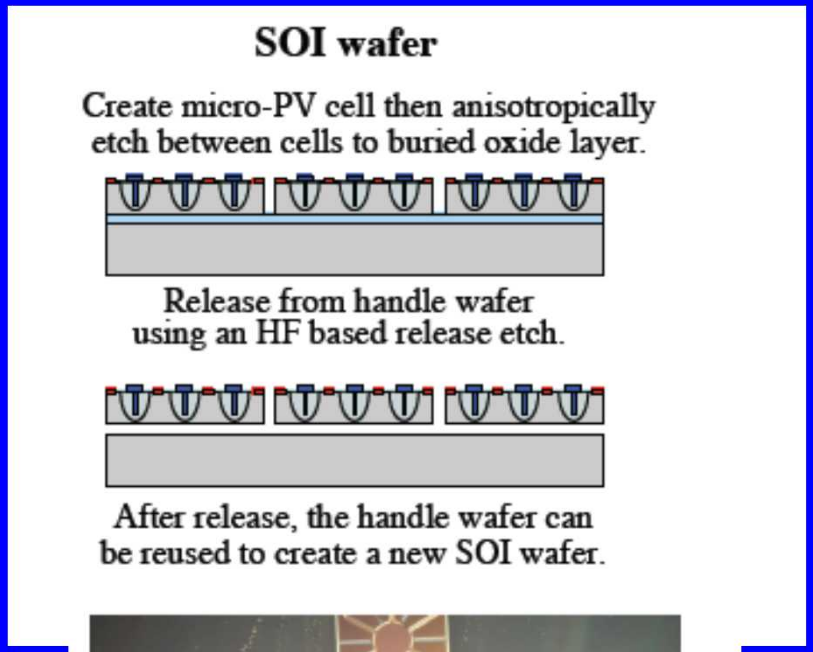
Low-cost lift-off silicon solar cells



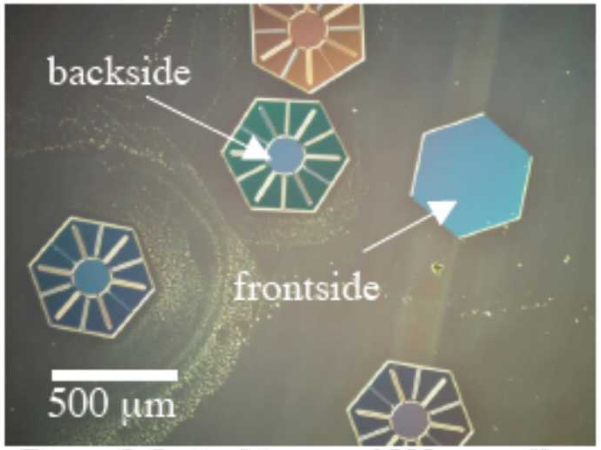
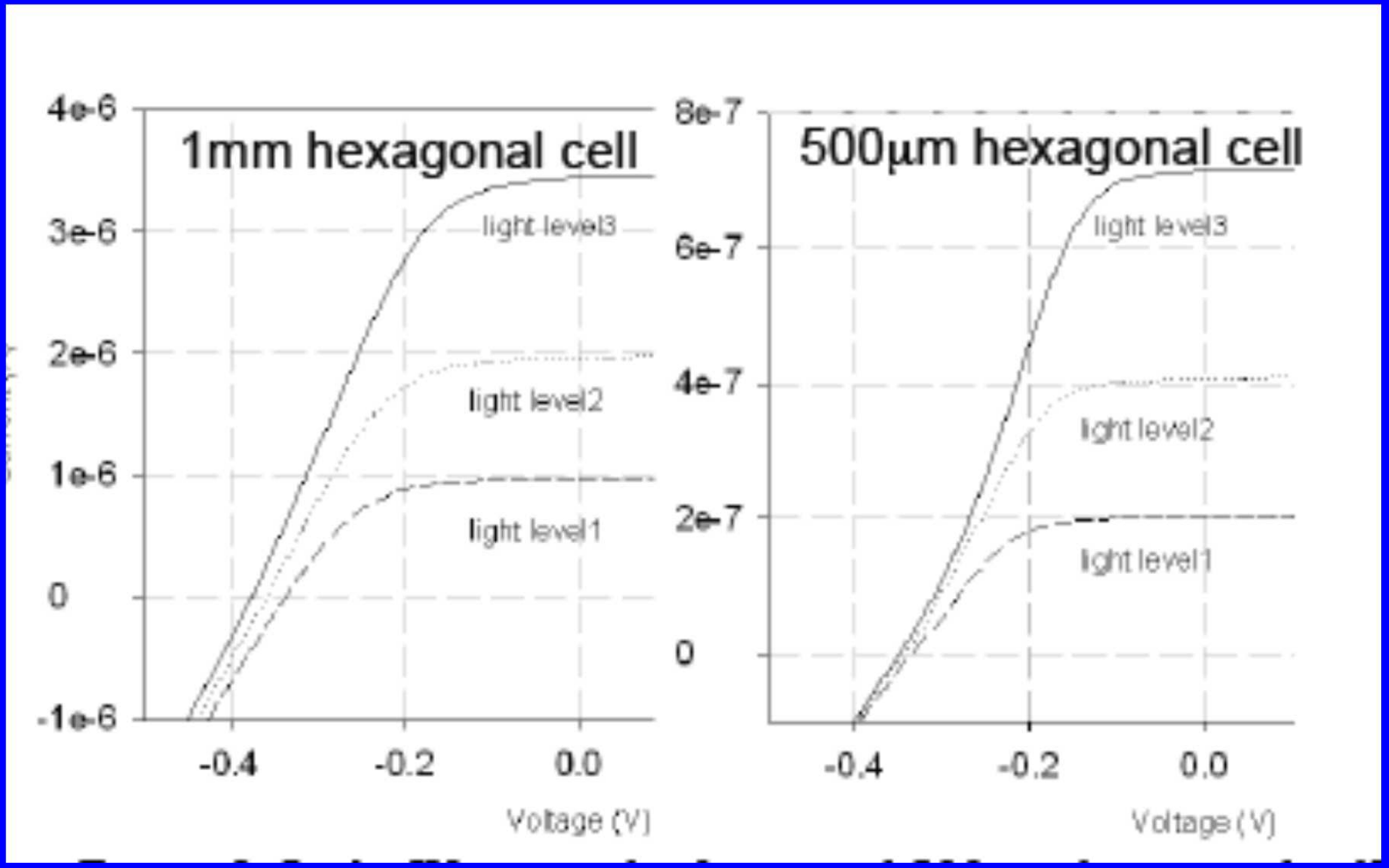


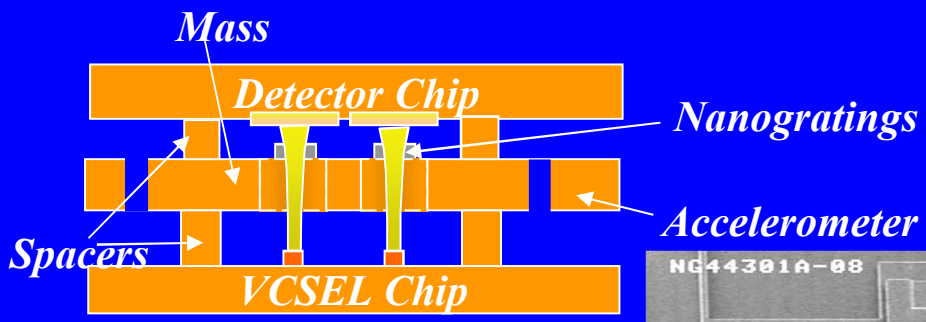
Figure 2 Optical image of 500 μm cells.

- Silicon material accounts for 50% of module cost of single-crystalline silicon solar cells.
- Most of the solar spectrum absorbed in first 10-20μm of silicon.
- SOI release technology allows of factor of 10 savings in silicon material by re-use of silicon substrates.

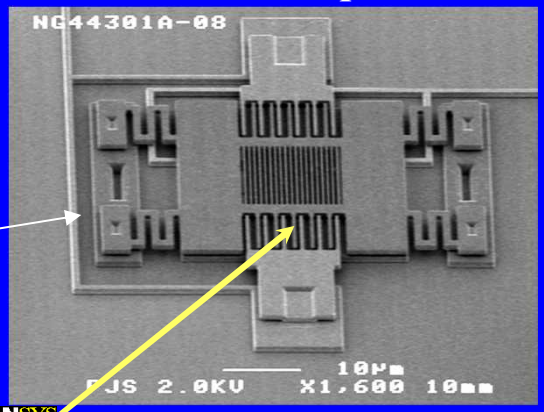
Low-cost lift-off silicon solar cells



Complex SOI systems: Nano-g accelerometer



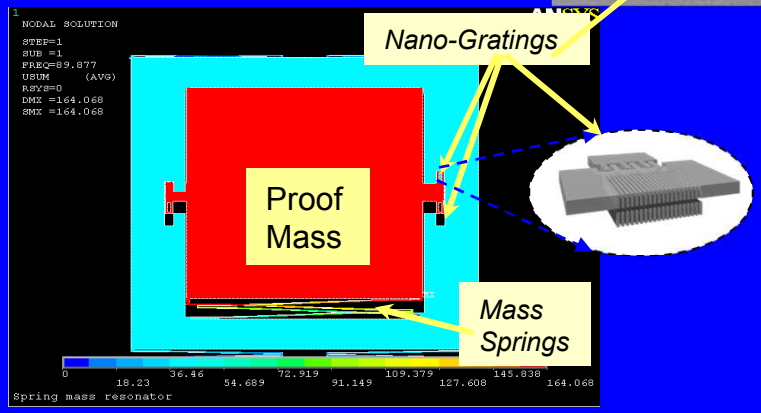
Accelerometer concept



Dual layer nanograting test device

Combines:

- Near-field coupling of sub-wavelength gratings
- Integrated proof mass from through-wafer bulk micromachining



- Record displacement sensitivity **12 fm/√Hz**
- Record low Mass Resonant Frequency for a MEMS device **~ 40 Hz**
- Record Thermal noise floor **~10nG/√Hz**

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Our devices have used a wide variety of SOI wafers.

- Device-layer doping has varied:
  - Degenerately doped (0.005 ohm-cm) surface silicon is used for ion traps and SOI accelerometers
  - Lightly doped (10-20 ohm-cm) surface silicon is used for optical devices, structural silicon layers in which doping doesn't matter, or electronic devices in which doping will be controlled by process.
- Device-layer thickness have varied from:
  - thin (~0.3μm) for active transistors and optical elements
  - to 50μm for robust mechanical layers for ion traps and accelerometers.
- Buried-oxide thickness has varied from:
  - 0.2μm for CMOS to
  - 3μm for photonic crystals.
- Soitec and Ultrasil are our suppliers.

Our experience deviates from common beliefs.

- Belief: thicker BOx is desirable for structures that will be released
  - When the BOx is etched away to free the device layer, the thicker box should release more quickly due to faster transport of the etch chemistry, and a larger gap should be less prone to sticking.
- Our experience: We have achieved complete release even with a thick device layer and a 1 μm BOx

Conclusions

- Radiation-hardening of CMOS circuits drove Sandia to investigate SOI in the mid-1990s.
  - Developed material science and process expertise as a result.
- Familiarity with SOI led to extensions beyond integrated circuits using flexibility inherent in the MESA fabrication facilities.
- The processing flexibility inherent in SOI has enabled Sandia to develop a wide variety of novel devices.