SAND2016-3417J

Micron-scale three-dimensional subtractive manufacturing

D. Bruce Burckel, Patrick S. Finnegan, M. David Henry, Paul J. Resnick, and Robert L. Jarecki Jr.

Emerging nano-photonic[1] and nano-opto-mechanical [2] applications benefit from fabrication of complex three-dimensional structures. Creation of micrometer scale and sub-micrometer scale structures can be performed either additively, or subtractively. Additive techniques, where material is deposited, such as direct laser write [3,4], interferometric lithography [5,6], nano-origami [7,8] and colloidal self-assembly [9] have been used to create a wide array of complex sub-micrometer structures. Examples of subtractive fabrication of three-dimensional structures, where material is removed, are less common.

Microelectronic fabrication requires the ability to create sub-micrometer and deep sub-micrometer scale patterns in resist and subsequent transfer of these patterns to the substrate. Plasma-based etching is the dominant etching technique and is used to create contact holes, define transistor gates, and pattern blanket metal layers into patterned interconnects. In plasma etching, a space-charge neutral region of ionized atoms and electrons is created inside the etch chamber. At the cathode a plasma sheath develops, where a large voltage drop develops accelerating etchant species ions at the surface of the wafer, where the material to be etched becomes volatilized and removed via vacuum pump[10]. The process of etching at the wafer surface is an enormously complex combination of plasma dynamics, gas phase kinetics and surface chemistry, but it is our ability to successfully navigate this complicated space which has enabled the creation of today's state-of-the-art 22-nm transistors as well as breathtaking high-aspect-ratio MEMs and more niche microfabrication structures.

In most applications, plasma etching occurs through a patterned planar etch mask, either a soft mask such as photoresist or a hard mask such as oxide or nitride, in a direction normal to the wafer or substrate surface. This is the case in high volume manufacturing processes used in integrated circuit manufacturing as well as in many micromachining applications. Complex three-dimensional structures can be created using this approach in a layer-by-layer fashion [11,12]. For some next generation applications etching of more complex 3-dimensional structures are required and alternative approaches to traditional top-down plasma based etching are sought.

Rather than being distributed throughout the etch chamber, the electric field responsible for accelerating the ions inside the chamber is concentrated in the narrow "plasma sheath" which conforms to the surface of the substrate. Simply tilting the substrate with respect to the nominal etching direction in an attempt to etch at oblique incidence is unsuccessful in most circumstances because the plasma sheath conforms to the substrate, once again accelerating the ions in the normal direction to the now-tilted substrate surface (Fig. 1(A)). Oblique incidence etching is possible using a Faraday cage to alter the local plasma sheath, redirecting the energetic ions at an oblique angle with respect to the substrate surface normal (Fig. 1(B)). The plasma sheath conforms to the periphery of the Faraday cage, while inside the cage, the electric field is zero. By selecting a mesh of appropriate dimension, the accelerating electric field can be completely screened inside the cage, while ions accelerated by the plasma sheath are able to penetrate the screen, following their initial trajectory unabated until they strike the sample

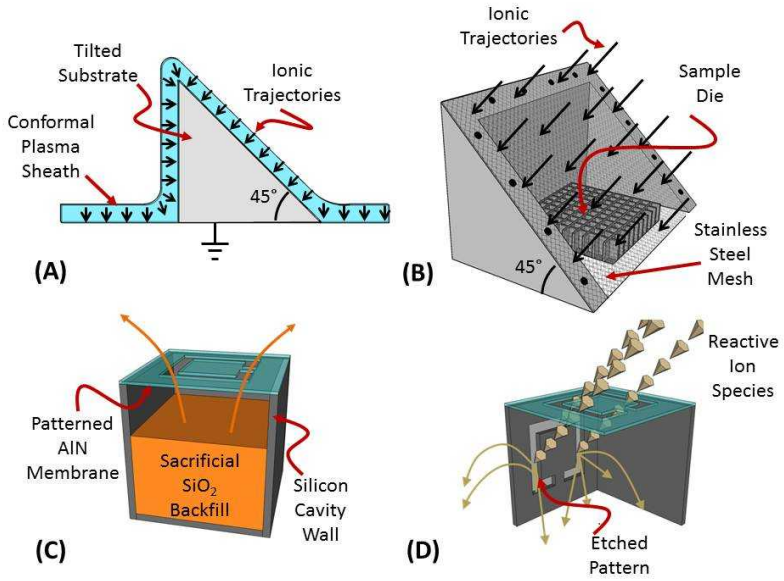

Fig. 1 (A) Schematic diagram showing the conformal plasma sheath directing the etchant species normal to the tilted surface; (B) Oblique view of a Faraday cage with a mesh screen. The Faraday cage redirects the plasma orientation while the screen allows the ions to pass through; (C) Schematic diagram of the formation of the suspended patterned membrane; (D) Schematic diagram of oblique etching through the patterned membrane.

at an angle defined by the Faraday cage geometry. This technique has been used to perform oblique etching on planar patterns using standard parallel plate etch systems. [13-16]. It is also possible to etch in multiple directions simultaneously using Faraday cages with multiple surfaces covered with mesh. In a similar vein, in [17] the authors fabricated a structure directly on top of the substrate to redirect the incident ions obliquely onto the substrate. Here we combine the oblique directionality provided by a Faraday cage with a suspended patterned membrane to demonstrate robust three-dimensional patterned etching of vertical silicon sidewalls, generalizing planar top-down etching into truly three-dimensional subtractive patterning approach.

Recently, we demonstrated membrane projection lithography (MPL) as a method for creation of 3-dimensional metamaterial structures[18-19] in a polymer material system. In the MPL process, directional metal deposition is performed into unit cells through a patterned, suspended membrane, resulting in the deposition of metal-inclusions on the interior face(s) of the unit cell. MPL is capable of producing high fidelity 3-D inclusions at sub-micrometer dimensions with < 100 nm spatial resolution. The basic MPL process flow is covered in detail in a CMOS compatible material system [20], however we provide a brief synopsis of the approach for completeness. Formation of the dense array of unit cells begins by depositing a silicon nitride hard mask on a single crystal silicon substrate, and patterning the nitride with the desired array of unit cells, in this case, a square array of unit cells with micrometer scale lateral dimensions. Deep reactive ion etching is used to etch approximately topography into the silicon substrate. A PECVD oxide is then deposited, filling the cavities and overfilling the unit cell matrix. Chemical mechanical polishing is then used to planarize the sacrificial oxide back to the nitride layer etch mask, which now becomes a polish stop. Aluminum nitride is then deposited over the unit cell matrix

and patterned with a deep-UV scanner and subsequent etch step. The oxide backfill can now be removed through the patterned AlN membrane (Fig. 1C), yielding the final suspended patterned membrane positioned over the unit cell. There is considerable freedom of choice for the unit cell dimensions, for this work, we created both cubic unit cell matrices with two micrometer cubic cavities and 100 nm and 300 nm thick walls between neighboring cavities.

A stainless steel block was machined into a 45-45-90 degree wedge with a 1.4 cm x 1.4 cm cavity. Stainless steel mesh (Goodfellow, Inc.) with a wire diameter of 66 μm, with a grid spacing of ~ 6 wires/mm and nominal aperture of approximately 100 μm was used to form the ion-permeable surface mounted on the edges of the machined 45 degree face of the cage (Fig. 1(B)).

The two most common forms of plasma etching are inductively coupled plasma (ICP) etching and reactive ion etching (RIE). We have successfully etched using both etching approaches in multiple different etch systems.

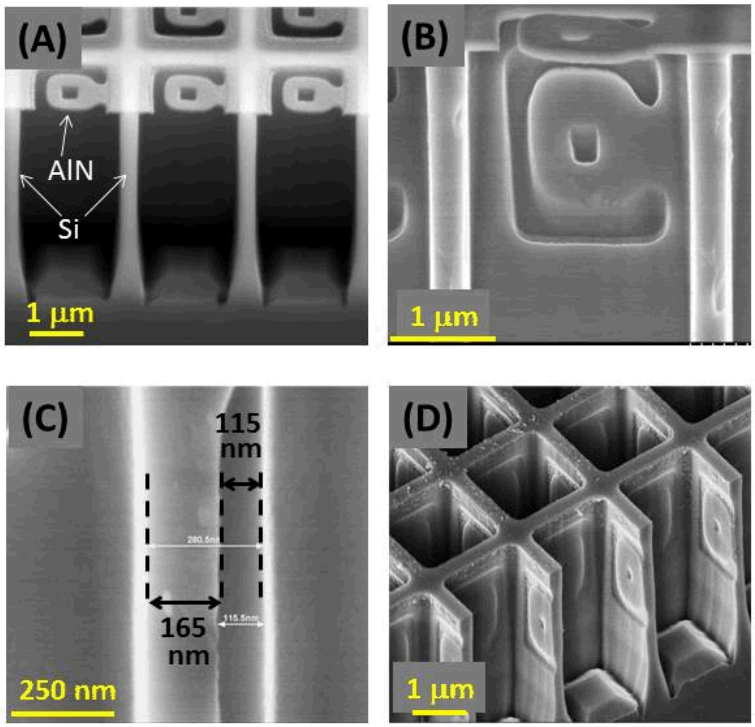

Fig. 2 (A) Cross-section SEM image showing the suspended patterned aluminum nitride membrane over unit cells in high aspect ratio silicon topography; (B) Cross-section SEM image of an etched feature in the vertical silicon wall; (C) Cross-section SEM image showing the etch depth into the wall, where 115 nm of silicon was etched into a 280 nm thick silicon wall; (D) Oblique SEM image showing two consecutive etches after a 90 degree rotation of the sample in the Faraday Cage.

Fig. 2(A) shows an SEM image of the high-aspect ratio silicon structure to be etched. The structure consists of a two-dimensional array of rectangular parallelepiped unit cells with a coaxial split-ring resonator (SRR) patterned AlN membrane. The obvious etch notch between the unit cell wall and floor at the bottom of the unit cell is due to the etch used to form the unit cells, and can be eliminated by

optimizing the etch parameters. The sacrificial oxide backfilling the unit cell formed a keyhole which resulted in the coaxial "dot" in the middle of the SRR pattern. Although unintentional, this dot demonstrates the formation of high fidelity patterns this approach is capable of transferring. Three unit cells of a dense array of similar unit cells are shown. A Versaline ICP with a Cl_2/CF_4 mixture (20 sccm, 20 sccm), background pressure of 10 mTorr, RF power of 500 W was used to etch the silicon. The cross-section SEM in Fig. 2(B) shows the successful transfer of the membrane pattern into one vertical face in the interior of the unit cell after 300 seconds of etching. Fig. 2(C) shows a cross-section SEM of the etched wall, where 115 nm of the 280 nm thick wall was etched, yielding an etch rate of 3.8 A/s. (Note: the etch parameters have not been optimized for etch rate). In Fig. 2(D), two shorter consecutive etches were performed with a 90 degree rotation of the sample between etches so that two adjacent faces of the unit cell have been decorated. Additionally, in Fig. 2(D), the AlN membrane was removed in a basic SC1 clean, a standard CMOS cleaning solution (10:1:1, $H_2O:HN_3OH:H_2O_2$). No apparent degradation of the AlN mask was evident after 600 s of combined etching.

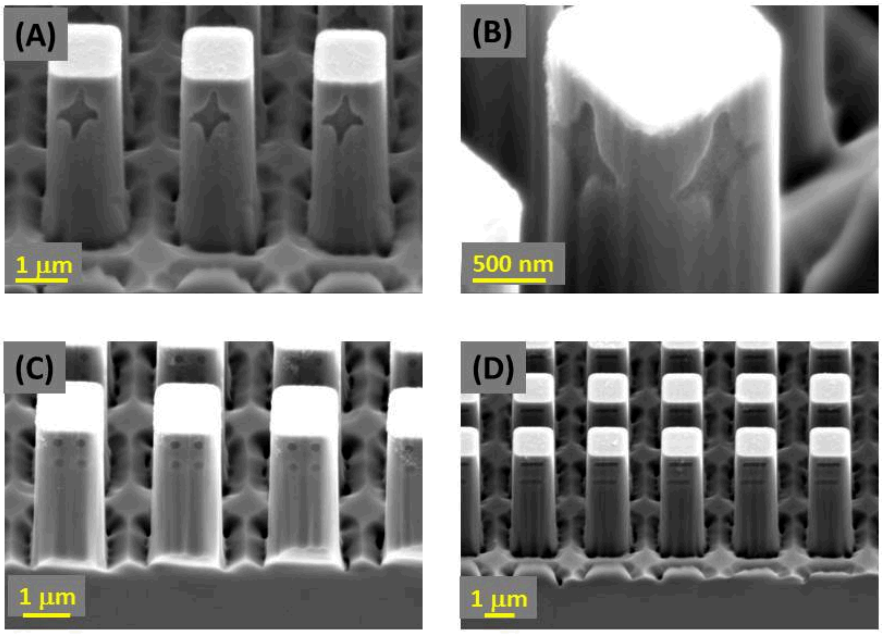

Fig. 3 (A) Oblique SEM image of silicon pillars patterned with a cross on a single side; (B) Oblique SEM image of a pillar patterned on multiple sides; (C) Oblique SEM image of pillars with ~100 nm isolated etched features; (D) Oblique SEM image of ~100 nm etched dashes.

In Fig. 3(A-D) we show MPL-Etching results on the external faces of silicon pillars, demonstrating that the approach is quite versatile. In Fig. 3(A), a single cross is etched into the vertical face of the pillar. The distortion of the cross is a faithful representation of the distorted membrane pattern, due to the difficulties in resolving these deep sub-micrometer features using the available optical stepper. Fig. 3(B) shows a pillar with 2 consecutive etches performed after a 90 degree rotation of the sample. Again, no obvious Fig. 3(C) shows isolated dots while Fig. 3(D) shows parallel dashes. The smallest dimension in both of these patterns is approximately 100 nm.

Fig. 4 contains SEM images of through wall etching using an RIE system with an SF_6/Ar gas mixture (14 sccms/3 sccms) at ~10 mTorr, with 350 W RF power and 650V DC bias. In Fig. 4(A), the coaxial SRR is

etched. The unit cell wall at the top ~2/3 of the SRR pattern is completely etched through, revealing the unit cells in the row behind the cleaved face. Due to the slight flaring of the unit cell wall, the bottom of the SRR failed to etch completely through. Of note is the coaxial dot (also etched through) demonstrating a qualitative measure of the possible resolution of this technique. In Fig. 4(B), an x-pattern was significantly over-etched through the vertical wall. Although the pattern fidelity on the side wall has been lost due to the overetching, the pattern in the floor of the unit cell is well defined and can only result from the flux of etchant species through the horizontal membrane, through the vertical silicon wall and into the floor of the neighboring unit cell.

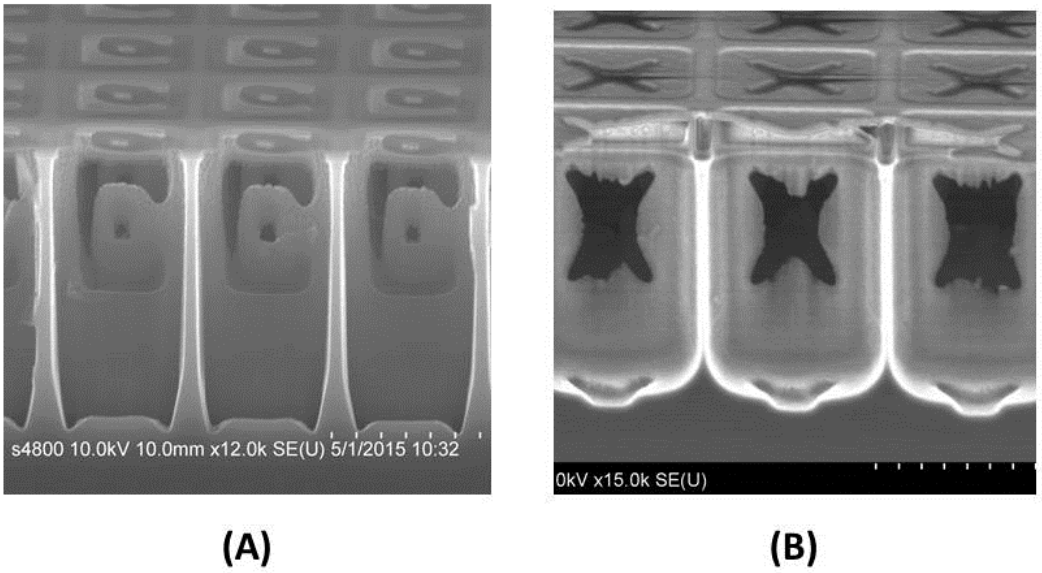

Fig. 4 Through wall patterns created using an RIE etch with SF_6/Ar gas mixture. (A) Cross-section SEM of a coaxial split ring resonator. The patterned wall of the neighboring unit cell is visible through the patterned wall in the foreground; (B) Cross-section SEM showing an x pattern etched completely through the wall and into the floor of the neighboring unit cell.

Given the success of the MPL approach as a deposition technique, the success of an MPL-based etching approach might seem assured. One significant difference between deposition in an e-beam evaporator and a plasma etch chamber is the ambient pressure. In a metal evaporator, metal is deposited somewhere between 10^{-7} Torr - 10^{-6} Torr, while typical etch pressures range from 10^{-3} Torr- 0.1 Torr. One of the metrics which is used to assess etch quality is resolution. The increased pressure inside the etch chamber could possibly affect this by causing gas phase collisions in the volume of the Faraday cage, resulting in redirection of the incident etchant species even in the absence of applied field. While we have not performed rigorous resolution experiments, we have empirical evidence which indicates this approach is capable of resolving < 50 nm features (Supplemental Information).

Demonstration of the ability to etch complex patterns into high aspect ratio structures has the potential to impact a wide variety of next generation micro and nano structured research. In structured electromagnetic research, complementary metamaterials are formed following Babinet's principal where continuous metallic films are patterned with clear openings in the form of split ring resonators or

other resonant structures. Where the standard resonators operate on the electric field, the CMM resonators operate on the magnetic field (or vice versa). For non-metallic structured electromagnetic materials, researchers are using solid prisms of high index semiconductors formed into dielectric resonators with significantly lower loss than metallic resonator based metamaterials. The quality factor (Q-factor) of these structures is dramatically impacted by the shape and symmetry of the dielectric resonator. The patterned etch presented here could be used to dress the faces of the dielectric resonator with structure to modify the Q-factor or alternatively, complete low-index (air) dielectric resonators could be formed in the high index background, forming complementary dielectric metamaterials.

Acknowledgements

The authors would like to acknowledge Bonnie McKenzie for providing SEM images and Major Monochie for fabrication of the Faraday cages. This work was supported by the Laboratory Directed Research and Development program at Sandia National Laboratories, a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

[1] A. M. Jones, C. T. DeRose, A. L. Lentine, D. C. Trotter, A. L. Starbuck, R. A. Norwood, "Ultra-low crosstalk, CMOS compatible waveguide crossings for densely integrated photonic interconnection networks," Opt. Expr., **21**, 12002-12013 (2013).

[2] H. Shin, J. A. Cox, R. Jarecki, A. Starbuck, Z. Wang, and P. T. Rakich, "Control of coherent information via on-chip photonic-phononic emitter receivers," Nat. Comm. **6**, 6427, (2015).

[3] J. K. Gansel, M. Thiel, M. S. Rill, M. Decker, K. Bade, V. Saile, G. von Freymann, S. Linden, and M. Wegener, "Gold helix photonic metamaterial as broadband circular polarizer," Science, **325**, 1513-1515, (2009).

[4] M. S. Rill, C. Plet, M. Thiel, I. Staude, G. von Freymann, S. Linden, and M. Wegener, "Photonic metamaterials by direct laser writing and silver chemical vapour deposition," Nature Materials, **7**, 543-546, 2008.

[5] D. B. Burckel, C. M. Washburn, A. K. Raub, S. R. J. Brueck, D. R. Wheeler, S. M. Brozik and R. Polsky, "Lithographically defined porous carbon electrodes," Small, **5**, 2792-2796, (2009).

[6] X. Xiao, T. E. Beechem, M. T. Brumbach, T. N. Lambert, D. J. Davis, J. R. Michael, C. M. Washburn, J. Wang, S. M. Brozik, D. R. Wheeler, D. B. Burckel and R. Polsky, "Lithographically defined three-dimensional graphene structures," ACS Nano, **6**, 3573-3579, (2012).

[7] J. H. Cho and D. H. Gracias, "Self-assembly of lithographically patterned nanoparticles," Nano Letters, **9**, 4049-4052, (2009).

[8] J.H. Cho, M. D. Keung, N. Verellen, L. Lagae, V. V. Moshchalkov, P. Van Dorpe, and D. H. Gracias, "Nanoscale origami for 3D optics", Small, **7**, No. 14, 1943-1948, 2011.

[9] Y. A. Vlasov, X. Z. Bo, J. C. Sturm, and D. J. Norris, "On-chip Natural Assembly of Silicon Phontonic Bandgap Crystals," Nature, **414**, 289-293, 2001.

[10] S. A. Campbell, The Science and Engineering of Microelectronic Fabrication (Oxford University Press, New York, 1996).

[11] J. G. Fleming, S.Y. Lin, I. El-Kady, R. Biswas, and K. M. Ho, "All-metallic Three-dimensional Photonic Crystals with a Large Infrared Bandgap," Nature, **417**, 52-55, 2002.

[12] J. Valentine, S. Zhang, T. Zentgraf, E. Ulin-Avila, D. A. Genov, G. Bartal, and X. Zhang, "Three-dimensional optical metamaterial with a negative refractive index," Nature, **455**, 376-380, 2008.

[13] G. D. Boyd, L. A. Coldren and F. G. Storz, "Directional reactive ion etching at oblique angles," Appl. Phys. Lett., 36, 583-585, (1980).

[14] B. Cho, S. Hwang, J. Ryu, I. Kim, and S.H. Moon,"Fabrication method for surface gratings using a Faraday cage in a conventional plasma etching apparatus," Electrochem. And Solid State Lett. 2, 129-130 (1999).

[15] J.-K. Lee, S.-H. Lee, J.-H. Min, I.-Y. Jang, C.-K. Kim, and S.H. Moon, "Oblique-directional plasma etching of Si using a Faraday cage,"J. Electrochem. Soc. 156, D222-D225 (2009).

[16] M.J. Burek, N.P. de Leon, B.J. Shields, B.J.M. Hausmann, Y. Chu, Q. Quan, A.S. Zibrov, H. Park, M.D. Lukin, and M. Lončar, Nano Lett. 12, 6084 (2012).

[17] S. Takahashi, K. Suzuki, M. Okano, M. Imada, T. Nakamori, Y. Ota, K. Ishizaki, and S. Noda,"Direct creation of three-dimensional photonic crystals by a top-down approach," Nat. Mater. 8, 721-725 (2009).

[18] D. B. Burckel, J. R.Wendt, G. A. Ten Eyck, A. R. Ellis, I. Brener, and M. B. Sinclair," Fabrication of 3D metamaterial resonators using self-aligned membrane projection lithography," Adv. Mater., 22, 3171-3175, (2010).

[19] D. B. Burckel, J. R. Wendt, G. A. Ten Eyck, J. C. Ginn, A. R. Ellis, I. Brener, and M. B. Sinclair, "Micrometer-scale cubic unit cell 3D metamaterials," Adv. Mater., 22, 5053-5057, (2010).

[20] D. B. Burckel, P. J. Resnick, P. S. Finnegan, M. B. Sinclair and P. S. Davids, "Micrometer-scale fabrication of complex three dimensional lattice + basis structures in silicon," Opt. Mater. Expr., 5, 2231-2239, (2015).

Supplemental Information

Etch Resolution

In practical terms, resolution must be measured in two ways: 1) The smallest resolvable sparse features; and 2) The closest placement of two or more dense features. While we have not established rigorous quantitative measures of these two metrics, we do have qualitative data that indicates the technique is capable of resolving sparse features with dimensions <50 nm. Consider the two cross-section SEMs in Fig. SI1. During the AlN membrane pattern etch for this experiment, etch residue was deposited on the walls of the patterned photoresist used to define the membrane pattern. An incorrect sequence during the photoresist removal stage resulted in the formation of a gossamer thin halo, or etch veil surrounding the patterned membrane (Fig. SI1(A)). This veil has been eliminated in subsequent processing runs, but it provides an interesting probe into the fine-feature pattern transfer of this approach. Figure SI1(B) shows a cross section SEM of an etched feature in a vertical silicon wall. The top of the etched feature is fairly smooth, as this edge was defined by the bottom edge of the AlN membrane, which is smooth. The inner edge of the etched feature has a pronounced high spatial frequency roughness, matching that of the etch veil. This edge in the etched feature is defined by the top of the AlN membrane which, in this case possesses the veil. In this case, the fine sub-50 nm roughness of the veil is transferred into the silicon.

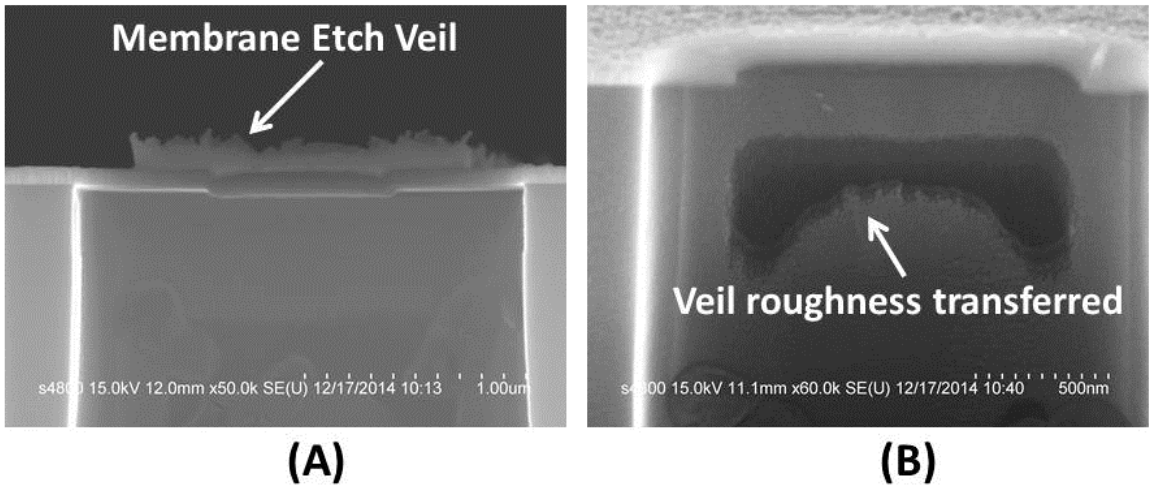

Fig. SI1 (A) Cross-section SEM showing the etch veil present in the membrane, formed during the AlN pattern etch; (B) Cross-section SEM showing a vertical silicon wall where the high spatial frequency roughness of the veil has been transferred into the wall.

In Fig. SI2 more examples of etched patterns are shown. In SI2(A), a cross pattern is transferred into the side wall. In this case the etch was performed to just short of breakthrough. Small regions of each cross have started to breach the wall, but the wall under most of the pattern is intact. The pattern is very well defined, with smooth edges. In Fig. SI2(B), a dipole pair pattern was etched significantly past break through, as in Fig. 4(B) in the main text. Again, the presence of the pattern in the floor is due to the

breakthrough of the unit cell wall, and continued etching into the floor of the neighboring unit cell. The silicon segment between the two dipole elements is ~ 100 nm across.

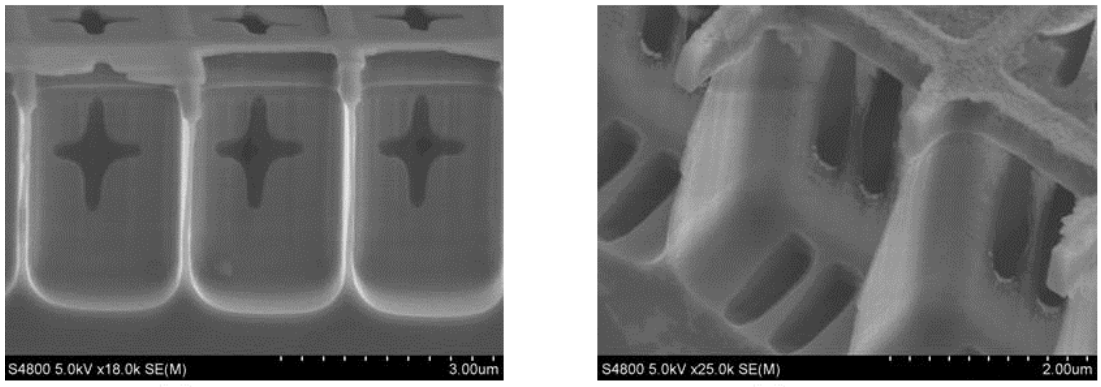

Fig. SI2 (A) Cross-section SEM image of a cross pattern etched to the point of breakthrough; (B) Cross-section SEM image of a dipole pair etched completely through the wall and into the floor of the neighboring unit cell. The silicon between the etched dipole features is ~100 nm wide.