Total Dose and SEU Hardness Assurance Qualification Issues for Microelectronics

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I. Introduction

A great deal of work has been done over the past 20 years to develop reliable, cost-effective hardness assurance test procedures to assess and assure the radiation hardness of integrated circuits for use in space and/or high-energy particle accelerator applications. Test guidelines have been developed for total dose hardness assurance qualification (e.g., the U. S. test guideline MIL-STD-883, Method 1019 and the European test guideline BS 22900) and for single event effects (SEE) hardness assurance qualification (e.g., JESD57 and ASTM F1192). These guidelines depend on laboratory tests that do not always match the exact conditions of the use environment because of time, cost, and facility limitations. For example, it is not practical to expose devices for years at extremely low dose rates to the total dose levels expected for multiple year space applications. Instead, the total dose response of microelectronics in these types of applications must be bounded by using laboratory radiation sources at moderate dose rates that can be completed within a reasonable time frame (a few hours to a few months). In addition, heavy ion test facilities cannot produce ions with energies equivalent to those present in space. Thus, lower energy ions must be used to assess the SEE performance of ICs in space environments. To develop reliable, cost-effective hardness assurance test methods, a detailed knowledge of the basic mechanisms that control the total dose radiation and SEE response of microelectronics is important. As our knowledge of the basic mechanisms of radiation effects has evolved over time, improvements to existing test methods have been made.

It is important to note that hardness assurance test methods are used to define tests that may provide significant insight into device behavior in radiation environments (i.e., space). They have been developed based on extensive test results of discrete devices and ICs. However, the mechanisms for radiation effects can vary widely for different device technologies and for different applications. It is the users responsibility to evaluate test results and to determine their applicability to part performance in the environment of interest. In other words, a test method is a tool for test engineers, but it provides no explicit guarantees or assurances for every device type, technology, or use environment. In many cases (especially those involving specialized device types and non-standard applications), a radiation-effects expert may be required to evaluate and interpret data to ensure device survivability in the use environment.

Here we will discuss hardness assurance test methods for total dose and SEE qualification. For total dose qualification, the main test methodologies used in the U.S. and Europe will be reviewed and differences between the guidelines will be discussed. A brief discussion of the fundamental mechanisms that form the foundation for the methodologies will also be presented. A more in-depth discussion of the mechanisms that control the radiation response of microelectronics can be found in the work presented by Schwank as part of this short course. This will be followed by a discussion of important total dose hardness assurance issues that include preirradiation elevated temperature stress (PETS) effects, enhanced low-dose rate sensitivity (ELDRS), selecting the optimum laboratory radiation source, determining worst-case bias conditions, and understanding the implication of characterization temperature. Following these discussions we will discuss some emerging issues relevant to SEE

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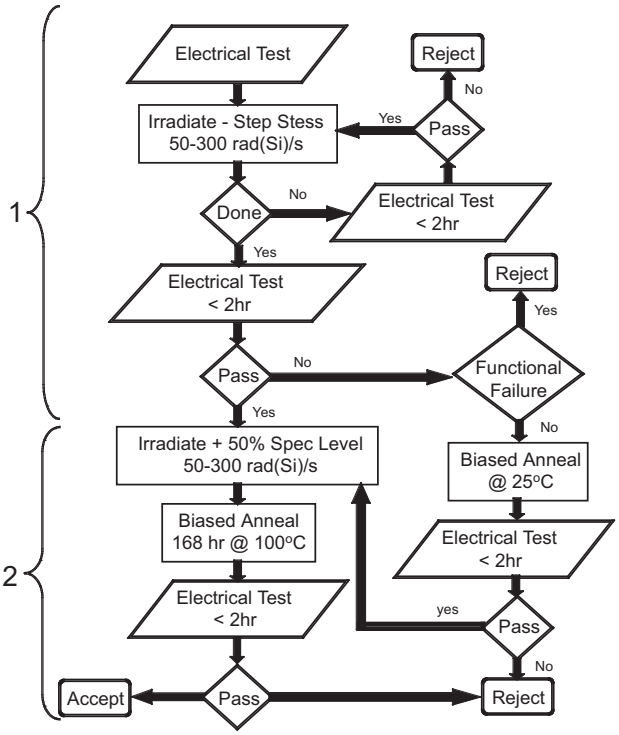

Fig. 1. Test flow for MIL-STD-883, Method 1019.7.

device qualification that are not covered in present SEE test guidelines. Specifically, we will discuss proton energy and angular dependence of proton-induced single-event latchup (SEL), the impact of total dose on single-event upset (SEU), and issues associated with high versus low energy heavy ion testing. The hardness assurance implications of these issues will be addressed.

II. Total dose hardness assurance test issues

A. Total dose hardness assurance test methods

There are a number of qualification test methods that define total-dose testing of microelectronics. These include MIL-STD-883, Test Method (TM) 1019 used in the US and its European counterpart, ESA/SCC Basic Specification (BS) No. 22900. While there are differences between these two test methods, both are intended to provide conservative estimates of the total dose response of microelectronics for use in low-dose-rate applications.

Figure 1 shows the main test flow for MOS devices as specified in the latest version of TM 1019 (version 7). This test method is broken into two phases. The first phase of the test method is a conservative test for parametric or functional failure due to radiation-induced oxide-trapped charge buildup in n- and p-channel gate-oxide or parasitic field-oxide transistors. Trapped positive charge in these oxides causes the threshold voltage of n-channel gate and parasitic field oxide transistors to shift toward depletion mode. Large shifts in threshold voltage will cause excessive leakage current to flow from the drain to source of n-channel gate-oxide transistors and can also cause leakage between transistors [1], [2]. In fact, radiation-induced increases in this leakage current limits the radiation hardness of most commercial integrated circuits (ICs). This phase of the test procedure requires an irradiation at 24±6°C to a specified dose at a dose rate of 50 to 300 rads(SiO_2)/s followed by a room temperature electrical test (24±6°C). The irradiation and electrical testing is done at 24±6°C because radiation effects have been shown to be temperature sensitive [3]–[10]. However, as discussed below, because of this temperature sensitivity electrical characterization testing should also be performed at the temperature extremes of the system environment. During irradiation the devices must be biased using the worst-case bias configuration. This is the bias condition the induces the most radiation induced damage in the device. Worst-case bias conditions are technology dependent and are discussed in detail later in this section. Between irradiation levels, all pins of the device should be shorted together to reduce annealing effects. The time from the end of an irradiation to the start of electrical testing shall not exceed 1 hour and the start of the next irradiation level must take place within 2 hours of the end of the prior irradiation.

It is important to point out that for some devices in a very low dose rate environment, the first phase of TM 1019 is known to be overly conservative and thus the method allows one to perform extended room temperature anneals to better estimate the performance of devices at low dose rates [11]–[13]. These types of anneals are allowed only for parametric failure (parameters that exceed their specification limit) and not for functional failure. Room temperature anneals are usually effective for devices whose parametric degradation is associated with the buildup of oxide-trapped charge and for devices with fast annealing rates. TM 1019 limits the time for room temperature anneals to the maximum time calculated by dividing the total ionizing dose specification for the devices by the maximum dose

rate for the intended use.

In some cases, a second phase (rebound test) of TM 1019 is required. The second phase consists of an additional irradiation equal to 50% of the specified dose, followed by a 168-hour anneal at 100°C under worst-case bias conditions. The additional irradiation is required because of uncertainties in defining the worst-case bias conditions to use during irradiation and anneal [11], [13], [14]. In addition, this overtest is large enough to account for the observed increase in transistor threshold voltage for transistors irradiated at elevated temperatures as opposed to transistors irradiated at room temperature and annealed at 100°C for one week [15]. Typically, irradiations and anneals are performed under static bias conditions, and do not account for the possibility of enhanced rebound voltages often observed during switched-bias or AC irradiations [5], [16]–[18]. After the 1-week anneal, the devices should again be characterized at room temperature. This phase of the test method is used to bound the degradation that is associated with the buildup of interface-trap charge by maximizing the buildup of interface-trap charge while simultaneously annealing a large amount of oxide-trapped charge. It is a conservative test for parametric or functional failures due to the long-term buildup of interface traps [7], [11]. At the present time, this test is only applied to MOS-like technologies that could exhibit time-dependent effects (TDE), e.g., trapped-hole annealing and interface-trap buildup, over long time periods. A device intended for space application must pass both phases of TM 1019.

BS 22900 has a similar test flow to that of TM 1019. However, there are a few important differences. During the first phase of the test procedure, the irradiations specified by BS 22900 are performed in a range of dose-rate windows, i.e., either between 1 to 10 rads(SiO_2)/s or 0.01 to 0.1 rads(SiO_2)/s at a temperature of 20$\pm$10°C with parts biased using worst-case bias conditions. Note that both test methods permit testing to be performed at the dose rate of the intended application if agreed to by the customer. During the second phase of the test procedure, no additional irradiation is required, only biased anneals. The anneals consist of a 24-hour anneal at room temperature followed by a 168-hour anneal at 100°C. Similar to TM 1019, these anneals are used in an effort to account for time-dependent effects in the space environment. The reason no additional dose is required as part of the second phase of BS 22900 is because BS 22900 seeks to accurately identify worst-case conditions during a required evaluation test, which is used during the qualification testing. Electrical testing is performed before and after the irradiations and after the room/elevated temperature anneals at room temperature. A more detailed description of the test philosophy, similarities, and differences between TM 1019 and BS 22900 are given in Ref. [19].

The main test flows of TM 1019 and BS 22900 define test procedures for MOS devices that provide significant insight into device behavior in low-dose-rate space environments. These test procedures were actually developed based on our fundamental understanding of the mechanisms that control radiation effects (as discovered primarily in the 80s). However, the 90s led to the discovery of a few new radiation effects phenomena that are not addressed by the main test flow. These include ELDRS in bipolar linear devices and preirradiation elevated temperature effects observed in both MOS and bipolar devices. While the mechanisms that control these effects are not fully understood, there is enough knowledge about the mechanisms to define hardness assurance test procedures, which can assess the impact of these effects. In fact, modifications have been made to TM 1019 to address these relatively new radiation effects. These modifications will be discussed next. In addition, there are a number of issues that can affect the reliability of hardness assurance tests that need to be considered when qualifying devices in space radiation environments. These include selecting the optimum laboratory radiation source, determining worst-case bias conditions, and understanding the implication of characterization temperature. These issues will also be reviewed.

B. Enhanced low-dose-rate sensitivity

Since the early 1990s, it has been known that some types of bipolar devices exhibit enhanced low-dose-rate sensitivity (ELDRS) at low electric fields [21]–[27]. This means that the amount of total dose degradation in bipolar transistors and ICs that is observed at a given total dose is greater at low dose rates than at high dose rates. Note that ELDRS is more than a simple time dependent effect as often observed for MOSFETs. In ELDRS

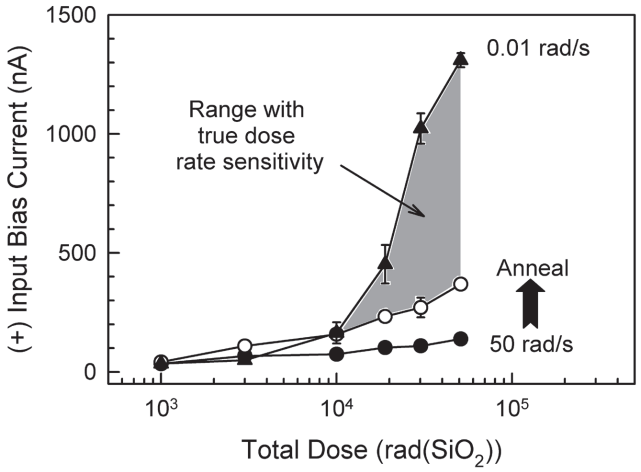

Fig. 2. I_{B+} versus total dose for LM111s subjected to a 175°C, 300-hr preirradiation elevated temperature stress. The devices were irradiated at 0.01 (triangles) and 50 rad(SiO_2)/s (circles) with all pins shorted. Following the 50 rad(SiO_2)/s irradiation, the devices were annealed at room temperature with all pins shorted for a time equivalent to the low dose rate irradiation (open circles). (After [20].)

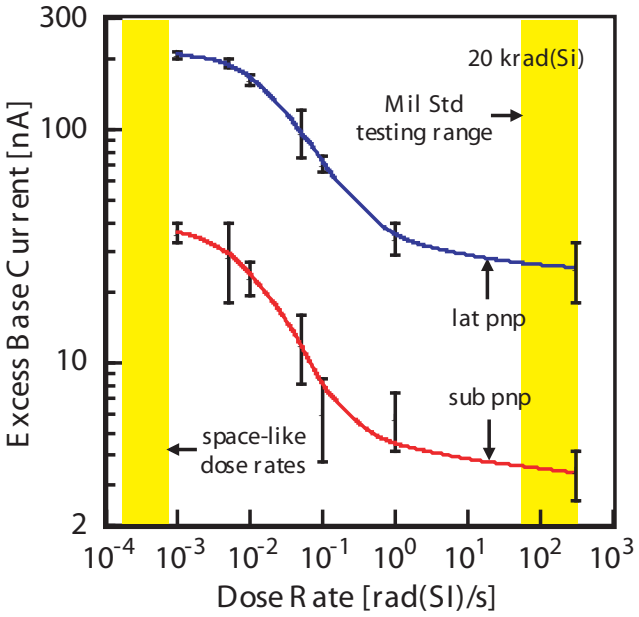

Fig. 3. Effect of dose rate on excess base current in the lateral and substrate PNP bipolar transistors. All data were measured at V_{EB} = 0.7 V. (After [31].)

devices, degradation at low-dose rates can be significantly more than at high-dose rates even after taking differences in the time of the irradiations into account, i.e., ELDRS is a "true" dose-rate effect. (This is discussed in more detail below.) In general, total ionizing dose degradation in bipolar devices results from the buildup of radiation-induced charge in the field oxides used to isolate the base and emitter contacts and the creation of recombination centers at the Si/SiO_2 interface. ELDRS in NPN transistors has been attributed primarily to increased positive oxide-trap charge buildup in the isolation oxide overlying the base-emitter junction [27], [28]. This charge enhances the surface recombination rate in the p-base region. On the other hand, lateral and substrate PNP transistors are primarily affected by increased interface-trap charge buildup in the thick isolation oxide over the emitter-base region [26], [29]. In most cases, ELDRS effects have been shown to be more important for lateral or substrate PNP transistors than for NPN transistors [24]. In fact, Johnston and co-workers [24] showed that the relative damage at low dose rates (< 0.01 rad(SiO_2)/s) for junction-isolated linear processes could be greater than a factor of two larger in linear bipolar circuits dominated by PNP transistor response than in those dominated by NPN transistor response. A data compendium of bipolar linear circuits that exhibit ELDRS can be found in Ref. [30].

ELDRS is illustrated in Figure 2, which is a plot of the input bias current (I_{B+}) for LM111 voltage comparators versus total dose for dose rates of 50 and 0.01 rad(SiO_2)/s [20]. The voltage comparators were irradiated and annealed with all pins shorted. As observed in Figure 2, voltage comparators irradiated at low-dose rates have a much larger increase in input bias current than voltage comparators irradiated at high-dose rates with a room temperature anneal for an equivalent time to the low-dose-rate irradiation time for the same total dose. At dose levels up to 10 rad(SiO_2), there are no "true" dose-rate effects. However, for higher total dose levels, the high-dose-rate irradiation plus room temperature anneal does not degrade I_{B+} nearly as much as the low-dose-rate irradiation. Thus, the difference observed at the higher total dose level (shaded region in the figure) can be attributed to "true" dose-rate effects. This ELDRS effect can cause failure of ICs in satellite environments not observed in standard laboratory testing. As such, ELDRS severely complicates hardness assurance testing for space environments.

Developing an accelerated hardness assurance test method to estimate the "true" low-dose-rate effects in bipolar devices remains a very challenging

issue facing the radiation effects community [32], [33]. Unfortunately, high-dose-rate irradiation followed by room temperature annealing, which can often accurately estimate the radiation response of CMOS devices at low dose rates [7], [8], does not accurately estimate the low-dose-rate response of many types of bipolar devices [20], [21], [25]. CMOS devices generally exhibit time-dependent effects rather than "true" dose-rate effects. Time-dependent effects can also exist in bipolar devices and must not be confused with true dose-rate effects. "True" dose-rate effects make it difficult to develop quick and accurate total-dose hardness assurance test methods for predicting the radiation response of bipolar devices. Currently, the most promising rapid screen involves the use of elevated temperature irradiations at relatively low dose rates ($\leq$1 rad(SiO_2)/s) [34]–[36]. However, the optimum irradiation temperature for this procedure varies from technology to technology [30], [35], does not always bound the low-dose-rate response, and the required dose rate is significantly lower than the current dose rate range (50 to 300 rad(SiO_2)/s) normally used for qualifying CMOS technologies. In addition, it has recently been suggested that if the radiation-induced charge that is responsible for ELDRS (whether it be interface or border traps) can anneal at 100°C, then elevated temperature irradiations may also cause some annealing of radiation-induced charge [37]. This is consistent with previous data on MOS devices that show some interface-trap annealing at radiation temperatures above 90°C [38]. These data help explain why high-dose-rate irradiations at elevated temperatures, in some cases, underestimate low-dose-rate degradation. Whether this occurs likely depends on the rate-limiting mechanisms of hydrogen interactions (i.e., passivation and depassivation of interface traps) at the silicon/silicon dioxide interface [39]. As a result, manufacturers do not have a reliable laboratory test guideline for timely assessment of the radiation hardness of their bipolar technologies. Nevertheless, irradiating at elevated temperature is allowed by TM 1019 if characterization testing shows that this procedure can bound the low-dose rate induced degradation for bipolar, BiCMOS, or mixed-signal devices. Without prior characterization testing, the only test procedure for ELDRS that is currently allowed by TM 1019, requires that parts be irradiated at dose rates of $\leq$ 10 mrad(SiO_2)/s. For most devices the amount of enhanced degradation has been observed to saturate at these dose rates. This is shown in Figure 3 [31]. This figure shows the effect of dose rate on excess base current in lateral and substrate PNP bipolar transistors. The amount of degradation for both lateral PNP and substrate PNP transistors begins to saturate at dose rates below approximately 10 mrad(SiO_2)/s. Of course, there are always exceptions to this general observation. Johnston et al. [34] showed enhanced degradation between 5 mrad(SiO_2)/s and 2 mrad(SiO_2)/s for a LM324 op-amp manufactured by Motorola. However, this is the only known part to exhibit this behavior.

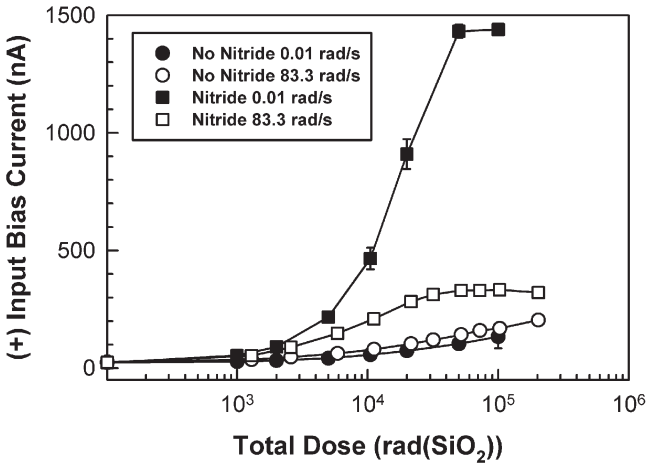

Fig. 4. I_{B+} versus total dose for LM111s with and without the nitride passivation layer removed, irradiated at 0.01 or 83.3 rad(SiO_2)/s with all pins shorted. (After [40].)

On a positive note, researchers have recently shown that by changing the final chip passivation layers it is possible to significantly reduce or eliminate ELDRS in some bipolar linear technologies [40]–[43]. It has been shown that devices fabricated without passivation layers do not exhibit ELDRS or pre-irradiation elevated temperature stress (PETS) sensitivity (discussed in detail next), while devices from the same production lot fabricated with other passivation layers are ELDRS and PETS sensitive. It has also been shown that removing the passivation layers on devices that exhibit ELDRS could mitigate ELDRS and PETS effects, as illustrated in Figure 4 [40]. While this is obviously not a practical solution to the ELDRS and PETS problems for ICs to be used in space systems, it does appear to indicate that ELDRS and PETS effects are probably

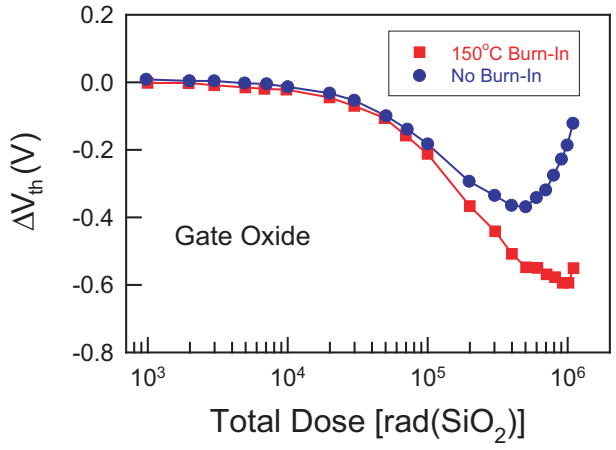

Fig. 5. Threshold-voltage shift versus total dose for gate oxide n-channel transistors with and without a PETS irradiated with a 10 keV x-ray source with a 5 V gate-to-source bias. The PETS was for one week at a temperature of 150°C. (After [47].)

not intrinsic to many bipolar process technologies prior to deposition of the final passivation layer. In addition, ELDRS and PETS effects do not appear to be inherently related to circuit design or layout, but are related to mechanical stress effects, hydrogen in the device, or a combination of the two. It appears that mechanical stress induced by the passivation layers might play a critical role in determining the radiation response of bipolar linear ICs. Passivation layers can easily alter mechanical stress in the die. The introduction of thermal cycles and moisture after fabrication have been shown to further impact the film stress [44], [45]. These two facts are consistent with both changes in radiation response between unpassivated and passivated devices at high-dose rates, and the observation of PETS sensitivity in passivated devices. These results suggest that proper engineering of the final chip passivation layer might eliminate ELDRS and PETS effects in bipolar integrated circuits. In addition, it has recently been shown that hydrogen introduced during the packaging cycle can have an impact on the radiation response of bipolar linear devices that exhibit ELDRS [46]. As a result, it is recommended that all hardness assurance testing be conducted on devices in their final package configuration.

C. Preirradiation elevated temperature stress (burn-in) effect

ICs are exposed to numerous thermal cycles (e.g., during packaging, reliability testing, system assembly and system use) during their life time and prior to their exposure to radiation. It has been shown that these preirradiation elevated temperature stresses (PETS) can dramatically change the total dose radiation response of both MOS [47]–[50] and bipolar [51], [52] devices. Examples of the effects of preirradiation elevated temperature anneals are shown in Figures 5 and 6 [47], which are plots of the threshold-voltage shift for MOS gate-oxide (Figure 5) and field-oxide (Figure 6) transistors versus total dose. Transistors with and without a preirradiation 150°C, one-week anneal (typical burn-in conditions) were irradiated with 10-keV x rays with a 5-V gate-to-source bias. At the higher radiation levels, both the gate-oxide and field-oxide threshold-voltage shifts were larger for the transistors subjected to the preirradiation elevated temperature anneal. The larger threshold-voltage shifts for the transistors subjected to a preirradiation anneal could be due to either an increase in radiation-induced oxide-trap charge, a decrease in interface-trap charge, or both. Based on charge-separation measurements [47], [48], it was shown that for these devices the major cause for the larger threshold-voltage shifts for the devices subjected to a preirradiation anneal was less radiation-induced interface-trap buildup in gate oxides and more radiation-induced oxide-trapped charge buildup in field oxides. These changes in radiation-induced charge buildup have been shown to lead to larger increases in IC static power supply leakage current during irradiation, and to a lesser degree increases in timing parameters. The functionality of the devices can also be impacted. In addition, It has been shown that some linear bipolar technologies are also sensitive to PETS [51], [52]. The mechanisms for the PETS effect for linear bipolar technologies appear to be qualitatively similar to those for CMOS technologies.

Note that not all technologies exhibit a PETS effect. However, for those technologies that do, the magnitude of the PETS effect can be affected by the time and temperature of the preirradiation elevated temperature stress but appears to be independent of the PETS bias condition [48]. The effects of time are

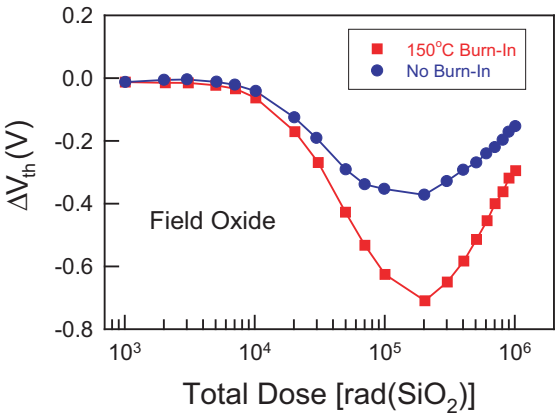

Fig. 6. Threshold-voltage shift versus total dose for field oxide n-channel transistors with and without a PETS irradiated with a 10-keV x-ray source with a 5-V gate-to-source bias. The PETS was for one week at a temperature of 150°C. (After [47].)

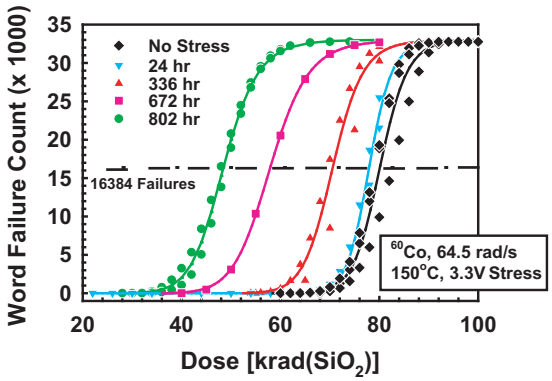

Fig. 7. Increase in the word failure count for a checkerboard pattern written to 3.3-V Paradigm SRAMs versus dose for SRAMs with no pre-irradiation stress or various pre-irradiation stresses up to 35 days at 150°C. (After [49].)

illustrated in Figure 7 for 3.3-V Paradigm SRAMs [49]. Figure 7 is a plot of the increase in word (or byte) failure count as a function of total dose for a complement checkerboard pattern written to the SRAMs. Data for SRAMs with no stress or a 24-, 336-, 672-, and 802-hour pre-irradiation 150°C stress with nominal values of V_{DD} applied during the elevated temperature biased stress are shown. The SRAMs were irradiated using a Co-60 source in steps up to 100 krad(SiO_2) at a dose rate of 64.5 rad(SiO_2)/s. As the pre-irradiation stress time increases, the word failure count curves shift to lower doses. These data suggest that the PETS effect

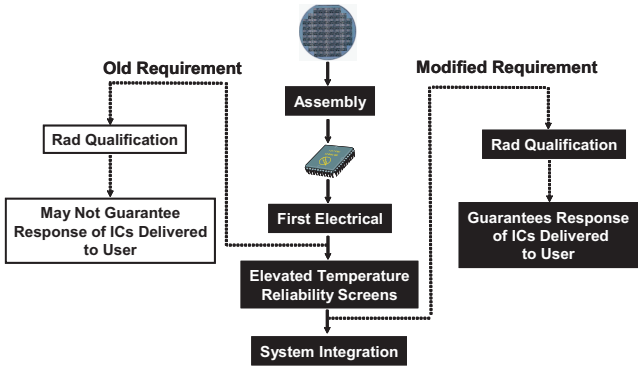

Fig. 8. Modifications made to MIL-STD-883, TM 1019 to account for PETS effects. (After [49].)

is associated with a thermally activated process. It has been found that the activation energy is 0.38 eV [48]. This activation energy is close to the activation energy of 0.41 eV for trapped hole compensation [7] and the activation energy of 0.45 eV for the diffusion of molecular hydrogen in bulk fused silica [53]. The latter suggests that the PETS effect may be related to the diffusion of molecular hydrogen. The lack of a strong bias dependence is consistent with this mechanism. The preirradiation stress could also affect the spatial and energy distribution of hole-trap precursors in the oxide (this may also involve the diffusion of hydrogen related species), leading to differences in trapped-hole distributions following irradiation. Clearly, more work needs to be performed to conclusively identify the mechanisms for the PETS effect.

The effect of preirradiation elevated temperature stresses on IC radiation response is clearly a concern for hardness assurance testing. The U. S. military test guideline TM 1019 has been modified to address PETS effects as illustrated in Figure 8. Before the modification, the test guideline permitted manufacturers to qualify the total-dose radiation response prior to elevated temperature reliability screens. This raised the possibility that the total-dose radiation response of ICs sensitive to PETS effects could be significantly different than the radiation response of ICs used for qualification testing. Thus, TM 1019 was modified to require manufacturers to perform radiation qualification testing on ICs after burn-in. Unless it has been shown by prior characterization or by design that burn-in has negligible effect on total dose radiation-induced degradation, radiation testing must be performed after subjecting parts

to burn-in or the manufacturer must develop a correction factor that accounts for changes in total dose response resulting from subjecting product to burn-in. While these changes to TM 1019 are a step in the right direction, they may underestimate the radiation response of PETS sensitive devices at the end-of-life of system use [49]. As noted above, the PETS effect appears to be associated with a thermally activated process. Thus, as PETS sensitive devices continue to be exposed to thermal cycles during system assembly, one would expect that the total dose response of the devices could continue to degrade. Thus, the estimated degradation measured on devices after burn-in, as required by TM 1019, may not be a conservative estimate of the worst-case degradation observed at the end-of-life. To determine the response of PETS sensitive devices at the end of life, one would need to account for all thermal cycles that the device is exposed to after burn-in, including thermal cycles that the devices are exposed to during system assembly and use [49]. Otherwise, the amount of radiation-induced degradation may be severely underestimated.

D. Optimum laboratory radiation sources for hardness assurance testing

Total-dose degradation of electronic devices used in space is caused primarily by exposure to high fluences of electrons and protons. However, Co-60 gamma and x-ray sources are more cost effective for routine evaluation of the radiation hardness of electronic devices for these applications. In this section, we will review which of these two sources are best suited for simulating energetic electrons or protons. X-ray sources can operate at higher dose rates than most Co-60 sources and can be used to irradiate individual die at the wafer level. Because of these properties, x-ray sources are often used for process development and control [54], while Co-60 gamma sources are normally used for hardness assurance testing [55]. The justification for using Co-60 gamma sources for hardness assurance testing is based primarily on historical practice rather than on technical grounds. Some work has been performed comparing the differences in total-dose degradation for x-ray and Co-60 irradiations. In some cases, good correlation between Co-60 and x-ray radiation-induced degradation was observed [56]; however, in other cases large differences were observed [13], [57]. Thus, it is important to determine which radiation source is best suited for simulating energetic electrons or protons. Recent work [58] comparing the radiation-induced response of pMOSFET dosimeters showed that the radiation-induced response for high-energy protons (60 to 200 MeV) was only 65-85% of the Co-60 radiation-induced response. This result raises concern that Co-60 radiation sources may not be the best radiation source for simulating device response in proton-rich space environments.

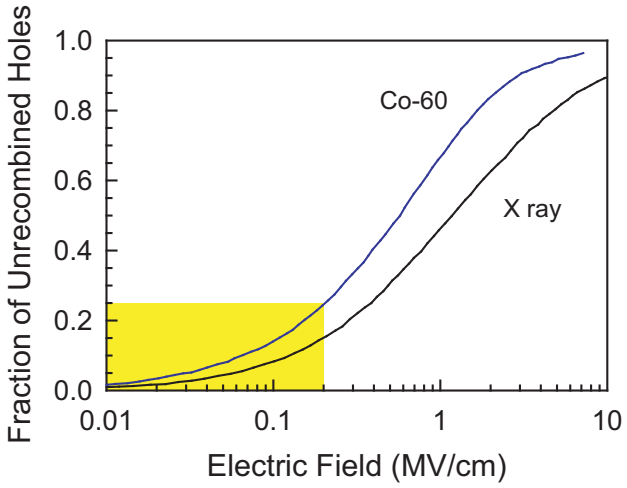

Fig. 9. Fraction of holes that escape recombination for 10-keV x-ray and Co-60 irradiations as a function of oxide field. (After [59].)

To understand why there might be differences in the radiation-induced degradation in devices irradiated with Co-60 or x-ray irradiation, one must examine the differences in charge yield between the sources. If an electric field exists across the oxide of an MOS transistor, once released, electrons in the conduction band and holes in the valence band will immediately begin to transport in opposite directions. Electrons are extremely mobile in silicon dioxide and are normally swept out of the silicon dioxide in picoseconds [60], [61]. However, even before the electrons can leave the oxide, some fraction of the electrons will recombine with holes in the oxide valence band. This is referred to as initial recombination. The fraction of holes that do not recombine is referred to as the charge yield. The amount of initial recombination is highly dependent on the electric field in the oxide and the energy and type of incident particle [59], [62]. In general, strongly ionizing particles form dense columns of

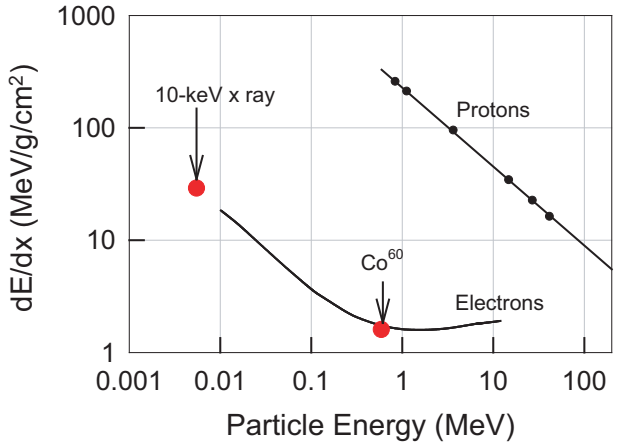

Fig. 10. Stopping power versus particle energy for electrons and protons. Also shown are the average stopping powers for secondary electrons emitted by 10-keV x rays and 1.2-MeV gamma rays. (After [63].)

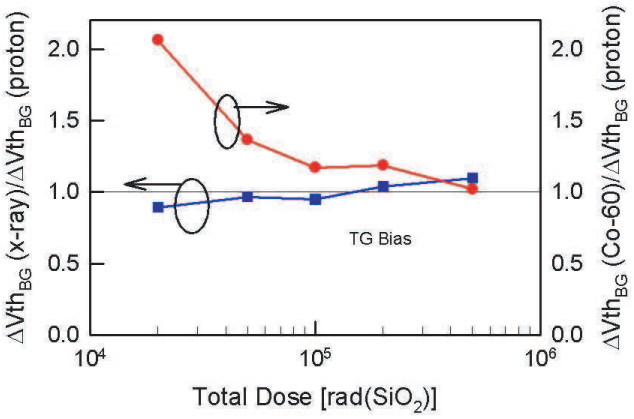

Fig. 11. Ratio of x-ray to 41.4-MeV proton and Co-60 gamma to 41.4-MeV proton radiation-induced back-gate threshold-voltage shifts as a function of total dose for SOI transistors. Transistors were irradiated with either a 0 V or TG bias configuration. (After Ref. [67])

charge where the recombination rate is relatively high. On the other hand, weakly ionizing particles generate relatively isolated charge pairs, and the recombination rate is lower [62]. Figure 9 is a plot of the fraction of unrecombined holes (charge yield) versus electric field for Co-60 and x-ray irradiations [59]. The plot shows that there can be significant differences in the charge yield between the two sources. In fact, at low fields the relative difference can be very large (>50%). Thus, the laboratory radiation source, x-ray or Co-60, that best matches proton or electron radiation-induced degradation in space may depend on which source gives the best match in charge yield.

Unfortunately, there is presently limited data in the literature for the charge yield of electrons and protons for the energy range of these particles in space [64]. To gain insight into which laboratory radiation source gives the best match in charge yield to electrons and protons, one can examine the stopping power for electrons and protons in SiO_2. Figure 10 is a plot of the stopping power in SiO_2 for electrons and protons versus particle energy [63]. The energy range shown for protons and electrons covers that typically found in space [65]. Also shown in the figure are the calculated average values of stopping power for secondary electrons generated by 10-keV x rays and 1.25-MeV Co-60 gamma rays. These values are based on calculations using the Sandia radiation transport code CEPXS/ONELD [66]. The interaction of a 10-keV photon and a 1.25-MeV photon with a thin layer of SiO_2 produces a secondary electron spectrum with an average energy of 5.5 keV and 590 keV, respectively. The stopping power of the electrons generated by a 10-keV photon more closely matches the stopping power of the lower energy protons (20 to 60 MeV) than the stopping power of electrons generated by a 1.25-MeV photon. On the other hand, the stopping power of the electrons generated by a Co-60 photon more closely matches the stopping power of the electrons in space (up to 7 MeV) [65].

As a result, we can expect that for low energy protons, the charge yield of the protons is more closely matched by the charge yield of the secondary electrons generated by a 10-keV photon (x-ray) than the secondary electrons generated by a 1.25-MeV photon (Co-60 gamma). This suggests that, at least for lower energy protons, a 10-keV x-ray source may better simulate the radiation-induced degradation caused by protons than a Co-60 radiation source. This was indeed found to be the case [67]. Figure 11 shows the ratio of the back-gate transistor threshold-voltage shift for x-ray and proton irradiations and the ratio for Co-60 gamma and proton irradiations for SOI transistors irradiated in the 0 V and transmission-gate (TG) bias configurations. The x-ray and proton data were taken at a dose rate of 270 rad(SiO_2)/s and the Co-60 gamma data were taken at a dose rate of 50 rad(SiO_2)/s. X-ray data taken at 270 and 50

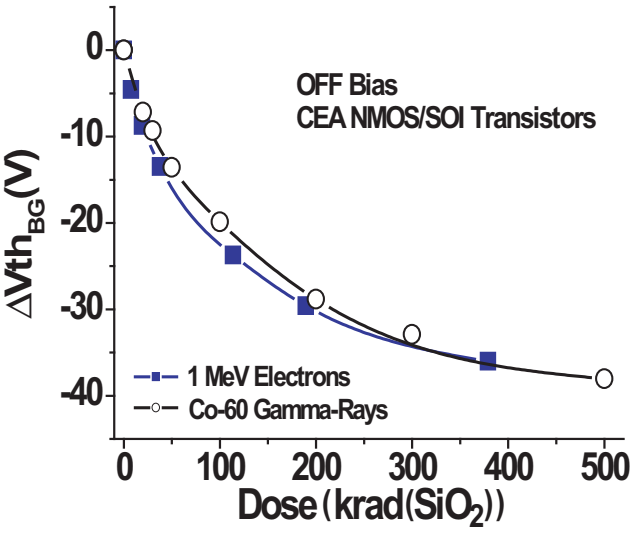

Fig. 12. Back-gate transistor threshold voltage shift versus total dose for CEA SOI transistors irradiated with Co-60 gamma rays and 1-MeV electrons with the OFF bias configuration. (After [64].)

rad(SiO_2)/s showed no noticeable differences in back-gate threshold-voltage shift for the different dose rates for devices irradiated to total doses up to 500 krad(SiO_2). Hence, the fact that the data were taken at somewhat different dose rates should not affect the conclusions. Within experimental uncertainties, the x-ray and proton radiation-induced back-gate threshold-voltage shifts are nearly equal for all total dose levels and bias conditions examined. However, the ratio of Co-60 gamma and proton back-gate threshold shifts varies widely, especially for low total doses. The fact that there is agreement in the back-gate threshold-voltage shifts at high total doses is not surprising. At this point, the threshold-voltage shift is significant and therefore the internal field in the oxide is also significant. Thus, a low field condition in the oxide is no longer satisfied. Note that this is due to the size of the threshold voltage shift in these devices, not the total dose. Devices that shift more or less with dose will therefore reach this point at different dose levels. For this proton energy, these total dose levels, and these devices, x-ray irradiations simulate proton radiation-induced degradation much better than Co-60 gamma irradiations. Good correlation between x-ray and proton radiation-induced degradation has been observed for proton energies between 20 and 200 MeV and also in the radiation-induced degradation of field oxides in bulk-silicon technologies [67].

The flux of electrons and protons in space varies widely with orbit altitude and inclination. For example, for low earth orbits (especially for orbits passing through the South Atlantic Anomaly), the proton flux can be very high compared to the electron flux. In contrast, for higher orbits, the proton flux can be very low in comparison to the electron flux [65]. Based on the results of Schwank et al. [67], for SOI and bulk-silicon transistors, laboratory x-ray irradiations may more closely simulate proton-rich environments such as low-earth orbits (at least in the energy range of 20 to 200 MeV) than laboratory Co-60 gamma irradiations. This contradicts the commonly accepted tenet that Co-60 gamma sources should be used for all hardness assurance qualification. As previously discussed, the better match between x-ray and proton radiation-induced damage is likely due to a closer match of the initial charge yield at low electric fields. However, this does not preclude the use of Co-60 gamma radiation sources for device qualification in proton-rich environments. Co-60 gamma radiation sources may overestimate the total dose degradation and, therefore, are a more conservative radiation source. In contrast, we note from Figure 10 that Co-60 gamma irradiation more closely matches the stopping power (and hence, the charge yield) of electrons than x-ray irradiation. Thus, to simulate total dose degradation in electron-rich environments such as geosynchronous orbits, Co-60 gamma sources are probably still the optimum laboratory radiation source for device qualification, as shown in Figure 12 [64]. Figure 12 is a plot of the back-gate threshold voltage shift versus total dose for transistors irradiated to total doses up to 500 krad(SiO_2) with Co-60 gamma rays and 1 MeV electrons in the OFF bias configuration. The 1-MeV electron data are in very good agreement with the Co-60 data; the differences are within experimental uncertainties due to errors in dosimetry or to part-to-part variations. This observation is consistent with the similarity observed between the charge yield of Co-60 gammas and 1-MeV electrons in thermal gate oxides as discussed above.

E. Worst-case bias

The worst-case radiation and anneal bias conditions for ICs should be determined through an analysis of the system application and characterization testing. As will be discussed below, the

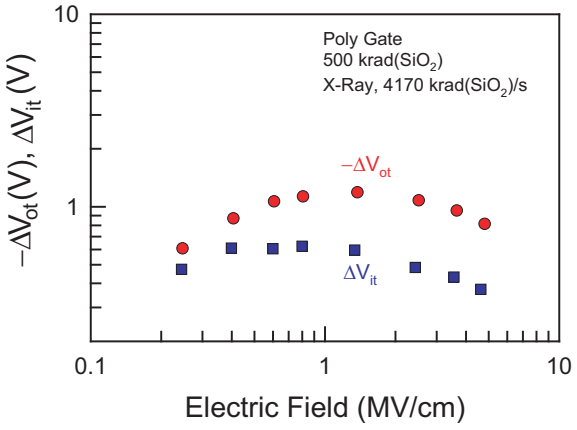

Fig. 13. Voltage shift due to oxide and interface-trap charge versus electric field for n-channel transistors irradiated to 500 krad(SiO_2). (After [68].)

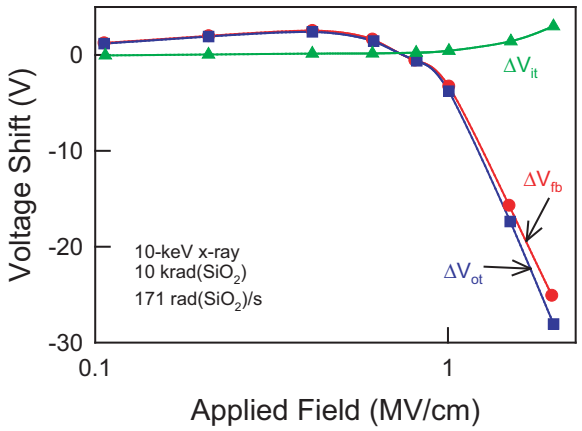

Fig. 14. Flatband voltage shift and the threshold-voltage shift due to oxide and interface-trap charge versus applied field during x-ray irradiation for capacitors fabricated using a traditional field oxide insulator as the gate dielectric. (After [2].)

worst-case bias condition will depend on the failure mechanism(s), which can vary as a function of circuit parameters, dose rate, and temperature. As a result, characterization testing should be done over the full range of system operating conditions.

1) Si bulk devices: It is well known that bias conditions can have a large effect on the amount of radiation-induced degradation. For gate oxides, the maximum threshold-voltage shift for oxide-trap and interface-trap charge occurs at intermediate values of electric field. This is illustrated in Figure 13, which is a plot of the measured radiation induced voltage shift due to oxide and interface-trap charge for polysilicon gate transistors irradiated to 500 krad(SiO_2) [68]. At high electric fields, the threshold-voltage shifts due to oxide-trap and interface-trap charge decrease with increasing electric field strength because the capture cross section for holes decreases with increasing electric field [69]–[73]. At low electric fields, the threshold-voltage shifts due to oxide-trap and interface-trap charge are small because the number of radiation-induced electron/hole pairs which escape initial recombination (charge yield) is small (see Figure 9). Thus, the maximum threshold-voltage shifts due to oxide-trap and interface-trap charge occur at moderate electric fields (1 to 2 MV/cm).

For advanced IC technologies with very thin gate oxides (<10 nm), radiation-induced oxide-trapped charge buildup in field oxides and in SOI buried oxides normally dominates the radiation-induced degradation of ICs. The worst-case bias for parasitic field oxide leakage current is the highest operating voltage of the technology. The worst-case bias condition for radiation-induced charge buildup in field oxides is the bias condition that maximizes the electric field across the field oxide. This is clearly shown in Figure 14, which is a plot of the flatband, oxide-trap charge, and interface-trap charge voltage shifts versus applied field for capacitors irradiated with 10-keV x rays to a total dose of 10 krad(SiO_2) [2]. The capacitors were fabricated using a traditional field oxide as the gate dielectric. The dielectric was deposited using a traditional shallow-trench isolation (STI) process. For these bias and irradiation conditions, there is no significant buildup of interface-trap charge in the field oxide. However, at high electric fields, there is a very large radiation-induced buildup of oxide-trapped charge, which causes a very large threshold-voltage shift of the field oxide transistor. After irradiation, the threshold-voltage shift was greater than 25 V for electric fields greater than 2 MV/cm. Depending on the initial threshold voltage of the field oxide transistor, this radiation-induced threshold-voltage shift may be large enough to cause large increases in transistor leakage current.

While the electric field across the majority of field oxides are generally very low for most advanced technologies having operating voltages less than 5 V, this is not the case for all areas of the field oxides. For example, very high electric fields can

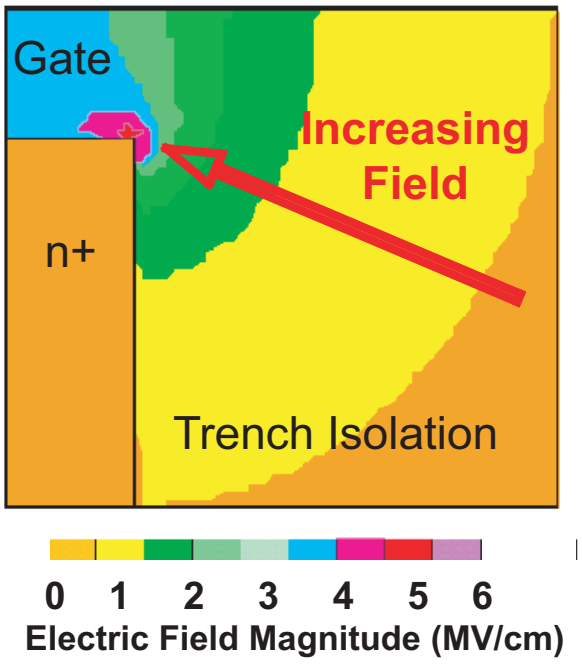

Fig. 15. The cross sections illustrate the electric field magnitude near the corner of the shallow-trench isolation for the case in which the trench insulator is planar with the 13-nm gate oxide. Electrostatic potential in the trench region was simulated with the polysilicon gate that extends over the STI (not shown) biased at 5 V and all other regions grounded. (After [2].)

occur at the corners of STI oxides, as illustrated in Figure 15 [2]. In this figure, simulations show that the electric field can be as high as ∼6 MV/cm at the Si corner of the n+ region (source/drain region of an n-channel gate oxide transistor). Although the electric field decreases rapidly with distance from the trench corner (down the trench sidewall or into the trench region), the electric field still remains relatively high (>1 MV/cm) for the first 20 nm. Thus, the bias condition that will result in the maximum electric field across the STI is the bias condition that gives the maximum voltage drop between the gate and the substrate. This bias condition is normally the ON bias condition, where the gate is at the bias supply voltage, V_{DD}, and the source, drain, and substrate are grounded. Although these results were demonstrated for STI, similar results are obtained for ICs with LOCOS isolation.

Conceptually, selecting a worst-case bias for bulk-silicon ICs can be difficult because the worst-case bias for gate and field oxides may be different. However, for advanced technologies where the irradiation response is dominated by radiation-induced parasitic leakage current, the optimum worst-case bias for an IC is that which maximizes parasitic field oxide leakage, i.e., the maximum operating voltage. Ideally, an IC should be irradiated in the state that produces the most radiation-induced degradation and the IC should be tested post-irradiation in the condition that shows the most electrical degradation. For example, a transistor can be irradiated in the ON state to produce the largest radiation-induced leakage current and measured in its lowest current state (the OFF state), which will show the largest increase in leakage current. Similarly, to observe the largest increase in current in an SRAM, one often irradiates the IC in a checkerboard pattern and then measures the IC leakage current post-irradiation in the complement checkerboard pattern [47], [54], [74].

2) SOI devices: Worst case bias conditions for SOI devices can be more difficult to determine than for bulk Si devices. For SOI devices, the radiation response is controlled by charge buildup in the SOI buried oxides in addition to charge buildup in the gate and field oxides. Similar to field oxides as discussed above, the buildup of radiation-induced charge in SOI buried oxides is dominated by positive oxide-trapped charge. Therefore, the electric field condition that results in the maximum back-gate threshold-voltage shift in an SOI transistor is the bias condition that causes the most radiation-induced hole trapping near the back Si/SiO_2 interface. This will be the bias condition that results in the maximum electric field strength in the buried oxide underneath the channel region. For typical gate lengths and buried oxide thicknesses, the bias condition that produces the largest electric fields underneath the channel and the most hole trapping is the transmission gate bias configuration for partially-depleted transistors. The transmission gate (TG) bias configuration is defined as source and drain biased at V_{DD}, while the gate and body contacts (if available) are grounded. Simulations and data [75] have also shown that the OFF bias condition (drain at V_{DD} and all other contacts grounded) can result in very large back-gate threshold-voltage shifts. The bias configuration that results in the largest back-gate threshold-voltage shifts depends on the ratio of the transistor gate length and the buried oxide thickness [75]. These simulations have been experimentally verified [57], [75], [76]. Figure 16 is a plot of the measured back-gate threshold-voltage shifts versus gate length

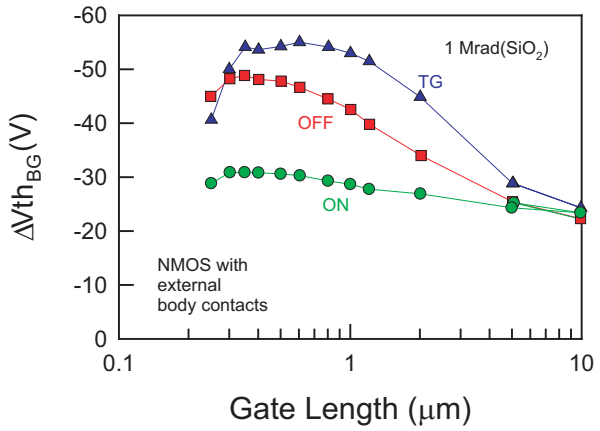

Fig. 16. Back-gate threshold-voltage shift versus gate length for an n-channel SOI transistor irradiated with x rays to a total dose of 1 Mrad(SiO_2). Transistors were biased in the ON, OFF, and TG bias configurations. (After [75].)

for partially-depleted n-channel SOI transistors irradiated with 10-keV x rays to a total dose of 1 Mrad(SiO_2) [75]. The buried oxide thickness was 413 nm. The largest back-gate threshold-voltage shifts observed were in transistors irradiated in the TG bias configuration. However, for transistors with gate lengths near the standard technology gate length of 0.25 μm, the back-gate threshold-voltage shifts were approximately the same for transistors irradiated in the TG and OFF bias configurations. The smallest back-gate threshold-voltage shifts were for transistors irradiated in the ON bias configuration. These results for the worst-case bias configuration for partially-depleted SOI transistors are just the opposite of that for the worst-case bias configuration for radiation-induced charge buildup in field oxides discussed above.

For fully-depleted SOI transistors, the worst-case bias is not as well defined as for partially-depleted SOI transistors. Similar to the case for partially-depleted SOI transistors, Jenkins and Liu [77] showed that for some SOI technologies, the worst-case bias for radiation-induced charge trapping in the buried oxide was the transmission gate bias configuration. However, for other technologies, the worst-case bias was determined to be the ON bias configuration [78].

Because the worst-case bias configuration for radiation-induced charge buildup in field oxides and SOI buried oxides may be different, hardness assurance testing of SOI devices can be difficult. Both parasitic field oxide leakage and transistor leakage induced by radiation-induced charge trapping in the buried oxide can be very large. Thus, both must be accounted for. This is especially important when estimating IC hardness from transistor testing. Both radiation-induced field oxide and buried oxide leakage will contribute to the leakage current of gate-oxide transistors. Radiation-induced field oxide leakage will also contribute to the leakage current of the back-gate transistor. To ensure worst-case conditions are satisfied, SOI transistors should be irradiated in the ON and TG or OFF bias configurations. For ICs, the different worst-case bias configuration is less problematic. For instance, regardless of the input bias conditions, in an SRAM approximately half of the transistors will be irradiated in the ON bias configuration and the other half will be irradiated in the OFF bias configuration. Some transistors will also be irradiated in the TG bias configuration. Therefore, worst-case bias conditions in an SRAM are automatically probed using standard input bias conditions. However, for SOI circuit types where the number of OFF (or TG) and ON biased transistors can be considerably different, ICs may require testing in multiple bias configurations to ensure worst-case conditions are satisfied.

3) Bipolar devices: In contrast to MOS devices in which the worst-case bias condition is typically a DC bias condition at the maximum operating voltage of the device, the worst-case bias condition for some bipolar devices can actually occur at low electric fields. Specifically, this applies to bipolar devices that exhibit ELDRS, where the amount of degradation was observed to be maximum at low bias levels (i.e., all pins grounded) [27]. The worst-case bias condition for a bipolar IC that exhibits ELDRS will depend on the circuit parameter that is most sensitive to low-dose-rate irradiation. In general, the worst-case bias condition for changes in input bias current of a bipolar linear IC is all pins grounded; whereas the worst-case bias condition for changes in offset voltage is for devices biased in a DC bias condition. While these are general observations, it is a good practice to do characterization testing to determine the worst-case radiation bias conditions for ICs before performing qualification testing.

F. Implication of characterization temperature

ICs are often required to operate over a wide range of temperatures in many system applications. For example, military hardened devices are often specified to operate from -55°C to 125°C, whereas COTS devices might be required to operate over a smaller temperature range, e.g., -40°C to 85°C. It is well known that device characteristics are impacted by operation temperature. Whatever the temperature range specified, manufacturers typically guarantee that their devices will operate within limits specified in the product specification over this temperature range. The manufacturer establishes these limits by routinely characterizing devices as a function of temperature before irradiation. However, the same device characteristics affected by operation temperature (e.g., threshold voltages, leakage currents, and carrier mobilities) are also affected by ionizing radiation. [54], [74], [79]–[82]. Unfortunately, because the annealing of radiation induced oxide-trapped charge can be enhanced by increasing temperature [3]–[8], the current total ionizing dose test guidelines (TM 1019 and BS 22900) require devices to be kept at room temperature during irradiation and pre- and post-irradiation electrical characterization to minimize temperature-induced annealing effects. Because of this, the radiation response of devices are often not characterized over the full system temperature range. However, it has recently been shown that by not characterizing the radiation response of devices over the full system temperature range, the total-dose hardness of some devices can be overestimated [83].

This is illustrated in Figure 17, where large increases in static power supply current (I_{DD}) with temperature were observed for 1M (128k×8) CMOS SRAMs fabricated by Cypress Semiconductor. These SRAMs were fabricated using a 0.25-μm 5-V bulk silicon technology with a 6-transistor cell design. Figure 17 is a plot of I_{DD} versus temperature for the SRAMs irradiated with 95-MeV protons at TRIUMF [84] at a dose rate of ∼14 rad(SiO_2)/s. The devices were irradiated at 25°C with V_{DD} = 5 V and characterized at 25°C and 80°C. SRAMs were first irradiated to a given total dose and then characterized at room temperature and then at elevated temperature. After the elevated temperature characterizations, the SRAMs were cooled to room temperature and then irradiated with protons to a higher total dose level. As is evident from the figure, increasing the measurement temperature resulted in an increase in post-irradiation I_{DD}. For example, at a total dose of 72 krad(SiO_2) the leakage current measured at 25°C was 2.5 mA and at 80°C was 5.1 mA. In addition to an increase in leakage current, increasing the measurement temperature also caused the SRAMs to functionally fail at lower total dose levels. At the highest total dose level investigated, 161 krad(SiO_2), the SRAMs were still functional when characterized at 25°C. However, when the SRAMs were characterized at 80°C they failed functionally at total dose levels above 72 krad(SiO_2). These results show the impact of characterization temperature on SRAM parametric and functional performance.

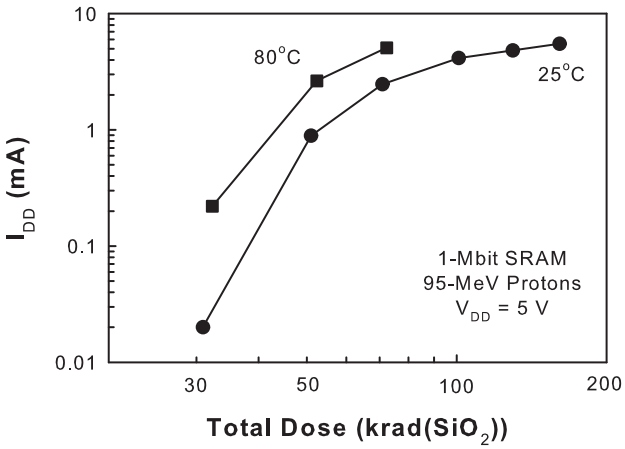

Fig. 17. Static supply leakage current versus temperature for 1-Mbit SRAMs irradiated with 95-MeV protons at a dose rate of 17 rad(SiO_2)/s at room temperature (25°C) with V_{DD} = 5 V and characterized at room temperature and 80°C. (After [83].)

Ref. [83] also showed that transistors and a mixed-signal ASIC could exhibit significantly more post-irradiation parametric degradation when characterized at elevated temperatures. The results suggest that if elevated temperature operation is required for system application, it is imperative that devices be characterized at elevated temperatures, as well as at lower temperatures. The data of Figure 17 demonstrate a case where elevated temperature characterization caused increased parametric degradation and functional failure at lower total dose levels than room temperature characterization. It is possible that for other device types and/or technologies that enhanced parametric degradation and functional

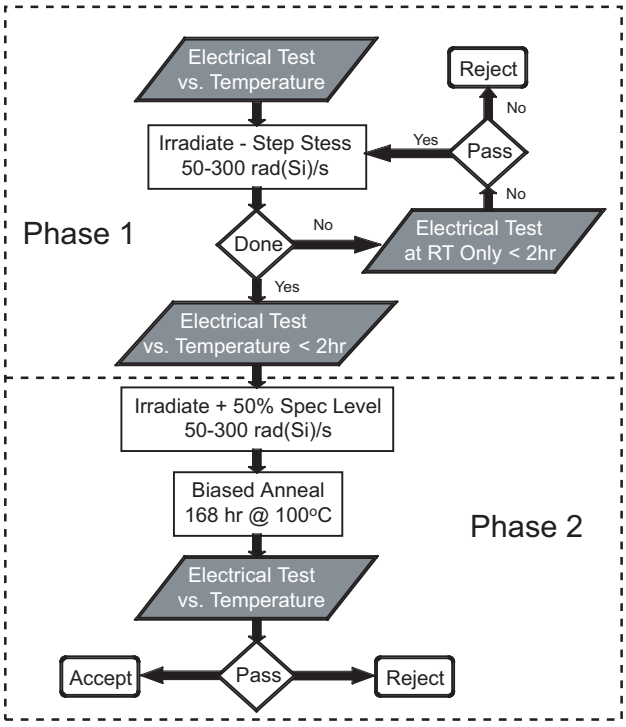

Fig. 18. Technique for integrating post irradiation temperature effects in a hardness assurance plan based on TM 1019. The shaded boxes highlight steps in the test procedure that could be modified to ensure device hardness over the system temperature range. (After [83].)

failure could be observed at cold temperatures. As a result, to ensure system functionality, it is essential that devices be characterized over the the full system temperature range pre- and post-irradiation.

We now illustrate how characterization tests over the temperature range of the system can be incorporated into TM 1019 (similar changes could be made to BS 22900). Figure 18 is a flow diagram based on TM 1019. We have added steps to the flow diagram that could be used to ensure device hardness over the system temperature range. The devices should be characterized at room temperature and at the low and high temperature extremes of the system environment before irradiation. All devices should then be irradiated to the total dose specifications at a dose rate between 50 and 300 rad(SiO_2)/s, followed by electrical testing (Phase 1). If this is a step stress irradiation, the electrical testing should be done only at room temperature between each irradiation step. This is to ensure that minimal annealing of oxide-trapped charge occurs during the step stress.

Minimization of elevated temperature annealing can be very important to ensure that test Method 1019 remains conservative. It has been shown that the annealing rate (or neutralization) of oxide trapped charge can increase with temperature for some technologies [7], [8], [12], [85]. In addition, the buildup of interface traps also depends on temperature [9], [10]. Thus, because the purpose of Phase 1 of TM 1019 is to bound the degradation that is associated with the buildup of oxide-trapped charge, the most conservative approach to hardness assurance testing is to not increase the temperature until after the completion of the irradiation sequence, unless it is known via characterization testing that the annealing of oxide-trapped charge and the buildup of interface-trap charge is insignificant for the parts being characterized. After the final total dose exposure of Phase 1, the devices should be characterized at room temperature and at the low and high temperature extremes. Note that the sequence for testing should be started at low or room temperature and end at high temperature. Again this will reduce the amount of oxide-trapped charge annealing that might occur. For high temperatures above 100°C, there is a possibility that some annealing of interface-trap charge might also occur [3]–[6]. However, the amount of annealing (if any) will be related to the amount of time that the devices are at temperatures above 100°C. Thus, this time should be minimized.

Phase 2 of Method 1019 then requires a 50% overtest, followed by a 168 hour, 100°C biased anneal. As such, any annealing of oxide-trapped charge that occurred during the last high temperature electrical test that was part of Phase 1 will have no negative impact on Phase 2 results. After the 1-week anneal, the devices should again be characterized at room temperature and at the low and high temperature extremes.

Using this revised hardness assurance test method we can better ensure that ICs will operate over the specified system temperature range in a given radiation environment. This is a more comprehensive test procedure compared to irradiating and testing devices only at room temperature. However, this test procedure does not take into account the fact that in an actual system application a device could also be irradiated at any temperature within the system environment specification. The effect of irradiating at a temperature other than room temperature and subsequently characterizing over the entire operating temperature range was not investigated in [83].

Thus, more work needs to done to fully investigate these effects to determine if the revised test method will bound the worst-case irradiation response of devices irradiated and operated over the entire specified temperature range, which should be the main objective of any test method. As is the case with the current test method, this revised test method may be overly conservative for predicting the radiation response of devices for some scenarios; however, it is impossible to develop a generic test method that is not overly conservative for some scenarios while still bounding the worst-case radiation response for devices that are specified to operate in a radiation environment over a wide range of temperatures (i.e., -55°C to 125°C) and dose rates.

The above discussion applies primarily to ICs with MOS elements. However, many bipolar devices are used in both space and weapons applications. Total dose radiation-induced degradation in these devices can also be attributed to the buildup of both oxide- and interface-trap charge in isolation oxides over the base-emitter junctions [28], [36] and emitter-base regions [29], [51]. Thus, it is not difficult to imagine that the radiation-induced degradation of bipolar devices can also be enhanced by testing at extreme temperatures. However, additional investigations will need to be conducted to determine if and to what extent the combined environment (radiation and temperature) will impact the radiation response of these device types. Until additional tests can be performed, it is recommended that bipolar devices also be characterized over the expected application temperature range after irradiation. Of course, as discussed above, this should be done at the end of the irradiation cycles to minimize annealing effects.

III. Emerging SEE hardness assurance issues

The harsh environments of space can induce single-event effects (SEE) in ICs. Both heavy ions and protons can cause SEE. Heavy ions induce SEE primarily by depositing charge by direct ionization along the path of the ions. Proton-induced SEE can be much more complex. The linear energy transfer (LET) of protons is not high enough to cause SEEs by direct ionization in most devices. Instead, protons induce SEE by generating secondary particles with much higher LETs, but with relatively low energies. Also, the secondary particles produced by proton-material interactions can be emitted in any direction (i.e., in general, they do not follow the path of the proton). These properties can lead to complex mechanisms for proton SEE and make hardness assurance testing difficult.

There are a number of documents available in the U.S. on single event effects (SEE) testing. These include JEDEC Solid State Technology Association and ASTM (American Society for Testing and Materials) documents. JESD57 covers test procedures for the measurement of single-event effects in semiconductor devices from heavy-ion irradiation, JESD89 covers the measurement of alpha particle and terrestrial cosmic ray-induced soft errors in semiconductor devices, and ASTM F1192 covers standard guidelines for the measurement of single-event phenomena (SEP) induced by heavy-ion irradiation of semiconductor devices. These documents do a good job at defining the required procedures to follow for SEE testing. However, there have been a number of emerging issues relevant to SEE device qualification that are not covered in these documents. Specifically, these include proton energy and angular dependence of single event latchup (SEL), the impact of total dose on single-event upset (SEU), and issues associated with high versus low energy heavy-ion testing. In the following sections, these issues will be reviewed and the hardness assurance implications will be addressed.

A. Single event latchup

One of the most problematic single-event effects is single-event latchup (SEL) [87]. When a latchup occurs, the latchup state can be cleared only by removing power from the device. SEL can also lead to destructive IC failure. Thus, it is critical that hardness assurance tests for SEL be capable of accurately determining IC susceptibility to single-event latchup. The effects of bias and temperature on proton and heavy-ion induced SEL have been explored in detail [86]–[90]. Based on these works, it is known that the worst-case bias condition and temperature for both heavy-ion and proton-induced SEL are maximum power supply voltage and maximum system temperature. This is illustrated in Figures 19 and 20. Figure 19 is a plot of the SEL cross section versus bias voltage for 4M SRAMs with a nominal operating voltage of 3.3 V irradiated with

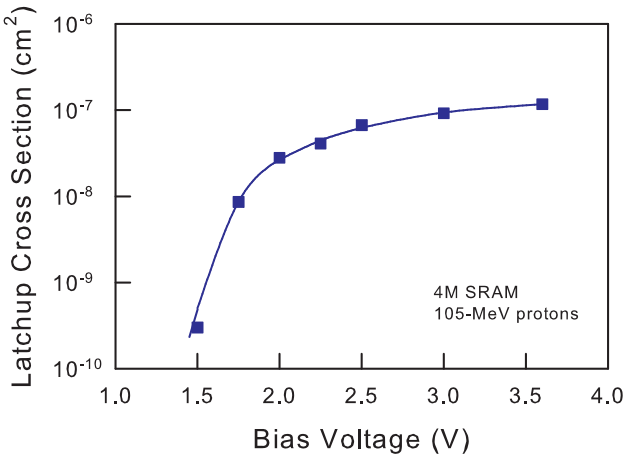

Fig. 19. SEL cross section versus bias voltage for SRAMs irradiated with 105-MeV protons.

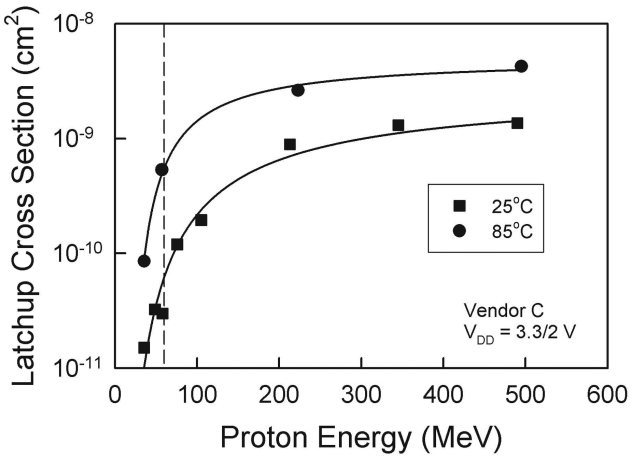

Fig. 20. SEL cross section versus proton energy for SRAMs characterized at temperatures of 25 and 85°C. (After [86].)

105-MeV protons. As the voltage is increased from 1.5 V to 3.6 V, there is approximately a three orders of magnitude increase in the latchup cross section. Figure 20 is a plot of the latchup cross section for SRAMs measured at 25°C (room temperature) and at 85°C. For these SRAMs, the SEL maximum cross section is much higher at 85°C than at 25°C (three to four times higher at the highest proton energy).

More recently, it has been shown that the probability of observing SEL during proton SEE testing can be a strong function of the proton energy used for testing [86]. This is clearly illustrated in Figure 21 [86]. Figure 21 is a plot of the SEL cross section as a function of proton energy for SRAMs manufactured by different commercial vendors measured at 85°C. As illustrated in the figure, the SEL

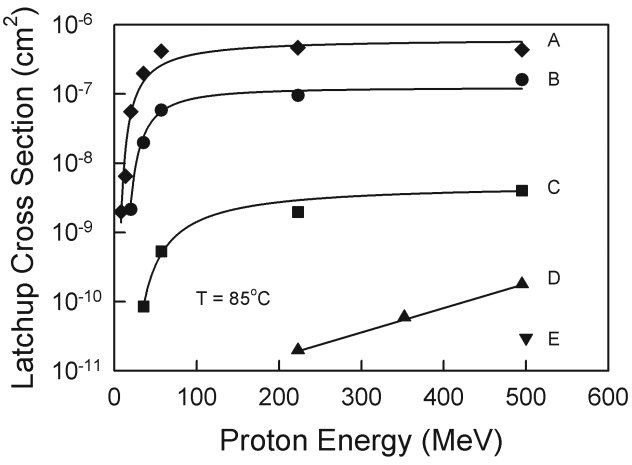

Fig. 21. Latchup cross section versus proton energy for five different SRAMs. SEL measurements were taken at a temperature of 85°C. (After [86].)

threshold and cross section is a strong function of the proton energy and can vary significantly between devices, ranging from SRAMs with low SEL thresholds and high cross sections to SRAMs with high SEL thresholds and low cross sections. In fact for vendor D and E SRAMs, the minimum proton energy required to observe SEL was 225 MeV and 495 MeV, respectively. These proton energies are higher than the energies available at many proton test facilities (typically between 60 and 200 MeV) used in the past to evaluate the SEL response of ICs. However, trapped protons in Earths radiation belts can have energies as high as 400 MeV [65] and galactic protons can have energies as high as 1 GeV. Thus, for systems where latchups cannot be tolerated, latchup testing should be performed using protons with energies at least equal to the maximum proton energy of the system environment. Although the proton fluence levels required to observe latchup in vendor D and E SRAMs would be much higher than obtainable in most systems, if many of these SRAMs were used in a system, in aggregate, the total cross section would be much higher and could result in realistic latchup probabilities for some space environments [91]. Conclusively excluding the possibility of latchup in such systems would require irradiating SRAMs to still higher fluence levels, probably necessitating the characterization of many SRAMs to avoid total dose damage of individual SRAMs.

These results strongly suggest that proton SEL hardness assurance testing should be performed at

the maximum proton energy of the system environment. If no proton test facilities are available with proton energies at least equal to the maximum proton energy of the system environment, SEL testing can be done using heavy ions with LETs greater than those expected from nuclear recoils generated by proton interactions. Remember that protons induce single-event effects through the generation of secondary particles with much higher LETs than those of the protons themselves. The maximum LET of secondary particles generated by proton-silicon interactions is approximately 11 MeV-cm^2/mg [92]. However, nuclear scattering cross section calculations for proton collisions with three high-Z materials (Cu, Ti, and W) common in many present-day high-density ICs show that secondary particles have a maximum LET of approximately 34 MeV-cm^2/mg for 500 MeV protons [86]. These data would suggest that if no SELs can be induced by heavy ions with LETs above ~40 MeV-cm^2/mg, no SELs should be observed in a proton environment. Of course, as new high-Z materials are incorporated into technologies, nuclear scattering cross section calculations will need to be updated to ensure that no secondary particles with higher LETs can be generated.

Another parameter that can greatly impact proton SEE hardness assurance testing is angle of incidence. The effect of angle of incidence on SEL cross section is illustrated in Figure 22, which is a plot of the SEL cross section versus proton energy for SRAMs irradiated at a temperature of 75°C at angles of incidence of 0 (normal angle) and 85 (grazing angle) degrees [93]. At each proton energy, the SEL cross section is larger for an angle of incidence of 85 degrees than for 0 degrees. This difference in SEL cross section between 0 and 85 degrees varies with proton energy. The difference in SEL cross section between low and high angles could easily affect the probability for detecting a latchup. Based on nuclear scattering calculations combined with 3-D device simulations, it has been suggested that the mechanism for the effect of angle of incidence on SEL hardness is a consequence of the LET and range distributions of secondary ions produced by proton-material interactions, coupled with an increase in SEL sensitivity (decrease in LET threshold) as angle of incidence is increased [93].

These results clearly show that proton-induced SEL hardness assurance testing should be performed

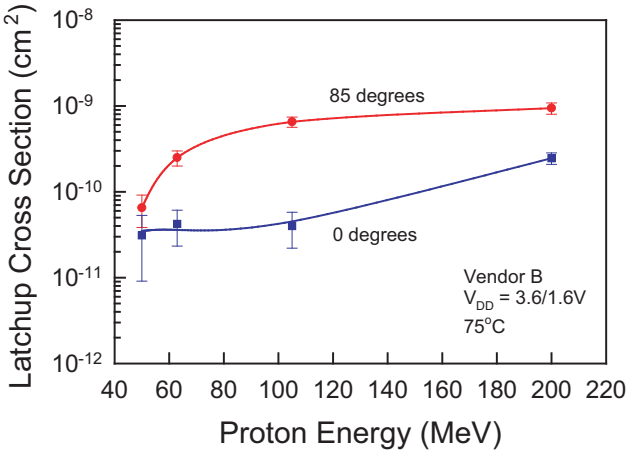

Fig. 22. Latchup cross section versus proton energy for SRAMs characterized at 75°C at angles of incidence of 0 and 85 degrees. (After [93].)

using the maximum power supply voltage, maximum proton energy of expected environment, maximum system temperature, and at grazing angle. Because of practical concerns of proton energy loss as protons transport through the sides of packages, system boards, etc., it is recommended that testing be performed at both grazing and normal angles of incidence. In general, proton-induced latchups due to high-LET secondary particles are rare events (i.e., have low cross sections), and therefore proton SEL hardness assurance test decisions should be made bearing overall system reliability requirements in mind. Hardness assurance decisions should take into account issues such as the flux of high-energy protons in the system environment and the probability of SEL that can be tolerated.

B. Impact of total dose on SEU

It has been shown that the SEU sensitivity of some devices can degrade be exposing them to total ionizing dose [94]–[99]. This is illustrated in Figure 23 [94], which is a plot of the SEU cross section for 4M SRAMs irradiated with 35.4-MeV protons versus total dose. The cross section was determined from the incremental number of errors divided by the incremental fluence at each radiation level. These results show that the proton-induced SEU hardness of ICs can be significantly affected by total dose. For the total dose range examined, the upset cross section increases exponentially with total dose. The cross section increased

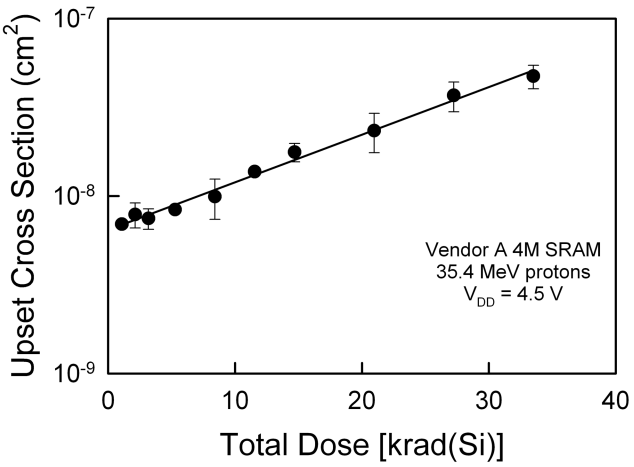

Fig. 23. Upset cross section versus total dose for 4M SRAMs. The devices were irradiated with 35.4-MeV protons with V_{DD} = 4.5 V. (After [94].)

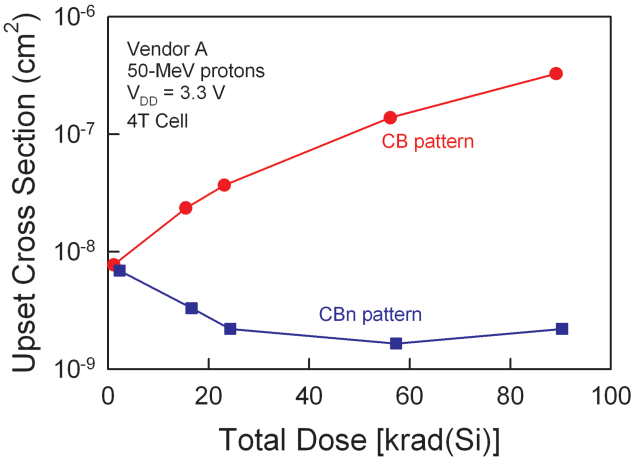

Fig. 24. Upset cross section versus total dose for commercial 4-Mbit SRAMs. The devices were irradiated with 50-MeV protons with V_{DD} = 3.3-V in a checkerboard pattern and characterized in either a checkerboard or checkerboard complement pattern. (After [99].)

from 7.9×10^{-9} cm^2 at a total dose of 1.1 krad(SiO_2) to 4.7×10^{-8} cm^2 at a total dose of 35.5 krad(SiO_2).

For older technologies with relatively thick oxides, the observed increased SEU sensitivity has been attributed to ionizing radiation-induced imbalances in the threshold voltages of the transistors within the memory cell [97]. The magnitude of the radiation-induced threshold voltage shifts can be considerably different for ON and OFF biased transistors, leading to large imbalances in the threshold voltages. This mechanism is not expected to be a major problem for most present-day technologies that have very thin gate oxides where there should be no significant amount of radiation-induced charge buildup in these oxides. For these technologies (specifically for SRAMs), it has been suggested that the enhanced SEU sensitivity with total dose is consistent with radiation-induced currents originating in the memory cells affecting the output bias levels of bias level shift circuitry used to control the voltage levels to the memory cells and/or due to the lowering of the noise margin of individual memory cells caused by radiation-induced leakage currents [94]. In addition, all SRAMs that showed an enhanced SEU sensitivity, also showed a radiation-induced increase in the static power supply leakage current [99]. Thus, it may be possible to screen SRAMs for enhanced SEU sensitivity with total dose by monitoring changes in the static power supply leakage current with radiation. For other device types, the optimum parameter that needs to be monitored with irradiation may be different than the static power supply leakage current.

This correlation of total dose degradation to SEU sensitivity has important implications for space applications where the total dose is due to either electrons or protons. From a hardness assurance perspective, it is important that devices that exhibit this type of enhanced SEU sensitivity with ionizing dose be SEU characterized at the maximum total dose level expected during mission lifetime.

The first step in a hardness assurance test program should be to determine via characterization testing whether or not a device exhibits a correlation of total dose degradation to SEU sensitivity. To determine this, total-dose irradiations can be performed by irradiating devices using Co-60 gamma rays, x rays, electrons, or protons prior to proton or heavy-ion SEU testing. If protons are used, care should be taken to ensure that the proton energy is below the SEU proton threshold for the devices to prevent the devices from changing bias states. It has been shown that the SEU sensitivity will depend on the irradiation bias configuration [99]. For example, the worst-case response for an SRAM could be with the device irradiated and characterized with the same pattern written to the memory array or with the devices irradiated with one pattern and characterized with the complement pattern. This is illustrated in Figure 24 [99]. This figure is a plot of the SEU cross section versus total dose for commercial SRAMs. All total-dose irradiations were performed with a checkerboard pattern written to the memory

array. The SEU cross section was measured with either a checkerboard or checkerboard complement pattern. The data show that the effect of total dose on SEU cross section depends strongly on the pattern written to the memory array during irradiation and SEU measurement. For these devices and test conditions, the memory pattern written to the memory array made more than two orders of magnitude difference in cross section at the highest total dose level. In addition, the time between total-dose irradiation and SEU characterization should be kept as short as possible to minimize possible room temperature annealing effects. (For some SRAMs [99], the mechanism for the total dose sensitivity has been related to radiation-induced increases in static power supply leakage current. Hence, because of annealing effects, for the SRAMs tested in [99], the most conservative test will be that which minimizes the time between total dose irradiation and SEU characterization, i.e., maximizes static power supply leakage current.) For proton SEU characterizations, total-dose irradiating devices with protons can easily meet this condition. For heavy-ion SEU characterizations, this condition may be difficult to meet for heavy-ion facilities without available total-dose facilities. During the SEU characterization phase, if the SEU sensitivity of a device is found to be total dose sensitive, it will be necessary to evaluate the SEU response of the device after exposure to ionizing irradiation to the maximum total dose levels of the system application.

If hardness assurance qualification needs to be done on devices that show increased SEU sensitivity with ionizing dose, the irradiations prior to SEU characterization should be conducted using the irradiation conditions that bound the total dose degradation expected in the system environment. This can be done by following the basic principles of TM 1019 (see section 2.1). As specified by the first phase of TM 1019, the devices could be irradiated using worst-case bias conditions to the maximum total dose at a moderate dose rate of 50 to 300 rad(SiO_2)/s. Of course this part of TM 1019 is a conservative test for parametric or functional failure due to radiation-induced oxide-trapped charge buildup, which can induce increases in static power supply leakage current. As such, this phase of the test will bound the radiation-induced increase in static power supply leakage current at moderate- to low-dose rates. However, as indicated above, this phase of TM-1019 is known to be overly conservative for estimating the response of the device and thus the method allows one to perform extended room temperature anneals to better estimate the parametric performance of devices at low-dose rates [11]–[13]. The time for room temperature anneals are limited to the maximum time calculated by dividing the total ionizing dose specification for the devices by the maximum dose rate for the intended use. Following the room temperature anneals, the SEU response of the device can then be evaluated.

Extreme caution must be used if devices are subjected to the second phase of TM 1019 (rebound test) prior to SEU characterization. While there may be some device types that have a total dose sensitivity due to variations in interface-trap buildup affecting SEU hardness, to date, the total dose sensitivity for present-day SRAMs has been related to increases in static power supply leakage current. For MOS devices, increases in static power supply leakage current are due to radiation-induced increases in oxide-trapped charge. The part of TM 1019 which bounds the degradation due to the radiation-induced buildup of oxide-trapped charge is phase one. The elevated temperature anneals associated with phase two can significantly over anneal the amount of oxide-trapped charge and hence, greatly underestimate the increase in radiation-induced power supply leakage current even at low dose rates. Therefore, unless it is known that the total dose sensitivity is due to the radiation-induced buildup of interface traps, it is highly recommended that devices be subjected only to phase one of TM 1019 prior to SEU characterization.

A second option is to just irradiate the devices using the worst-case bias condition at low-dose rate before SEU characterization. While the exact rate to use is not known, a reasonable dose rate might be less than or equal to 10 mrad(SiO_2)/s. This is the dose rate required to test bipolar devices that might have ELDRS. While there are currently no data available on the impact of total dose on the SEU sensitivity of bipolar devices, it is known that the enhanced degradation (due to ELDRS) appears to saturate at dose rates of below approximately 10 mrad(SiO_2)/s [31]. For MOS devices, this dose rate also seems reasonable. It is still significantly higher than the rate expected for most space applications and if increases in static power supply currents are observed at these dose rates, they will

most likely exist at even lower dose rates.

C. High vs low energy heavy ion testing

Heavy-ion testing at accelerator facilities is frequently used to study mechanisms of single-event effects (SEE), estimate on-orbit error rates, and qualify parts for use in space-based systems. Most facilities used for such SEE testing provide particles whose energies are on the order of a few (1-10) MeV per nucleon (or equivalently, MeV/amu). Unfortunately, heavy-ion energies in the actual space environment are considerably higher, reaching hundreds of GeV/amu with a peak flux at a few hundred MeV/amu [100]. The lack of accelerators capable of providing such relativistic ions has raised concerns about the fidelity of accelerator-based tests for simulating the response of parts to the real high-energy ion environment found in space [101]. Studies have in some cases shown differences in single-event upset (SEU) response with ion energy [102]–[104], while in other cases little difference has been seen [105]–[107].

Recently, an additional concern regarding high-energy heavy ions has been raised, namely, that of nuclear interactions between high-energy ions and the materials in integrated circuits [106], [108]–[110]. Typically, SEUs due to heavy ions are assumed to result from direct ionization caused by the release of electron-hole pairs along the path of an energetic charged particle incident on a device or integrated circuit (IC). This is in contrast to proton and neutron SEU, where upsets are attributed to ionization by reaction products (e.g., spallation products and Si recoils) produced indirectly by nuclear interactions between an incident energetic particle and the materials in the IC. In [106], Koga theorized that for heavy ions with very low LET (< 1 MeV-cm^2/mg), upsets caused by nuclear interactions might be observable if the threshold LET for upsets caused by direct ionization was high (for example, as would be the case for SEU-hardened SRAMs). Recent experiments [108] on hardened 4-Mbit SRAMs support this mechanism, with high-energy heavy-ion upsets observed for LETs less than 2 MeV-cm^2/mg in an SRAM that otherwise appears to have a primary upset threshold LET of greater than 20 MeV-cm^2/mg. While the SEU cross section for this mechanism is very low ($< 10^{-13}$ cm^2/bit), it has been predicted that this mechanism could still be a significant contributor to on-orbit error rates [111].

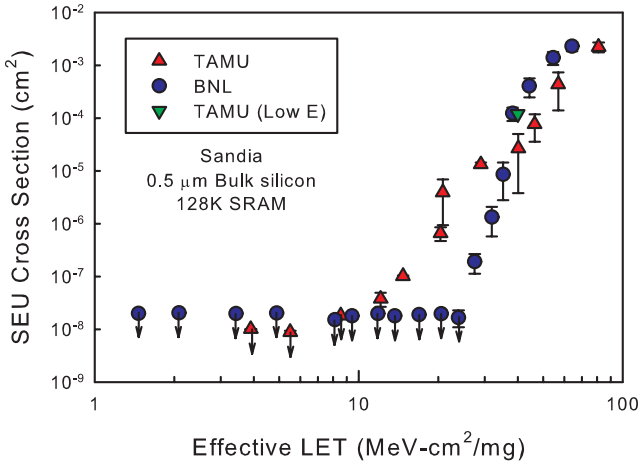

Fig. 25. Measured SEU cross section for 128-Kbit Sandia SRAMs taken with low-energy (BNL) and high-energy (TAMU) heavy ions.(After [110].)

Figure 25 shows the results of recent low- and high-energy SEU characterization of a bulk silicon 128-Kbit radiation-hardened SRAM [110]. Data were taken using low-energy ($\sim$1-10 MeV/amu) ions at Brookhaven National Laboratory (BNL) and high-energy (15-40 MeV/amu) ions at Texas A&M University (TAMU). Data points with a downward-pointing arrow indicate the upper bounds on the SEU cross section for LETs at which no upsets were actually observed. The SEU threshold LET of these SRAMs measured using standard low-energy ions is $\sim$28 MeV-cm^2/mg. In tests at BNL, no upsets were observed below an LET of $\sim$28 MeV-cm^2/mg, including repeated irradiations at an LET of 24 MeV-cm^2/mg with a cumulative fluence for all parts tested in excess of 2×10^8 ions/cm^2. These low-energy data indicate that if nuclear reaction-induced upsets in this technology exist, their cross section is less than 5×10^{-9} cm^2 at LETs less than 27.5 MeV-cm^2/mg. However, SEU data taken at TAMU indicate upsets still occur in these SRAMs with high-energy ions down to an LET of 12 MeV-cm^2/mg. In fact, at an LET of 12 MeV-cm^2/mg the high-energy SEU cross section is $\sim4\times10^{-8}$ cm^2, nearly a factor of ten higher than the *upper bound* for the low-energy SEU cross section at *twice* this LET! At an LET of 20 MeV-cm^2/mg, the high-energy SEU cross section is two orders of magnitude higher than the low-energy upper bound.

For LETs below the direct ionization upset

threshold region, it appears that at least in some cases high-energy ions can lead to higher cross sections than low-energy ions [108], [110]. This increase in SEU cross sections may be attributable to nuclear reaction-induced upsets, however, we cannot rule out the possibility that ion track structure plays a role. In general, it appears that ion energy effects will be very difficult to observe in commercial (SEU-soft) devices [106], [108]. Even in hardened devices, testing must be performed with very high fluences (we suggest $\geq 5\times10^7$ ions/cm^2) of heavy ions to observe this mechanism. Similarly, some evidence exists to support the occurrence of nuclear reaction-induced SEL from high-energy heavy ions in commercial (non-hardened) SRAMs [110]. Further tests are required to definitively prove the mechanisms for nuclear reaction-induced heavy ion SEU and SEL, and that such anomalies are not simply due to unexpected design sensitivities or ion beam contamination [106].

If it can be conclusively shown that differences in SEE response with ion energy are indeed due to secondary particles, many of our existing concepts for understanding and analyzing SEE must be called into question. For example, the usefulness of the primary incident particle LET as a parameter against which SEU cross sections are plotted will be dramatically reduced. Because upsets may be caused by secondary particles with higher LET than the primary incident ion, plotting such secondary particle upsets against the incident ion LET is largely meaningless. In addition, the concept of effective LET will break down as secondary particles don't follow an inverse cosine law based on the angle of incidence of the primary particle. Finally, many error rate prediction methods are implicitly based on charge deposition along path lengths of a primary ionizing particle passing through a sensitive volume. New methods based on an understanding of nuclear reaction cross sections will be required for cases where such reactions are important [109]. Testing at energies both above and below that required for nuclear reactions will likely be required to further refine these models [109].

Of course, one must consider whether such small upset or latchup cross sections contribute significantly to the overall on-orbit radiation-induced failure rates of ICs. For soft commercial devices we may expect direct ionization-induced SEU to dominate failure rates, however the situation is less clear for radiation-hardened devices that otherwise have low radiation-induced failure rates, and for SEL in commercial SRAMs that can often have higher threshold LETs for SEL than for SEU [86]. Detailed error rate analyses including the effects of nuclear interactions are necessary to accurately determine the significance of such effects. In addition, for systems utilizing a very large number of ICs, it should be remembered that even a small SEE cross section can have important system ramifications [91], and in such cases it is important to perform high-fluence measurements taking into consideration a system's total error rate requirements.

IV. Summary and Conclusions

To ensure device survivability in radiation environments, devices must be tested in the laboratory using radiation sources that, at best, only approximate the system radiation environment. As a guide to users, test methods have been defined that provide users with viable test procedures for defining laboratory tests for ensuring part performance in use environments. Two such test methods are the U. S. test guideline, TM 1019, and the European test guideline, BS 22900. While there are fundamental differences between TM 1019 and BS 22900, both methods provide reasonable estimates of IC response in low-dose-rate space applications. These test methods were developed based on our understanding of the basic mechanisms that control the radiation response of devices. By understanding these basic mechanisms, one should be able to understand the limitations of these hardness assurance test procedures, and be able to more accurately interpret the data obtained using these test methods. It is important to note that while these test methods provide excellent insight into device behavior at low-dose rates, it is the users responsibility to evaluate test results and to determine their applicability to part performance in the environment of interest.

As is expected, these test methods must evolve with time to account for recently discovered radiation effects phenomena and improvements in our understanding of the basic mechanisms that control the radiation response of devices. For example, TM 1019 has been modified to address both ELDRS and PETS effects. Without prior characterization testing, TM 1019 now requires that devices that could show ELDRS be irradiated at dose rates of

$\leq$ 10 mrad(SiO_2)/s. For PETS effects, TM 1019 requires manufacturers to perform radiation qualification testing on ICs after burn-in. Unless it has been shown by prior characterization or by design that burn-in has a negligible effect on total dose radiation-induced degradation, radiation testing must be performed after subjecting parts to burn-in or the manufacturer must develop a correction factor that accounts for changes in total dose response resulting from subjecting product to burn-in.

There are a number of issues that can affect the reliability of hardness assurance tests that need to be considered when qualifying devices in space radiation environments. These include selecting the optimum laboratory radiation source, determining worst-case bias conditions, and understanding the implication of characterization temperature. While Co-60 gamma radiation sources can be used for device qualification in both electron- and proton-rich environments. Co-60 gamma radiation sources may overestimate the total dose degradation in proton-rich environments and, therefore, are a more conservative radiation source than x-ray radiation sources. Selecting the worst-case bias conditions for hardness assurance qualification can be challenging. They will depend on the failure mechanism(s) that cause device degradation, which can vary as a function of device technology, circuit parameters, dose rate, and temperature. As a result, the worst-case radiation and anneal bias conditions for ICs should be determined through an analysis of the system application and characterization testing. In addition, ICs are often required to operate over a wide range of temperatures in many system applications. However, TM 1019 and BS 22900 only require characterization testing at room temperature following irradiation. This might not bound the worst-case response of an IC that could operate over a wide temperature range. Suggested changes to hardness assurance test procedures for including device operation over a wide temperature range are reviewed.

Test guidelines are also available for SEE hardness assurance testing (e.g., JEDEC JESD57 and ASTM F1192). Several emerging issues for SEE hardness testing not covered by these test documents have been reviewed. These include the effects of proton energy and angle of incidence on single-event latchup, total dose irradiation during space flight on proton- and heavy-ion induced single-event upset, and the effects of heavy-ion energy on single-event upset and latchup. These phenomena make SEE hardness assurance testing more complex. Proton-induced SEL hardness assurance testing should be performed using the maximum power supply voltage, maximum proton energy of expected environment, maximum system temperature, and at grazing angle. Because of practical concerns of proton energy loss as protons transport through the sides of packages, system boards, etc., it is recommended that testing be performed at both grazing and normal angles of incidence. For devices that show increased SEU sensitivity with exposure to ionizing dose, SEU qualification should be performed on devices exposed to the maximum dose expected in the system application. Because of the creation of high LET secondary particles due to the interaction of heavy ions or protons with semiconductor materials (especially high Z materials), it is important to conduct SEU and SEL testing using high energy heavy ions and protons. This can limit the number of facilities available for SEU and SEL testing. In addition, new error rate calculation methods based on an understanding of nuclear reaction cross sections are required to accurately predict SEU and SEL error rates in space environments. However, by accounting for these issues into a comprehensive test plan, the user will improve overall reliability of space systems.

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