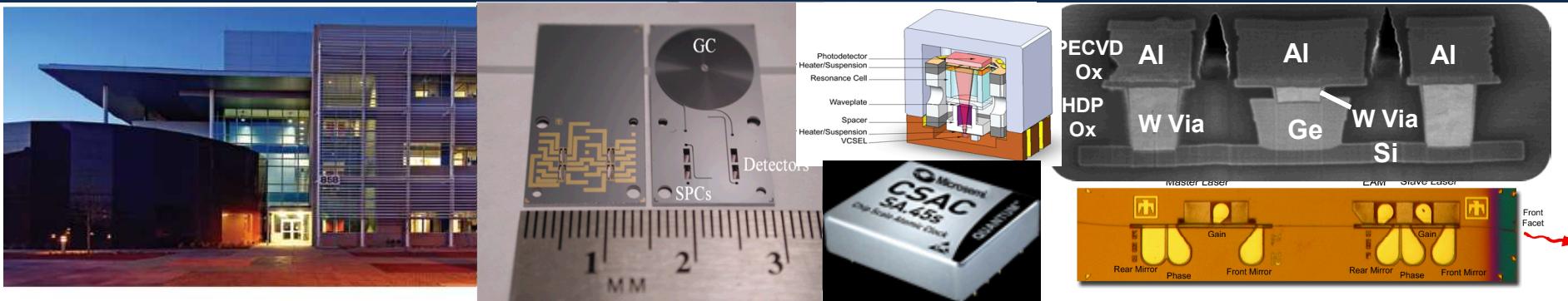


*Exceptional service in the national interest*



*Exceptional service in the national interest*



## **Introduction to Sandia National Laboratories and MESA**

### **Foundational Technologies at MESA**

#### **Integration Challenges**

#### **Integration Paths**

- Mechanical**
- Flip-Chip**
- Wafer Bonding**
- Direct Growth**
- Micromachining**

#### **Working With Sandia**

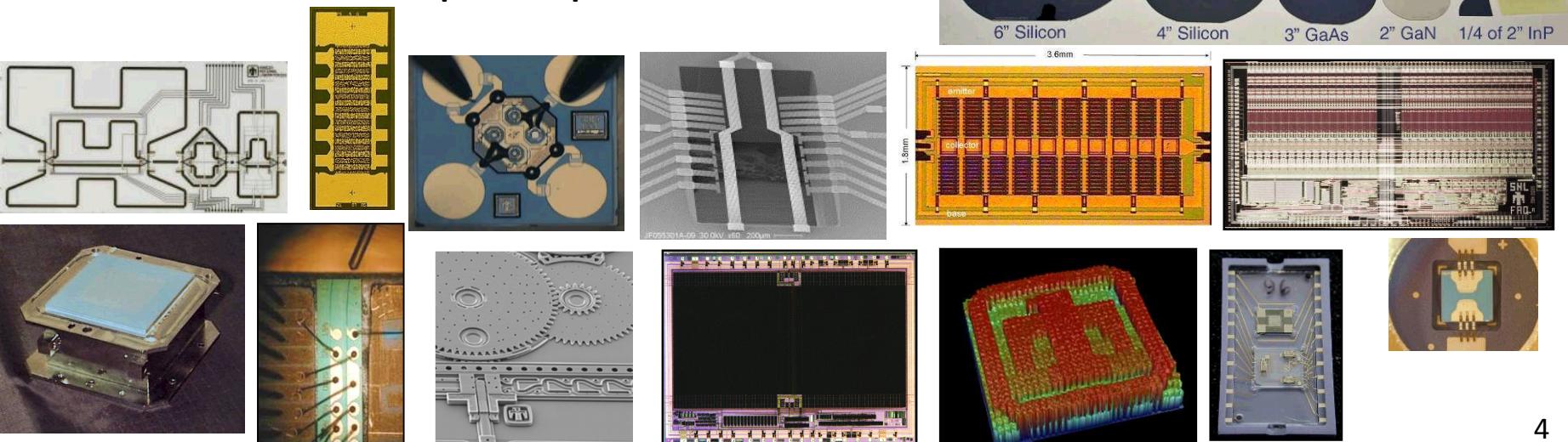
# Microsystems and Engineering Sciences Applications (MESA): 400,000 Sq-ft Complex with >650 Employees in Secure Facility



***MESA is an FFRDC-based development and production facility for any microsystem component or technology that cannot or should not be obtained commercially.***

# MESA Microfabrication Facilities

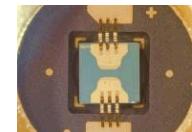
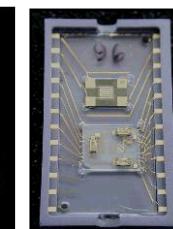
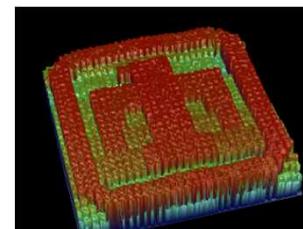
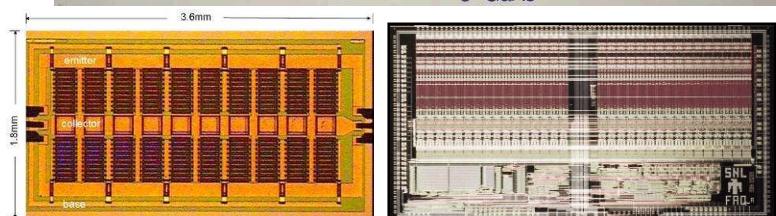
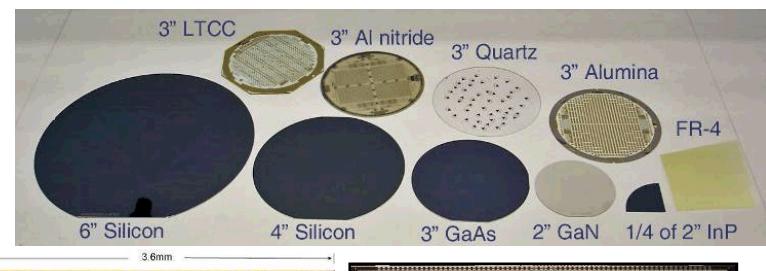
- MESA specializes in custom microelectronics, photonics, microtechnologies, and integrated systems
- NNSA's primary supplier of custom rad-hard ICs for weapon life extension programs and satellite systems
- Fast turn product capability: structured ASIC architecture
- Silicon bulk *and* silicon surface micromachining
- 6" silicon post-processing facility to support hybrid substrates and 3D integration (8" compatible)
- Compound semiconductor epitaxial growth
- Compound semiconductor discretes, IC's and MEMs
- Mixed-technology integration and processing
- Particularly suited to rapidly advance research concepts from TRL1-6 and deliver qualified products from TRL 7-9



**SiFab: 33,000 ft<sup>2</sup> Class 1/10/100**



**MicroFab: 16,600 ft<sup>2</sup> Class 10/100**

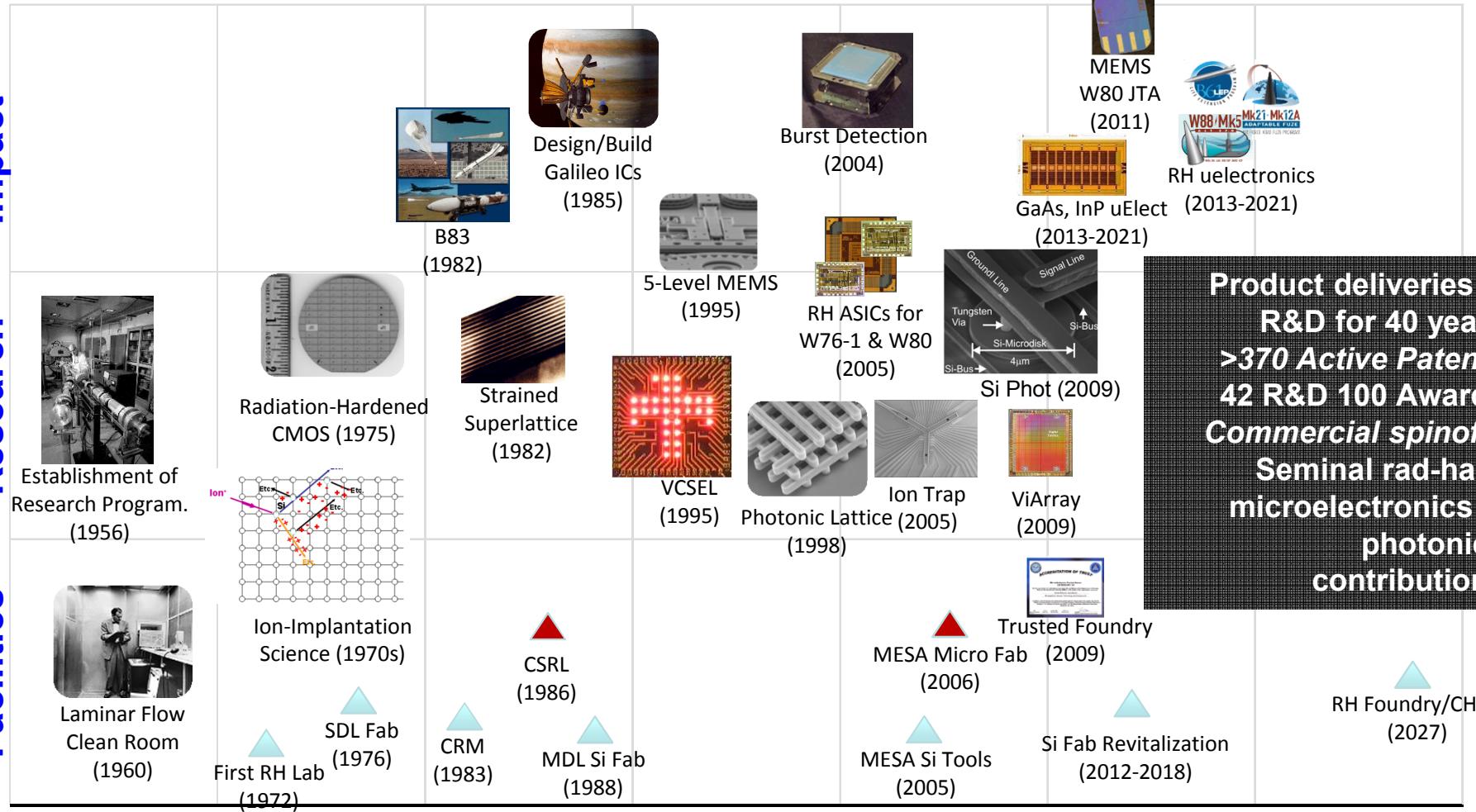


# R&D enables and sustains Sandia's Radiation-Hardened Microelectronics/Microsystems Capability

Impact

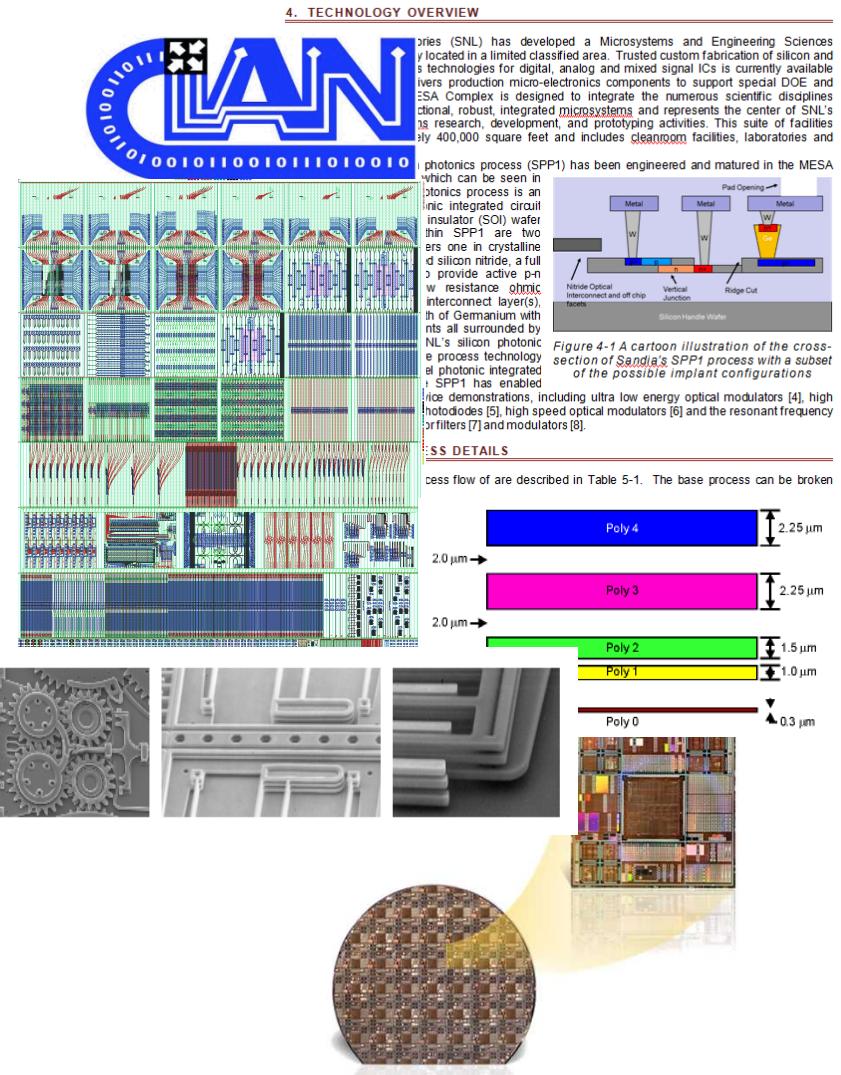
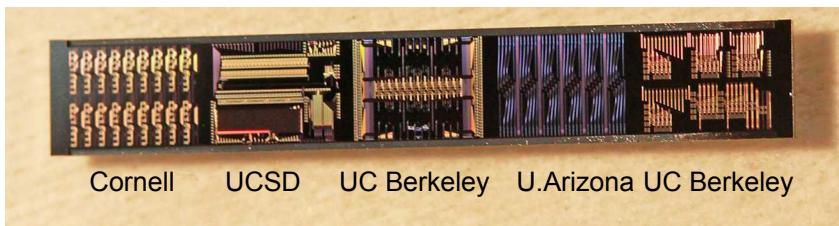
Research

Facilities



**MISSION:** Invent and mature integrated circuit and microsystems technologies that provide differentiation and impact for NW and other national security missions

- **SUMMIT V: 5 layer polysilicon MEMS process**
  - Developed design manual, DRC, many MPWs over the last decade
- **CMOS7 Electronics:** Rad-hard, mixed-signal ASIC/ViaArray: 0.35um, 3.3V core, 3.3V I/O, Cadence, MPWs since 2009
- **SPP1 Silicon Photonics Process:**
  - 250nm Si/3000nm BOx
  - fJ/bit mods, 45 GHz dets, filters, etc.
  - SiN 2-layer guides/xovers
  - Design manual, initial DRC, pilot MPW runs



# Trusted Advanced Pathfinder Products: Si Photonics

2014

*balanced homodyne resonant wavelength stabilization > 55C*

2013

*Si Photonics MPW (CIAN NSF ERC)*

2012

*24 GHz Si TW MZM*

2011

*45 GHz Ge Detector*

2010

*3 fJ/bit resonator modulator, 1V-cm MZM*

2009

*wavelength tunable rings over 35 nm*

2008

*2.4 ns Wavelength selective switch*

2007

*MicroDisk resonator infrared detector*

2005

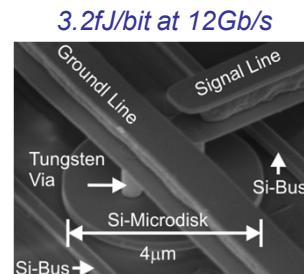
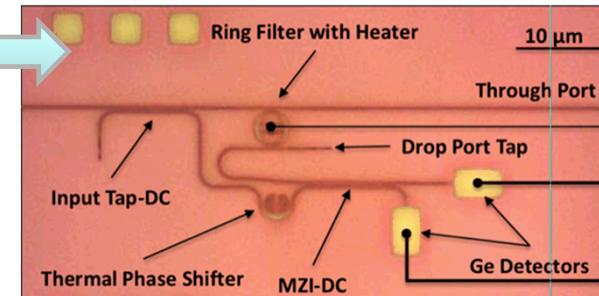
*$\text{Si}_3\text{N}_4$  low-loss waveguides*

2000

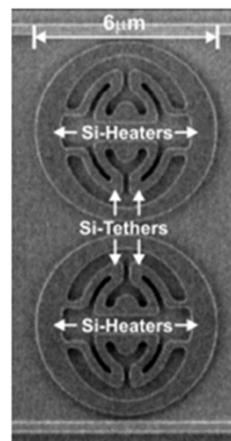
*$\text{SiON} / \text{SiO}_2$  (Clarendon Photonics)*

1990s

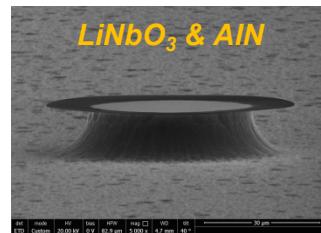
*$\text{Si PhC} & \text{Optical MEMS}$*



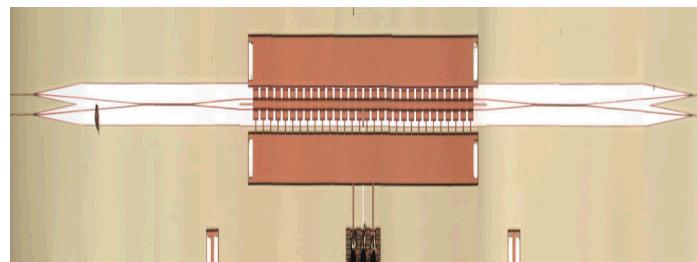
*Resonant Optical Modulator/Filter*



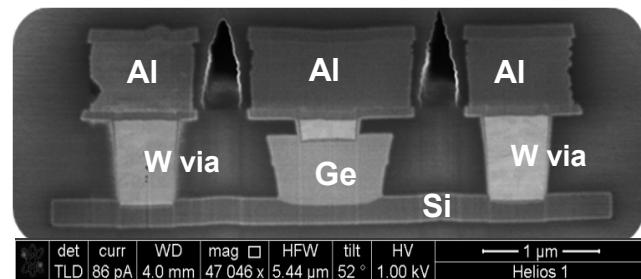
*Tunable Resonant Filter*



**MEMS process for additional capability**



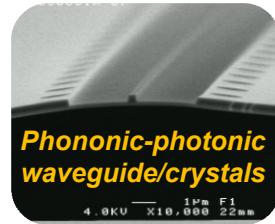
*24 GHz 0.7V-cm Travelling Wave MZI Modulator*



*45 GHz High-speed Ge Detector on Si*



*Suspended Si/SiN resonators*



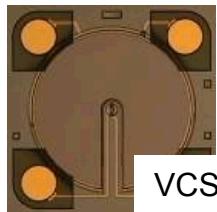
*Phononic-photonic waveguide/crystals*

# Trusted Advanced Pathfinder Products: III-V Photonics

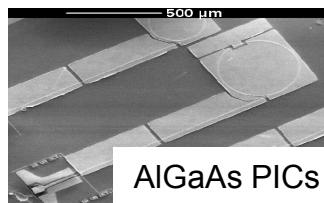
2010s



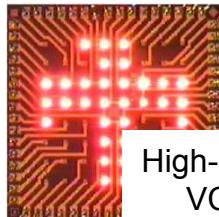
InGaAsP PICs



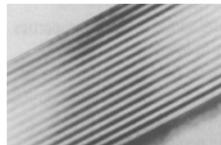
VCSEL+ PD



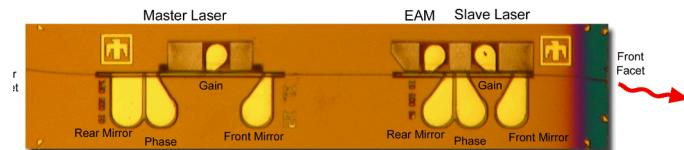
AlGaAs PICs



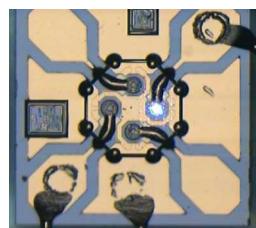
High-efficiency  
VCSELs



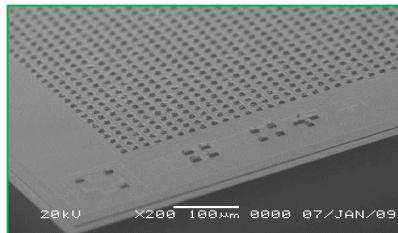
Strained-layer  
superlattices



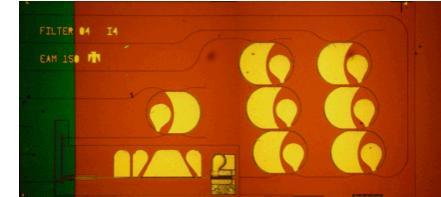
On-Chip Injection Locking  
Enhanced Modulation > 50 GHz, C-Band



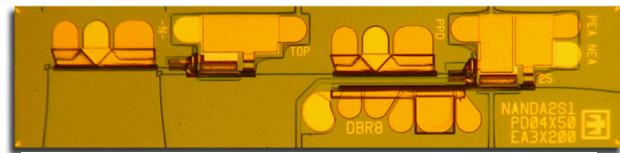
Single-Frequency Tunable VCSELs,  
For atomic spectroscopy and sensors



nBn FPAs in the SWIR, MWIR and LWIR,  
leveraging novel III-P and III-Sb materials



RF-Optical Channelizing Filter  
1-20 GHz RF on C-Band Light



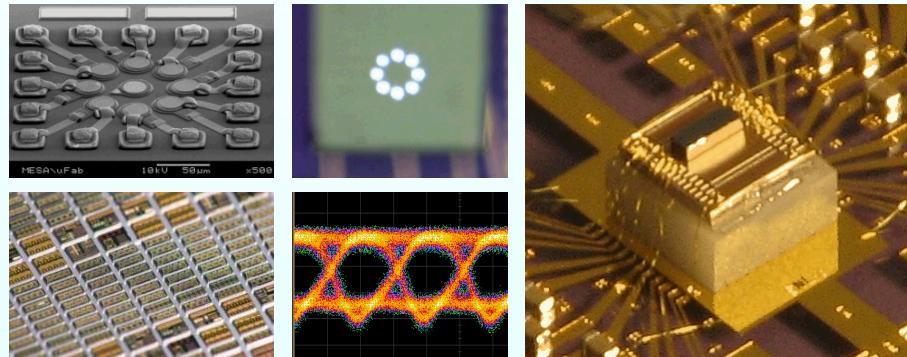
All-Optical Logic at >40 Gb/s, C-Band

- **Foundational Capabilities**
  - III-V compound semiconductor epitaxy, microfabrication, integration
  - Device physics, modeling, simulation
  - Microelectronics/optoelectronics, and complex mono/hetero-circuits
- **Prove, Advance Technology Readiness Level, Productize**
  - TRL1-6+: create, develop, prototype
  - NNSA QMS/QC-1-10; trusted
- **Trusted, low-volume, high-reliability products for harsh environments**

1980s

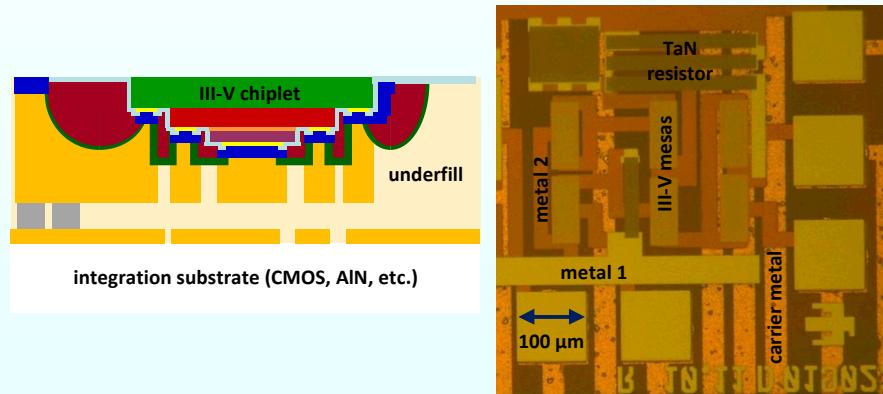
# Trusted Advanced Pathfinder Products: Heterogeneous Integration

## Optical Data Communications



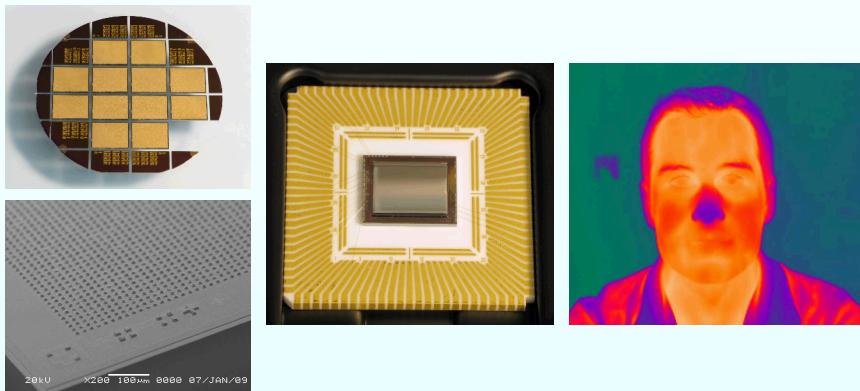
- GaAs- and InP-based devices: VCSELs, modulators, photodiodes
- dense integration onto 32-nm and 45-nm CMOS

## Heterogeneous III-V/CMOS Microelectronics



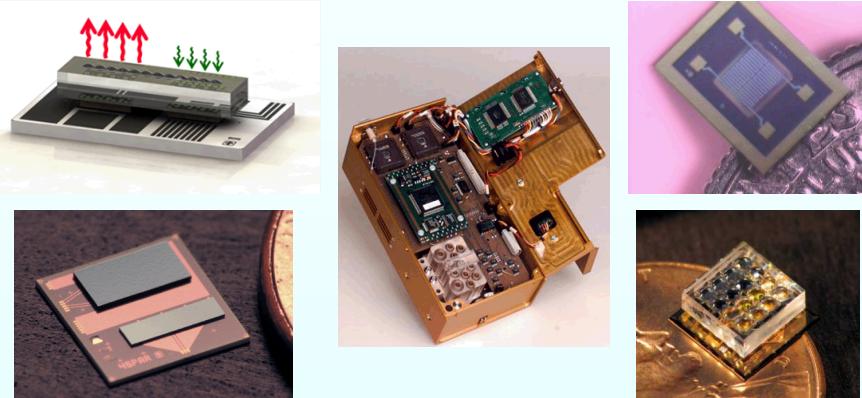
- complementary integration of GaAs and InP microelectronics
- III-V microelectronics circuitry on CMOS ASICs

## IR Imagers for Remote Sensing



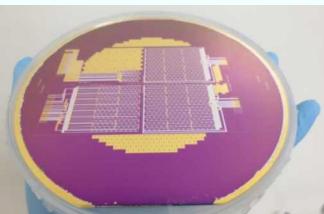
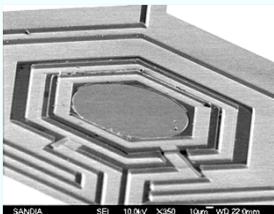
- nBn InAs/GaSb MWIR/LWIR detector arrays for large-format FPAs
- 10 μm indium bump bonding, underfill, thinning, AR coating
- hybridization to silicon ROICs with >99.99% interconnect yield

## Optical and MEMS-based Microsensors



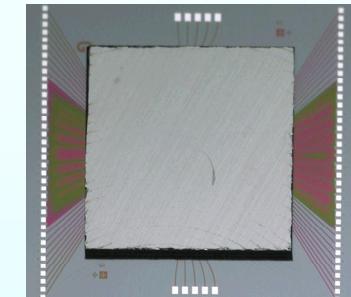
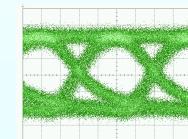
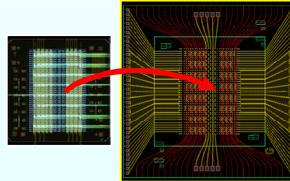
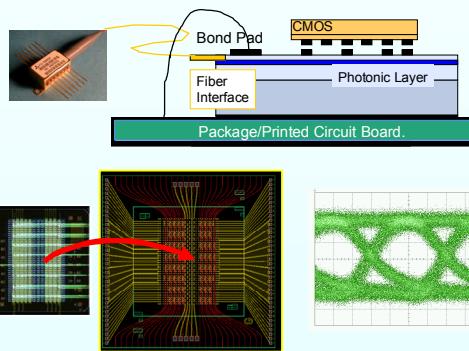
- chemical and bio sensors using MEMS and SAW devices
- g-hard optical microsensors with in-house photonics
- hybrid device integration with custom micro-optics

## Microsystem-Enabled Photovoltaics



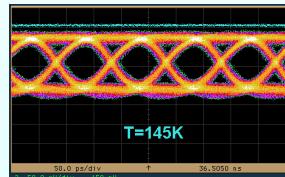
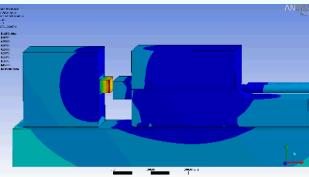
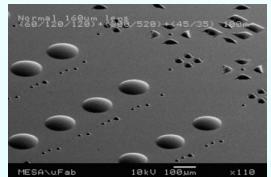
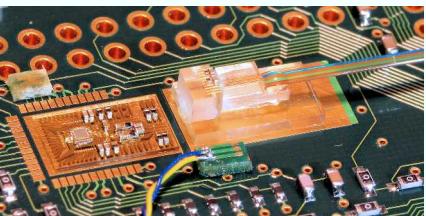
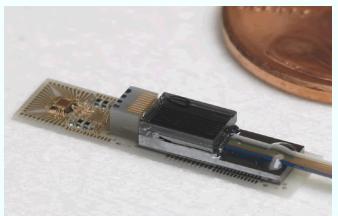
- wafer-level bonding for multi-junction solar cells
- InGaAsP/InP and InGaP/GaAs devices on silicon
- dielectric interfaces with III-V substrate removal
- integration with collection optics

## High Performance Computing



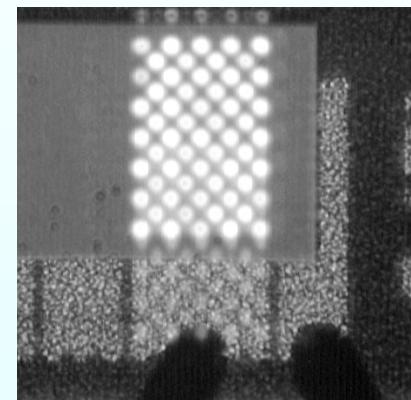
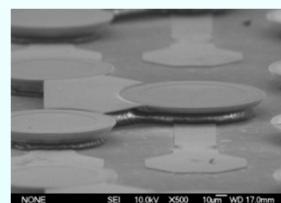
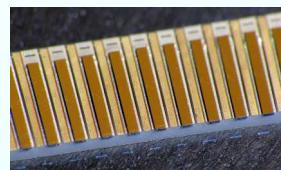
- silicon photonics on high-speed silicon ASIC
- independent optimization of electronics & photonics

## Extreme Environment Applications



- custom photonics, optics, electronics for cryogenic interconnects
- advanced optoelectronics and integration for radiation hardness

## High Performance Photonics

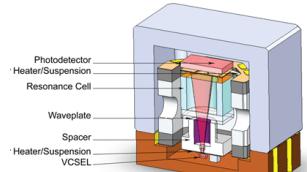
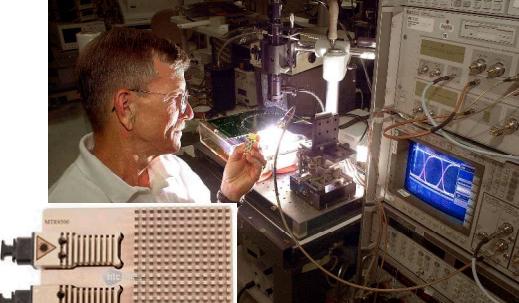
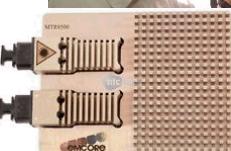
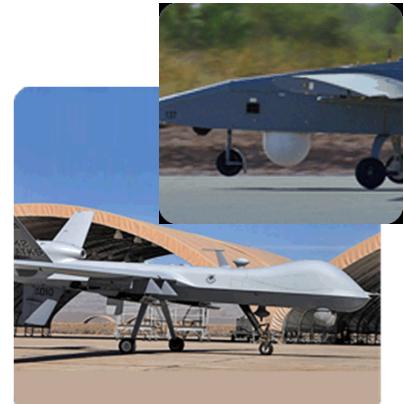


- high-power emitters on AlN and diamond
- RF packaging for high-speed test and measurement

# How Can Sandia Help?

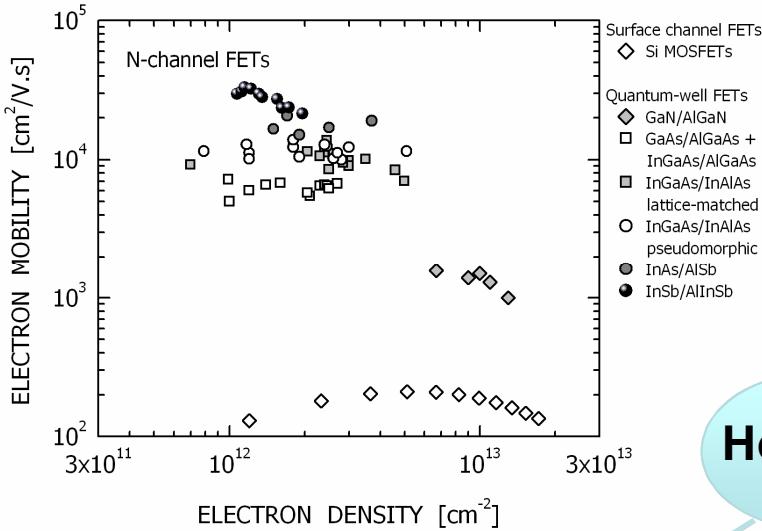
- **Expertise:** >30 years in III-V & Silicon Photonics R&D:
  - Toolboxes for internal and contract R&D
- **Capability:** Large flexible Si & III-V R&D Fab, Production rigor:
  - 65kft<sup>2</sup> fab, 10 epi reactors, >60 photonics staff, (60% Ph.D.)
  - Here today, here tomorrow... (NW IC deliveries)
  - Secure environment & staff, robust info-control (TRUST)
- **History of Technology Transfer to Industry:**



Processes	Devices	Subassemblies	Systems
<b>MEMS (Fairchild)</b>	<b>VCSEL CSAC (Microsemi)</b>	<b>POM (EMCORE)</b>	<b>SAR (General Atomics)</b>
Transfer of Sandia's Summit IV™ MEMS technology. Network Photonics Optical MEMS	Narrow $\lambda$ temp-stable VCSEL for Chip-scale Atomic Clock (DARPA)  	OC-192 Transponder Parallel Fiber Optic Module prototype development using VCSEL & PD arrays  	Copperhead & Lynx SAR (w/ GA Aero) on TigerShark & Predator UAVs ( <a href="#">IED detector being transferred to Army</a> )  

# Understanding the Challenges of III-Vs on Si

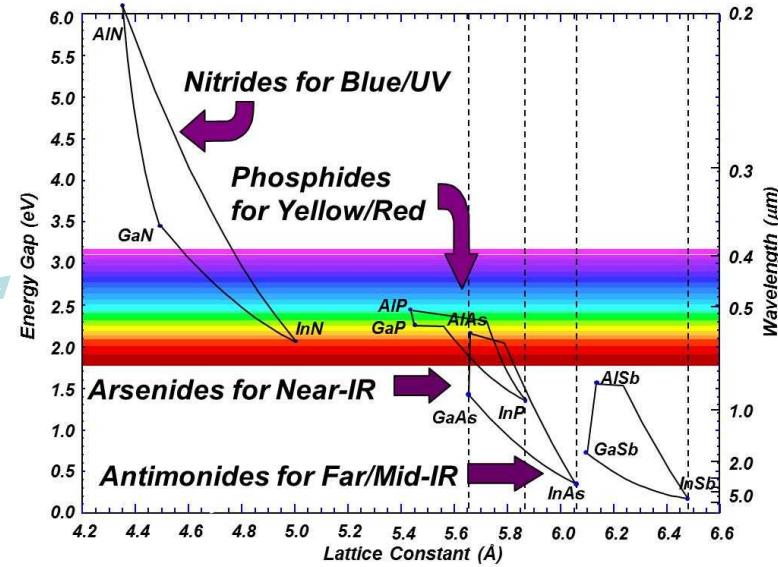
## Superior Characteristics



However

ESH Challenges

## Lattice Matching Challenges



And more...

## Hazardous Production Materials

AsH<sub>3</sub> – 3 ppm IDLH

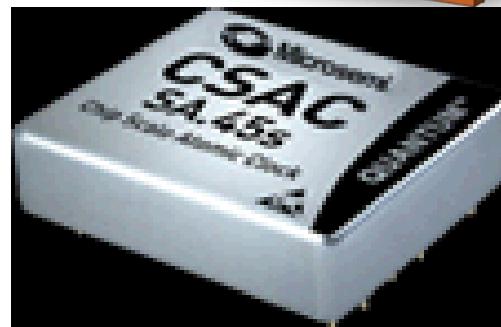
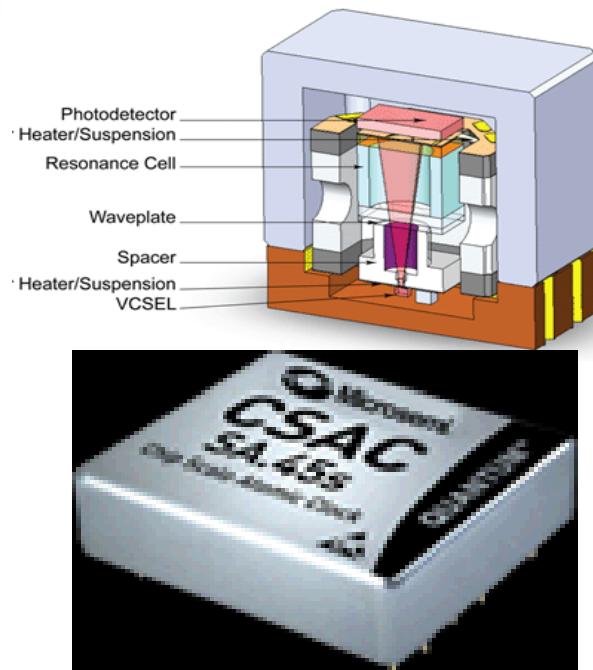
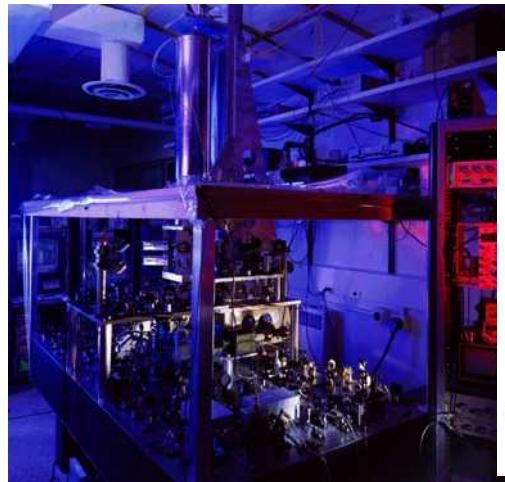
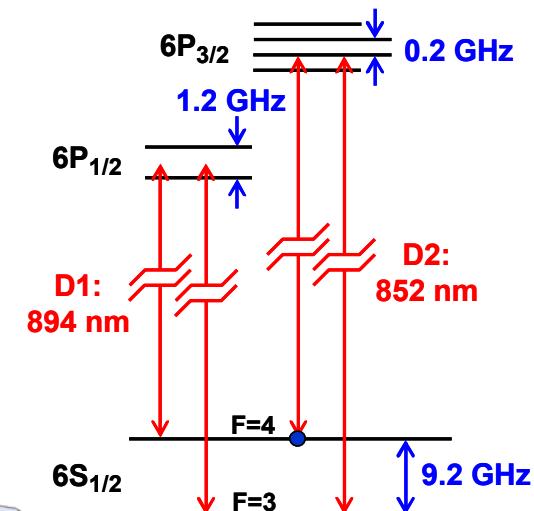
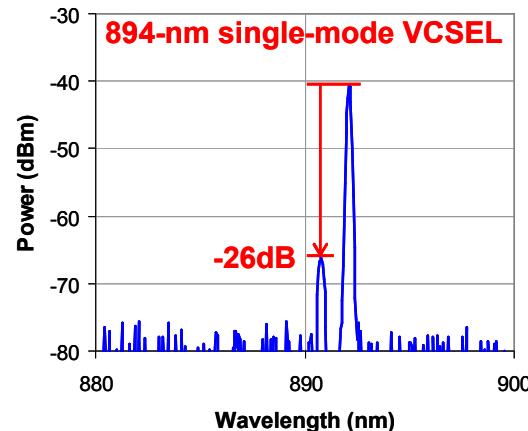
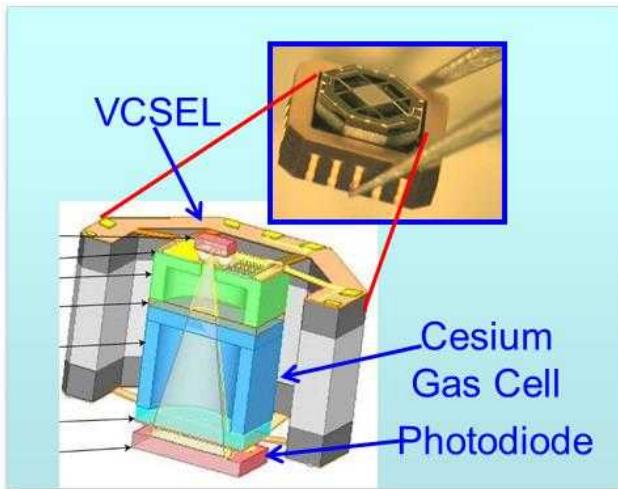
PH<sub>3</sub> – 50 ppm IDLH

III(CH<sub>3</sub>)<sub>3</sub> are pyrophoric

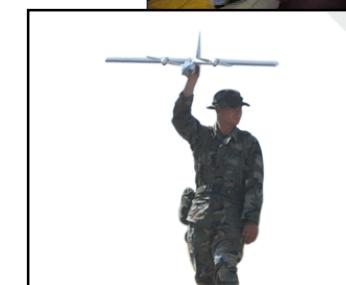
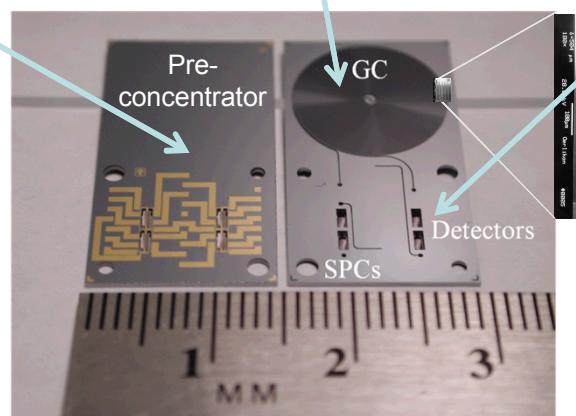
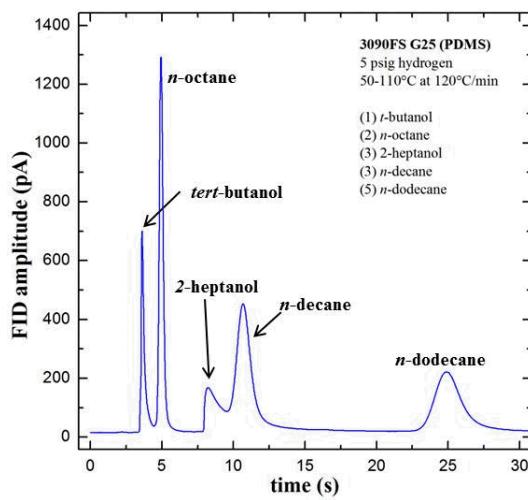
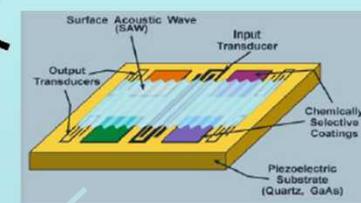
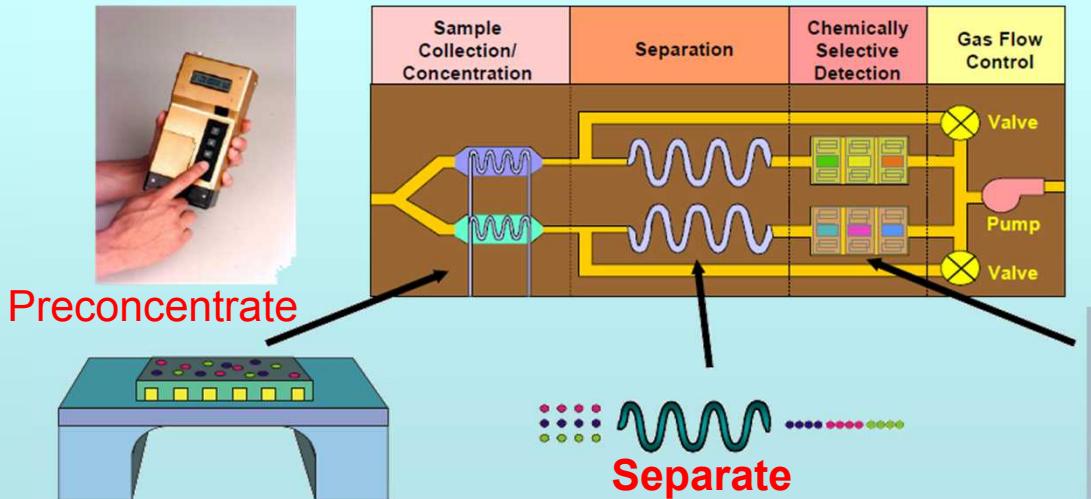
H<sub>2</sub> carrier gas run at 24 lpm/Tool

*Widely varying TCE  
Directional Properties  
Surface Termination is complex  
Heterogeneous interfaces must be understood  
Etc...*

# Mechanical Integration – Chip Scale Atomic Clock



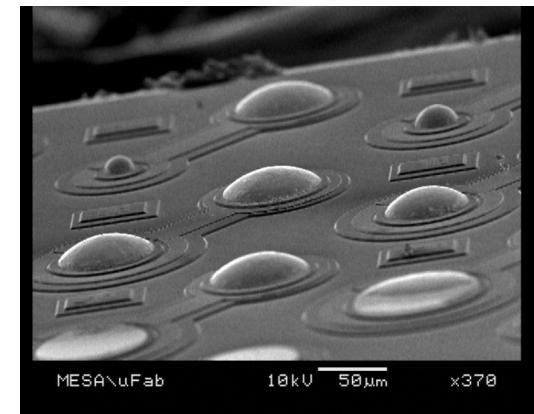
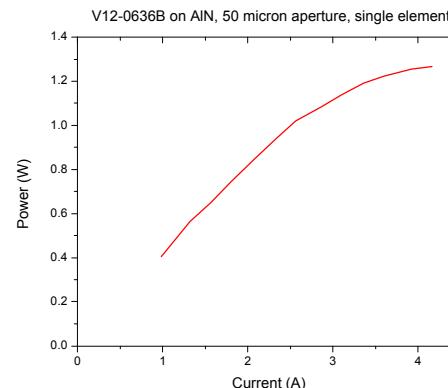
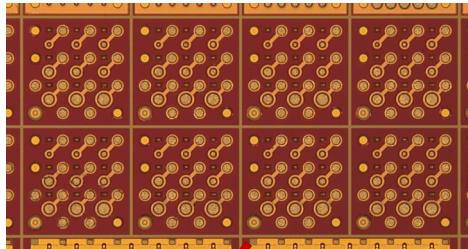
# Unifying Concept of Operation



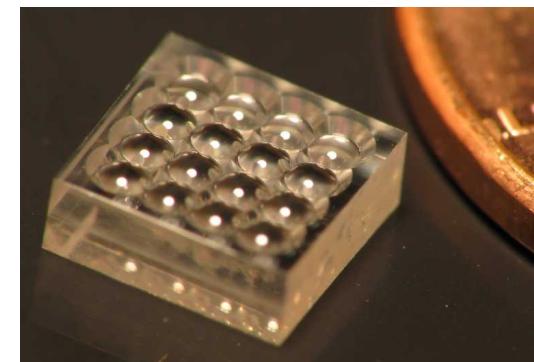
# Flip-Chip Integration – Tx Rx Assemblies

- **1x4 VCSEL arrays & 2x4 detector arrays attached to submount**
  - parallel drive of VCSELs for low impedance
  - parallel connection of PDs to sum photocurrent signal
- **Assemblies tested electrically prior to microlens integration**

2x4 InGaAs photodiode array

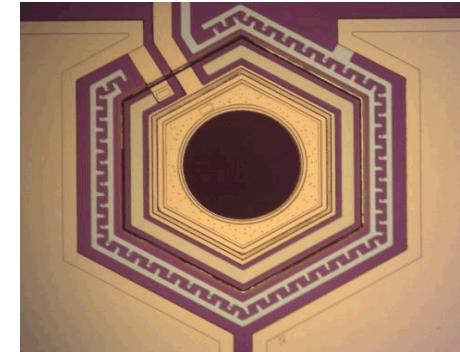
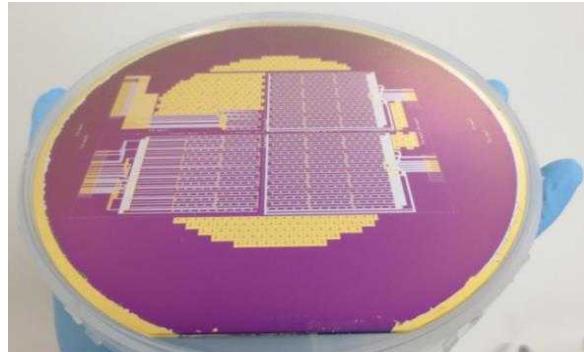
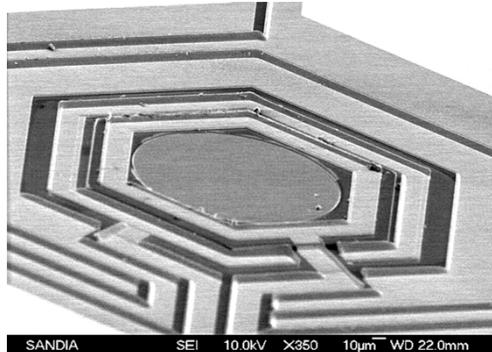


1x4 high-power VCSEL array  
(980nm, bottom-emitting)

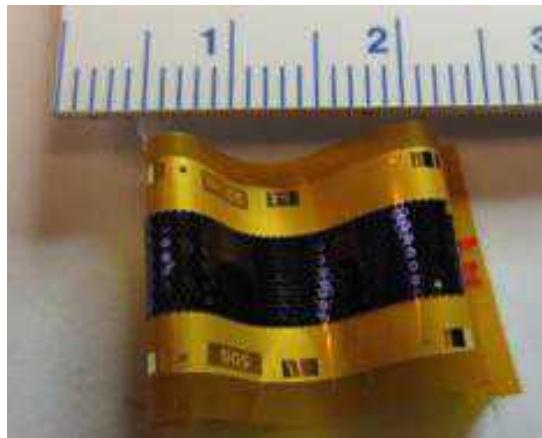


populated AlN fuse submount

# Direct Wafer Bond Integration – Microsystems Enabled Photovoltaics



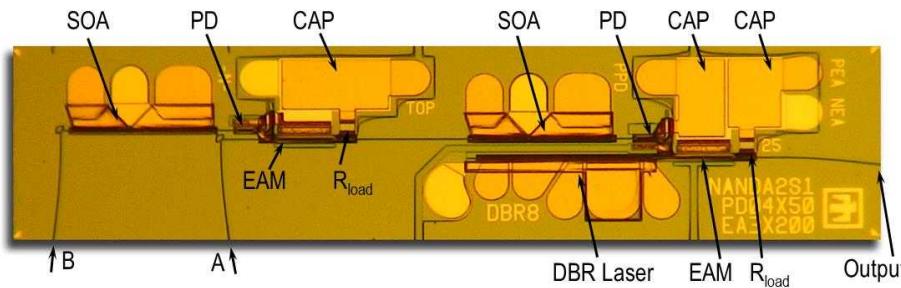
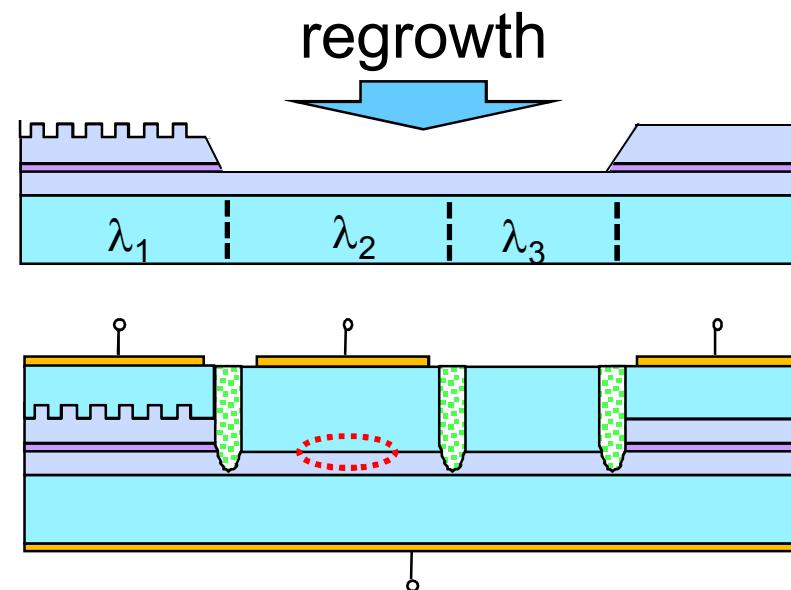
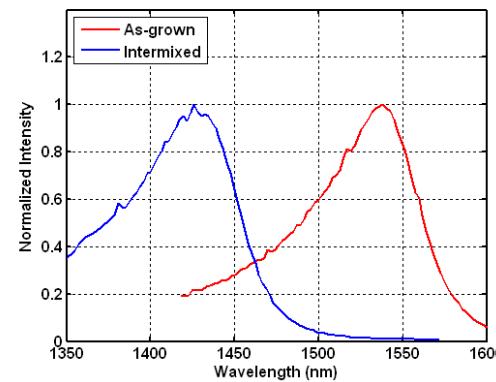
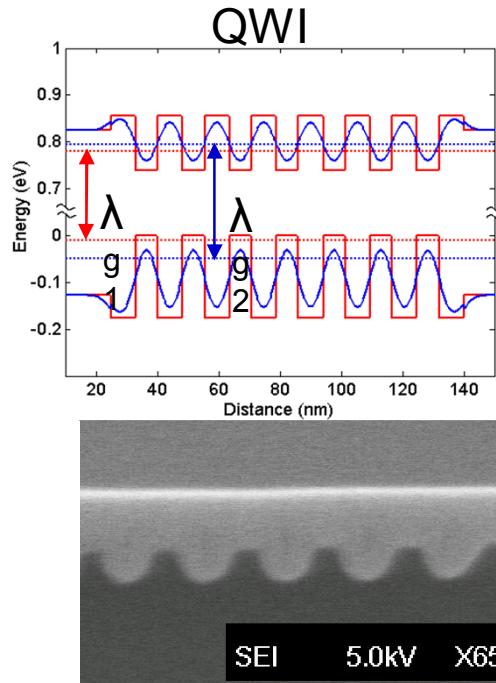
InGaAsP/InP and InGaP/GaAs devices on silicon



Flexible Substrates

Collection Optics

# Direct Growth for Integration – Photonic Integrated Circuits



Top View of Photonic Integrated Circuit



Integrated PIC  
Assembly



- **Competency and commitment in custom solutions for high reliability when industry is unable or unwilling to engage**
- **DOE supports National Lab involvement in strategy and project development for U.S. companies and universities with fairness of opportunity, without competing with industry, and with no organizational conflict of interest**
- **Decision to engage depends on unique value Sandia may contribute for enabling new understanding and securing a supply chain for national security applications**

*Sandia has a diverse array of technical expertise and co-located SMEs allowing us to*

