SAND2006-6356C

SiC Via Fabrication for Wide Bandgap HEMT/MMIC Devices

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October 30, 2006
210th ECS Meeting – Cancun, Mexico

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Motivation for Work

- Development of AlGaN/GaN HEMTs and MMICS for power amplifiers

- Through-wafer via holes in SiC substrates must be realized to enable low inductance grounding
  - Laser drilling at high rates (> 10 μm/min) has been demonstrated, but is a serial process and can generate particles
  - ICP etching is preferred for large wafers or devices with high via densities

SiC Plasma Etching

- Stable, strongly bonded material

- F-chemistry is most commonly used. CF_4, NF_3, and SF_6 have been used as the F-source gas.

- Energetic ion bombardment and hard masks may be required

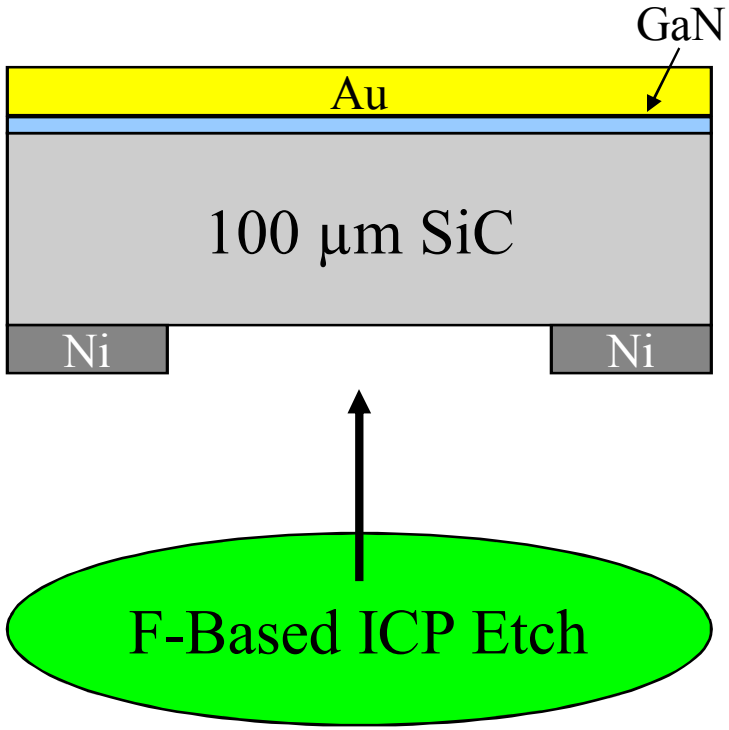
- O_2 can be added to the F-chemistry to provide an additional volatilization path for C (CO, CO_2, or COF_2) as well as increase the concentration of free radical F.

- C-removal is the rate-limiting step. Etch products are believed to be SiF_4 and CF_2 in pure F chemistry

- References: J. Vac. Sci Technol. A16, 885 (1997)
  J. Vac. Sci Technol. A16, 2204 (1998)
  Appl. Phys. Lett. 73, 76 (1998)
  Solid State Electron. 42, 743 (1998)
  J. Vac. Sci Technol. B16, 536 (1996)
  J. Vac. Sci Technol. B19, 1339 (2001)

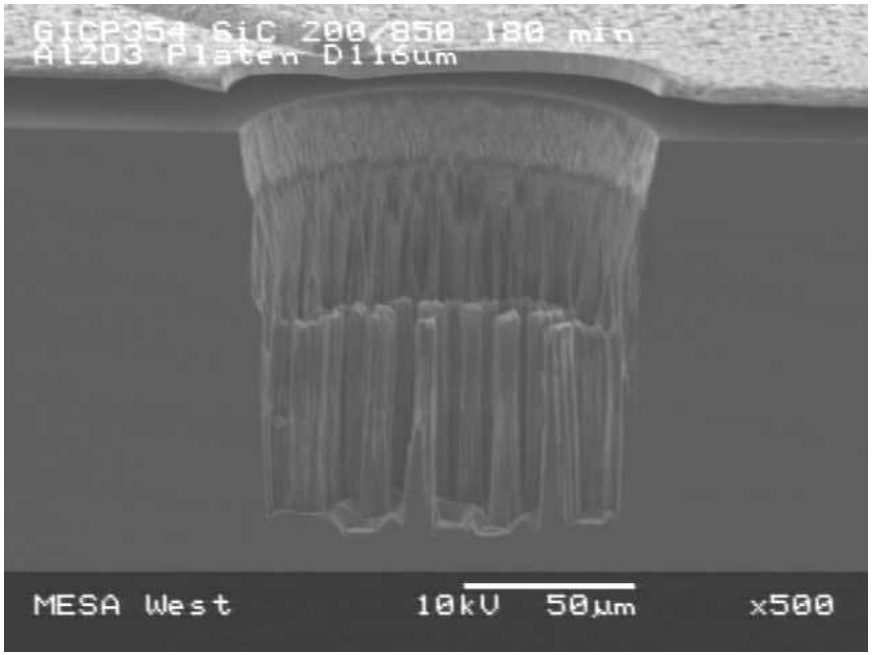
Process Requirements

- Develop ICP etch process for SiC vias
- Requirements:
  - Etch rate > 0.25 μm/min
    - SF_6/O_2 ICP plasma
  - Good selectivity to mask
    - Electroplated Ni demonstrates ~50:1
  - Aspect ratio ~ 1:1
  - No micro-masking
  - No trenching
  - Etch must stop before Au punch through
  - Ability to metallize via



Initial ICP SiC Via Etch Processes

- Full thickness SiC wafers: ~275 µm
- ICP Etch Conditions:
  - SF_6 = 50 sccm
  - O_2 = 10 sccm
  - Pressure = 7 mTorr
  - ICP Power = 750 – 950 W
  - RF Power = 100 – 250 W
  - Temp = 25 °C
  - Etch rate ~ 0.65 µm/min



Significant micro-masking observed

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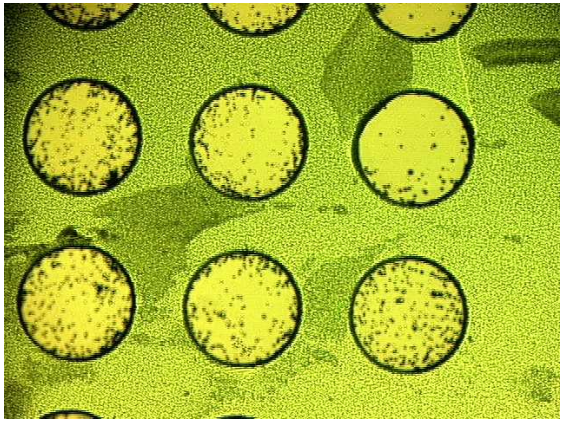
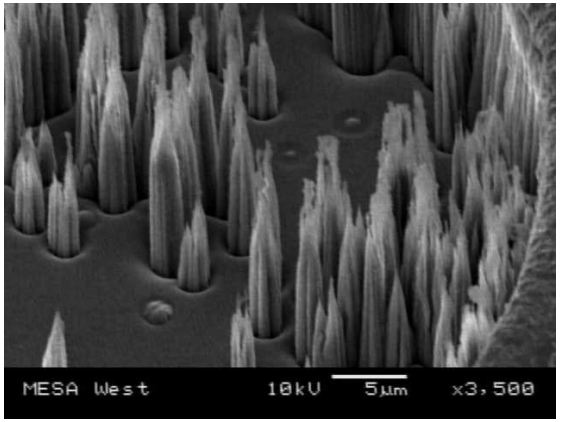
SiC Via Micro-masking

- Serious problem resulting in failure of vias
  - Micro–masking allows the formation of pillars in the vias
  - Can cause low via yield
- Goals:
  - Determine origins
  - Develop methods of reduction





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Possible Source of Micro-masking

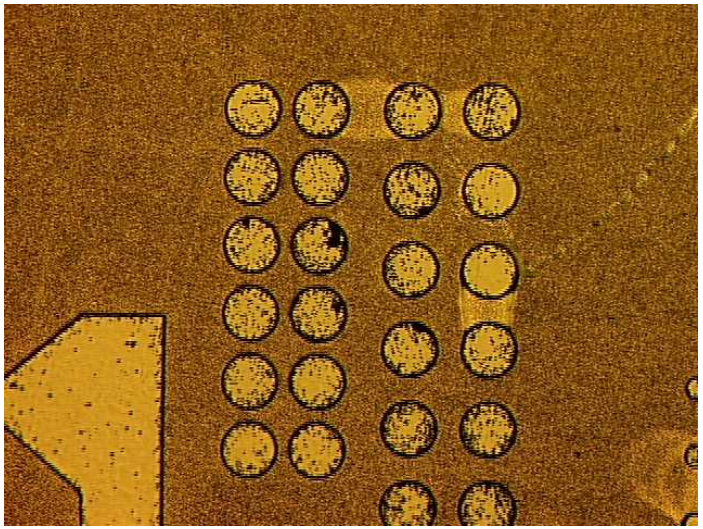
- Redeposition of non-volatile sputtered material
  - Potential source:
    - etch mask
    - platen
    - alumina clamp
- Defects in SiC
  - N-type SiC demonstrates greater amount of micro-masking than i-SiC
  - Greater density of pillars around edge of wafers

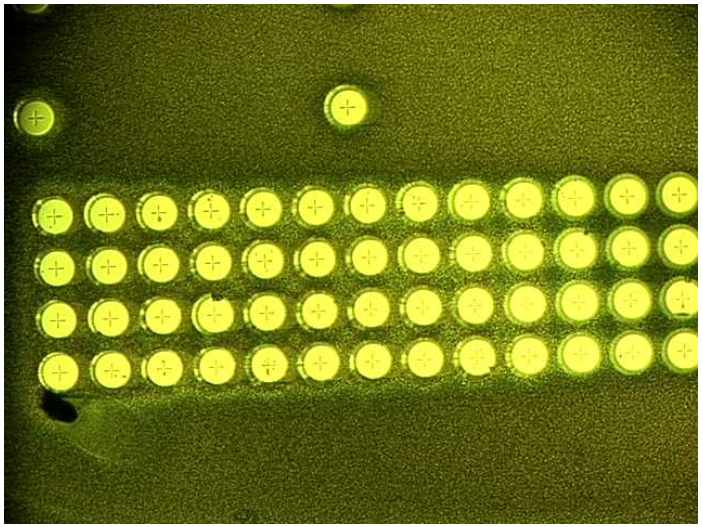
Micro-masking Source

- Etch Masks:
  - Resist
  - Al
  - Ni
  - SiO_2
  - SiN
- Platens
  - R-plane sapphire
  - Alumina
  - Aluminum Nitride (AlN)
  - Quartz
  - Silicon
  - Anodized aluminum
  - Ni-plated aluminum
  - Graphite
- Sealing problem of (porous) graphite solved by bonding bottom side of platen to Si wafer.

Micro-masking Source

- Thinned SiC vs std SiC
  - Large variation in micro-masking from wafer to wafer for thinned SiC
    - Indicates that wafers with less micro-masking had a better polish during lapping process
    - Origin of micro-masking introduced during lapping process
      - Creation of defects in SiC?
      - Embedded particles from lapping process?





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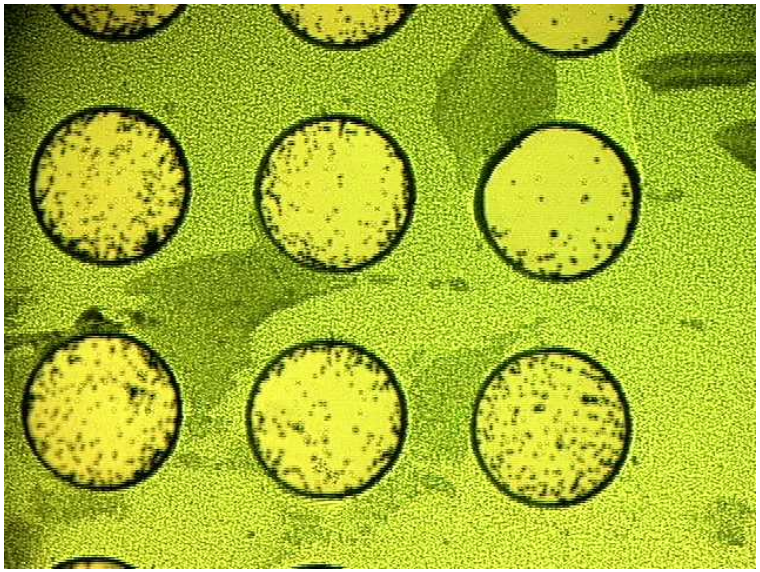
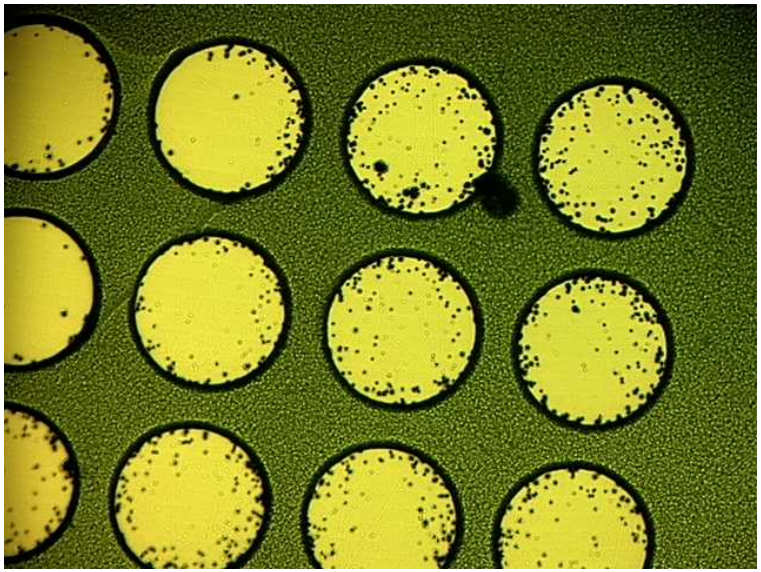
Reduction of Micro-masking: Ar Plasma Preclean

- Goal: eliminate particles on SiC surface that may initiate micro-masking
- Ar pre-clean prior to SiC etch

No pre-clean



Ar pre-clean
500 W ICP power
100 W rf power
40 sccm Ar
25C



~ 20% improvement in micro-masking with Ar pr-clean

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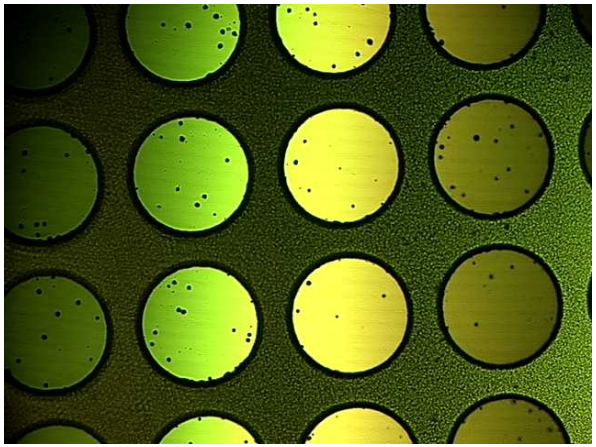
Ar Pre-clean

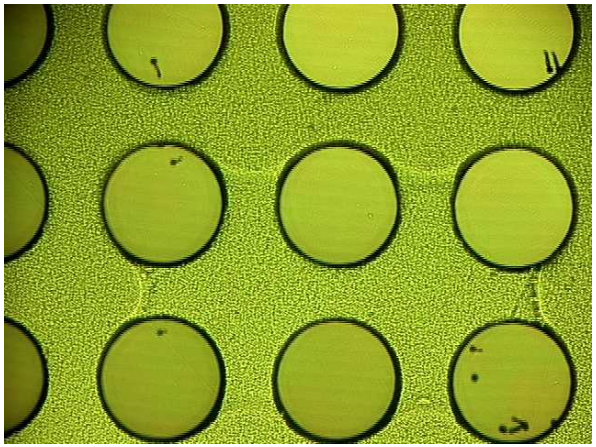
Increase power and time to improve removal of particles

750 W ICP power – 100 W rf-power Ar plasma

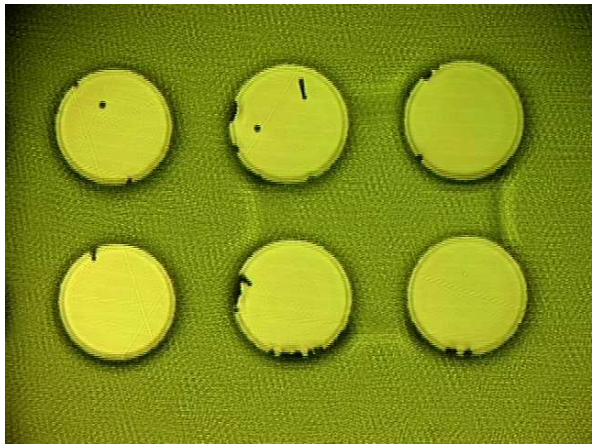
2 minutes



5 minutes



10 minutes



- Significant improvement over 500 W ICP power Ar plasma
- Improvement from 2 to 5 minute exposure
- Similar results for 5 and 10 minute exposures

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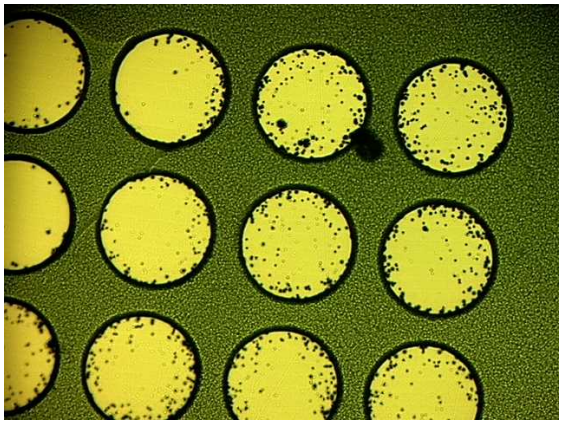
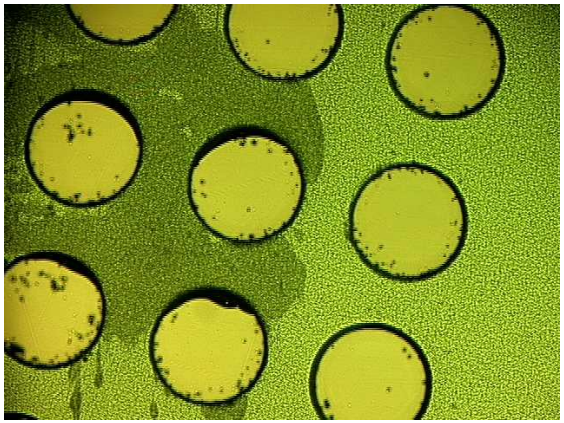
Reduction of Micro-masking: Etch Plasma Chemistry

- Goal: change plasma chemistry to remove particles from SiC surface and/or reduce etching of defects
- Addition of He or Ar to SF_6/O_2plasma

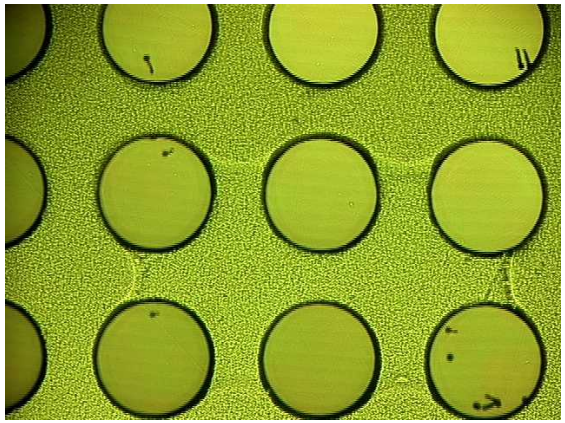
2 minute Ar pre-clean
SF_6/O_2 plasma



2 minute Ar pre-clean
SF_6/O_2/He plasma



5 minute Ar pre-clean
SF_6/O_2/Ar plasma



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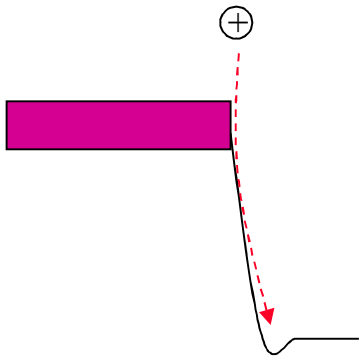
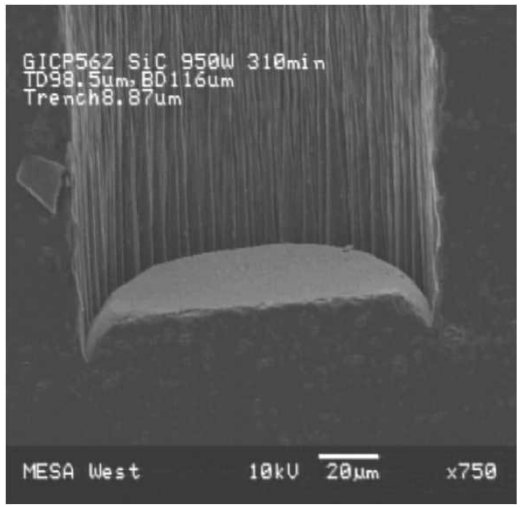
Trenching

• Reflected ions cause a localized increase in the ion flux at the feature bottom, leading to a localized increase in etch rate.

- ➢ diverging ion flux (caused either by sidewall charging or by diverging incident ions)
- ➢ tapered sidewalls (usually profiles are vertical during the etch process)





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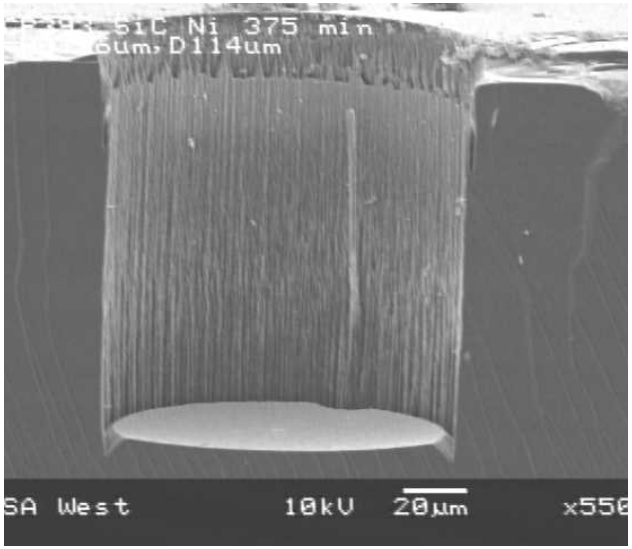
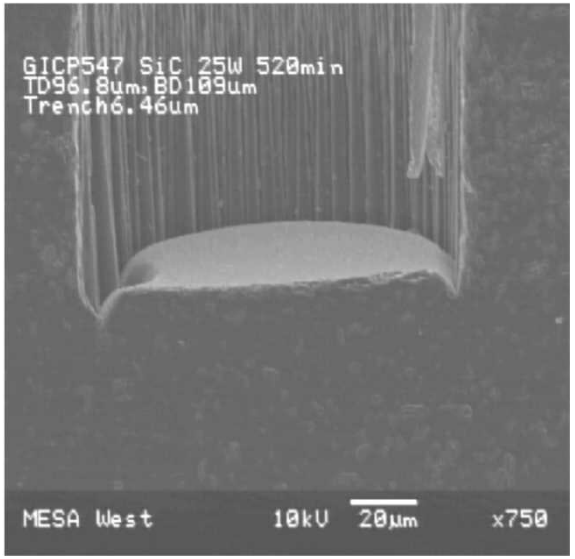
Reduce Trenching: Lower Ion Energy

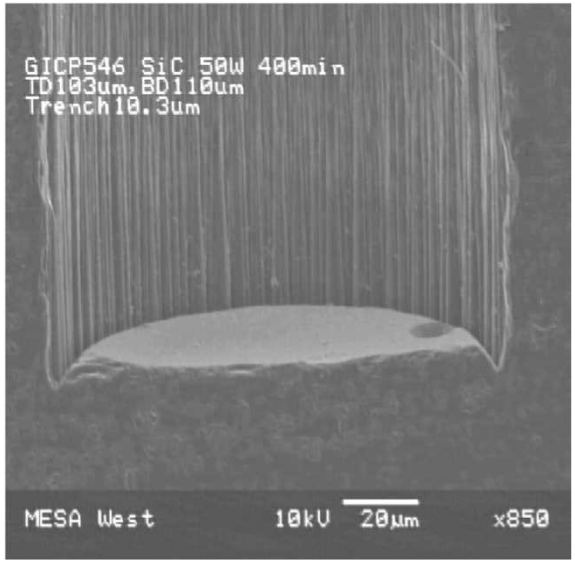
ICP	750 W
rf	100 W
Pressure	7 mTorr



ICP	750 W
rf	25 W
Pressure	7 mTorr



ICP	750 W
rf	50 W
Pressure	7 mTorr



- Reduction of rf-power – ion energy does not reduce trench depth
- Trench depth ~ 6 – 10 µm

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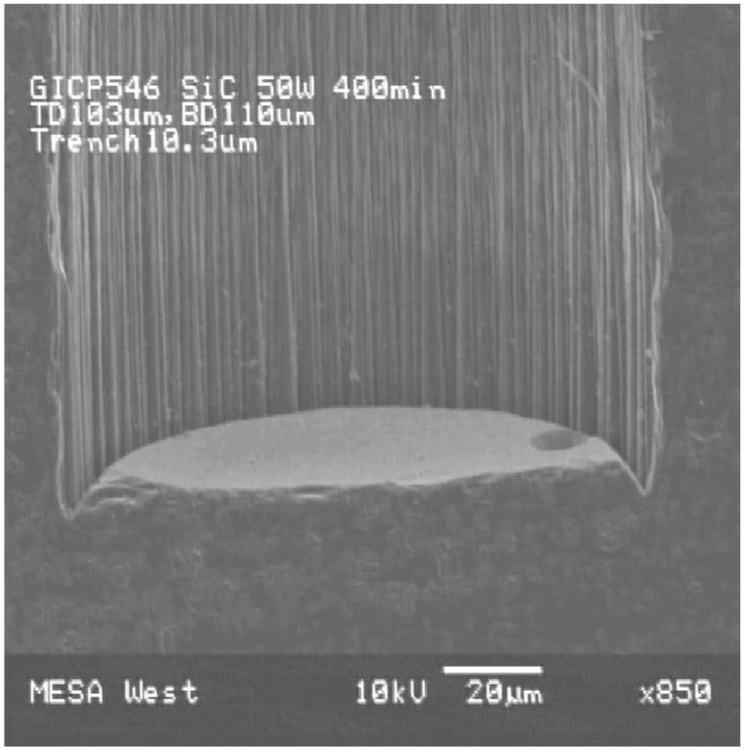
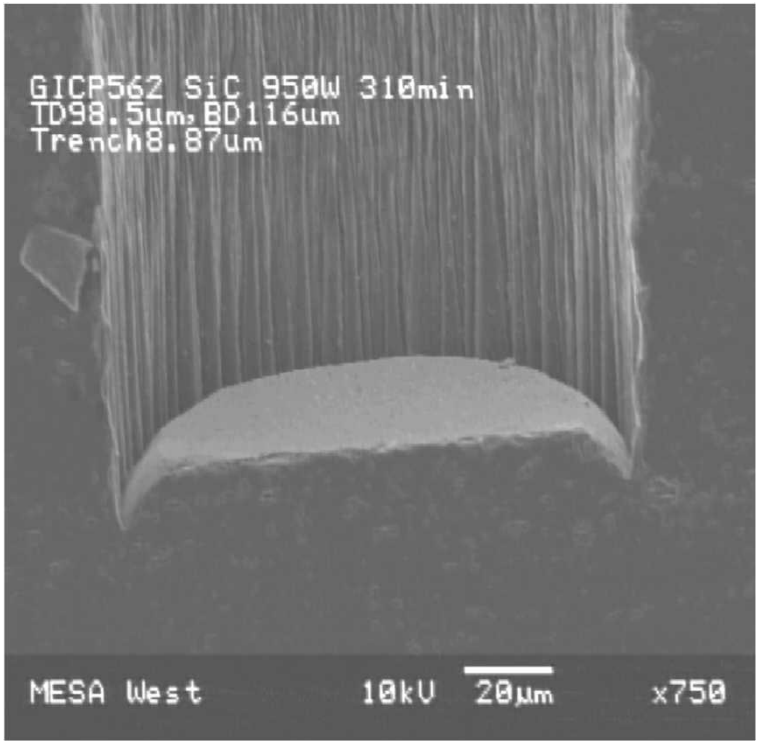
Reduce Trenching: Vary ICP Energy

ICP	750 W
rf	50 W
Pressure	7 mTorr



ICP	950 W
rf	50 W
Pressure	7 mTorr



- Changing ICP power – plasma density does not reduce trench depth
- Trench depth ~ 6 – 10 µm

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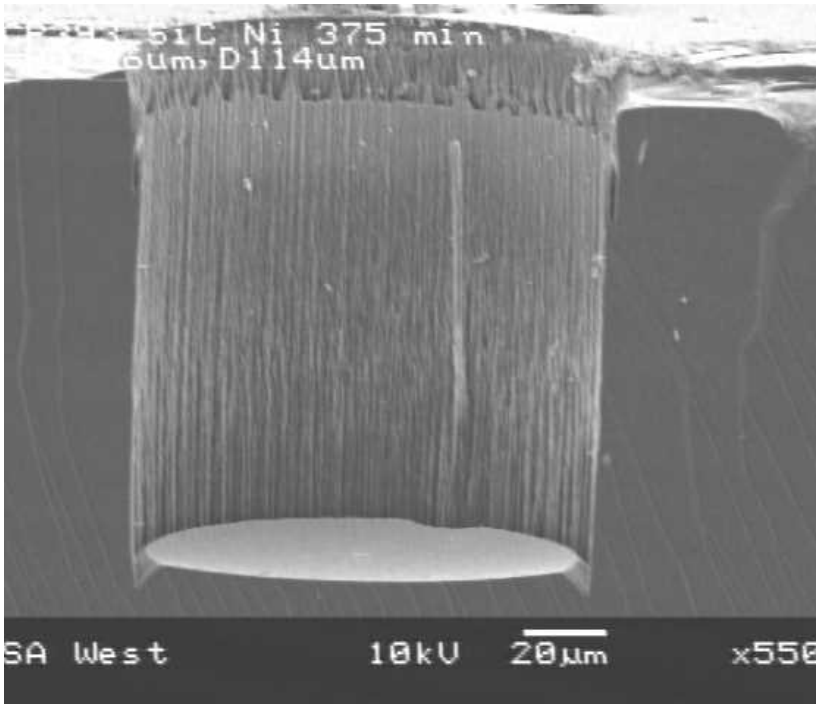
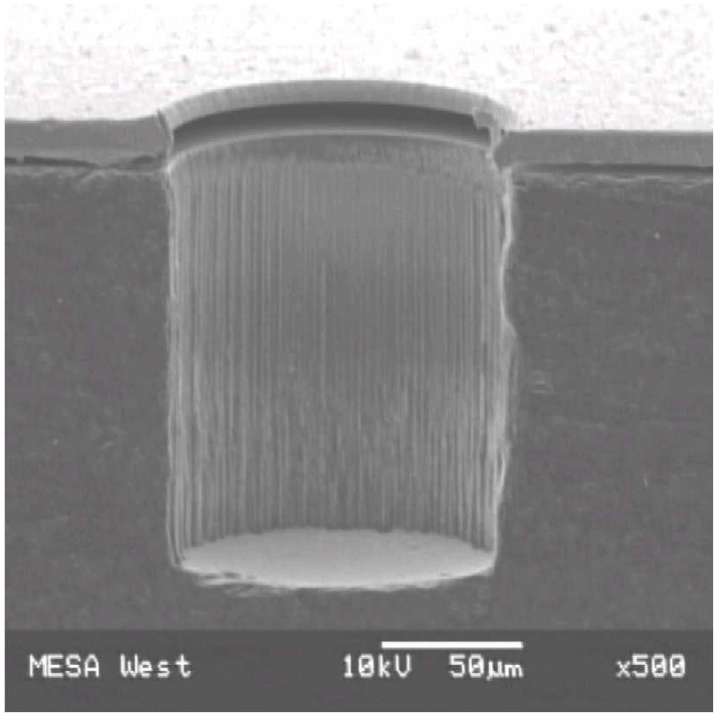
Reduce Trenching: Vary Pressure

ICP	750 W
rf	100 W
Pressure	7 mTorr



ICP	750 W
rf	100 W
Pressure	12 mTorr



- Changing plasma pressure eliminates trenching
- Also reduces etch rate

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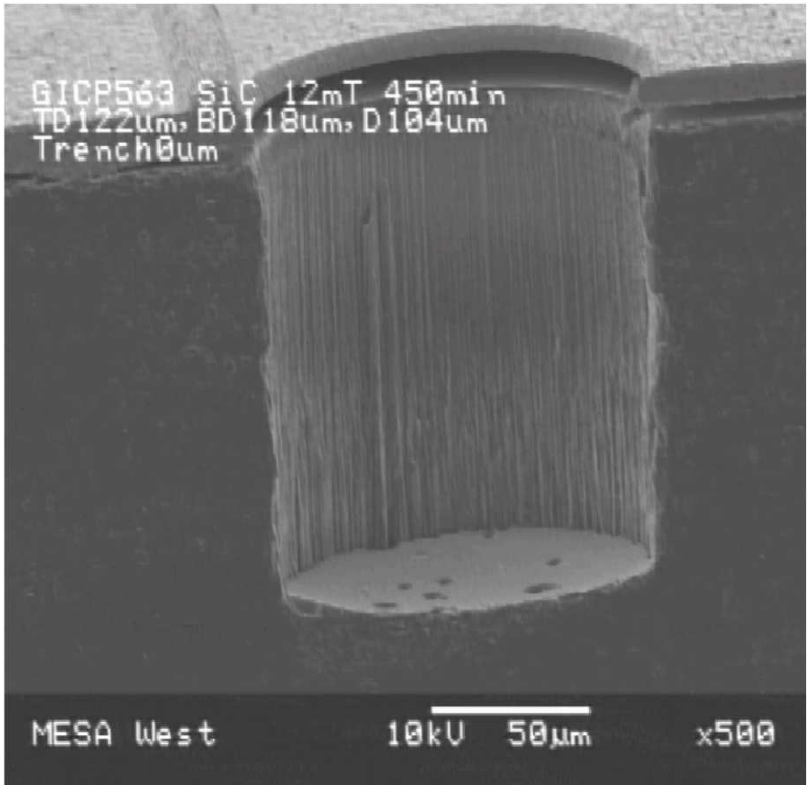
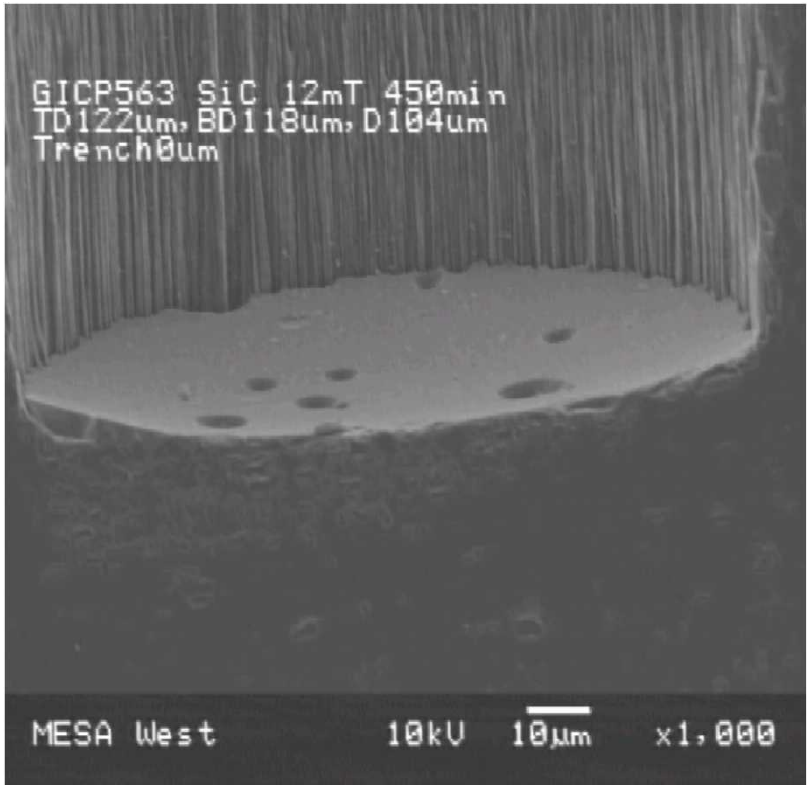
Trenching Eliminated





Temp	25C	Press	12 mTorr
ICP	750 W	rf	100 W
dc-bias	305 V	SF_6	50 sccm
O_2	10 sccm		

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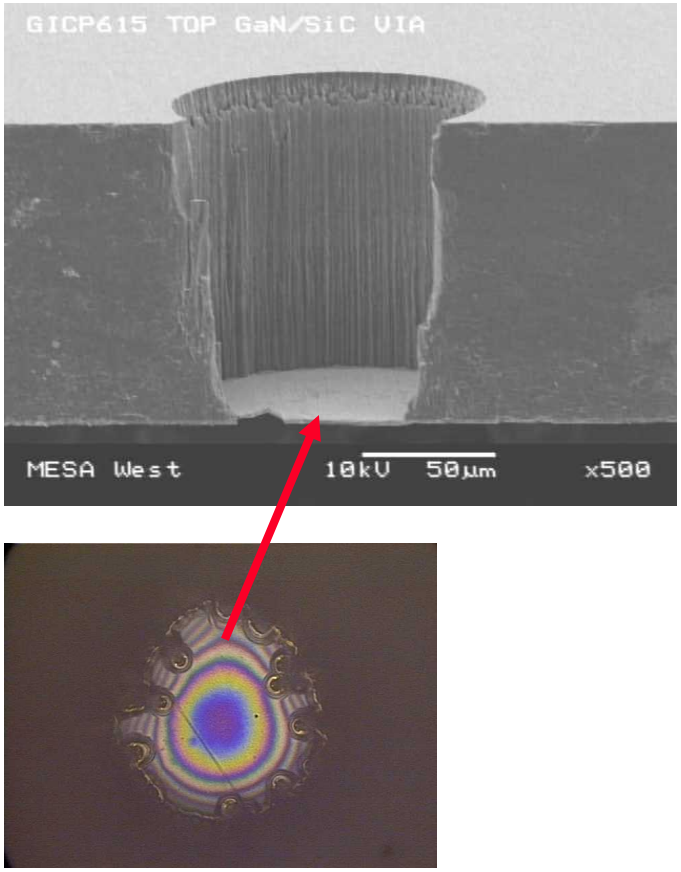
Etched Vias: Stop on GaN

- SF_6/O_2 plasma 750 W/100W/12 mTorr
- Etch time ~ 445 minutes
- SiC etch rate ~ 0.225 µm/min
- SiC:GaN etch selectivity is acceptable
- Optically determine end point (GaN has rainbow interference pattern)
- Via yield is low 30 – 40% for ¼ of a 2" wafer



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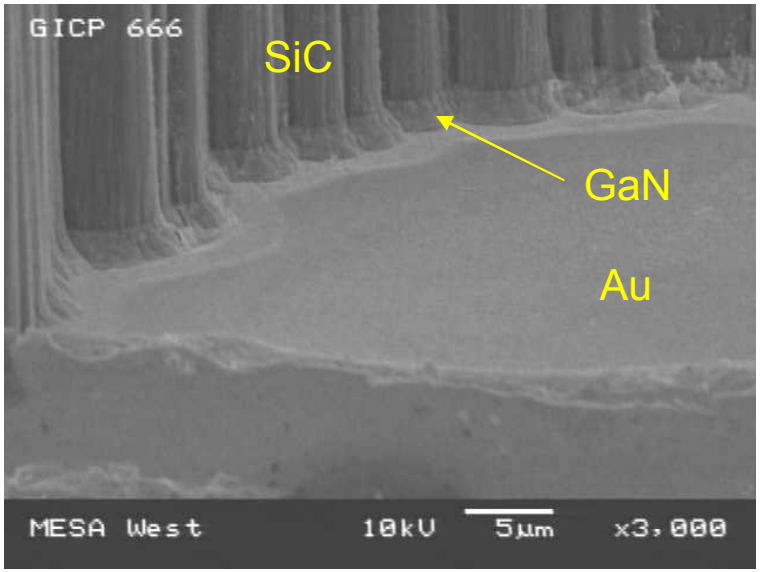
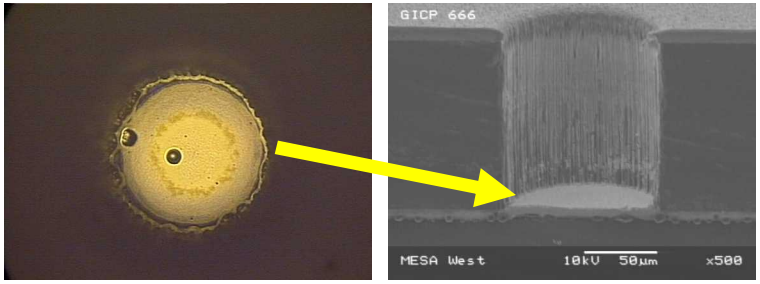
Etched Vias: Stop on Au

- SiC etch 750W/100W/12 mTorr SF_6/O_2
- GaN etch 350W/25W/3 mTorr Cl_2/BCl_3
  - GaN etch rate ≈ 1900 Å/min
  - Selectivity to Au ≈ 5:1
- SiC thickness uniformity critical due to high sputtering rate of GaN and Au
- Au at base of wafer (~4500 Å) reasonably unaffected by Cl-based etch
- End point determined optically when no GaN remains





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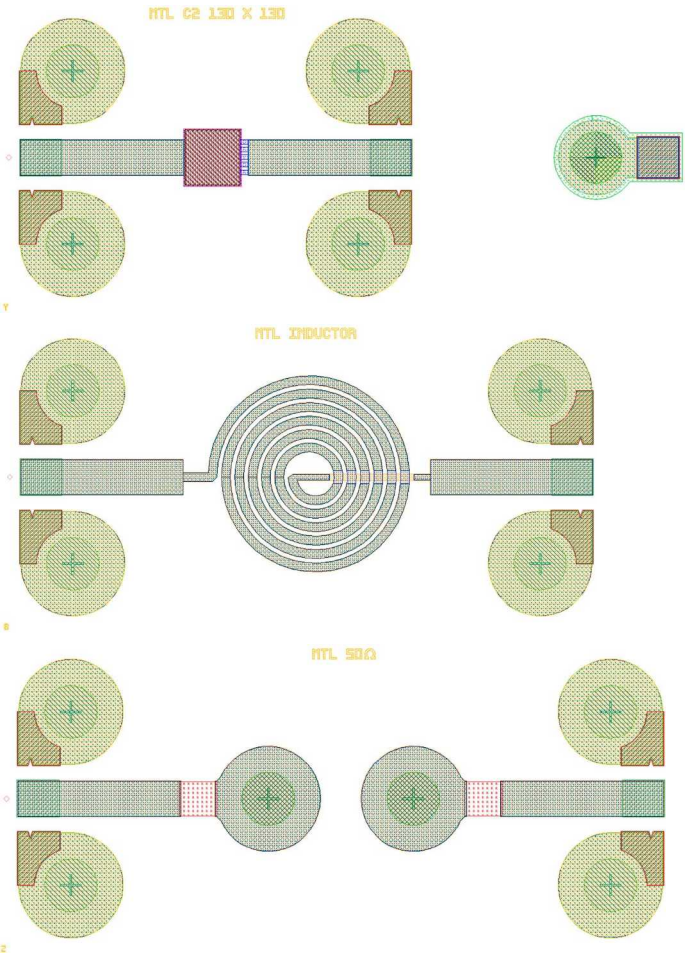
Etched Vias: Passive Structures

- Work with thinned samples extended to incorporate Passives2005 maskset structures patterned on GaN prior to SiC lapping
- Structures include resistors, capacitors, inductors, and transmission lines in CPW (no via) and Microstrip (via) geometries
- Mask also includes DC via test structures (single and serpentine chain) of various lengths
- Structures used for eventual MMIC design and GaN RF cal kit
- Work with thinned samples to date shows need to improve SiC lapping/polishing process



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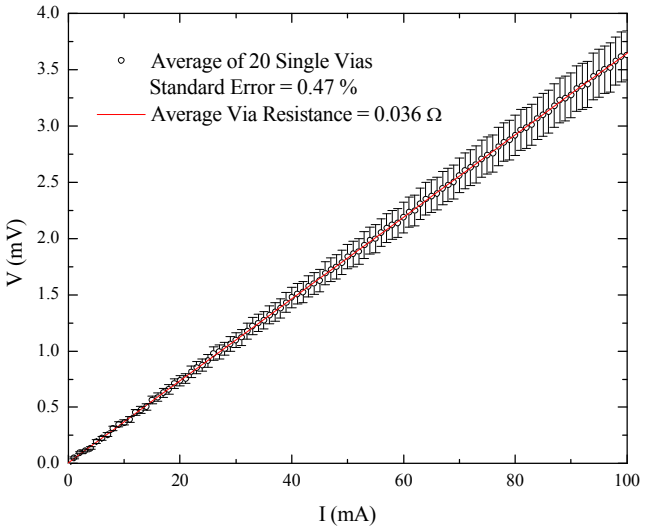
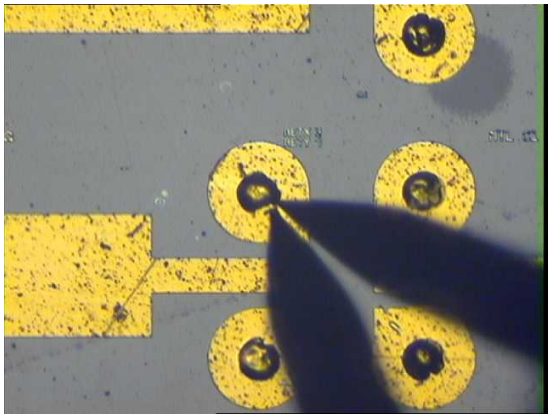
Etched Single Vias: Electrical Test Data

- Via etch process completed with 1000 Å Ti/10000 Å Au seed sputtered on backside followed by 5 µm Au plating
- Average of 20 single vias gives average resistance of 0.036 Ω
- Calculation shows that a filled via of 125 µm ∅ X 110 µm deep will have a resistance of 0.0002 Ω
- An annular (non-filled) via with the above average resistance will have a (wall) thickness of ≈ 0.60 µm
- Agrees with SEM cross sections of 5 µm plated test pieces
- Linear I-V (resistance = 0.035 Ω) out to 450 mA test limit





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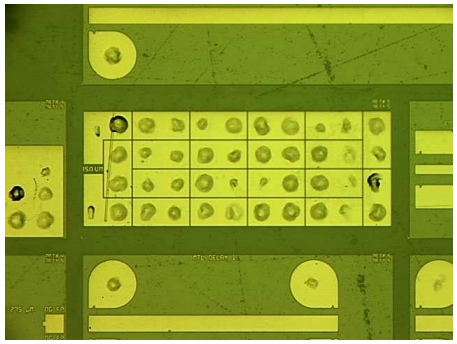
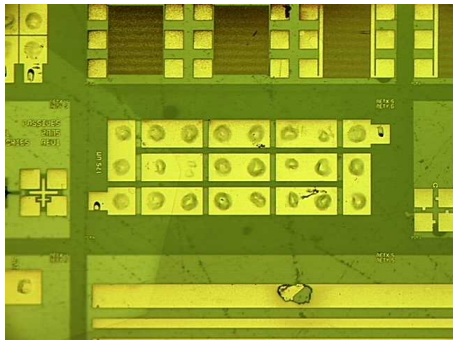
Serpentine SiC Via Chains: Electrical Data

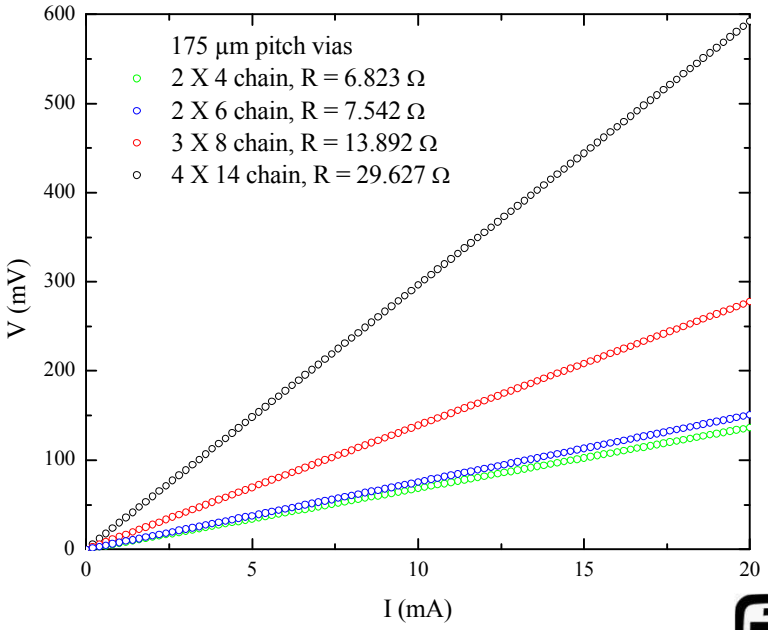
- Electrically tested via chains in 2 X 4, 2 X 6, 3 X 8, 4 X 10, and 4 X 14 patterns
- 1000 Å Ti/1 µm Au sputtered backside metal
- Backside streets etched with combination of wet etching and reactive ion beam etching (RIBE)
- High chain resistance (R) due to thin metal coverage on via sidewalls (~400 nm)
- Sidewall thickness approximately equal to RF skin depth (δ) in Au at Ku band (18 GHz = 580 nm)
- Indicates thicker (> 1 µm) sputtered metal layers required for low resistance vias (δ ↔ R)



4 X 10 Chain (150 µm pitch)



3 X 8 Chain (175 µm pitch)



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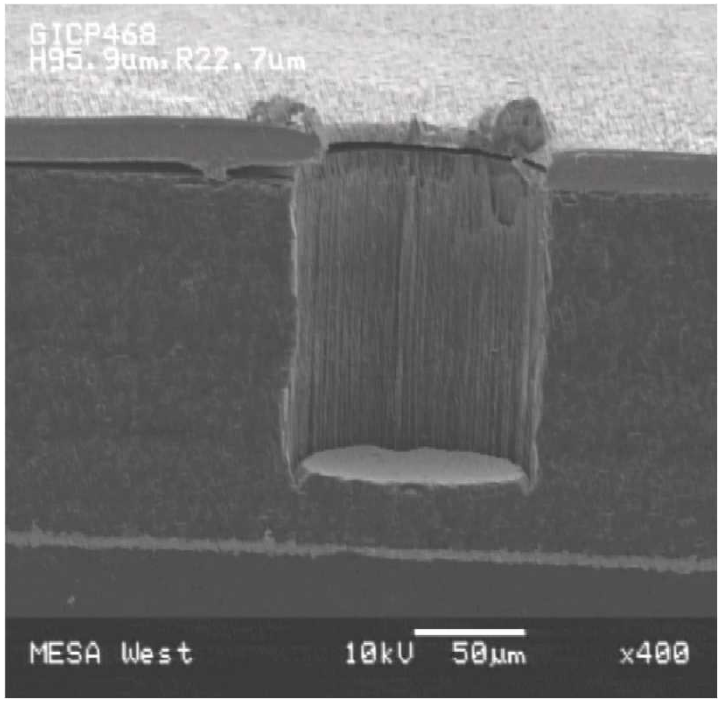
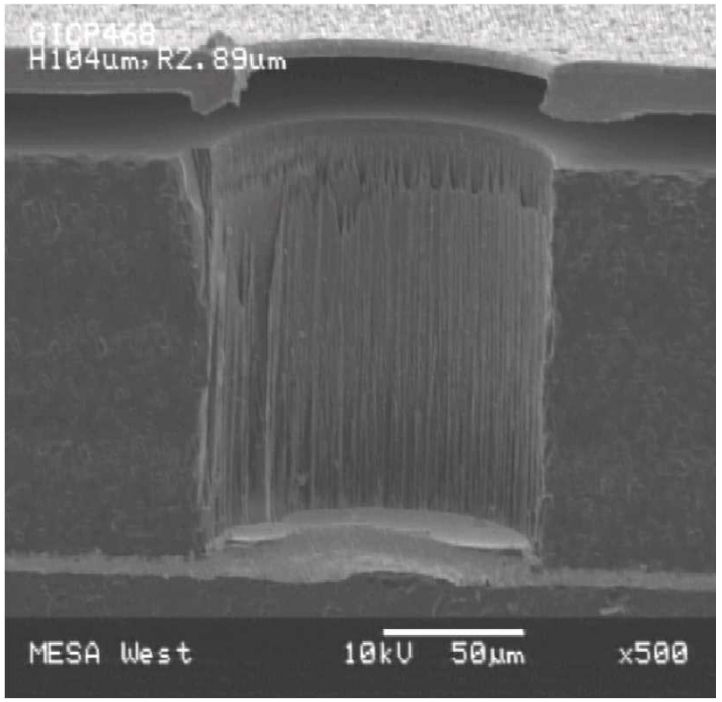
Etched Vias: Thinned SiC Wafers

- Non-uniform lapping/etching observed
- Possible solutions:
  - Improve lapping uniformity.
  - Optimize selectivity to frontside structure.





GICP 468: 10 to 20 µm difference in etch depth across wafer
May result in breakthrough of front side Au contact pads

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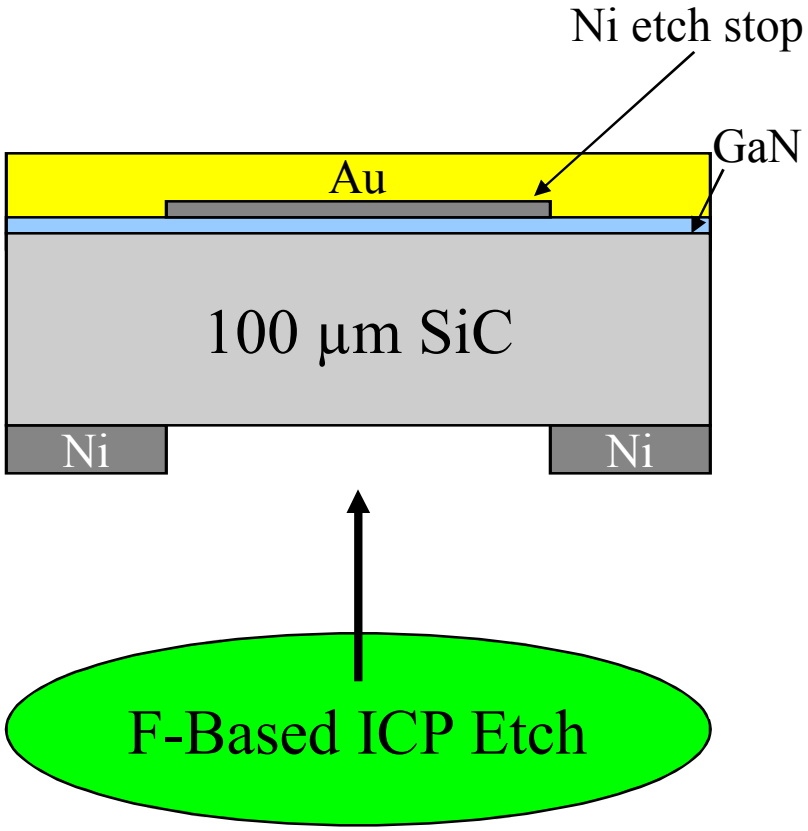
Issues to be Resolved: Au Breakthrough

- Au punch through during etch process results in failed vias
  - Results from non-uniform lapping and non-uniformity of the etch process
  - SF_6/O_2 high power ICP etch is not completely selective to GaN
    - Experiments demonstrate ~7:1 selectivity
    - GaN can be etched away in thinner areas, exposing Au which is then punched through
- Goal
  - Increase etch time before breakthrough occurs

Au Breakthrough: Ni Etch Stop

- Goal: Eliminate Au breakthrough during etch
- GaN should act as an etch stop, but is less effective at high ion energies
- Lower rf-power to improve selectivity, but plasma is unstable and SiC etch rate is decreased
- Solution: Introduce a more effective etch stop layer into device structure

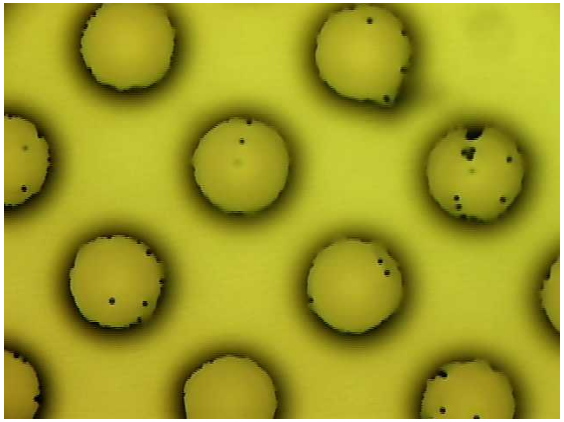


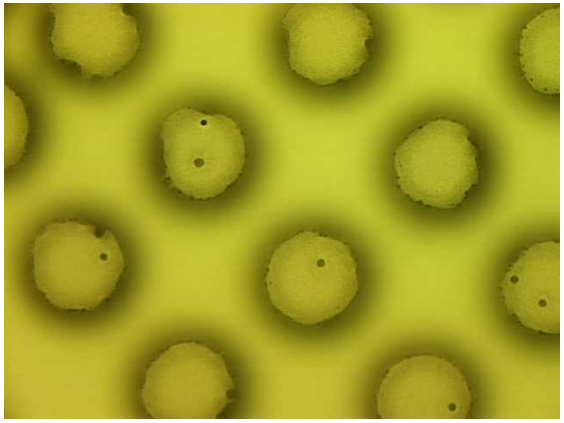
Au Breakthrough: Ni Etch Stop

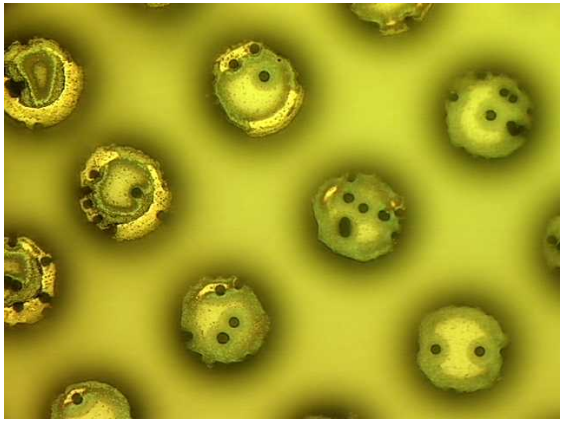
- Ni chosen due to availability and known selectivity from plated Ni via mask of ~ 50:1
- Experiments done on evaporated Ni indicate similar selectivity to SiC
- 1500A of Ni should allow for an overetch of ~ 10% or ~ 9 μm
- Combined with selectivity of GaN, this should allow for sufficient over etch times to compensate for non-uniform lapping and etch variation across a wafer

Au Breakthrough: Ni etch stop

- Test conducted on thinned wafer with blanket Ni and Au on front side
- ¼ of 2” wafer purposely lapped poorly to determine effectiveness; wedge of > 15 μm present
- Test successful, with no breakthrough 70 minutes of overetching (~15 % overetch)







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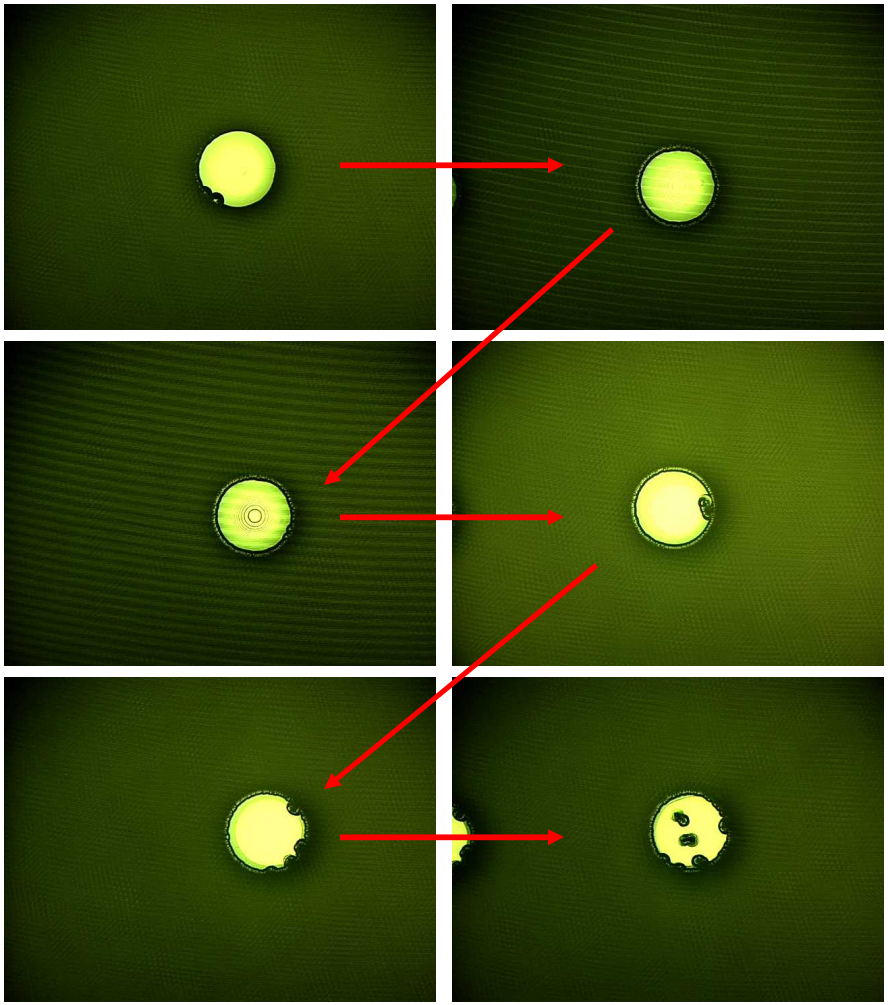
Indicators of SiC Breakthrough

- Ringed interference pattern observed as SiC thins
- Further etching reveals Au initially in center of via, expanding outward as etch time increases



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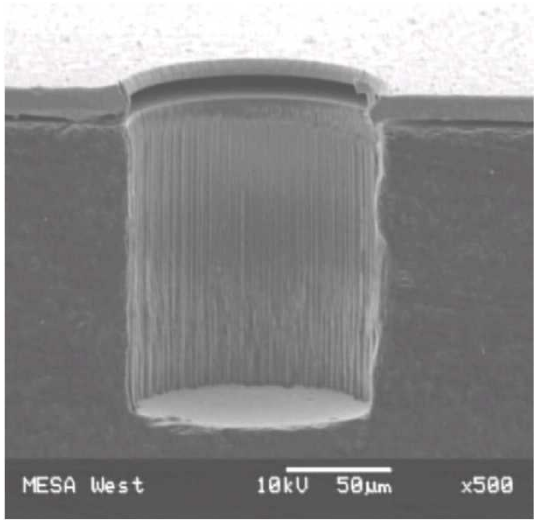
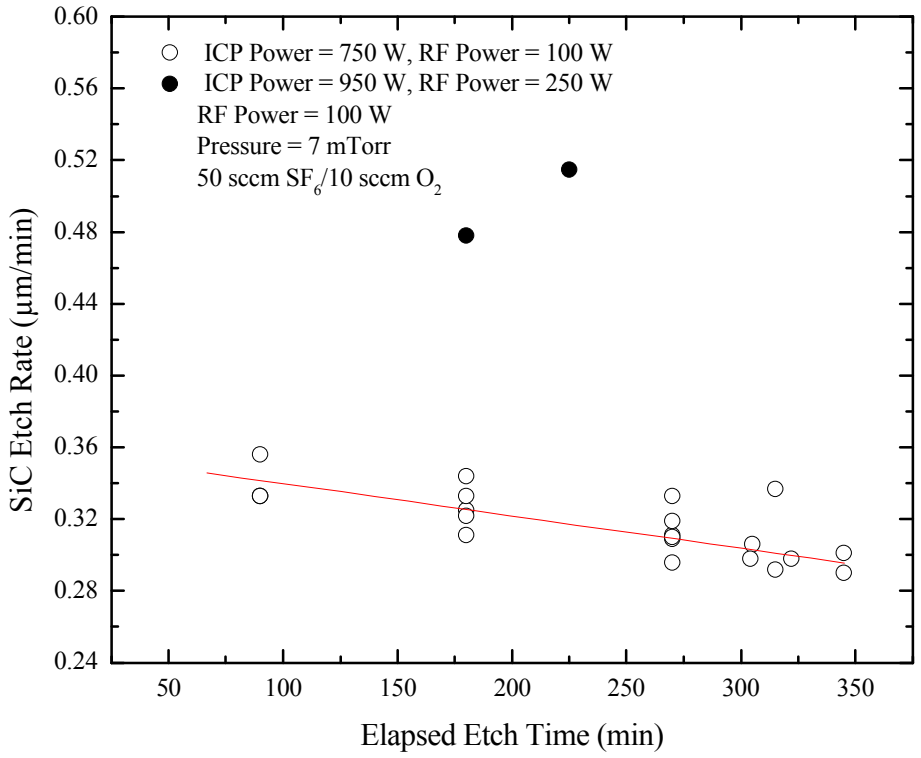
Issues to be resolved: Increase etch rate

- Etch rate very slow
  - Starting point is 0.25 μm/min
  - Rate decreases with increased etch depth
- Goals
  - Determine rate limiting factor
  - Improve process to increase rate without sacrificing improvements in trenching, micro-masking, or sidewall profile





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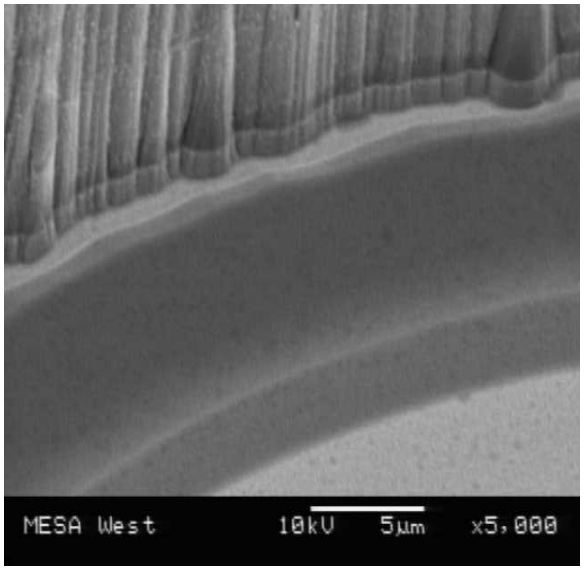
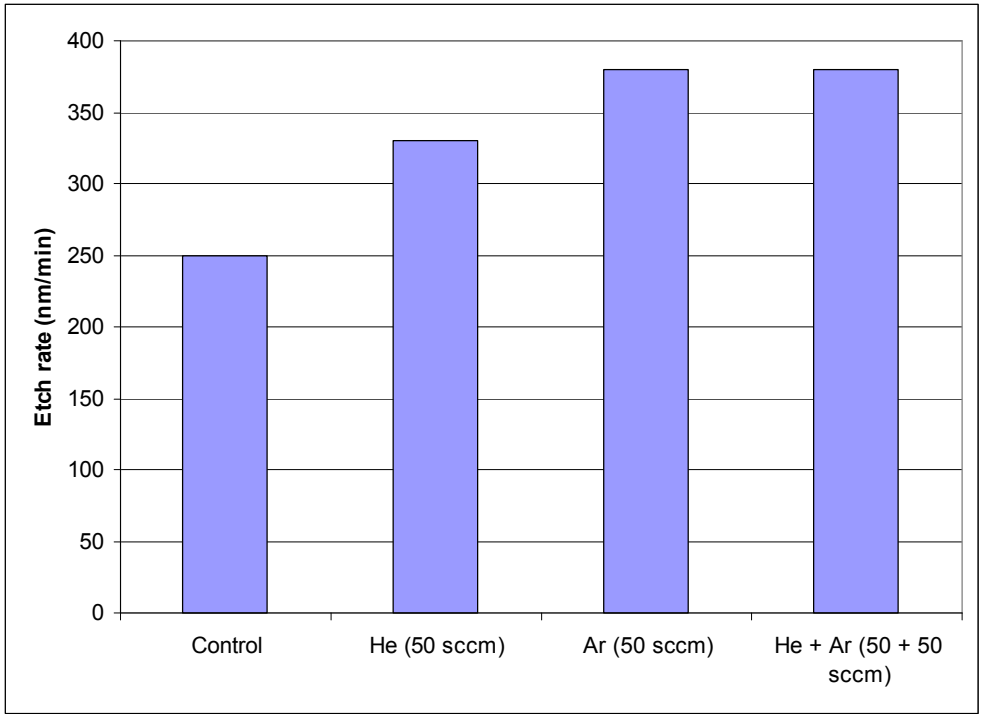
Increasing etch rate: Etch gas additives

- Goal: Increase ER by introducing gases to increase sputtering of SiC
  - Ar only
  - He only
  - Ar + He
- Etch rate increased with He and/or Ar
  - Highest etch rate with Ar implies a physical etch process





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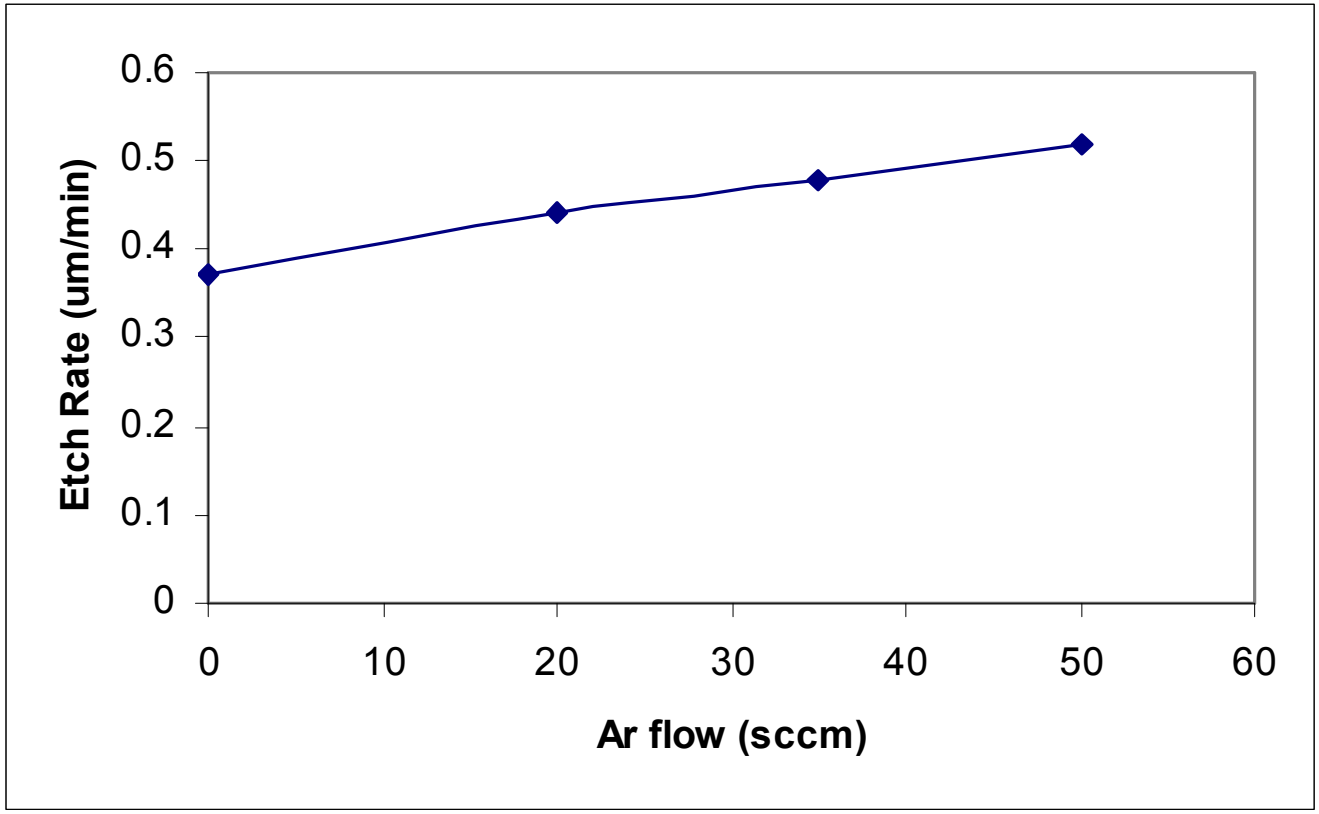
Increasing etch rate: Ar flow dependence

- Goal: determine optimal Ar flow rate
- Ar flows of 0, 20, 35, and 50 sccm examined
- 50 sccm (highest available) determined to be optimal



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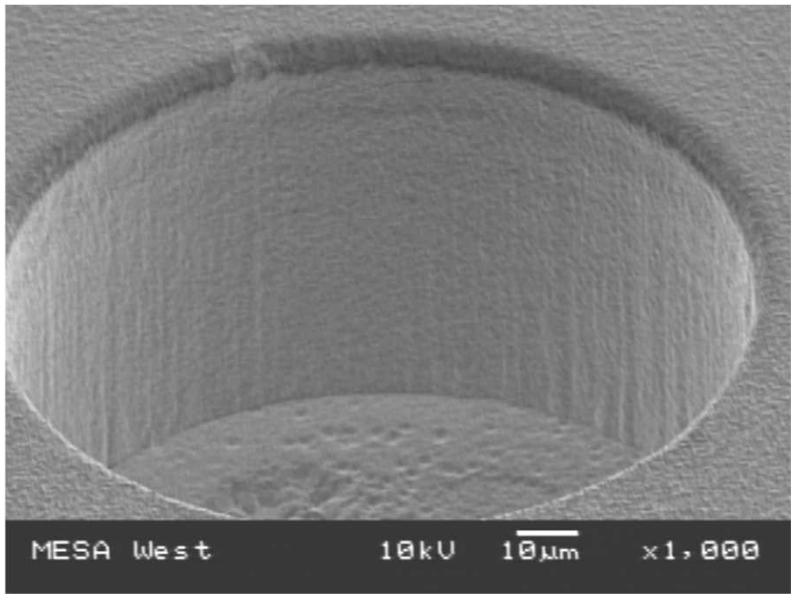
Results: Yield

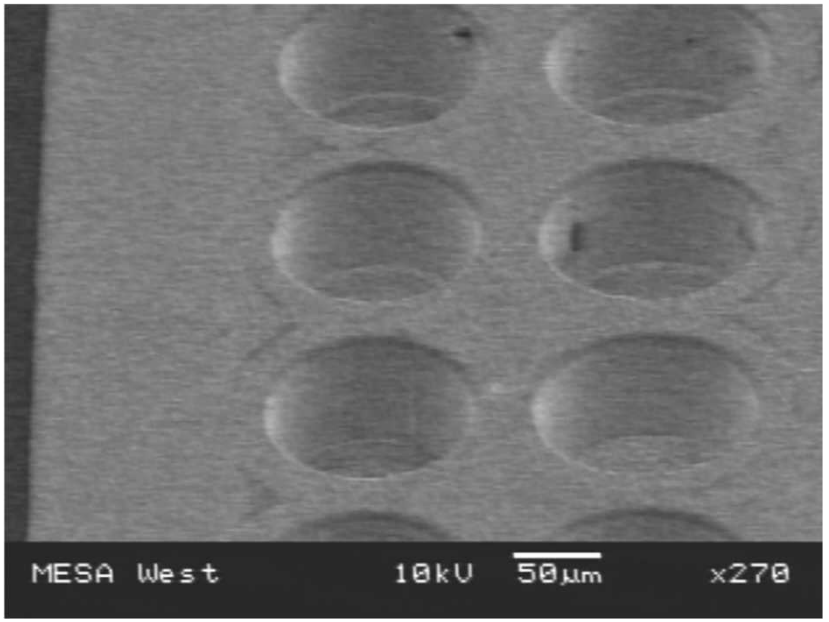
- Yield determined optically for test pieces is consistently close to 100%
- Pieces are either .75x.75cm or ¼ of 2”
- Results for first full 2” wafer are promising
  - No breakthrough despite 10 µm wedge
  - Almost all vias appear to be functional; exact percentage unknown until electrical testing

Experiment	Parent wafer	Yield
15	**NE0503**	**100%**
16	**NE0503**	**100%**
17	**SX-117-06**	**100%**
18	**A**	**100%**
19	**A**	**100%**
20	**NE0503**	**100%**
21	**NE0503**	**100%**
22	**NE0503**	**100%**
24	**NE0503**	**100%**
25	**NE0503**	**100%**
26	**NE0503**	**100%**
27	**NE0503**	**100%**
28	**NE0503**	**100%**
39	**NE0503**	**100%**
30	**NE0503**	**100%**
32	**SX-117-06**	**100%**

Au Plated Vias



SiC vias plated with Au



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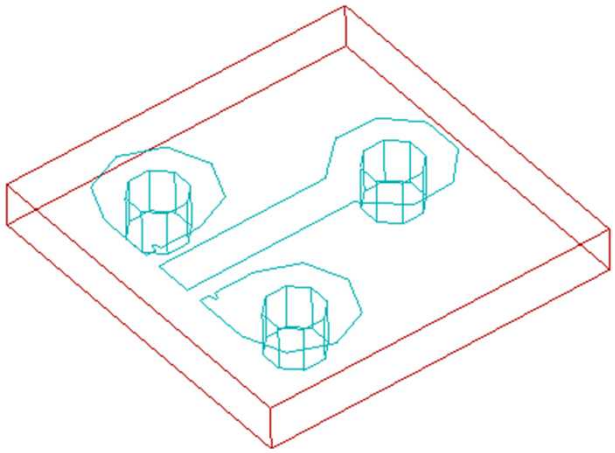
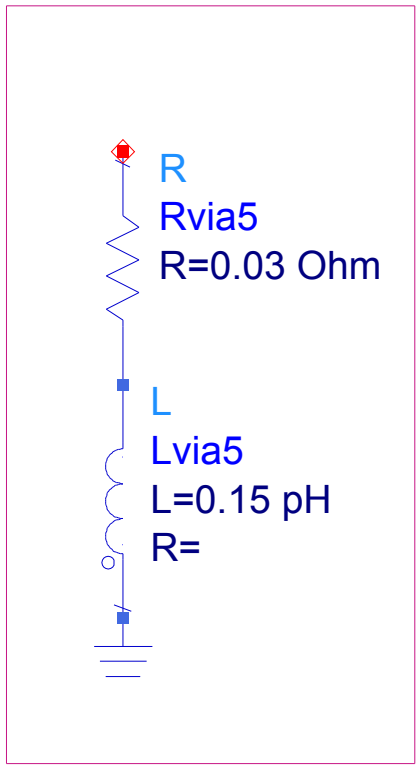
GaN MMIC Via
Circuit Model vs. RF Measured Data

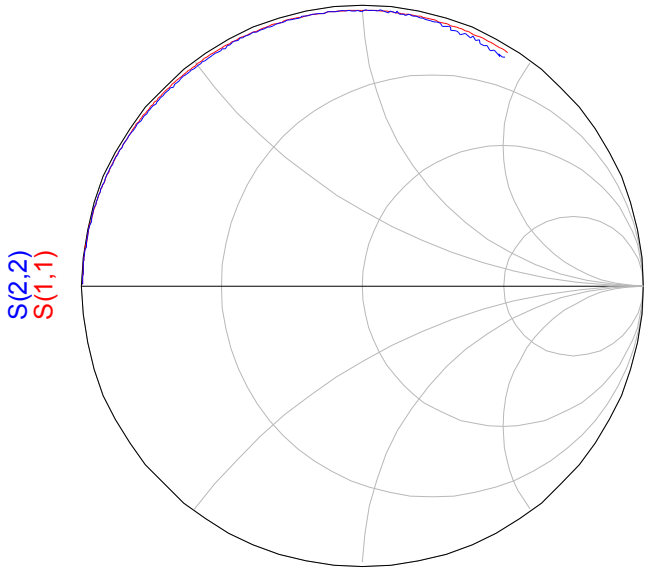


3-D Drawing of
Via Structure Measured

ViaModel



Red = Modeled
Blue = Measured



RF Impedance Plot

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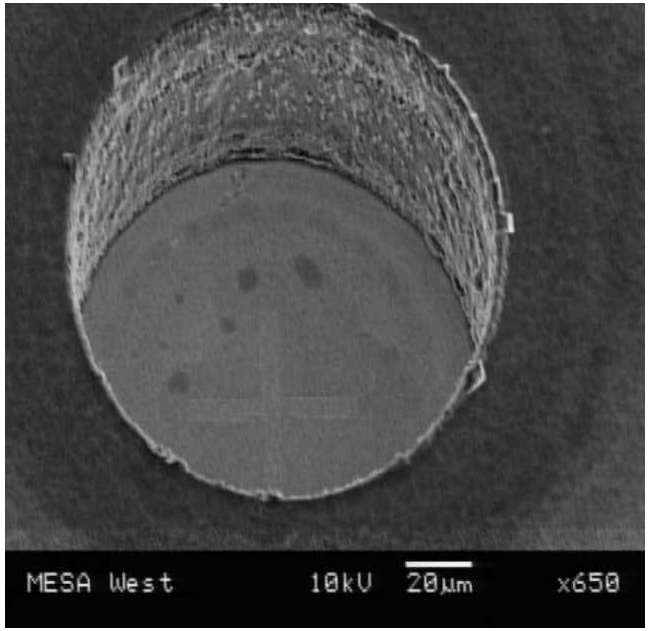
Conclusions

- Micro-masking has been reduced to acceptable levels with an Ar pre-clean step and the addition of Ar to the plasma chemistry
- Etch rate has been increased with the addition of Ar
- Lapping non-uniformity issues have been addressed
- Trenching has be eliminated with higher pressure
- Result: >95% via yield for thinned SiC wafers



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