Microsystems
Science, Technology & Components

SAND2015-5524C

Progress and Challenges in Developing a Reliable Embedded ReRAM Memory for Hostile Environments

Microelectronics Reliability and Qualification Workshop (MRQW)

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Outline

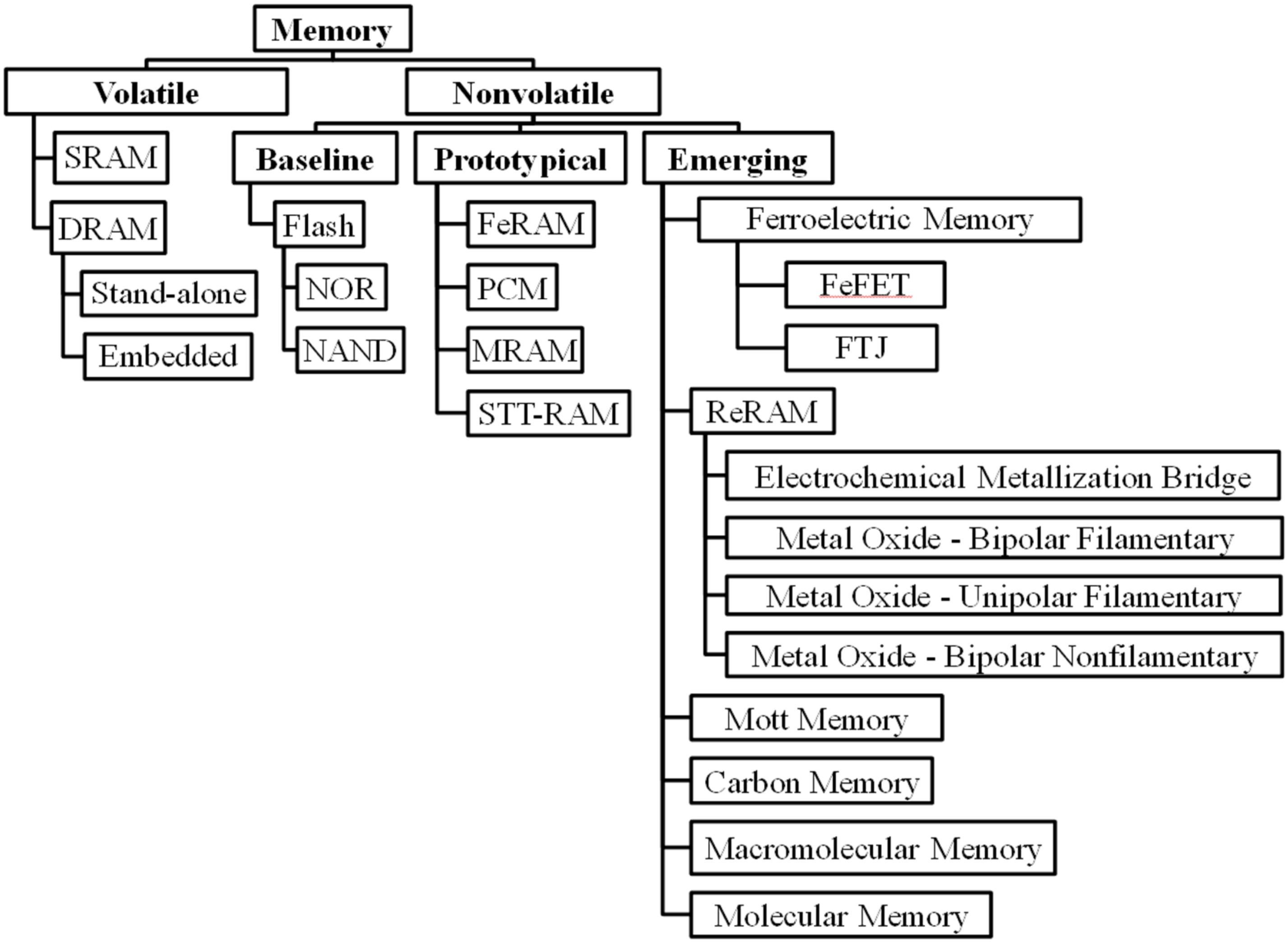
- **Introduction and Motivation**
- **ReRAM Development**
- **Characterization of Reliability**
- **Characterization of Radiation Effects**
- **Summary and Next Steps**

Emerging Memory

samsung.com

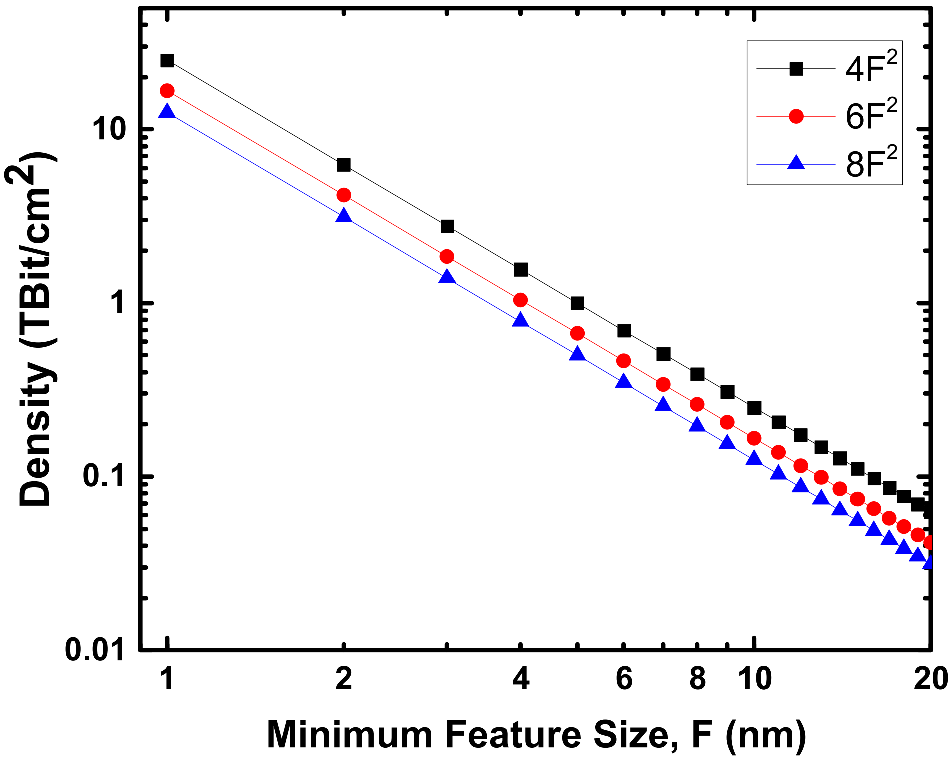
- We are in a significant era for memory
- <u>NAND Scaling:</u>
  - Amazing progress in recent years: Samsung has a 32 layer process enabling 256 megabit per die
  - 3D will quench density issues temporarily
  - Reliability suffers with scaling; 12 nm is theoretical FG limit
- <u>DRAM Scaling:</u>
  - Struggling to maintain reasonable eq. oxide thickness
  - Dielectric for cells <20 nm still TBD
- Limitations in sight for both of these giants!
- Storage Class Memory
  - Magnetic to DRAM latency gap
- End of transistor scaling: no obvious replacement
- End of flash/DRAM scaling: replacements on the horizon!

Emerging Memory Taxonomy

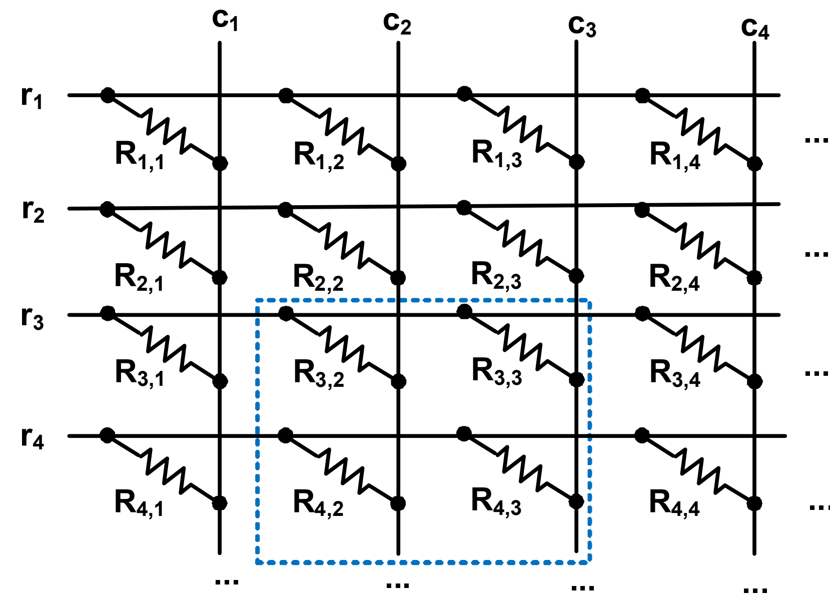


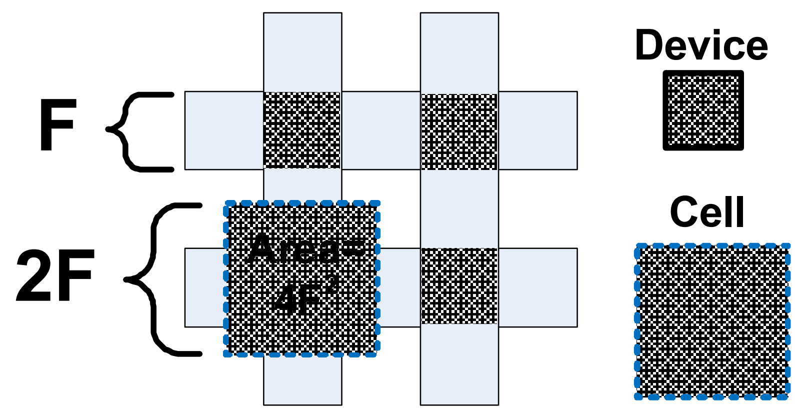
Resistive Crossbar Memories

- F=Feature size
- Max areal density possible → $4F^2$

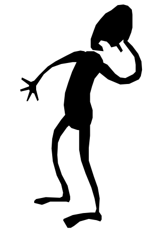


Marinella and Zhrinov, in Emerging Nanoelectronic Technologies, Wiley, 2014.





Emerging Memory Comparison



Biggest challenge for ReRAM: Catch-up

	DRAM	Flash (NOR-NAND)	ReRAM/Memristor	STT-MRAM	PC-RAM
	Production (30 nm)	Production (16 nm)	Development	Production (65 nm)	Production (45 nm)
Min device size (nm)	20	18	<10	16	<10
Density (F^2)	6	4+	4	8-20	$4F^2$
Read Time (ns)	< 10	10^5	2	10	20
Write Time (ns)	< 10	10^6	2	13	50
Write Energy (pJ/bit)	0.005	100	<1	4	6
Endurance (W/E Cycles)	$>10^{16}$	10^4	10^{12}	10^{12}	$>10^9$
Retention	64 ms	> 10 y	> 10 y	weeks	> 10 y
BE Layers	FE	FE	4	10-12	4
Process complexity	High/FE	High/FE	Low/BE	High/BE	Low/BE

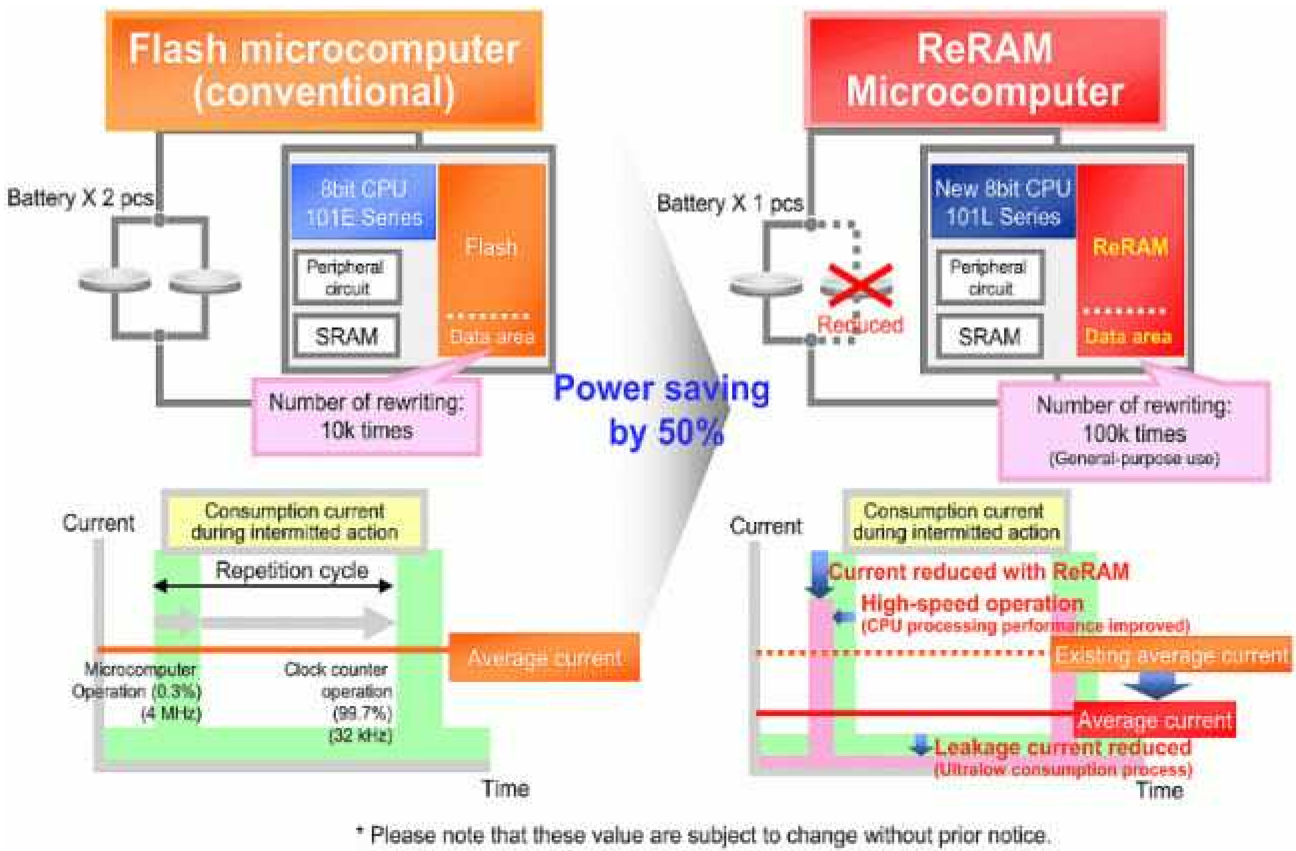
Biggest challenge for STT-MRAM: Balancing Retention/Scaling/Temperature/Write current

Biggest challenge for PCM: High erase current

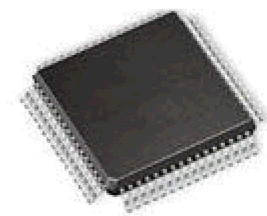
*****DISCLAIMER: Due to 10s of thousands of references on these technologies – many of these numbers are not universally agreed on!**

Panasonic MN101L ReRAM MCU

- **First bipolar metal oxide commercial product**
- **Power and time saving over flash MCU**



panasonic.com



Space Computing

- Sensors can collect terabytes of data
- <u>Stringent computer/memory requirements</u>
  - Radiation-hard: Total dose, single event, etc.
  - High reliability (10-15+ year missions)
  - Low energy
- <u>Desired</u>
  - High density
  - Fast read/write
- The leading emerging memories are *not charged based* (like flash) and hence are more resilient to radiation
  - *This will provide a major paradigm shift for space computers*!

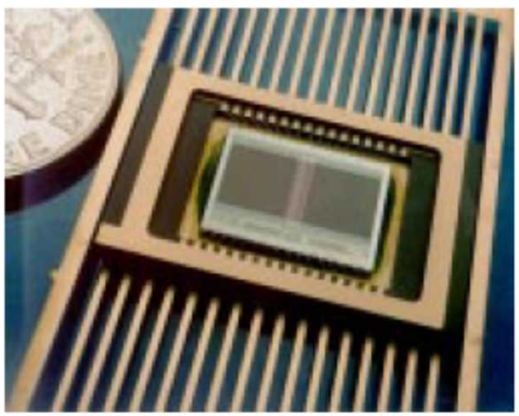
Orbital.com

Rad-Hard Nonvolatile Memory

Commercially available rad-hard nonvolatile memories

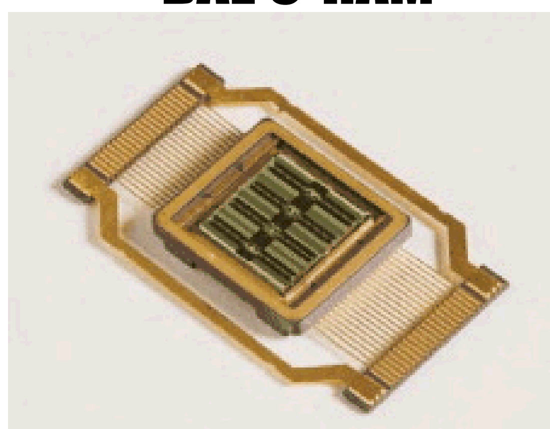
- **NG EEPROM: 1Mbit, 100ms write, 10^4 cycles, 1.25µm RHCMOS**
- **BAE C-RAM: 4Mbit (planned 20 Mbit), 70ns write**
- **Honeywell MRAM: 16Mbit die, 140ns write, 10^{12} cycles**
- ***Rad-hard memory requires a rad-hard CMOS base process***

NG Rad-hard EEPROM



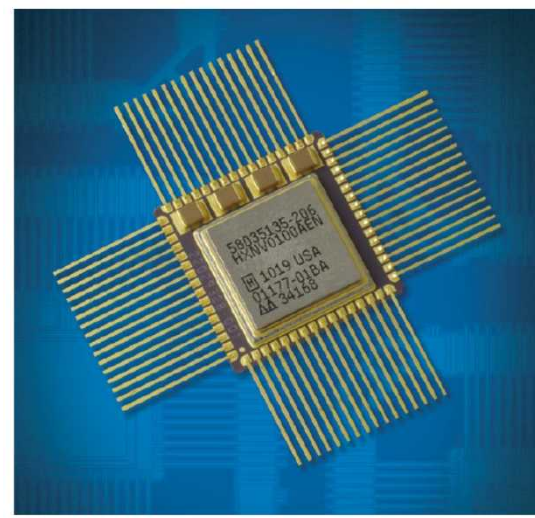
Rad Hard 256K EEPROM
northropgrumman.com

BAE C-RAM



baesystems.com

Honeywell M-RAM



honeywell.com

Outline

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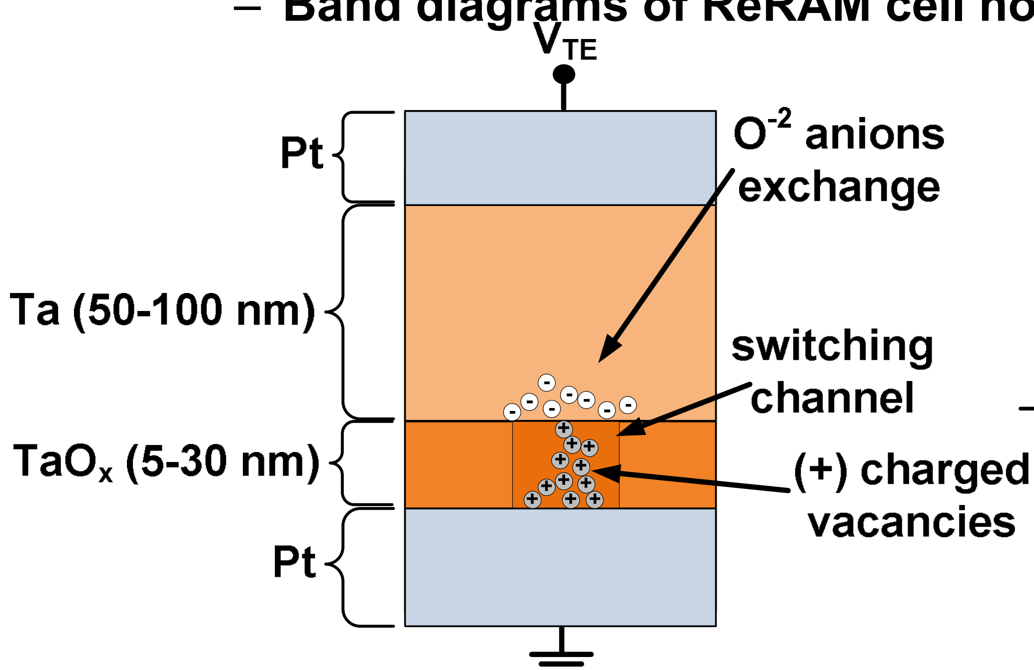
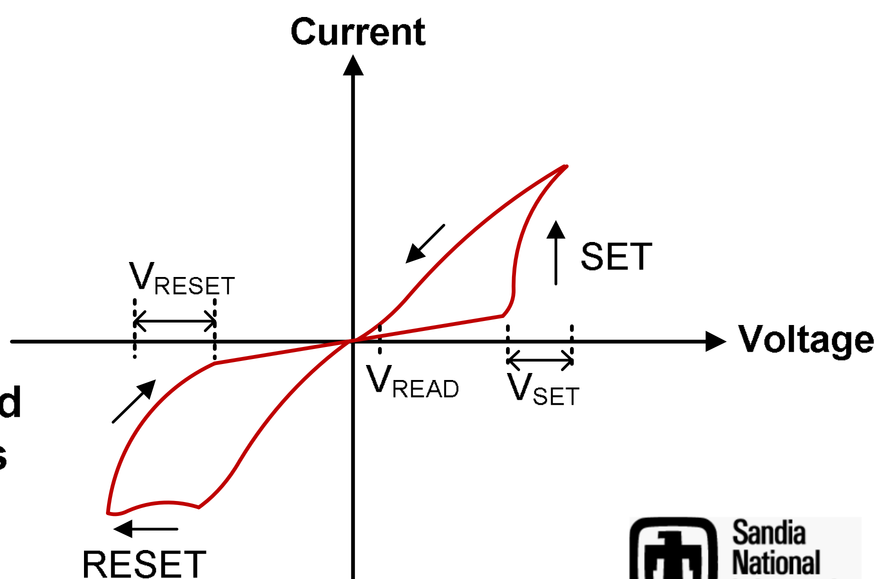
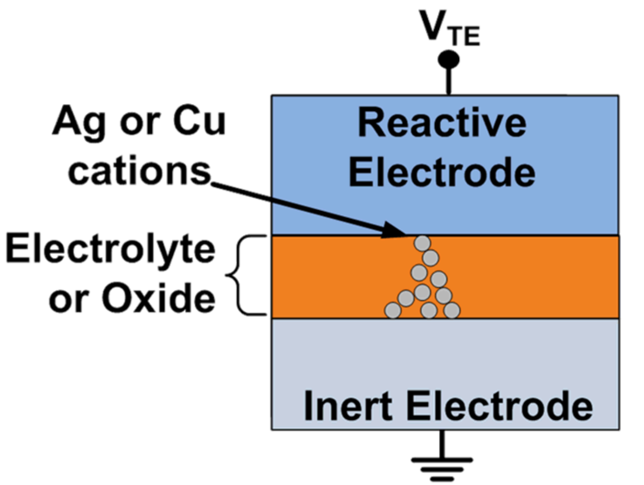
Bipolar Metal Oxide ReRAM

- "Hysteresis loop" is simple method to visualize operation
  - (real operation through positive and negative pulses)
- Hypothesized oxide resistance switching mechanism
  - Positive voltage/electric field: low R – O^{-2} anions leave oxide
  - Negative voltage/electric field: high R – O^{-2} anions return
- Common switching materials: TaO_x, HfO_x, TiO_2, ZnO
- Despite progress, details of switching mechanism still debated
  - Band diagrams of ReRAM cell not common!

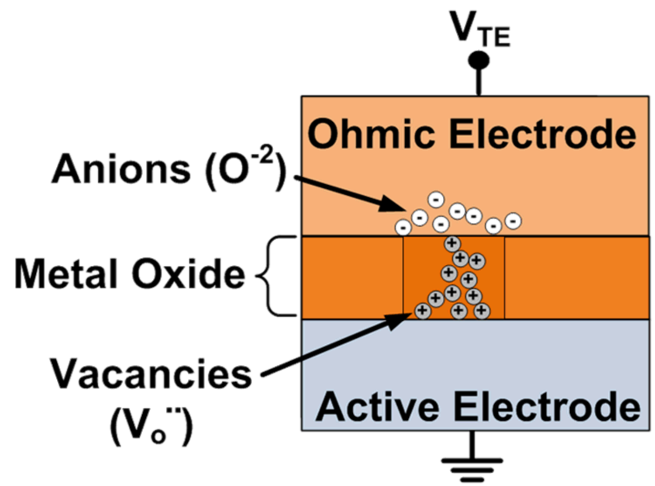




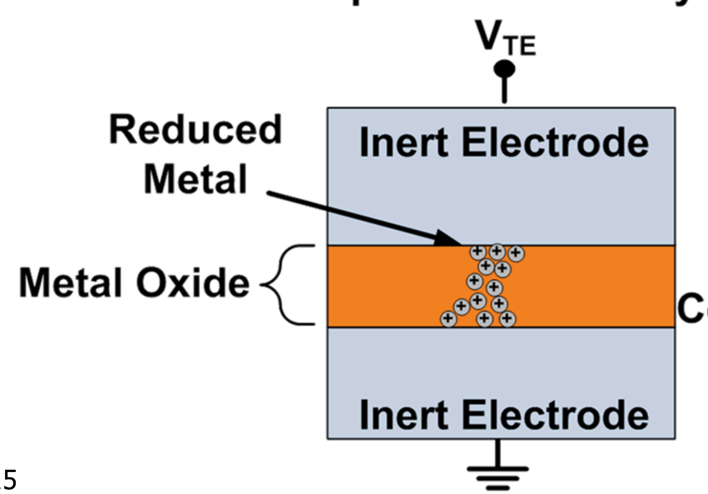
Electrochemical Metallization Bridge



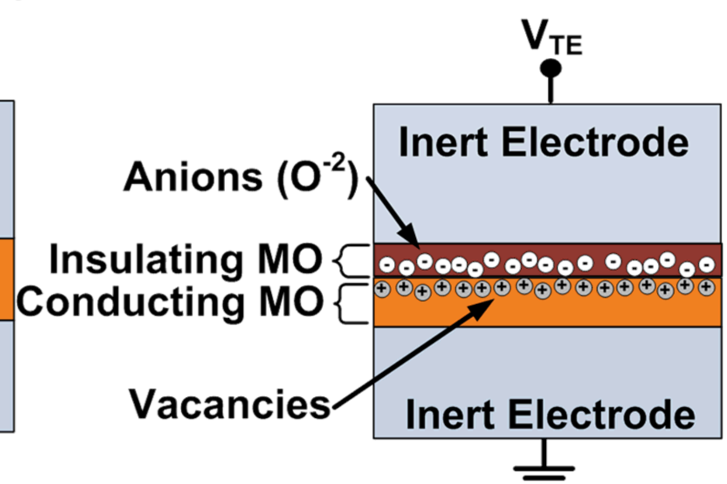
Metal Oxide: Bipolar Filamentary



Metal Oxide: Unipolar Filamentary



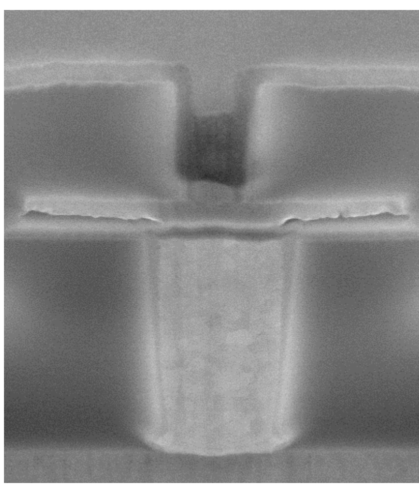
Metal Oxide: Bipolar Non-Filamentary

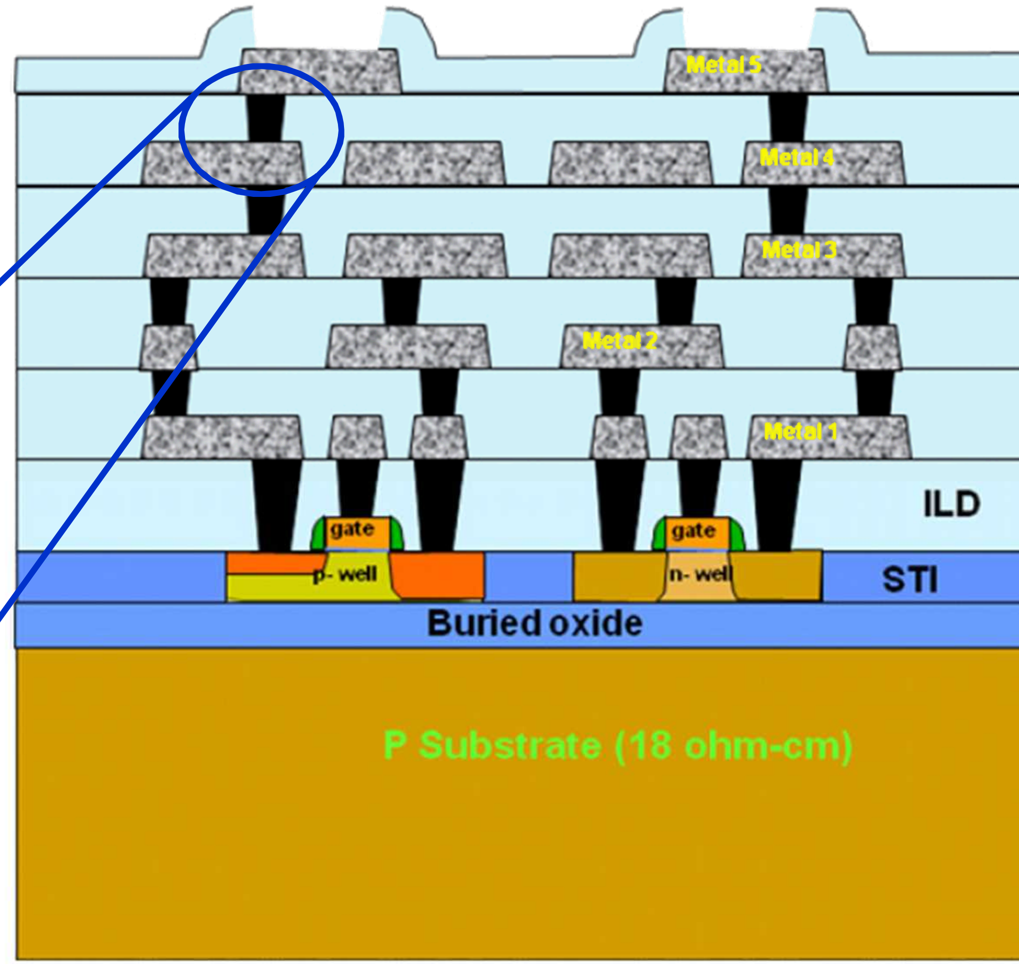


Sandia MESAFab Complex

Memristors + CMOS

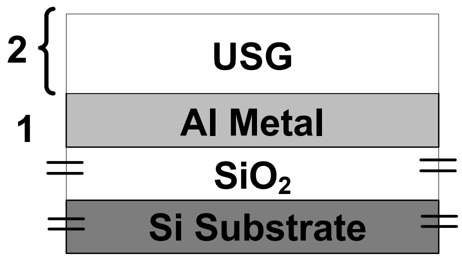
- Sandia CMOS7 Process
  - 3.3V, 350 nm, MOSFETs
  - SOI substrate
- ReRAM switching voltage ideal for this process



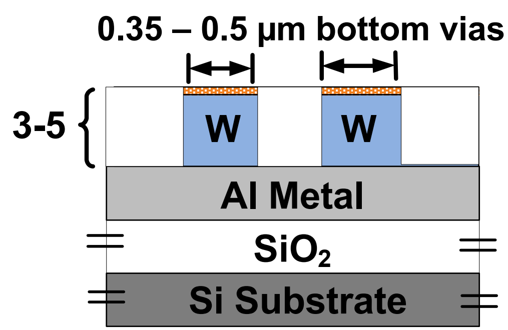


Process Flow

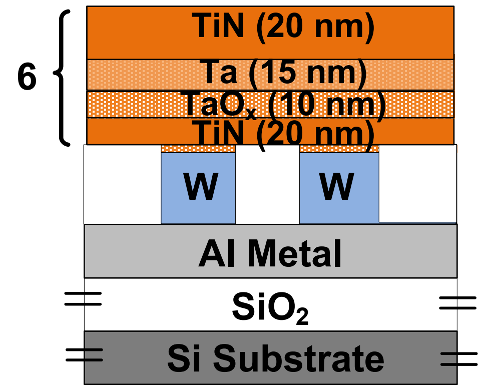
1. Deposit Bottom Metal (Al)
2. Deposit USG



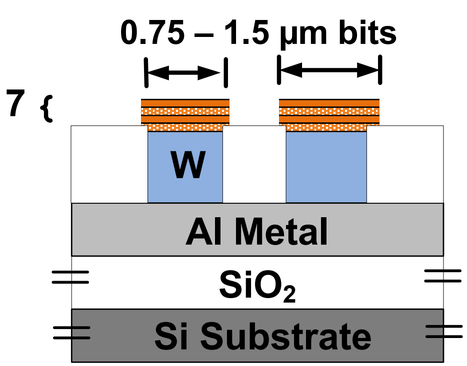
3. Etch via holes in USG
4. Deposit W and TiN layers
5. CMP



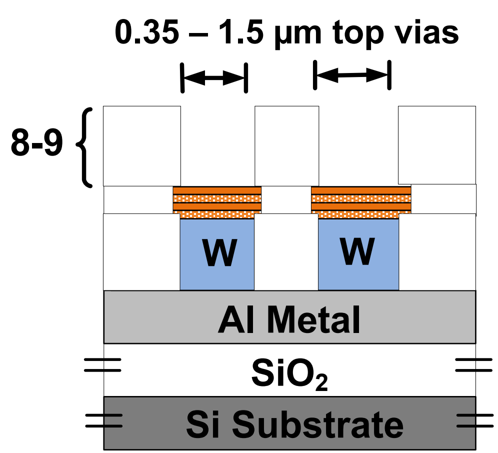
6. Deposit bit stack
(layers enlarged for clarity)



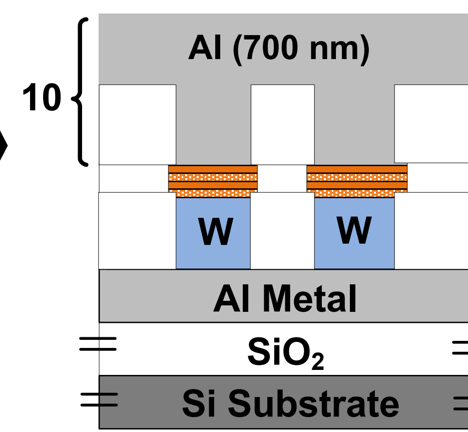
7. Etch bits



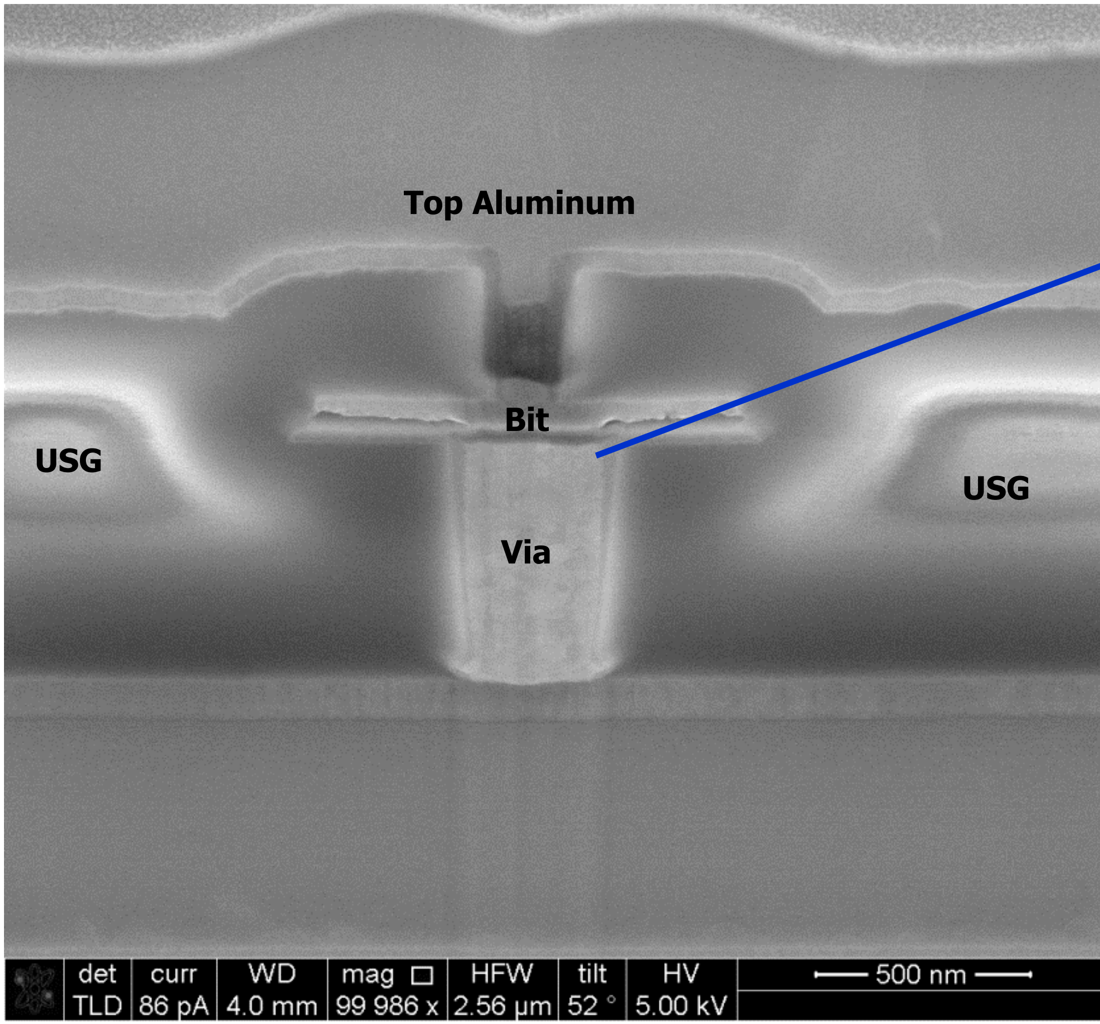
8. Deposit top USG
9. Etch top via holes in USG



10. Deposit top Al

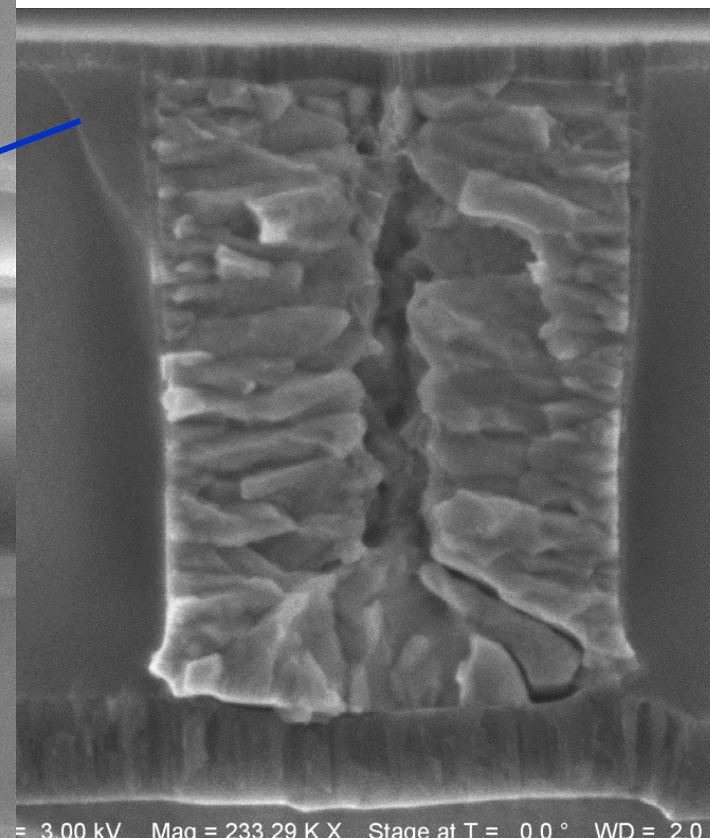


Final Structure

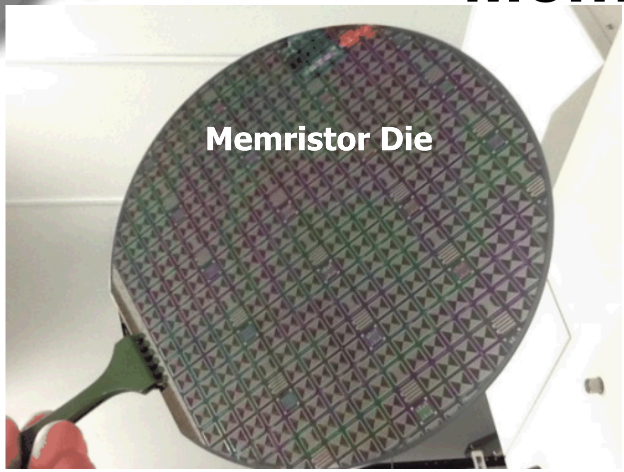


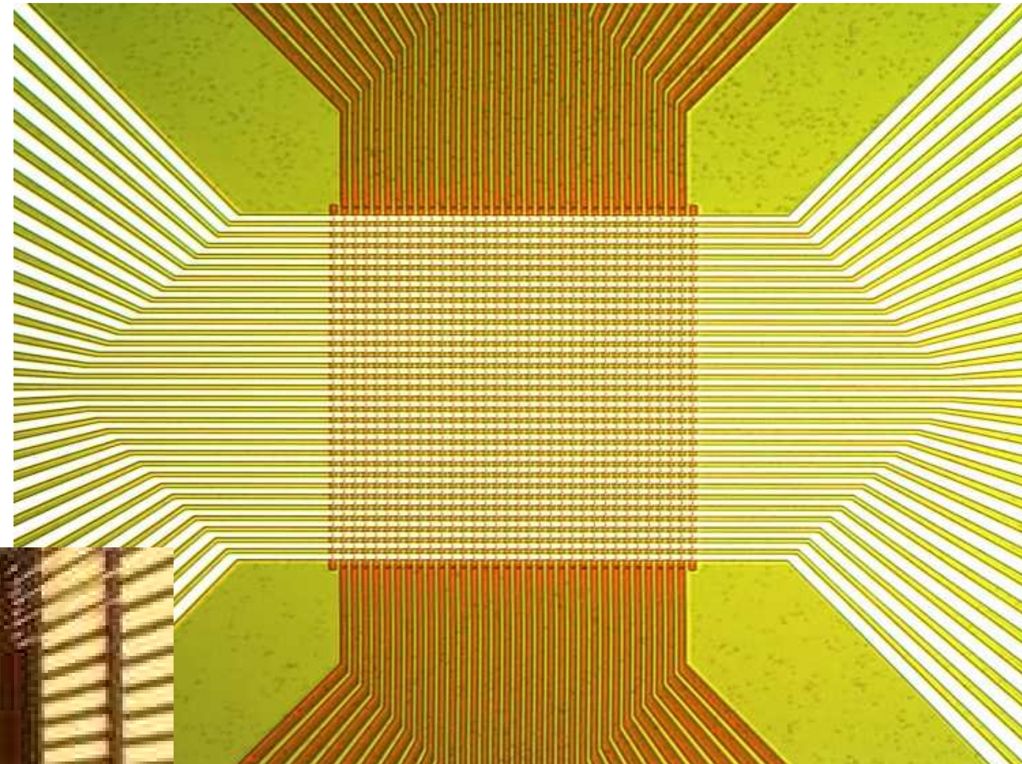
Important to have extremely flat surface under bit

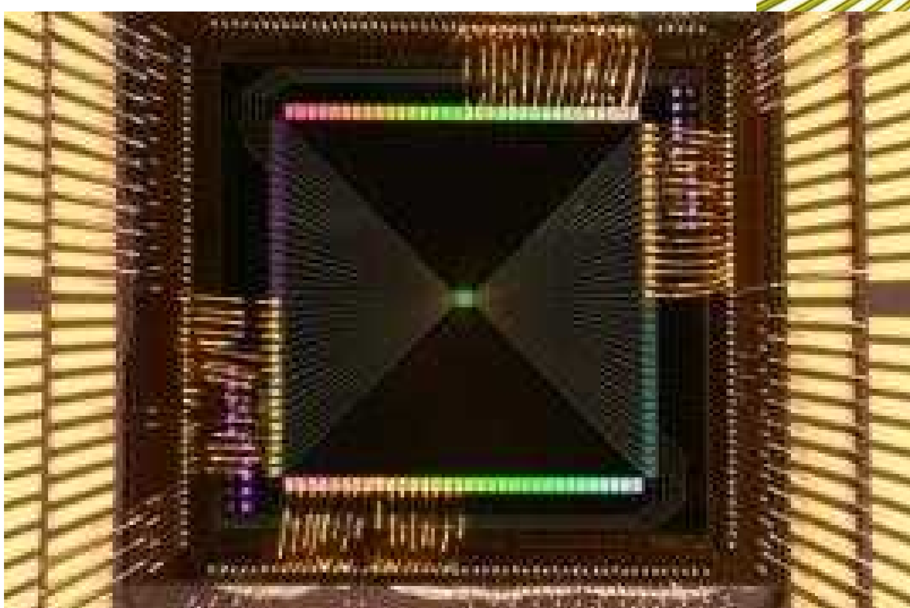
Polished TiN Surface



Memristor Crossbar Die



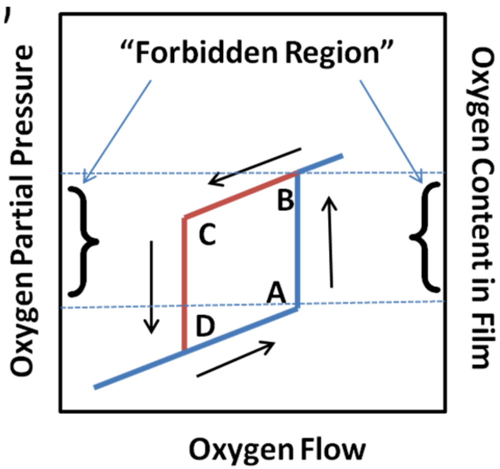




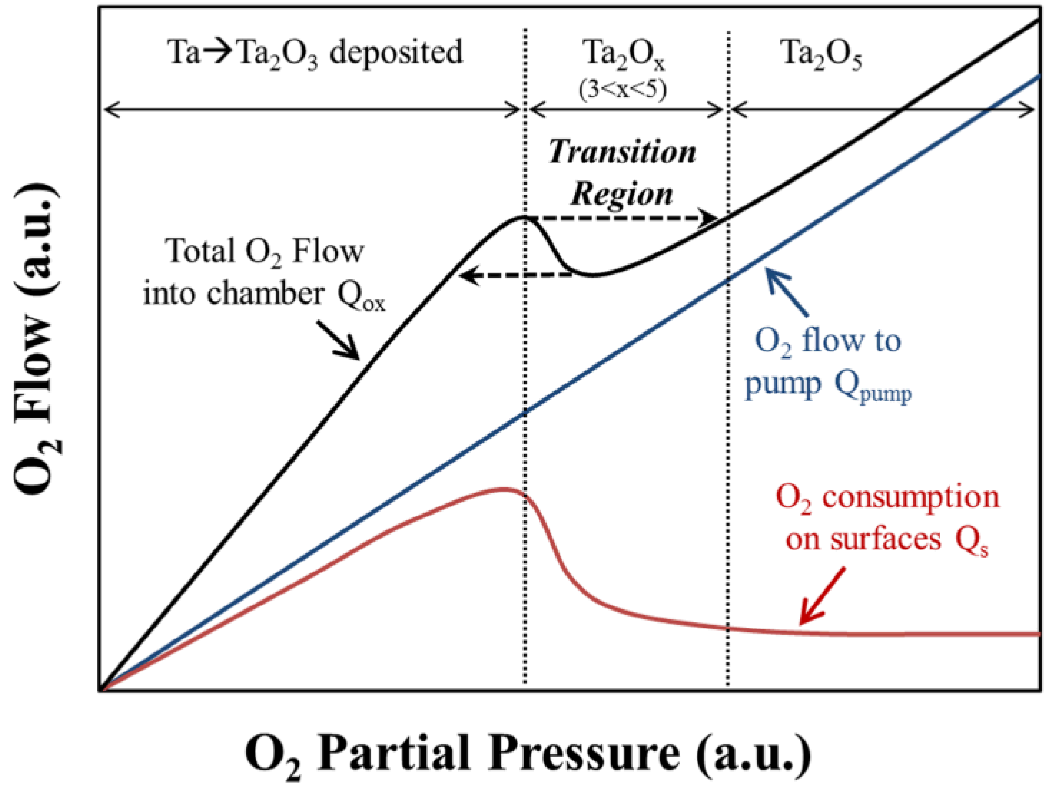
First Reliability Challenge: ESD!

Switching Film Development Challenge: Reactive Sputtering Stoichiometry

- **Target poisoning prevents easily reactive sputtering TaOx where 3<x<5**
- **This is the region we need to be in to get ideal ReRAM stoichiometry**
- **Used the forbidden region to calibrate flow-pressure with feedback**



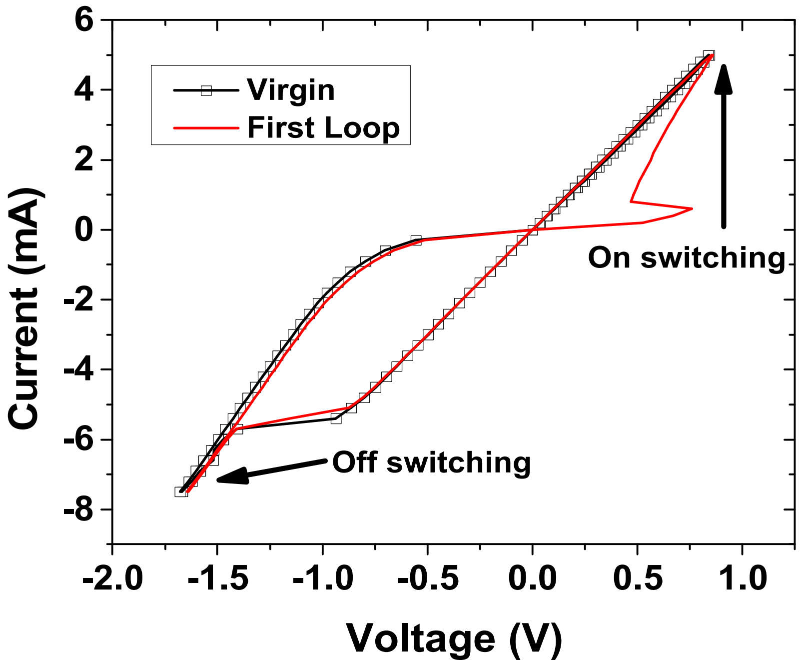
A.J. Lohn et al APL 103, 063502 (2013)



J.E. Stevens et al, accepted for publication by J. Vac Sci. Tech., 2013.

Basic Device Performance

- Typical devices form at very low currents
- Appear "forming free" in current sweep mode
- Do not need a high voltage transistor!!
  - This is a drawback of floating gate NVM
- Can be tailored by stoichiometry



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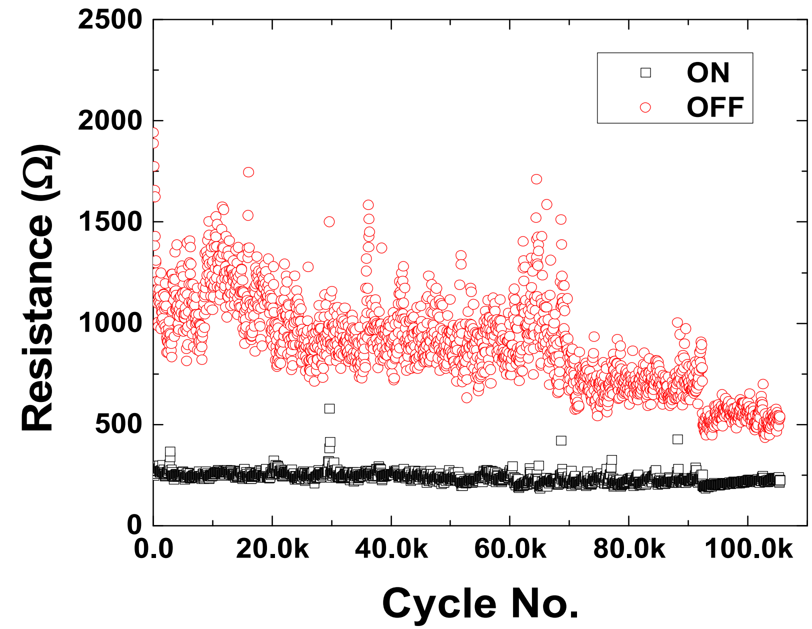
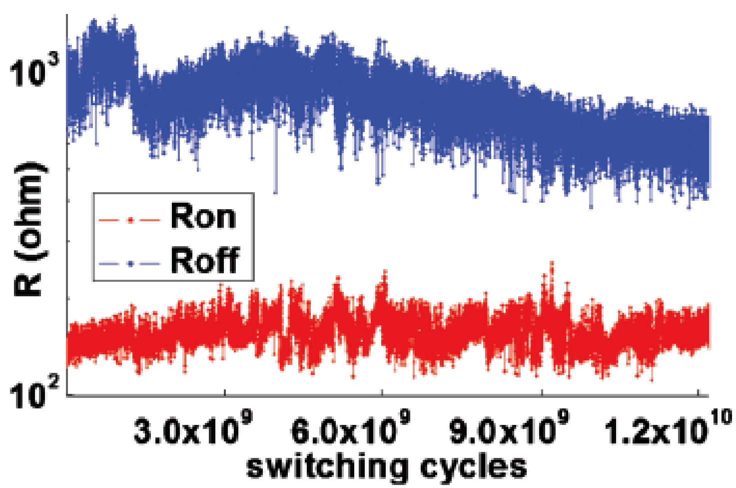
Endurance

- Sandia TiN/TaOx/Ta/TiN cell currently has max endurance of ~100k
- Currently optimizing cycling algorithms to improve this
- With Pt (Schottky) electrode, 10^{12} cycles have been reported

Sandia Pt/Ta/TaO_x/Pt CMOS Compatible Cell



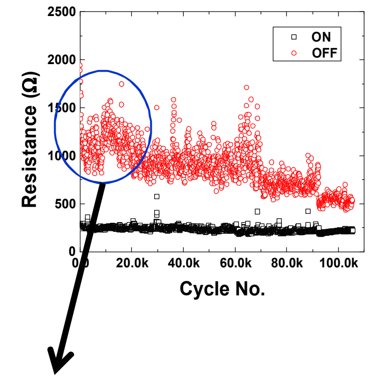
HP Labs Pt/Ta/TaO_x/Pt Cell

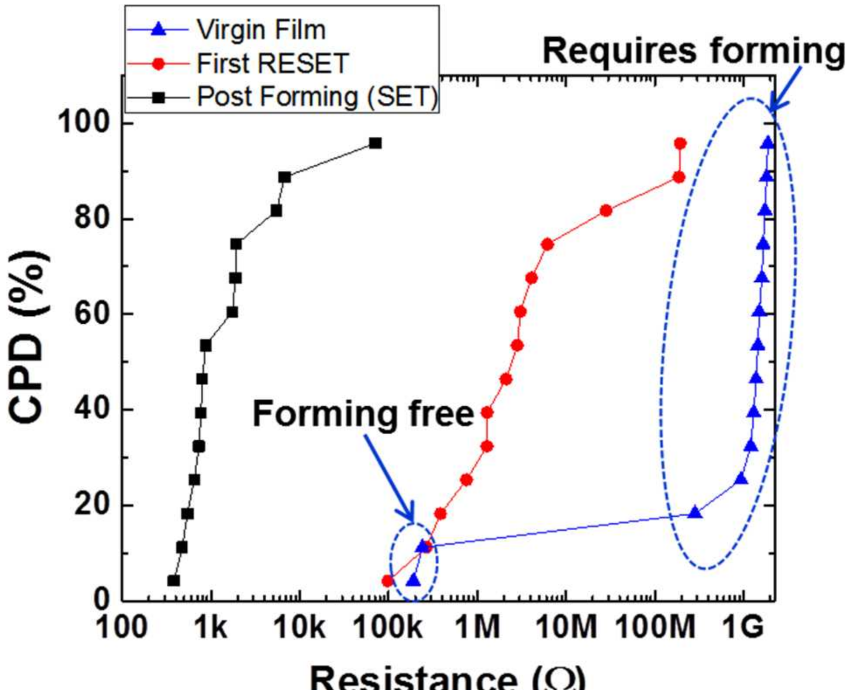


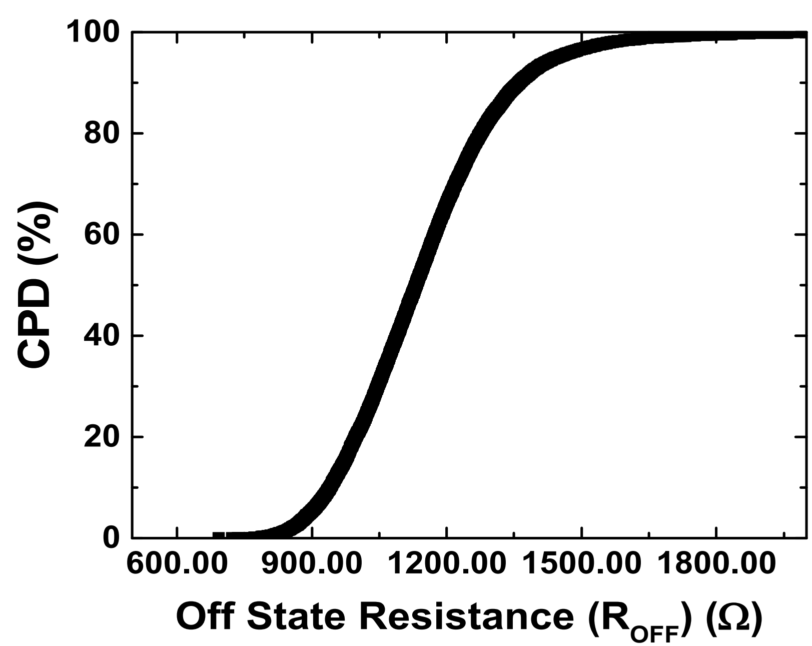
J.J. Yang, APL 97, 232102, (2011)

Variability and Noise

- **Interdevice variability**: device to device, can be >10x
  - Variations in film thickness, topography
- **Intradevice variability**: cycle to cycle, can be >2x
  - Fundamental physical attributes
- **Random telegraph noise:**
  - Affects read current, usually least significant

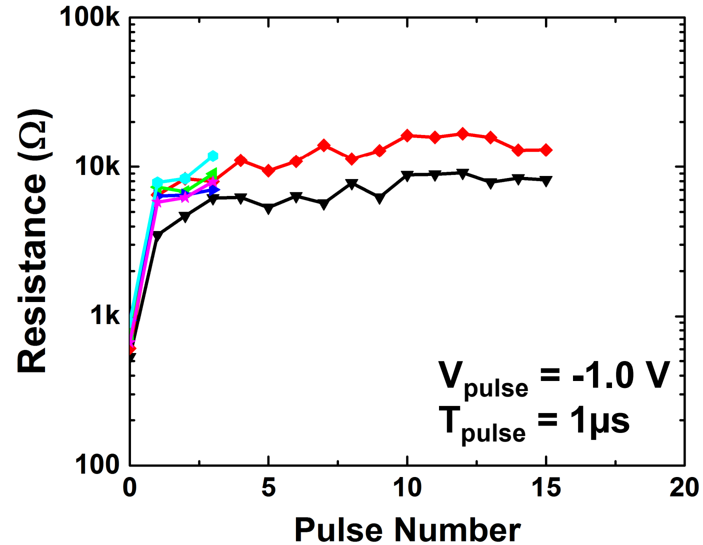


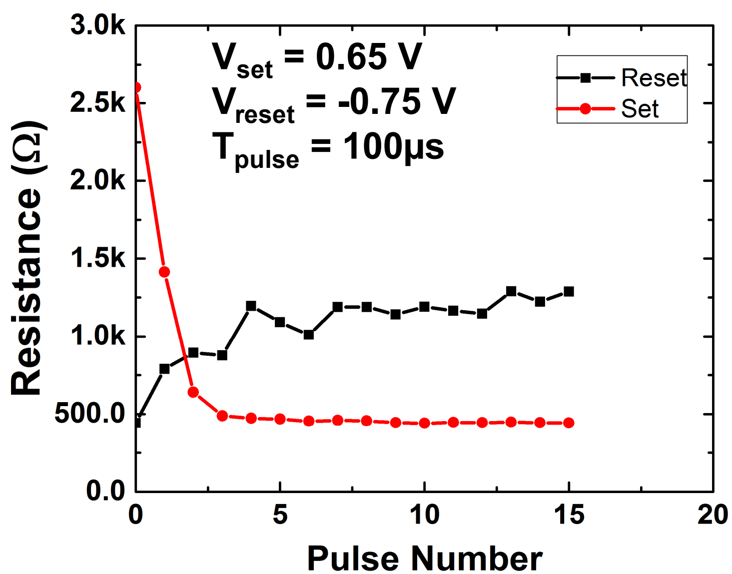


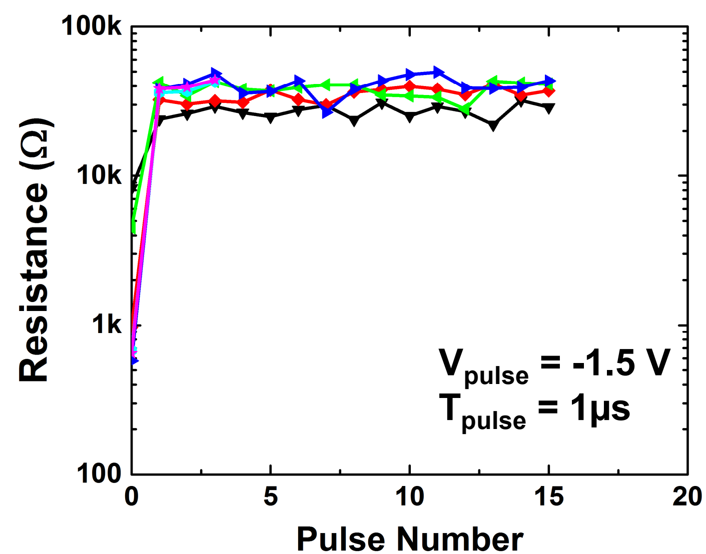


Set and Reset Transition

- Analog resistance tuning of TiN/TaO_x cell
- SET
  - Abrupt – thermal runaway?
- RESET
  - Gradual transition
  - Saturates for given amplitude

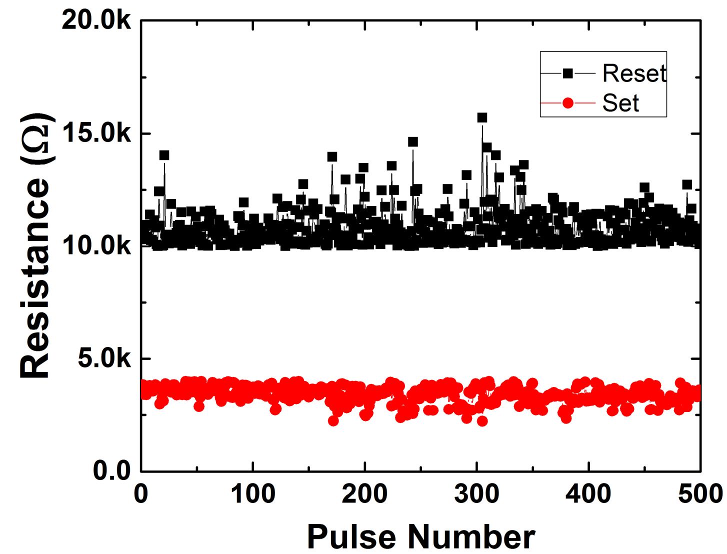


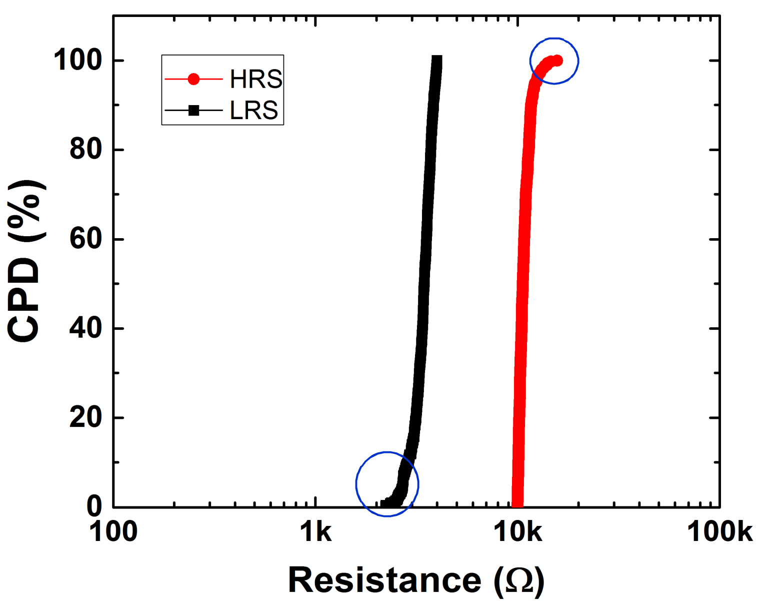


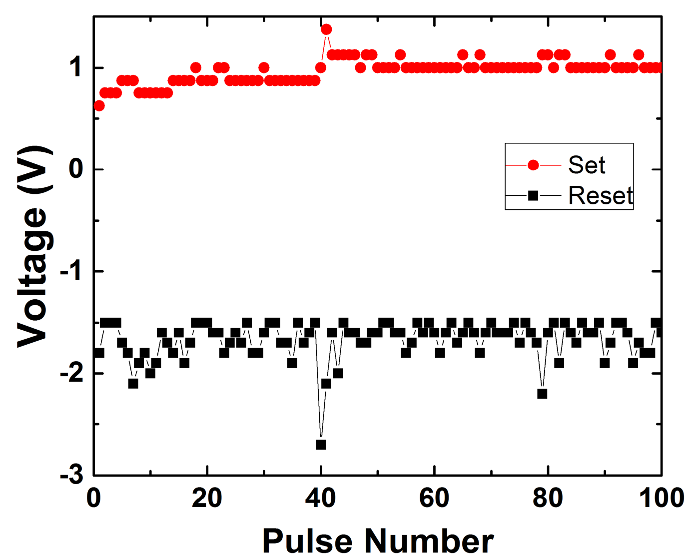


Closed Loop Cycling

- Resistance "find" routine
  - 400 μs pulses
  - V_{pulse}=0.5→$V_{R\text{-}target}$ (100 mV inc)
- End
  - $R>R_{target}$ (off)
  - $R<R_{target}$ (on)







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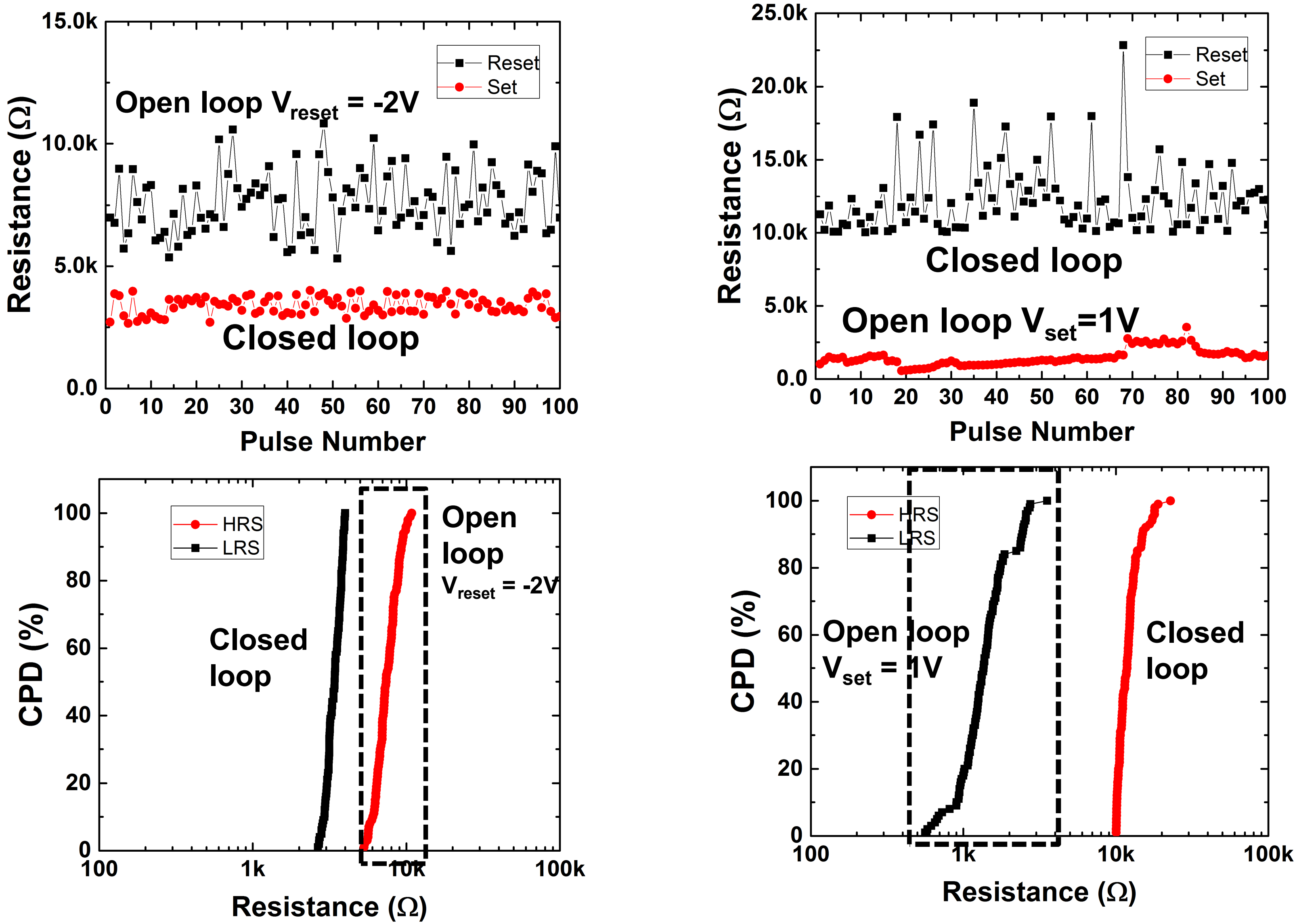
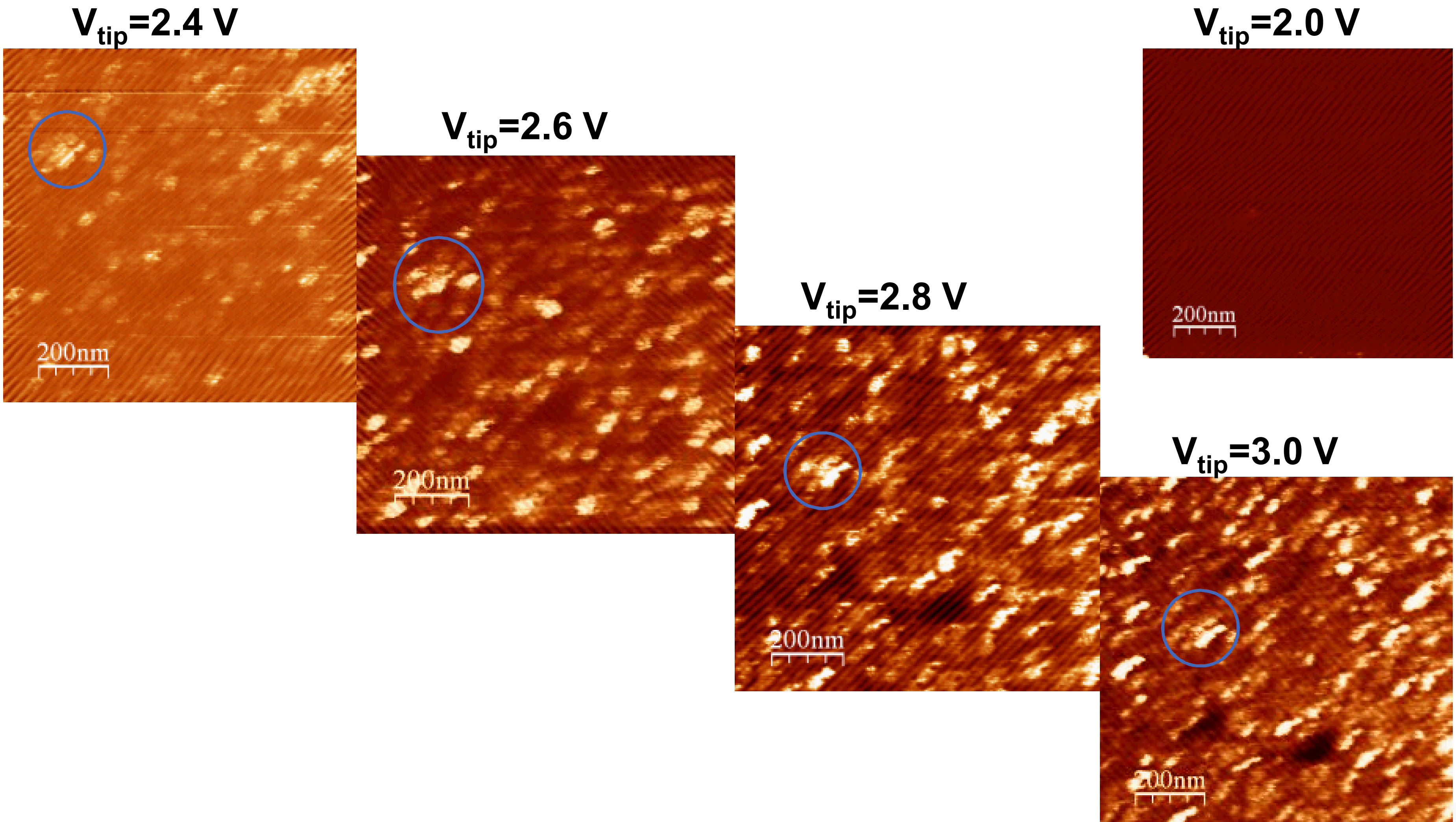
Open/Closed Loop Cycling

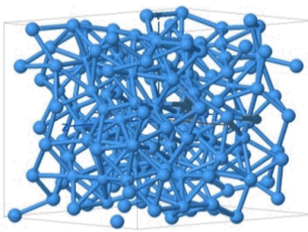


Possible Source of Variability

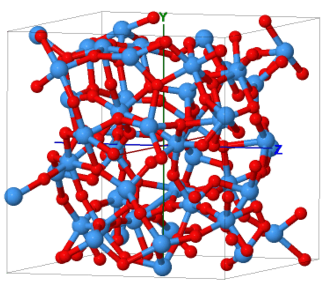


Marinella et al, EMC 2014

DFT Model: Ta_2O_x Structures



a-Ta160O2



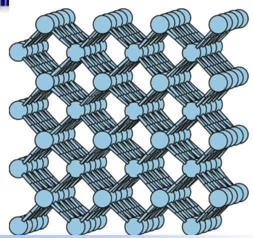
a-Ta48O120

amorphous

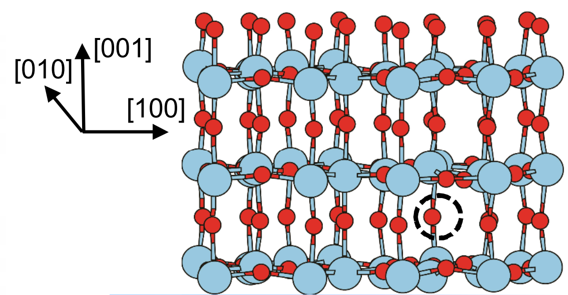
structure	Ta_2O_x x	O%	V_O%	charge
a Ta160	0.00	0.0	n/a	0
a Ta160O1	0.01	0.6	n/a	0
a Ta160O2	0.03	1.2	n/a	0
a Ta160O3	0.04	1.8	n/a	0
a Ta152O8	0.11	5.0	n/a	0
a Ta144O16	0.22	10.0	n/a	0
a Ta128O32	0.50	20.0	n/a	0
a Ta112O48	0.86	30.0	n/a	0
a Ta80O80	2.00	50.0	n/a	0
a Ta48O84	3.50	63.6	30.0	0
a Ta48O96	4.00	66.7	20.0	0
a Ta48O108	4.50	69.2	10.0	0
a Ta48O114	4.75	70.4	5.0	0
a Ta48O117	4.88	70.9	2.5	0
a Ta48O117	4.88	70.9	2.5	2+
a Ta48O118	4.92	71.1	1.7	0
a Ta48O118	4.92	71.1	1.7	2+
a Ta48O119	4.96	71.3	0.8	0
a Ta48O119	4.96	71.3	0.8	1+
a Ta48O119	4.96	71.3	0.8	2+
a Ta48O120	5.00	71.4	0.0	0

crystalline

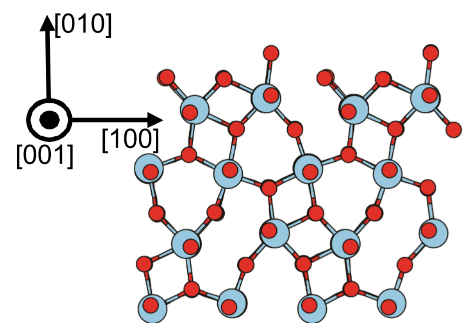
structure	Ta_2O_x x	O%	V_O%	charge
c Ta160	0.00	0.0	n/a	0
c Ta160O1	0.01	0.6	n/a	0
c Ta160O2	0.03	1.2	n/a	0
$\sigma_{O,xx}$, c-Ta_2O_5				
c Ta48O119	4.96	71.3	0.8	0
c Ta48O119	4.96	71.3	0.8	1+
c Ta48O119	4.96	71.3	0.8	2+
c Ta48O120	5.00	71.4	0.0	0
$\sigma_{O,yy}$, c-Ta_2O_5				
c Ta48O119	4.96	71.3	0.8	0
c Ta48O119	4.96	71.3	0.8	1+
c Ta48O119	4.96	71.3	0.8	2+
c Ta48O120	5.00	71.4	0.0	0
$\sigma_{O,zz}$, c-Ta_2O_5				
c Ta48O119	4.96	71.3	0.8	0
c Ta48O119	4.96	71.3	0.8	1+
c Ta48O119	4.96	71.3	0.8	2+
c Ta48O120	5.00	71.4	0.0	0



c-Ta160 (Ta)



c-Ta48O119 (V_O^{2+})

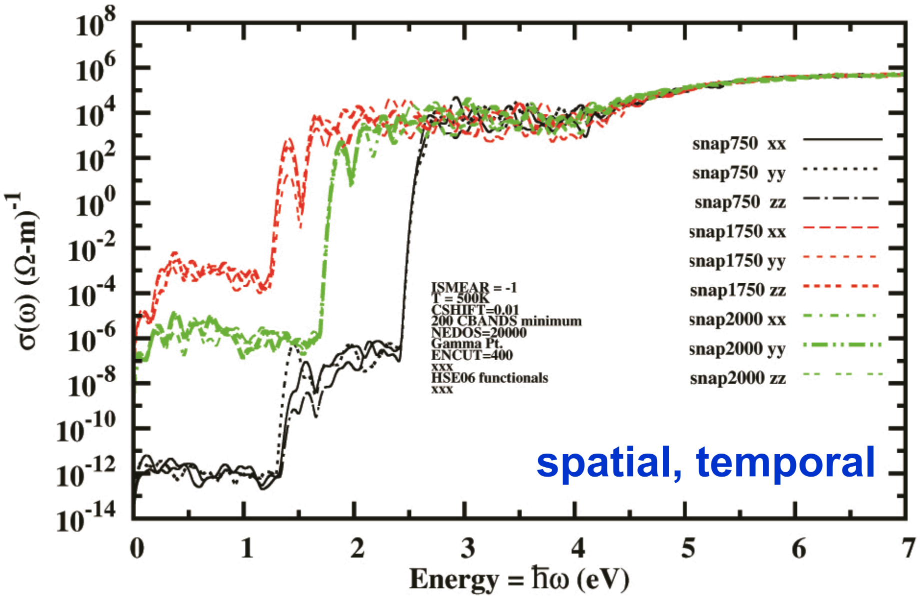


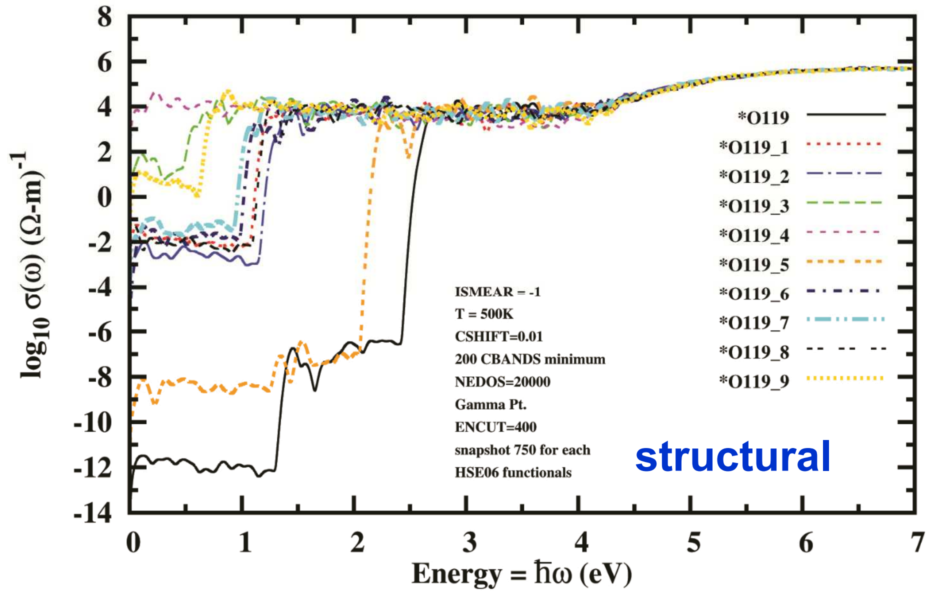
c-Ta48O120 (Ta2O5)

- ►Ta_2O_x structure library generated for conductivity calculations
- ►Parameter space samples composition, phase, temperature, and charge state

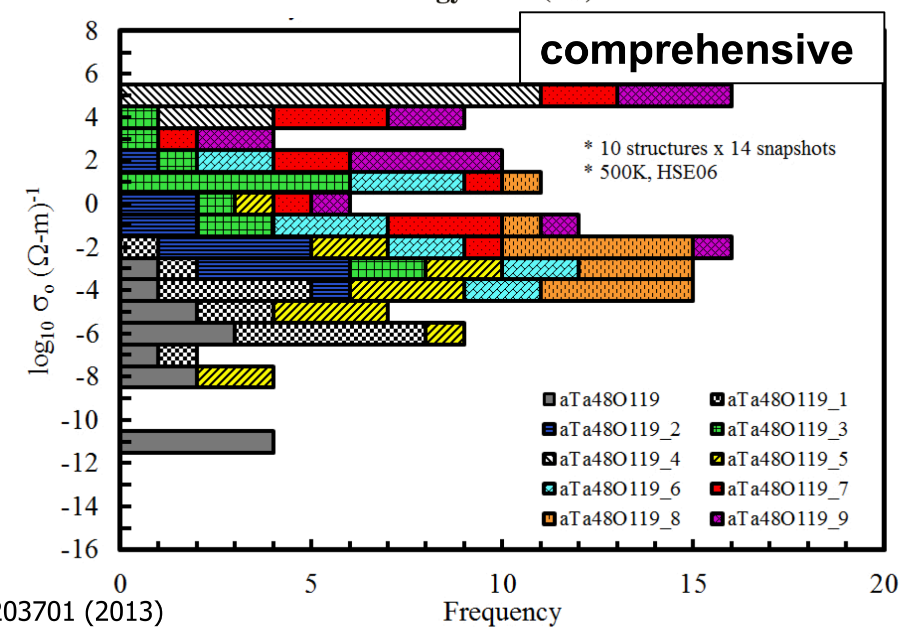
Bondi et al JAP 114, 203701 (2013)

Nanoscale Variability





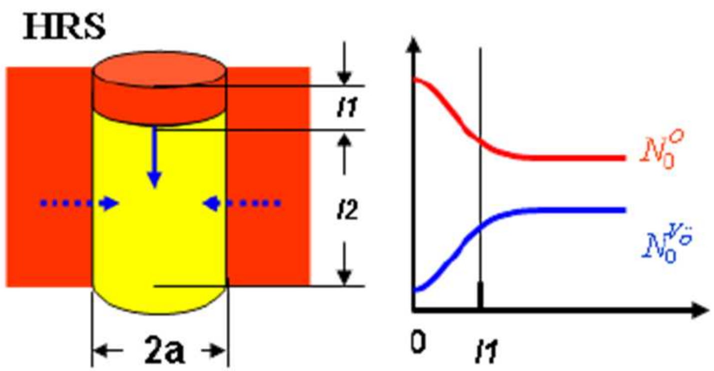
- DATA: 167-atom amorphous supercells containing 1 V_O^0, HSE06 functionals, T=500K
- Spatial variation: 1-2 orders of magnitude in σ_o
- Temporal variation: 9-10 orders of magnitude in σ_o
- Structural variation: 16 orders of magnitude in σ_o
- Anisotropy in σ_o relatively small effect at nanoscale

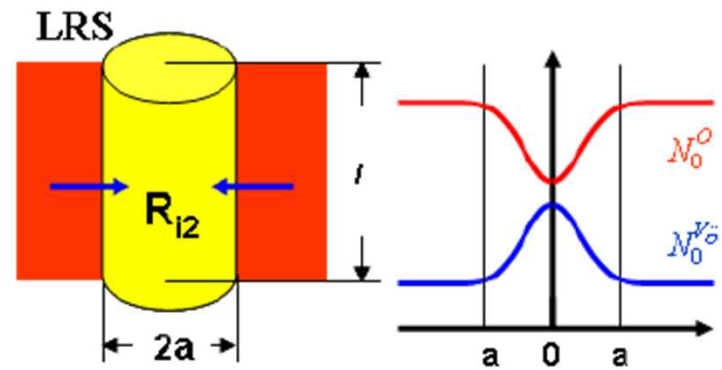


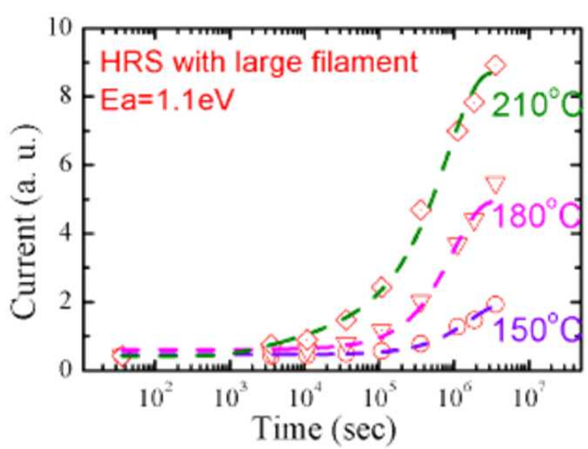
Bondi et al JAP 114, 203701 (2013)

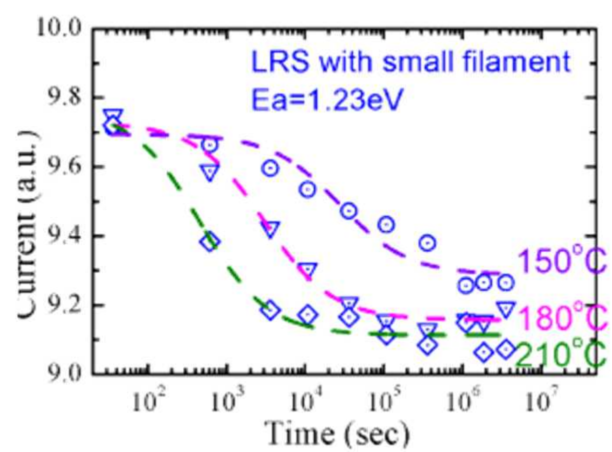
Panasonic Ta/TaO$_x$ Retention Model

- LRS is characterized by a radial concentration profile
- HRS is characterized by a vertical concentration profile





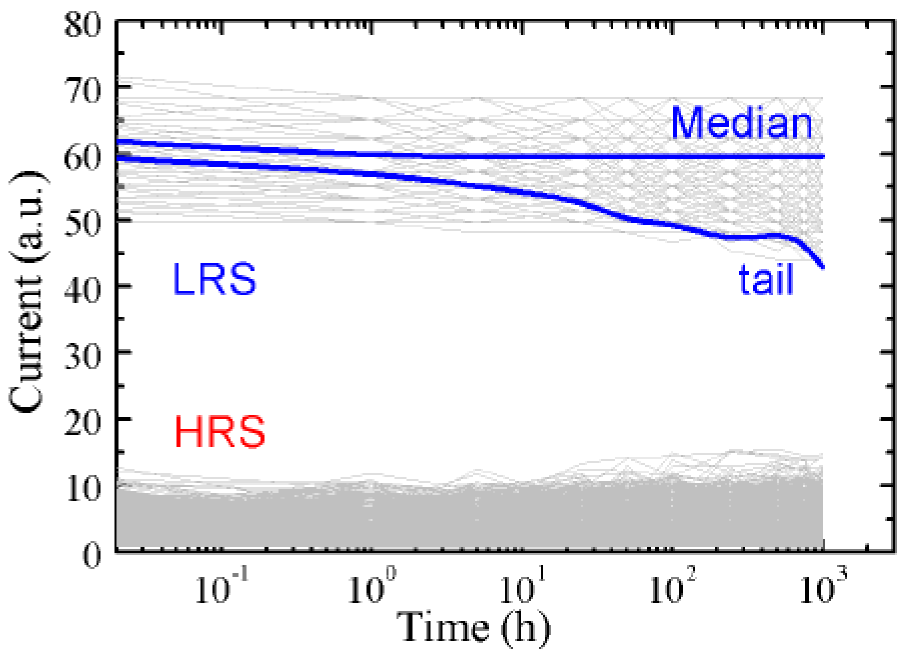


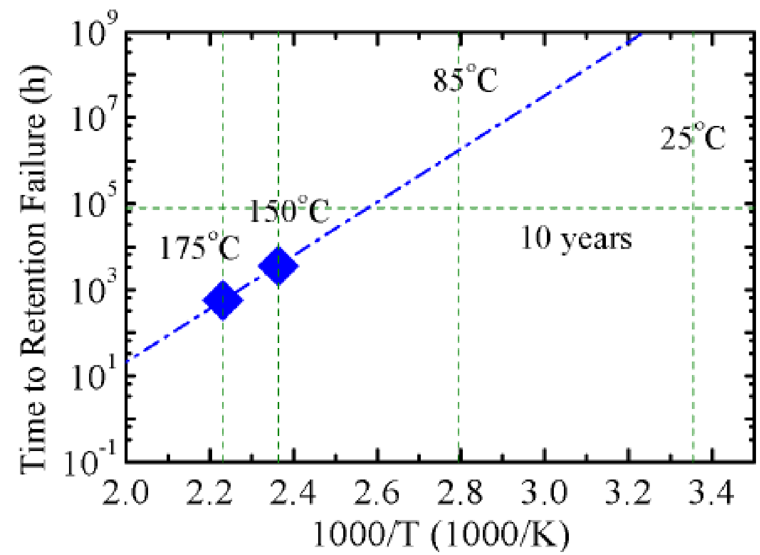


Z. Wei et al, IEDM 2008

Panasonic Ta/TaO_x Retention Model

- **Despite tail bits, 10 yr retention @ 85°C still predicted**





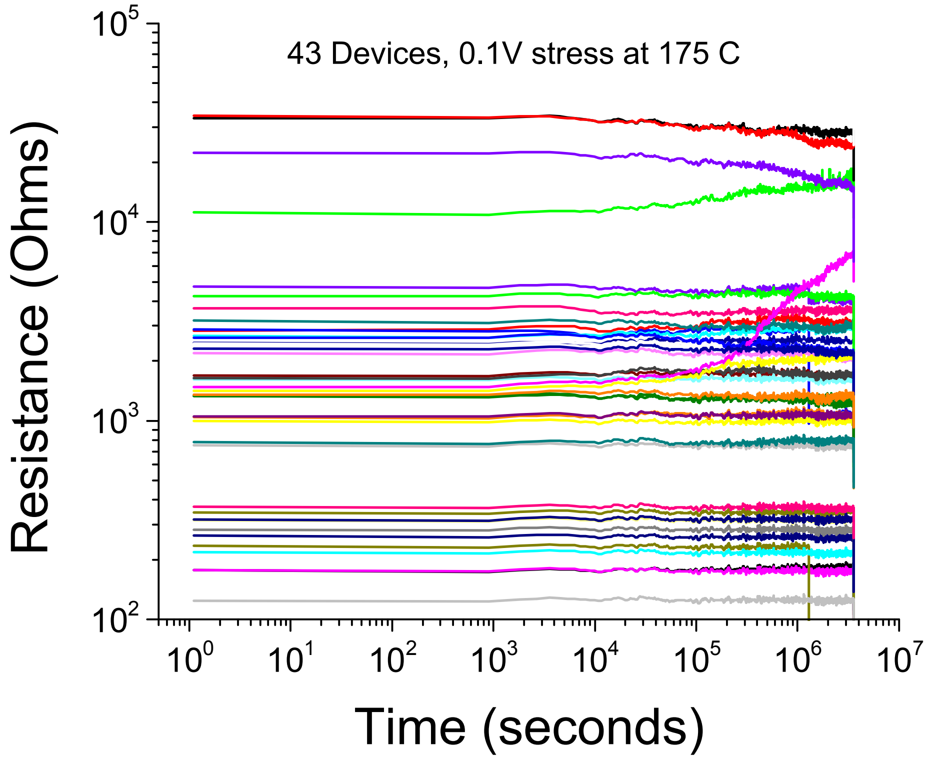
Z. Wei et al, IEDM 2008

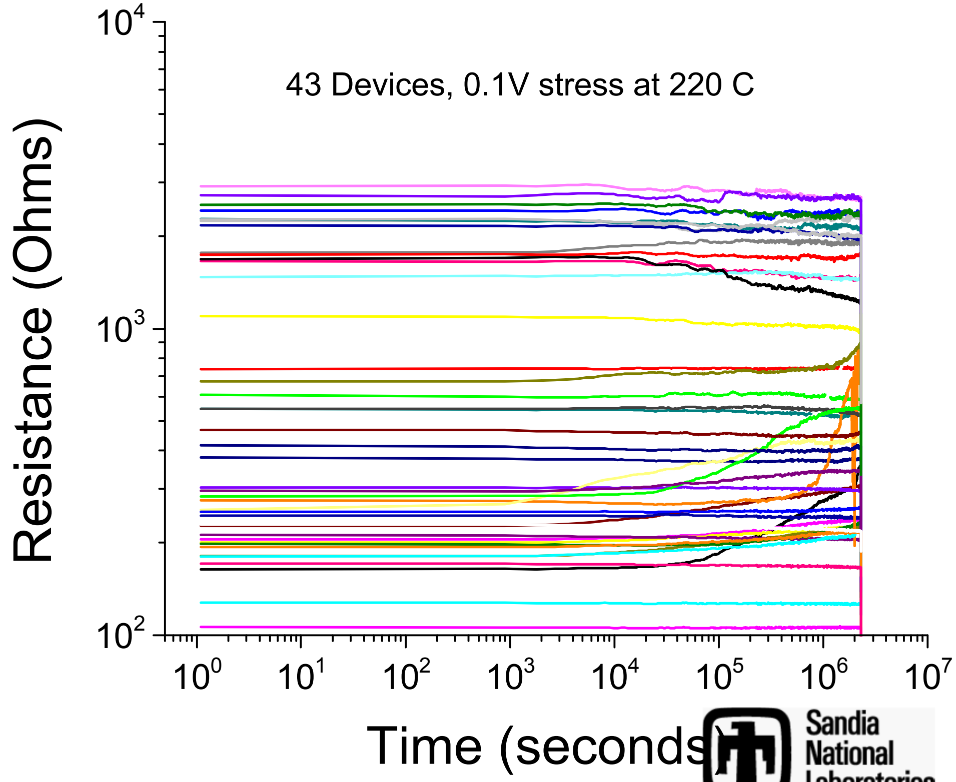
Retention Measurement

- Zeus/Aetrium system
  - Ambient temperature control up to 300°C
  - Long term voltage stress and intermittent IV read capability
- For retention measurements 0V bias is used, with 100mV read voltages tested every 15s until test is finished
- Multiple temperatures: 220, 175, and 150°C
- 48 devices tested at each temperature, should provide sufficient statistics

Retention Data

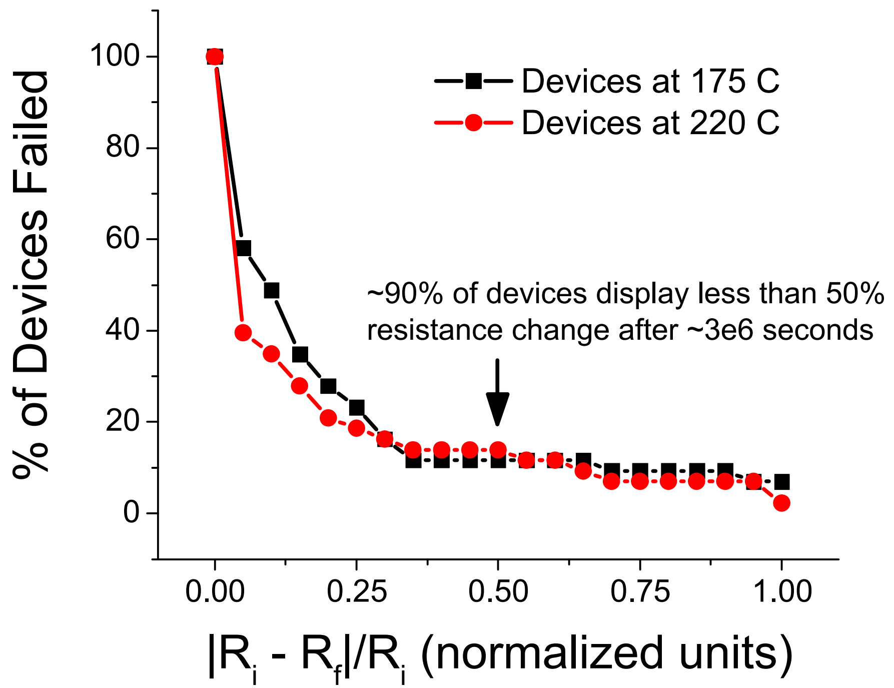
- ~98% devices show minimal resistance changes
- Appears to follow Panasonic model
- Tail bits are the key challenge





Retention Fail Rates

- **Low failure rates suggest a burn-in step could select the most resilient devices and not detrimentally lower yield**



Microsystems
Science, Technology & Components

Outline

- Introduction and Motivation
- ReRAM Development
- Characterization of Reliability
- Characterization of Radiation Effects
- Summary and Next Steps

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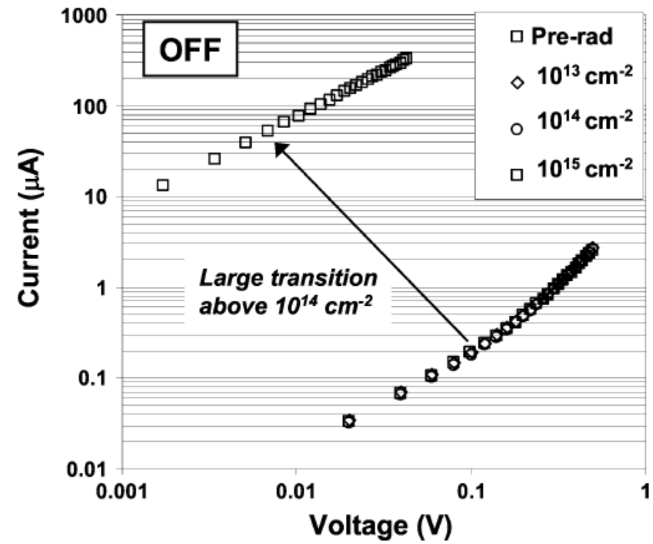
Displacement Damage vs. Ionization

- Different damage mechanisms investigated using various beams
- Different circuit configurations
  - Floating and shorted
- The following slides describe cell-only measurements of displacement damage and TID

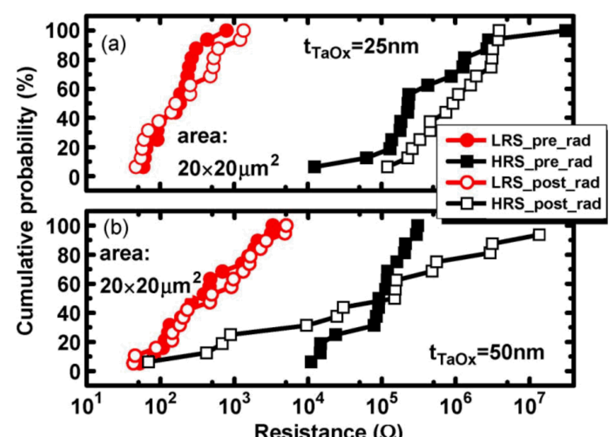
Displacement damage | 800 keV Ta | 28 MeV Si | 70 keV e^- | Ionization

Early TMO-ReRAM Radiation Experiments

- TiO_2
  - Little effect from 45 Mrad(Si) γ-rays and 23 Mrad(Si) Bi ions
  - Resistance change due to 1 MeV alpha particles and 350 keV protons
- TaO_x
  - Thickness dependence from Peking University
  - Resistance degradation due to 800 keV Si ions



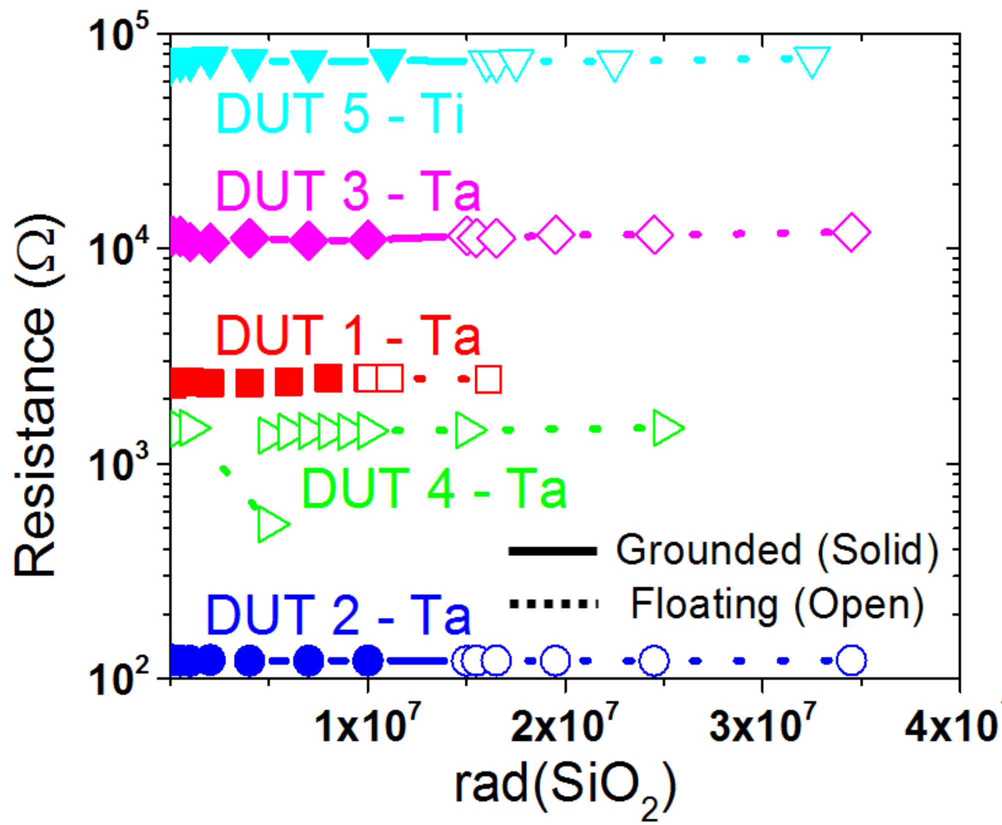
Barnaby *et al.*, *Trans Nuclear Sci*, vol. 58, pp. 2838-2844, 2011.



Zhang *et al.*, *Trans. Electron Devices*, vol. 58, no. 8 pp. 2800, Aug. 2011.

10 keV X-ray (Ionization) – TaO_x and TiO_2

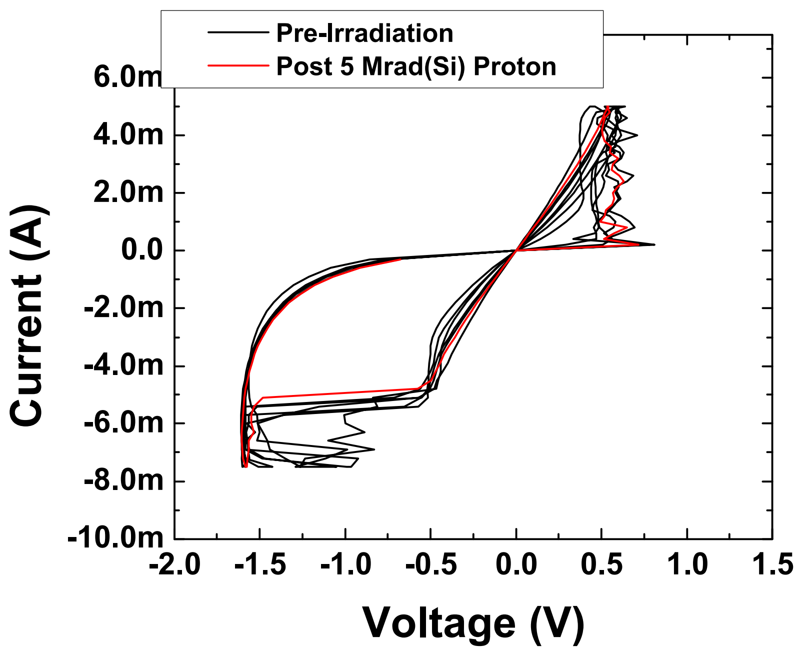
- Grounded and floating
  - Steps up to 10 Mrad(SiO_2)
- DUT 4 changed resistance at 4 Mrad(SiO_2)
  - No lasting damage
  - Unrepeatable
- No other effects on any devices



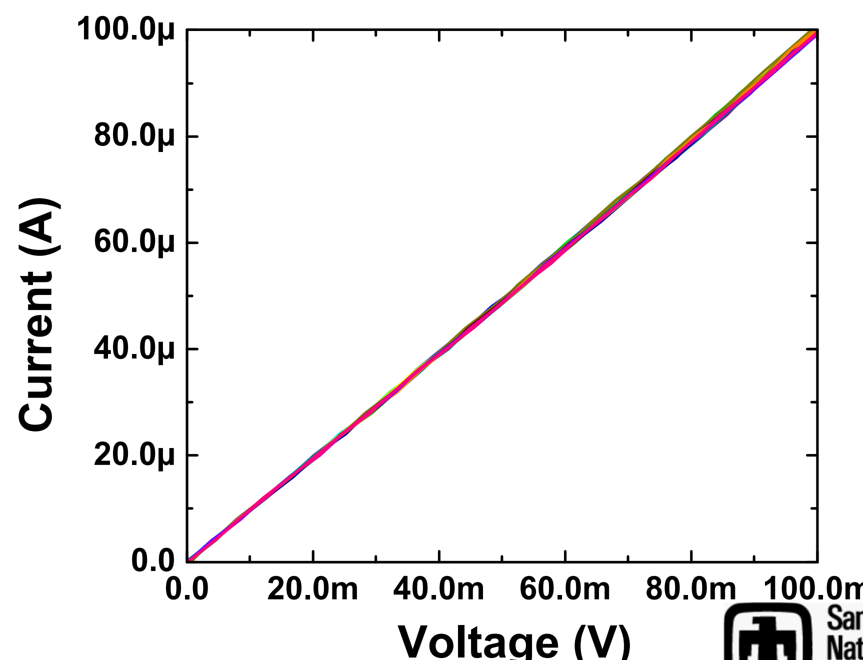
4.5 MeV Protons

- 4.5 MeV proton irradiation at Sandia's IBL
- In situ electrical testing in 10^{-5} torr vacuum
- 1 µm beam rastered across 25x25 µm area
- Little change up to 5 Mrad(Si)

Pre and Post Proton Irradiation I-V



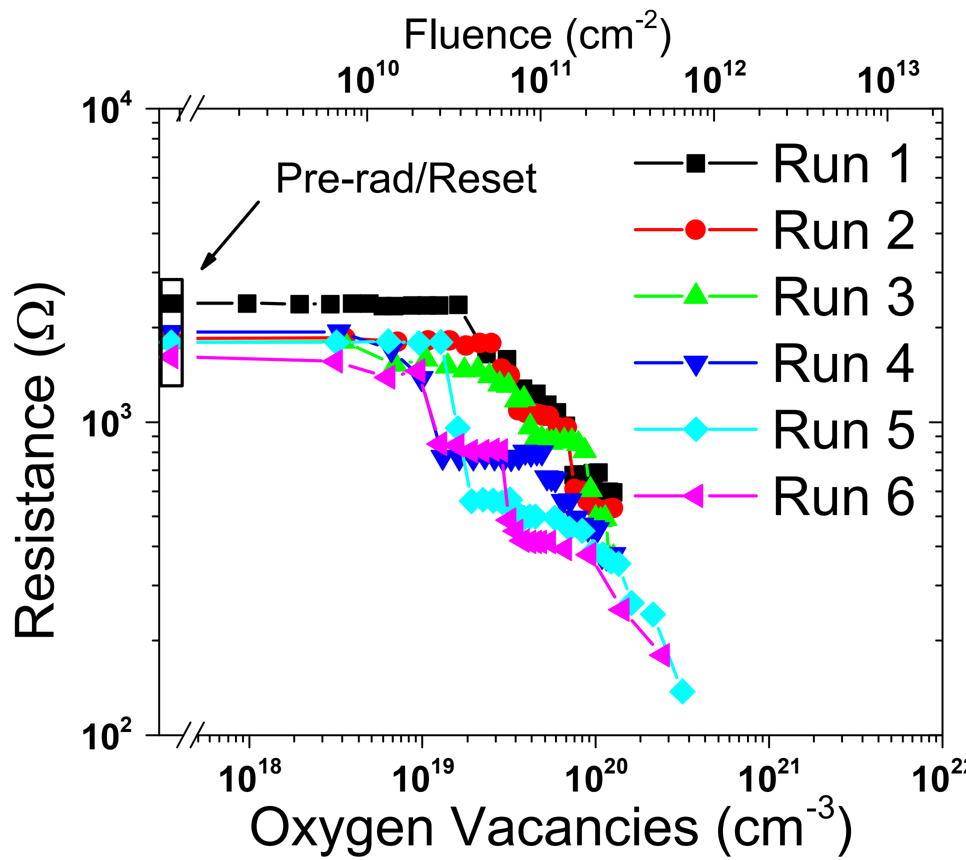
Read I-V Curves Between Proton Shots



Marinella et al NSREC 2012

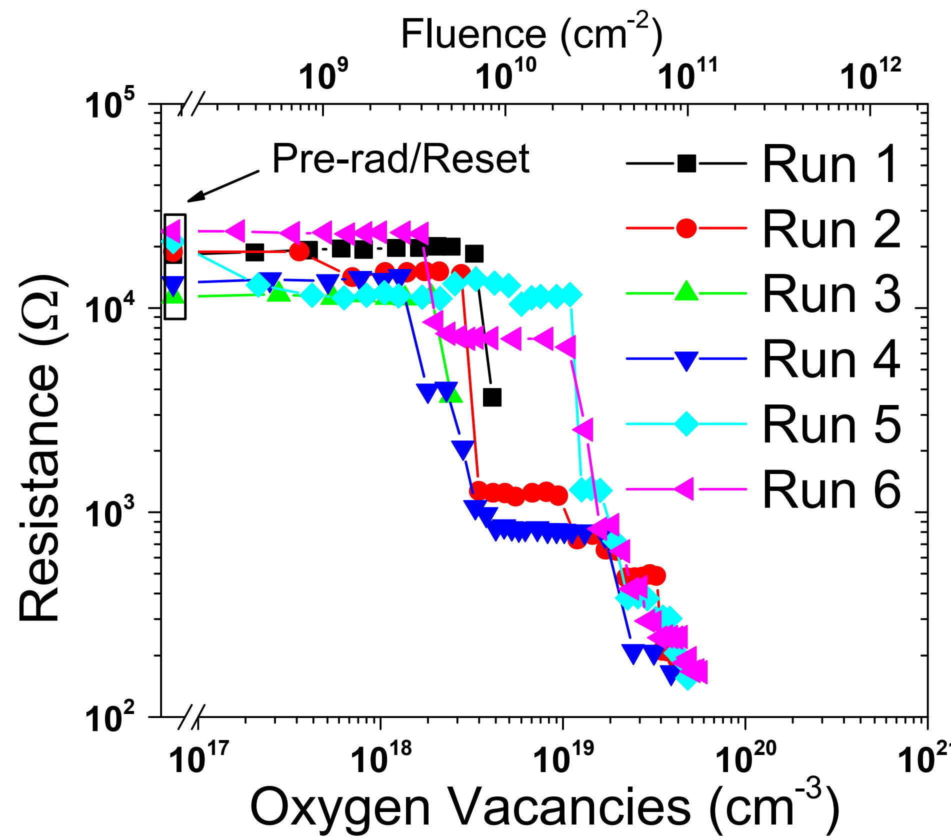
800 keV Ta (Displacement Damage) - TaO_x

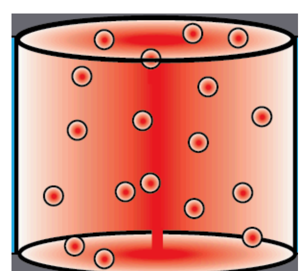
- **Displacement damage**
  - Gradual resistance degradation
- **Creation of oxygen vacancies**
  - Threshold ~10^{19} cm^{-3}
- **Reset operation recovers significant portion of resistance loss**
  - Cumulative damage



Displacement Damage Accumulation and Annealing

- Cumulative damage
  - Stochastic process
  - Not all added oxygen vacancies may be removed by oxidation/diffusion
- Repeated resetting can return device closer to original state
  - Runs 5 and 6





Microsystems Science, Technology & Components

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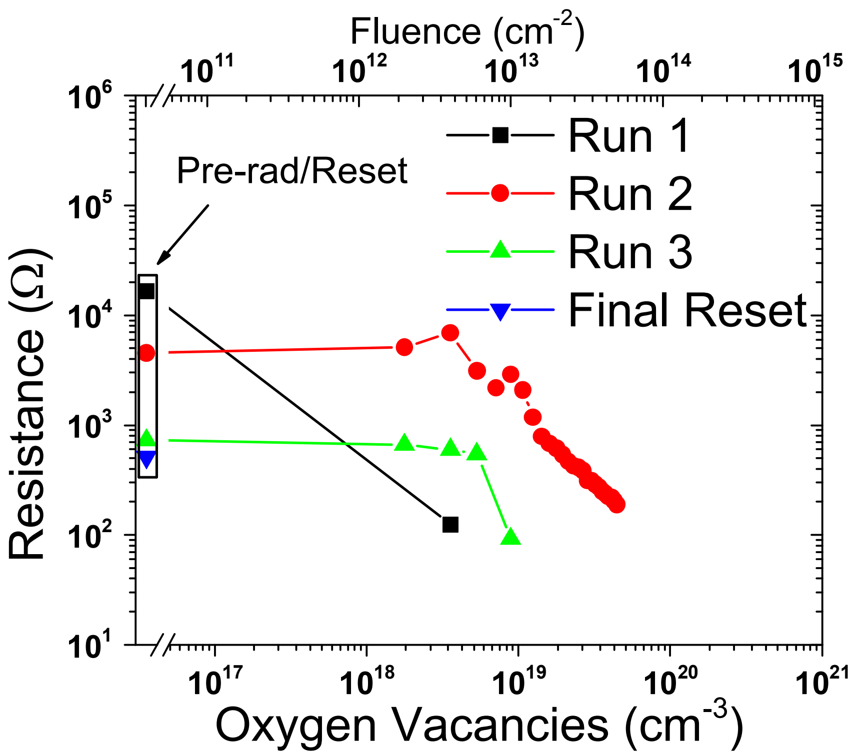
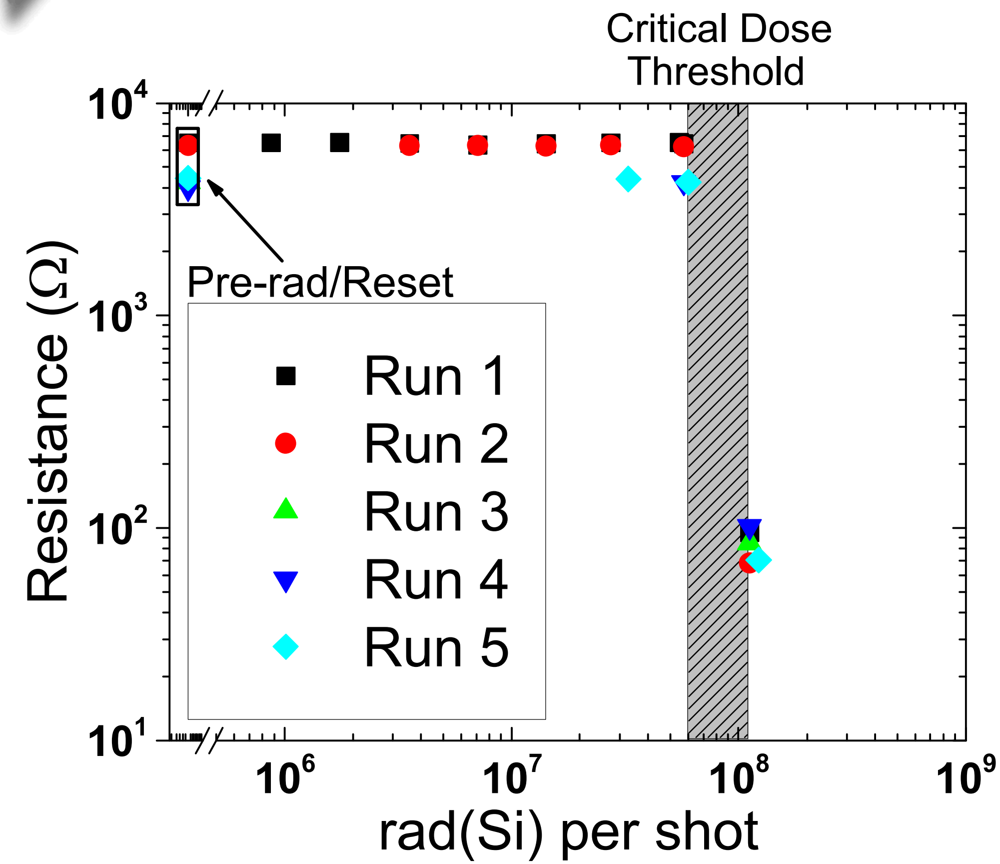
28 MeV Si (Combined Mechanisms) - TaO_x

- 28 MeV Si causes ionization and displacement damage
- Ionization
  - Threshold ~600 Mrad(Si)
  - Device to device threshold variation up to 10x
- Displacement damage
  - Shots in run two are half critical dose threshold
  - Oxygen vacancy threshold ~6.5×10^{18} cm^{-3}
  - Consistent with 800 keV Ta

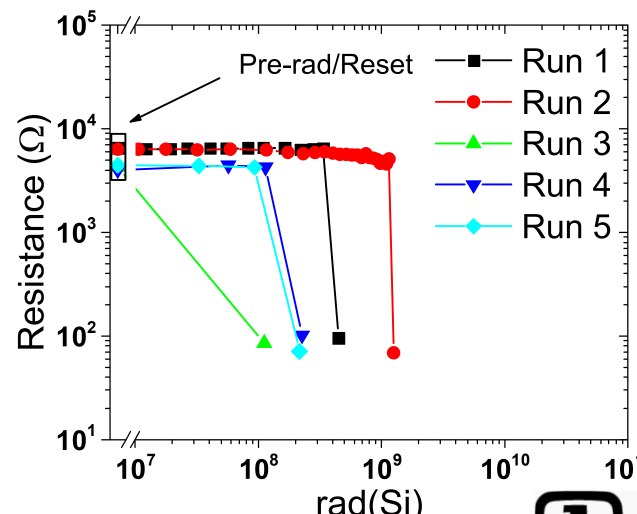


28 MeV Si (Ionization) - TaO_x



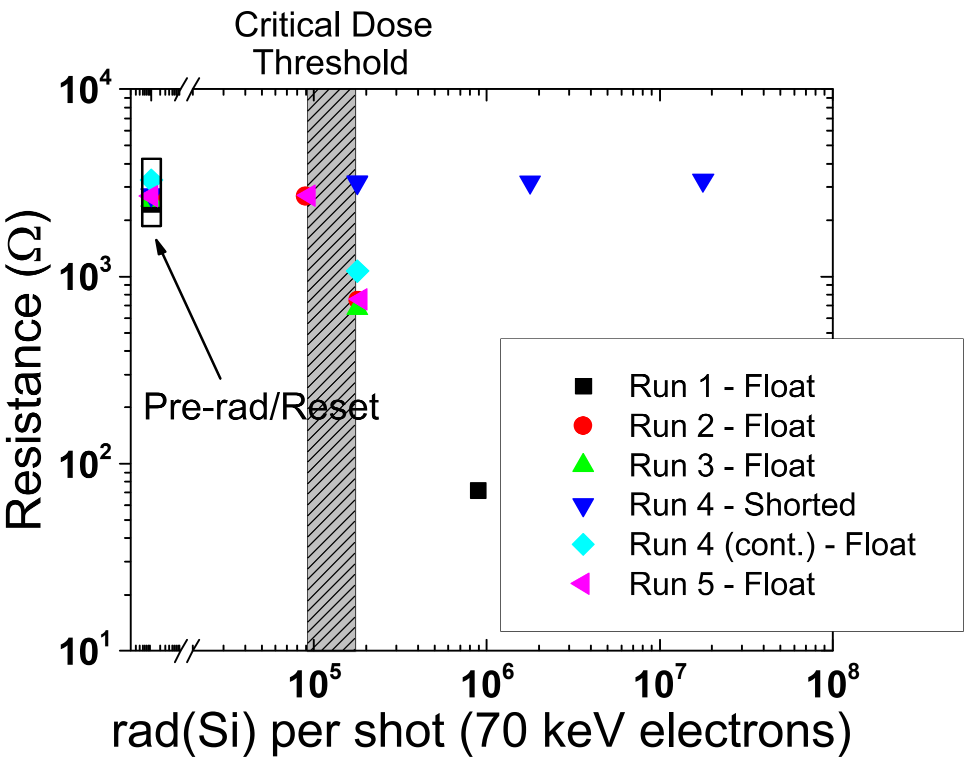
- **TID threshold varies between devices**

- **Resistance change abrupt and consistent**
- **Floating devices**
- **Ionization**
  - **Requires 60-120 Mrad(Si) Cumulative between reads**

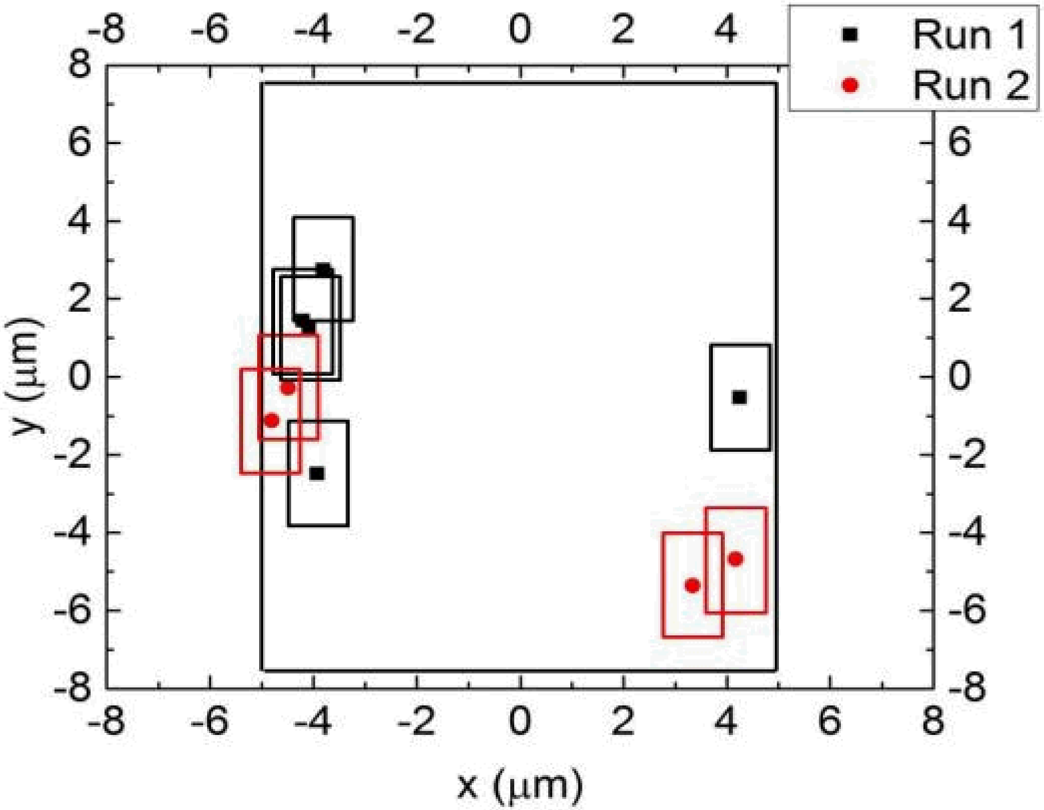


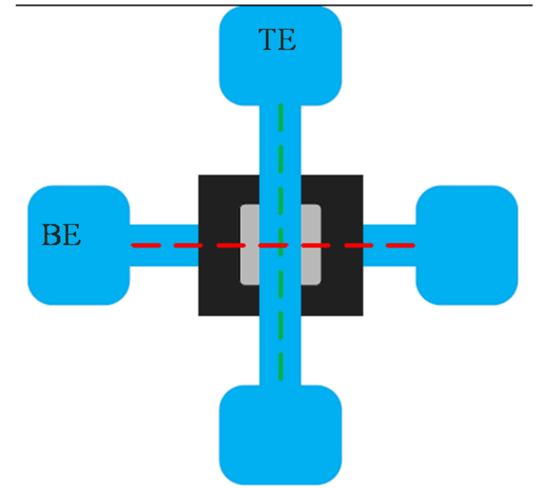
70 keV Electrons (Ionization) - TaO_x

- **Ionization**
  - **Threshold 100-200 krad(Si) per shot**
- **When pins are shorted no changes occur for doses up to 18 Mrad(Si)**
- **Resistance change varies with dose per shot**

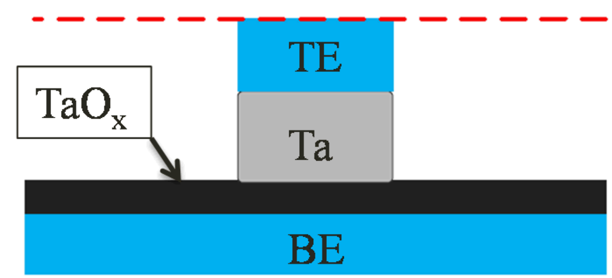


Mapping the Switching Filament

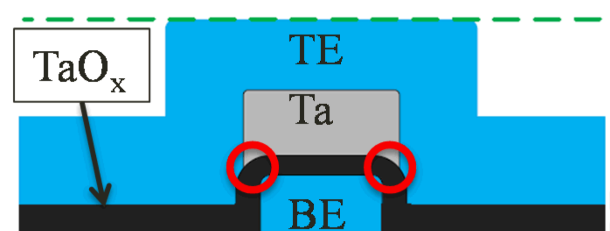




Cross Section 1

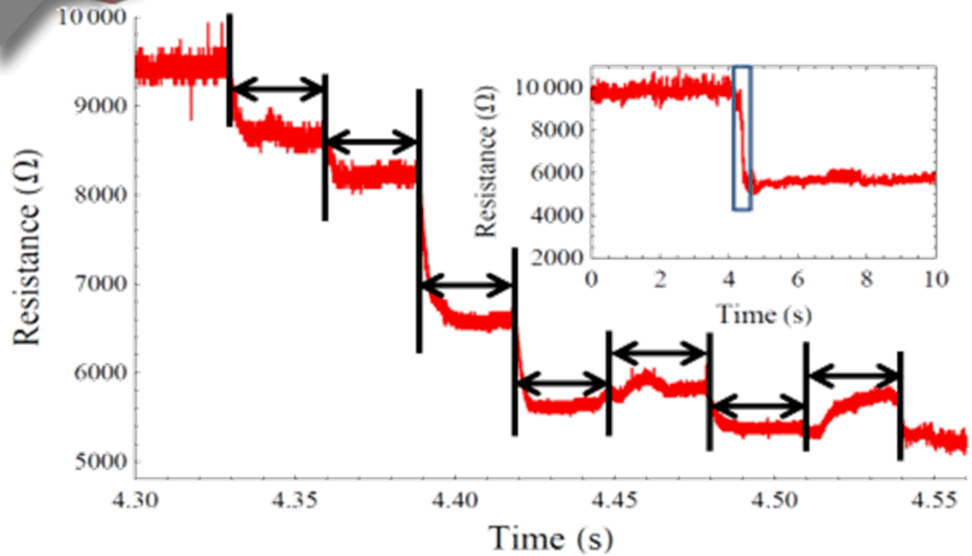


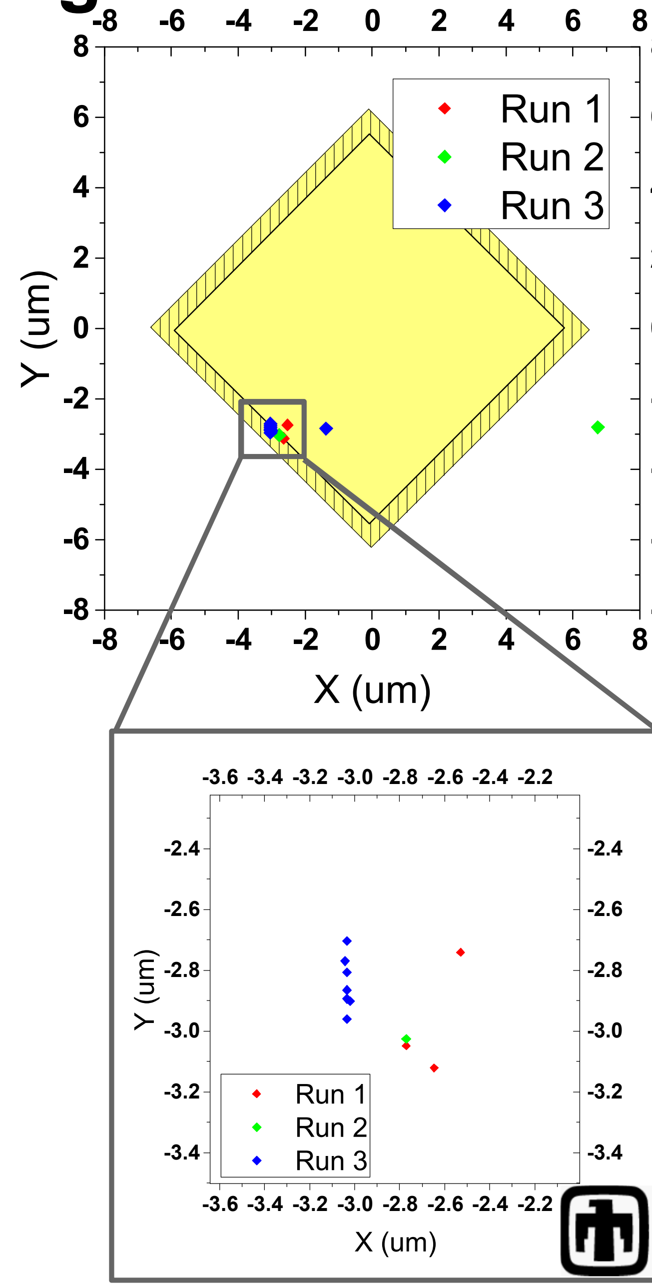
Cross section 2



- Filaments localized to the edges of the device structure
- We believe this is due to one of the following:
  1.) Edge of bottom electrode may have non-conformal oxide deposition
  2.) Higher electric fields at the edges during electroforming process

Mapping the Switching Filament





- Multiple raster scans using a ~50 nm spot size 200 keV Si beam across the device
- Observed change is resistance once per scan at approximately the same X location each time, indicating filament extends ~240x240 nm

Outline

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Summary

- ReRAM technology shows promise to replace traditional magnetic hard drives, flash, DRAM, and SRAM
- Sandia is developing this technology for radiation hardened electronics
- ReRAM switching voltages (<1.5V) are ideal for CMOS integration
- Reliability Challenges
  - Still need to understand the science of switching!
  - Variability: among devices, cycle to cycle, and read
  - Retention: tail bits
  - Radiation: cell responds generally well to TID and displacement, but subtle effects require understanding

Microsystems
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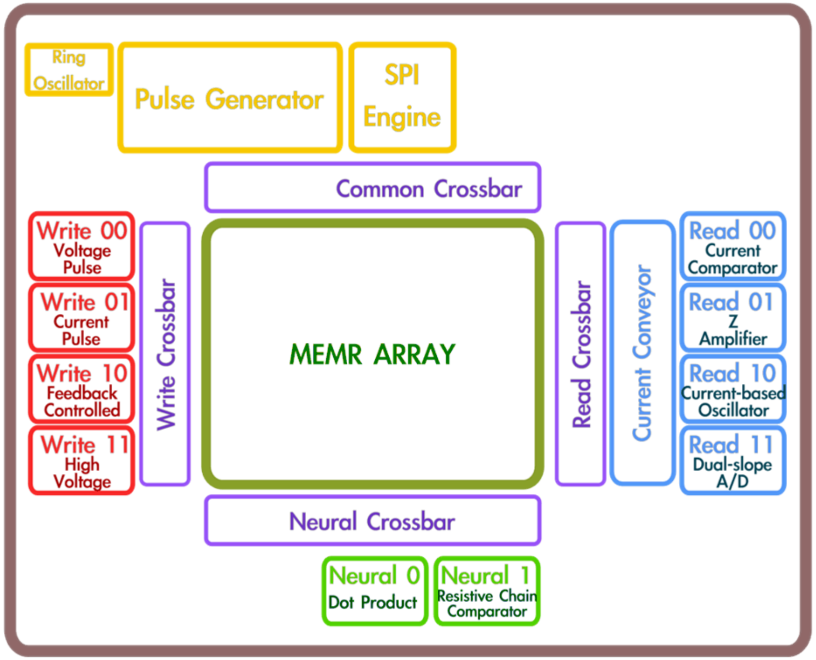
Future Work

- Integrate with CMOS7 ASIC 1T1R controller (first generation under test/debug)
- Assess reliability and radiation effects with full system, esp. transistor-cell interaction
- Further investigate the effects of radiation on more subtle, long term device properties
- Interested in collaborations on these topics

2^{nd} Gen Memristor ASIC Controller Block Diagram



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- Entire SNL ReRAM/Memristor team
- Management support, esp. Rich Dondero, Rick McCormick, Mike Daily, Gil Herrera
- This work was partially funded by Sandia's Laboratory Directed Research and Development (LDRD) Program