Impact of Interface Defects on Tunneling FET Turn-on Steepness

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Tunneling field-effect transistors (TFETs) have been investigated as a low-voltage replacement for the conventional field-effect transistor with a turn-on response steeper than 60 mV/dec. However, to date no device has achieved a steep turn-on at low voltage with an on-off ratio of 10^6 or greater. Among the main issues is the finite density of states inside the semiconductor bandgap arising from a large concentration of interface defects [1]. Though these states do not directly conduct current, carriers can be trapped then thermally emitted to the conduction band in a trap-assisted tunneling process, broadening the switching response of the device. Overcoming these effects may not be feasible with current levels of material defects.

The band-to-band tunneling conductance across a junction is approximately given by [2]:

$$G \propto \frac{\int (f_c - f_v) \cdot \mathcal{T}(E) \cdot D_J(E) \, dE}{\int (f_c - f_v) \, dE} = \langle \mathcal{T} \cdot D_J \rangle$$

where f_c and f_v are the n-side and p-side Fermi functions, $\mathcal{T}$ is the tunneling probability and D_J is the joint density of states of the two sides of the junction. From this we see that measuring the change in conductance with voltage directly gives how sharply $\langle \mathcal{T} \cdot D_J \rangle$ also changes. This quantity is of great interest for determining the current of the device. At high current, the steepness of the joint density of states is more important. Due to the presence of dopants and other impurities, the band edge has a finite slope on both sides, with even the best reported backward diodes showing a slope no better than 90 mV/dec in conductance measurements [2].

Carriers that tunnel into impurity states in the band tail are not free, but if the states are close to the band edge, the carriers are rapidly excited to the conduction band or valence band at room temperature. If sufficiently shallow, the impurity atoms can be fully ionized even at low temperatures. Interface defects, possibly contributed by the presence of a nearby gate oxide, can have a broad energy distribution inside the band gap [3]. If the states are deep inside the gap, the rate of thermal activation into the conduction or valence band can be slow, and the conductance is limited by the Shockley-Reed-Hall generation rate, rather than $\langle \mathcal{T} \cdot D_J \rangle$. This rate goes as $D_{it}(E_T) \cdot \exp[(E_C - E_T)/k_B T]$, where E_T is the energy level of the interface trap and D_{it} is the density of interface trap states [4]. Thus, while the Fermi level on one side of the junction lines up with a deep trap, the conductance is expected to have strong thermally activated behavior following the Boltzmann factor, with deeper traps seeing a higher energy barrier to thermal excitation.

To observe the distinct effects of trap-assisted tunneling in a TFET, we study the InGaAs/InAs nanowire structure in [5], shown in Fig. 2. In Fig. 3, the G_{DS}-V_{DS} response is plotted without changing the gate bias to reveal the turn-on steepness of the device independent from the gate electrostatic efficiency. Separate measurements are conducted at T=300K and T=77K. Well before the conductance saturates, the subthreshold slope S is strongly temperature-sensitive as long as the Boltzmann factor is more limiting than the rate of tunneling into the band tail. This is evident at 77K, where the thermally activated S is much steeper than the band tail. As V_{DS} increases, S gradually increases as the conductance becomes more limited by $\langle \mathcal{T} \cdot D_J \rangle$ than by SRH generation. The conductance in the on-state is lower for 77K due to other effects, such as bandgap narrowing with increasing temperature [5].

In summary, the effects of interface defects on the sharpness of the conductance switch can be seen both in the intrinsic band tail steepness (for shallow defects) observed at all temperatures, as well as in a subthreshold regime clearly dominated by thermal activation (for deep defects). To realize a steep turn-on, reduced dimensionality on both sides of the junction is needed [1]. However, increasing the tunneling probability of the device will increase not only the band-to-band current in the on-state but also leakage into the band tail. In order to achieve a turn-on steepness better than 60 mV/dec over at least six decades of current, a very high quality tunneling interface is needed, comparable to the best achieved interface trap densities in semiconductor systems. This suggests future investigation into the engineering of pristine material interfaces, possibly at atomic levels of control, with high yield.

References:

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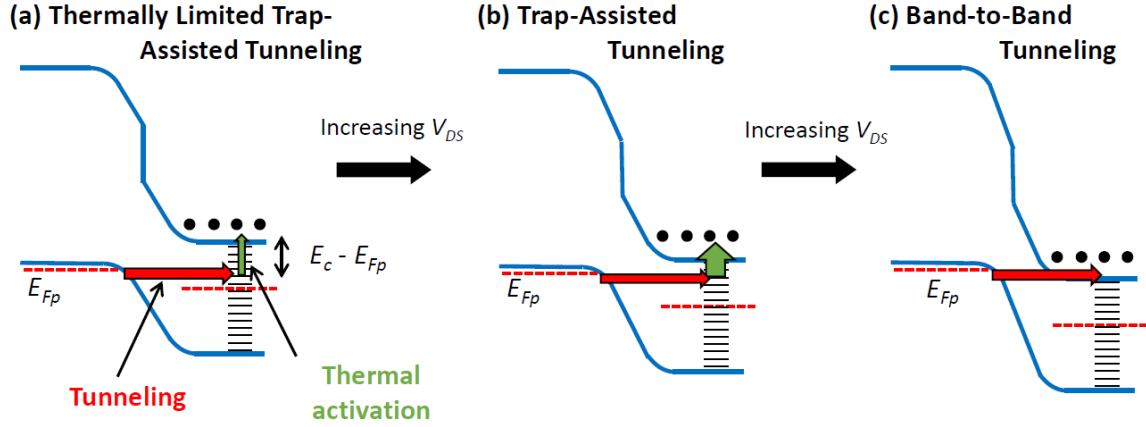
Fig. 1: Band diagram at the tunnel interface between the *p*-side and the channel. (a) When the *p*-side Fermi level E_{Fp} aligns with the mid-gap, carriers first tunnel into interface traps, but the rate of thermal excitation to the conduction band is slow due to the large thermal barrier $E_C - E_{Fp}$. (b) When E_{Fp} aligns with states close to the band edge, thermal excitation is rapid and the conductance is limited by the tunneling rate into shallow traps/band tail. (c) Current is dominated by direct tunneling between the conductance band and the valence band.
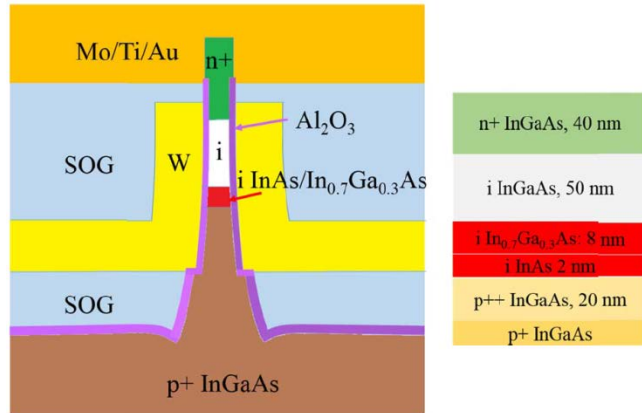

Fig. 2: Schematic of the InGaAs/InAs nanowire device, from [5]. The diameter of the nanowire is 50nm, the channel length is 60nm, and the Al_2O_3 gate dielectric has EOT = 1.2nm. The *p*+ side is the drain, the *n*+ side is the source.

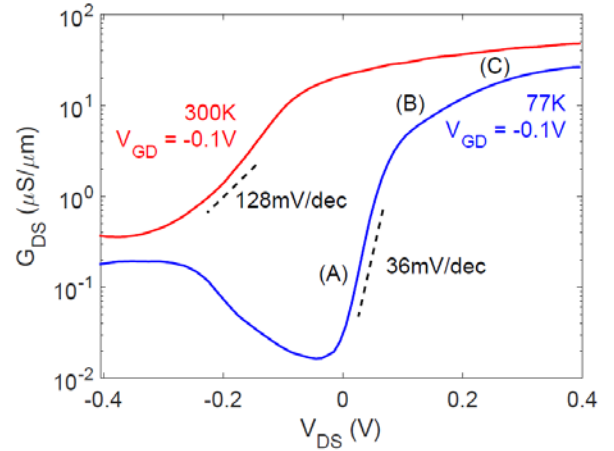**Fig. 3**: G_{DS} v. V_{DS} characteristics of a nanowire device in [5], measured at *T*=77K and *T*=300K. The labels (A)-(C) in the low-temperature curve correspond approximately to the mechanisms outlined in Fig. 1 (a)-(c).