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Project Title:
"Scalable, Economical Fabrication Processes for Ultra-Compact Warm-White LEDs"

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EXECUTIVE SUMMARY

Conventional warm-white LED component fabrication consists of a large number of sequential steps which are required to incorporate electrical, mechanical, and optical functionality into the component. Each of these steps presents cost and yield challenges which multiply throughout the entire process. Although there has been significant progress in LED fabrication over the last decade, significant advances are needed to enable further reductions in cost per lumen while not sacrificing efficacy or color quality.

Cree conducted a focused 18-month program to develop a new low-cost, high-efficiency light emitting diode (LED) architecture enabled by novel large-area parallel processing technologies, reduced number of fabrication steps, and minimized raw materials use. This new scheme is expected to enable ultra-compact LED components exhibiting simultaneously high efficacy and high color quality. By the end of the program, Cree fabricated warm-white LEDs with a room-temperature "instant on" efficacy of >135 lm/W at ~3500K and 90 CRI (when driven at the DOE baseline current density of 35 A/cm^2).

Cree modified the conventional LED fabrication process flow in a manner that is expected to translate into simultaneously high throughput and yield for ultra-compact packages. Building on its deep expertise in LED wafer fabrication, Cree developed these ultra-compact LEDs to have no compromises in color quality or efficacy compared to their conventional counterparts. Despite their very small size, the LEDs will also be robustly electrically integrated into luminaire systems with the same attach yield as conventional packages.

The versatility of the prototype high-efficacy LED architecture will likely benefit solid-state lighting (SSL) luminaire platforms ranging from bulbs to troffers. We anticipate that the prototype LEDs will particularly benefit luminaires with large numbers of distributed compact packages, such as linear and area luminaires (*e.g.* troffers). The fraction of total SSL luminaire cost made up by the LEDs themselves has steadily fallen over the past several years, but can still make up 30% or more of the bill of materials; the new LED design will radically lower this proportion. Ultra-compact, highly efficient LEDs with optimal distribution in the system will further benefit luminaire materials and assembly costs by reducing the complexity and volume of thermal management and optical subsystems.

GOALS AND ACCOMPLISHMENTS

Task 1: Virtual Wafer Formation

Virtual Wafer Chip Alignment

During prototype package fabrication development we utilized large-area chip arrays termed "virtual wafers". A principal requirement of this approach was proper alignment between the chip array and subsequent processing steps which define the reflective package floor, electrical contacts, and encapsulant (lens). The chips themselves must first be accurately positioned (in x and y), as well as in rotation (θ) with respect to an ideal square or rectangular grid. This is depicted in Fig 1 (left), which overlays these dimensions on a micrograph of an as-placed chip array. The chips are over-coated with phosphor and silicone encapsulant (lens), followed by transfer to a carrier after which the chip back plane is exposed for application of a reflective coating (see Fig. 1 right). We developed transfer methods which result in minimal chip misalignment after phosphor and encapsulant application, so the alignment between chips and

reflective coating depended more on the initial chip array accuracy as well as the alignment of the printing mask prior to coating application. Since the reflective coating acted as the package floor it had to be carefully aligned with the chips to avoid either overlap of chip contacts, or gaps at chip edges from which blue light could escape. Significant development was undertaken to quantify acceptable variations in chip position and coating opening alignment to the chip array, in order to maximize yield.

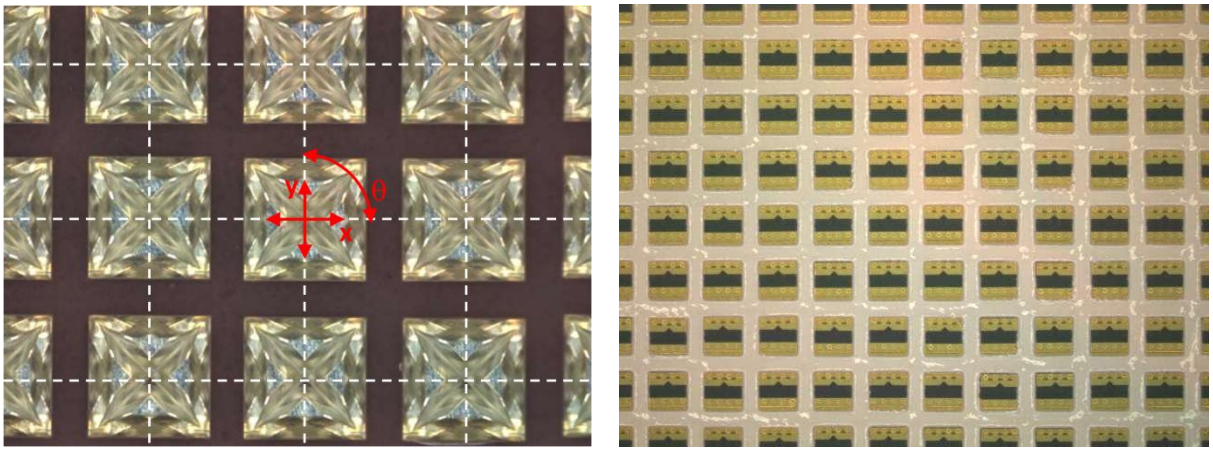

Fig. 1. Left: micrograph of an as-placed chip array, with orientation of x,y, and θ dimensions as well as an ideal grid (white dashed lines) indicated. Right: micrograph of a chip backplane which has undergone selective application of the reflective package floor. The coating must be accurately applied to avoid chip overlap as well as gaps around chip edges from which blue light could escape.

As indicated in Fig. 2 (left), the as-placed virtual wafer chip positional accuracy was typically <20µm, providing a good baseline for subsequent tolerance evaluations. These data were gathered from an automated optical microscope measurement system which could scan over the chip array and quantify positional errors with respect to an ideal grid.

The contour plot at right in Fig. 2 shows the variations in positional alignment of openings in the reflective coating (package floor). As described in the next section, initially there were large areas of the array in which the coating openings did not align well with the chips, which could ultimately lead to blue light leakage around the chip periphery. Displacements of more than ~50µm relative to the chip positions were thus considered unacceptable for opening position variation.

Process optimization was undertaken to correct the misalignment issues shown above, which largely involved alterations to key reflective coating parameters with respect to the underlying chip array. After several iterations, improvements were observed in the overall alignment of coating openings with the chips, as depicted in Fig. 3. With a few exceptions, alignment accuracy of <25µm was achieved, which is considered acceptable for high-yield scaling to larger array sizes.

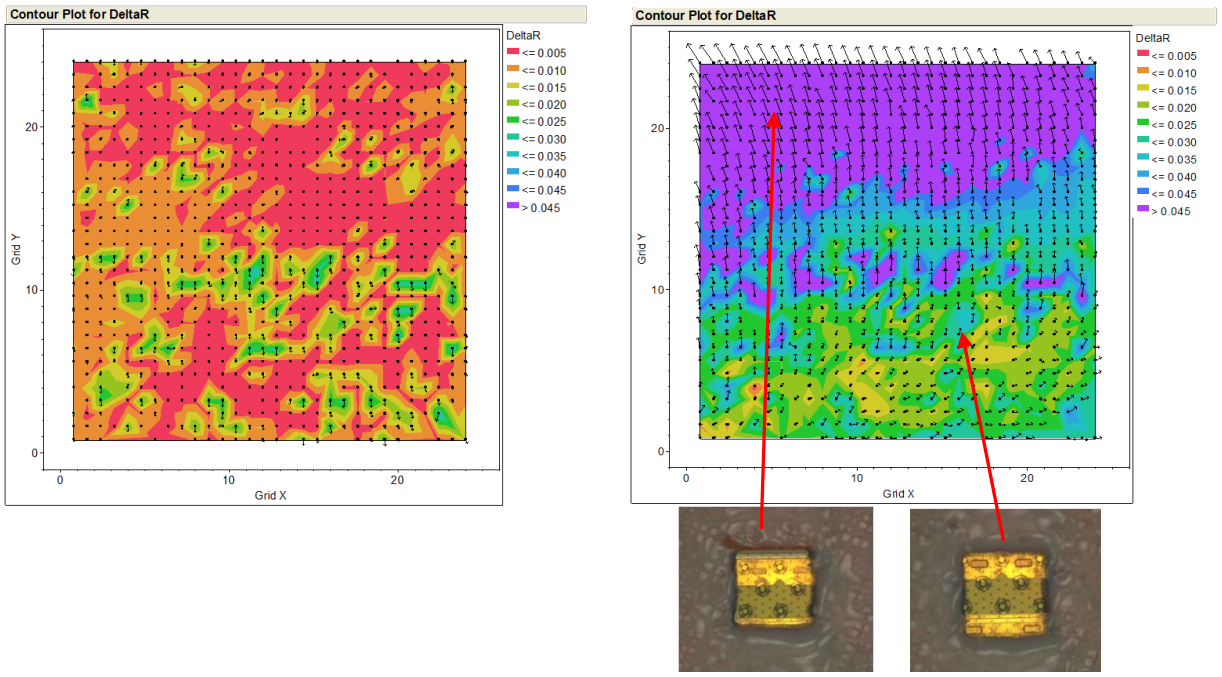

Fig. 2. Left: contour map of chip positional variation over a virtual wafer chip array. Right: misalignment of reflective coating openings relative to chip positions, with arrows indicating net displacement vector for each position. The micrographs below provide examples of misaligned and properly aligned openings.

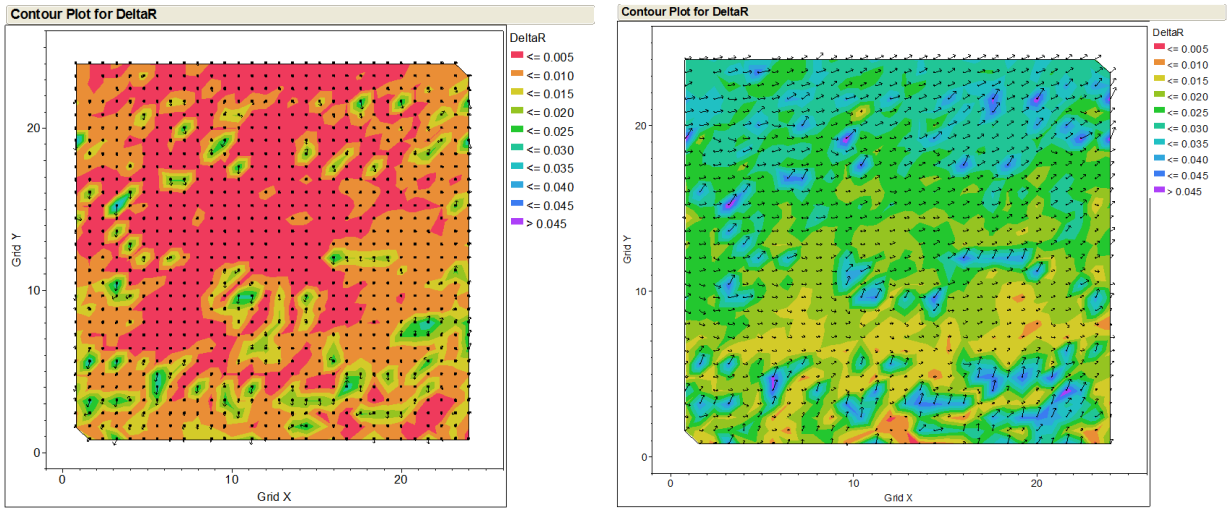

Fig. 3. Left: contour map of chip positional variation over a virtual wafer chip array. Right: misalignment of reflective coating openings relative to chip positions, with arrows indicating net displacement vector for each position. The net displacement of nearly all openings was <25µm, which is considered sufficient for subsequent processing steps and scaling to larger array sizes.

Reflective Package Floor

One of the primary cost reductions enabled by the prototype ultra-compact package geometry is the lack of a conventional package substrate. However, this approach also presents the challenge that some light may be emitted downward from either the phosphor or the chip itself. To mitigate this loss channel, we worked to develop a scalable application process that placed a highly reflective coating around the base of the chips. The reflective coating is based on earlier film development conducted during recently ended DOE project #DE-EE0005846.

The principal challenges in accurately applying the reflective coating related to chip positional accuracy (in both x/y and θ) in the virtual wafer array (described above), as well as alignment of the chips and the selective coating application. For the purposes of process development, virtual wafers of 20x20 and larger were created. Initial coating trials had mixed success in applying an even coating thickness while also defining openings through which the chip backsides (specifically the electrical contacts) would still be accessible. For example, as shown in Fig. 4 (left, center) it was not uncommon to observe too much overlap of the coating over the chip backside. After several coating application process development iterations, openings in the coating became more reproducible in position and size, as depicted in Fig. 4 (right). The overlap of the coating over the chip was enough to prevent light leakage around chip edges, but not so much as to obscure the contacts. The uniformity of this alignment over the entire virtual wafer array was quantified, as described above.

Fig. 4. Left and center: Examples of early reflective coating application trials, in which the coating overlapped the chip back-side (including electrical contacts) too much. Right: after coating application process development, the coating was reproducibly deposited with well-defined openings around chip positions.

Thermal Simulations

As originally conceived, the ultra-compact prototype package design would take the form of a chip directly soldered to printed circuit boards. While the removal of the conventional package substrate was attractive from a cost perspective, we considered trade-offs in other characteristics such as thermal management. We compared the thermal characteristics of chip-on-system configurations to conventional substrate-containing packages of similar chip size. A useful metric in this case is thermal resistance (R_{th}, units of °C/W), which indicates the temperature rise induced by a given amount of input electrical power that is not transformed into light. The

thermal resistance has implications for package design, but also places constraints on the thermal characteristics of the circuit carrier to which it is attached.

We utilized previously validated thermal simulation software to evaluate the effects of several key package and circuit board parameters on package thermal resistance. The first case was for a package containing a ~500µm chip, soldered to a metal-core printed circuit board (MC-PCB) and driven at a 1W input power (see Fig. 5). The thermal resistance was calculated at ~40°C/W, which resulted from the constrained thermal path from the chip to the MC-PCB via the solder joints (~60 W/m-K). In comparison, the Cree XQ-B package has a thermal resistance of ~17°C/W.

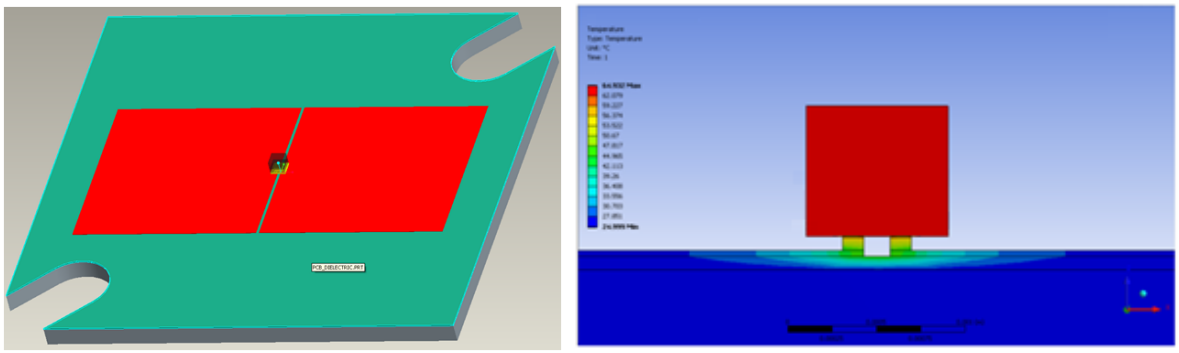

Fig. 5. Left: schematic of a package with a 500x500µm chip soldered directly to Cu traces (red) on a MC-PCB (green). Right: thermal simulation of the package at 1W input power, indicating ~40°C/W thermal resistance for the baseline condition.

When the package above was simulated as mounted to a ceramic submount (itself soldered to the MC-PCB with Pb-free solder), the R_{th} was reduced to ~35°C/W, an improvement over the direct chip-to-board case (see Fig. 6). This indicated the utility of a moderately conductive ceramic element as a lateral heat spreader prior to heat conduction into the board Cu traces and the MC-PCB itself.

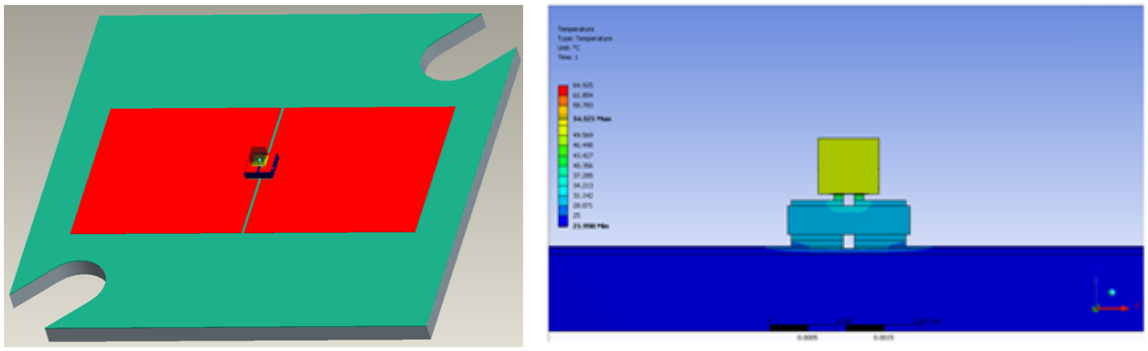

Fig. 6. Left: schematic of a package with a 500x500µm chip soldered directly to Cu pad (red) on a MC-PCB (green). Right: thermal simulation of the package at 1W input power, indicating ~35°C/W thermal resistance for the baseline condition.

The effect of Cu trace thickness was studied, with the results shown in Fig. 7. The thermal resistance decreased significantly with Cu trace thickness, from 35°C/W for the

baseline 35µm case to ~25°C/W for 110µm thickness. A thicker solder bond line caused higher R_{th} values at all Cu trace thicknesses, which was expected due to the inferior thermal conductivity of solder (~60 W/m-K) compared to Cu (~400 W/m-K). The situation was also affected by the composition of the PCB itself, as FR4 yielded higher R_{th} values at all Cu trace and bond line thicknesses studied.

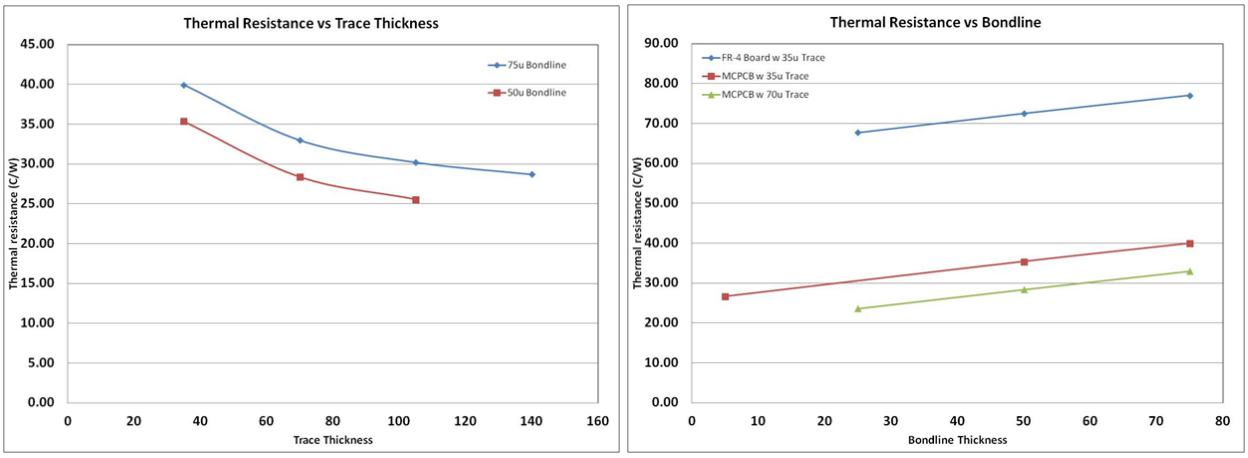

Fig. 7. Left: Package thermal resistance vs. Cu trace thickness on MC-PCB for 50µm and 75µm thick solder bond lines. Right: Thermal resistance vs. solder bond line thickness for 35µm and 70µm Cu trace thicknesses, compared to 35µm Cu traces on FR4 PCB.

We also evaluated the thermal behavior of a larger prototype package with a ~1000x1000µm chip, also driven at 1W input power. Two 35µm-thick Cu pad cases were considered, both on MC-PCB (see Fig. 8): one with the Cu pad slightly larger than the pacakge itself, and the other with a Cu pad of much larger area. This was done to illustrate the vital role of heat conduction within the thin Cu pad and traces, even on a thermally conductive substrate such as MC-PCB.

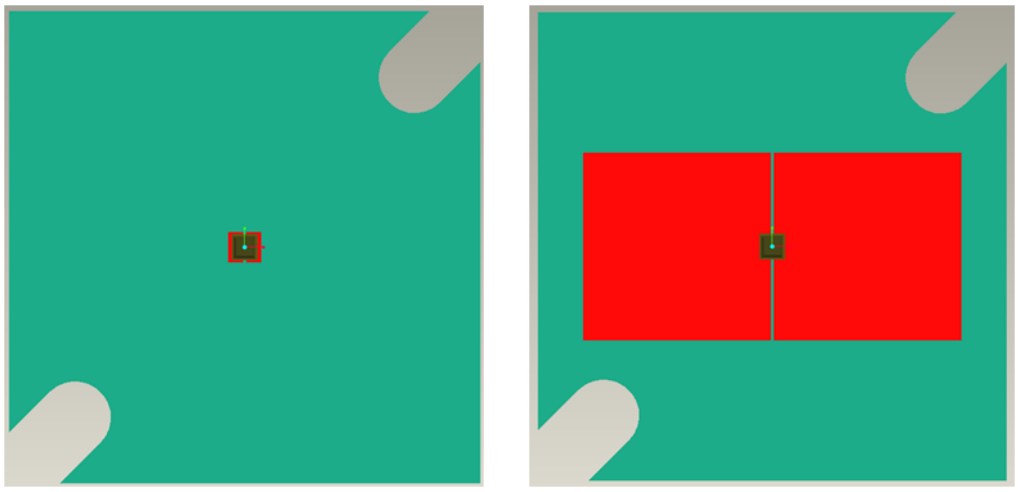

Fig. 8. Left: schematic of a package with a 1000x1000µm chip soldered directly to a Cu pad (red) on a MC-PCB (green). Right: the same package soldered to a Cu pad of much larger area.

As expected, the thermal resistance of the small-pad case was higher than the large-pad layout: 23°C/W vs. 12°C/W, respectively (Fig. 9). For comparison, the thermal resistance of the Cree XQ-D LED is ~7.5°C/W, owing to its thermally conductive substrate.

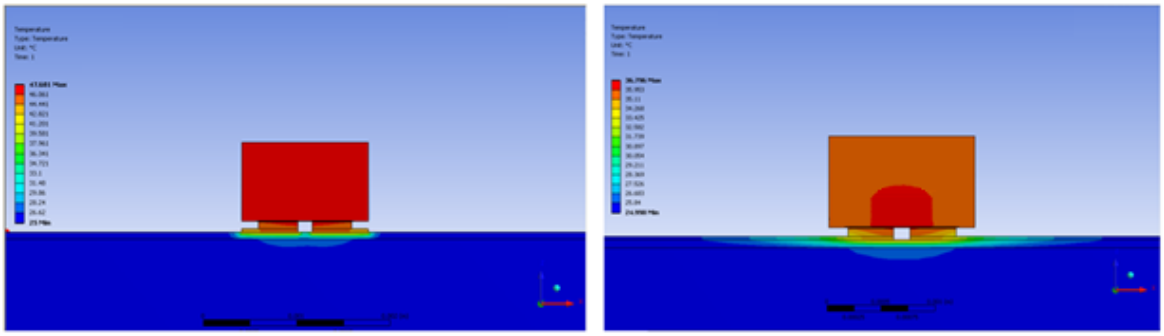

Fig. 9. Thermal simulations of the two cases depicted in Fig. 4: at left, a small package soldered to a small Cu pad of slightly larger size than the package itself; right: small package soldered to a Cu pad of much larger area.

The larger package thermal performance was analyzed for various Cu trace and bond line thicknesses. As shown in Fig. 10, the bond line thickness for this larger package did not affect R_{th} significantly, while the Cu trace thickness for the large-pad case reduced R_{th} to below 10°C/W. The large-pad package case was thus approaching the value for the conventional XQ-D package, indicating that further optimization could bring them to parity. This highlights the importance of circuit and board design for such prototype packages, since the critical thermal conduction pathways differ from conventional substrate-containing packages.

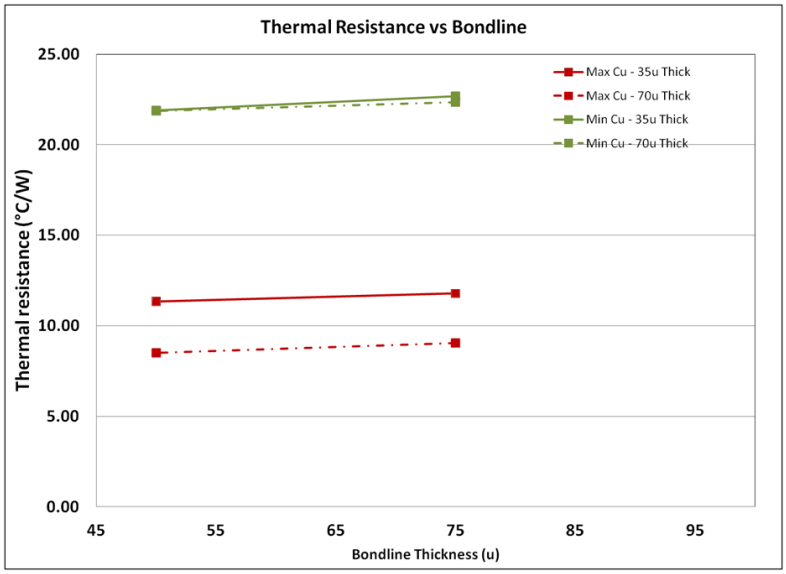

Fig 10. Thermal resistance for the large package (1000x1000µm chip) as a function of bond line thickness for combinations of Cu pad thickness and area. The R_{th} values for the large package with large Cu pad at the higher thickness (70µm) are nearly on par with the comparably sized XQ-D package, which has an AlN substrate.

Task 2: High Efficacy at High Color Quality

Downconverter Configuration

The configuration of downconverters in conventional LED packages takes the form of either a blended phosphor coating directly on the blue-emitting chip (*e.g.* Cree XT-E), or a uniform blended phosphor fill of the entire encapsulant (*e.g.* Cree CXA series). We investigated new downconverter configurations which could offer the advantage of lower "cross talk" and self absorption. Prototype packages of three variations with common downconverters materials but differing intra-package configurations were fabricated to yield a ~3000K color temperature and >90 color rendering index (CRI), and were compared to a baseline conventional configuration.

As shown in Fig. 11 (left), the color points of all packages were within a reasonably small range, making inter-package comparisons valid. The normalized luminous flux (*i.e.* LF divided by the blue chip radiant flux for each package) was measured and compared. In Fig. 7 (right) it is clear that all new configurations showed a higher normalized flux than the baseline case, with configuration "C" 12-13% higher on average. Meanwhile, comparison among CRI R_a (average index) and R_9 (deep red sub-index) values indicated that both metrics depended on downconverter configuration as well (Fig. 12). We note that some solid-state lighting applications have been assigned a *de facto* R_9 acceptability value of 50, which in this case would dictate that configuration A be used. However, it is unclear yet to what degree R_9 values of 40 and 50 can be visually distinguished; this would require further evaluation in representative viewing environments.

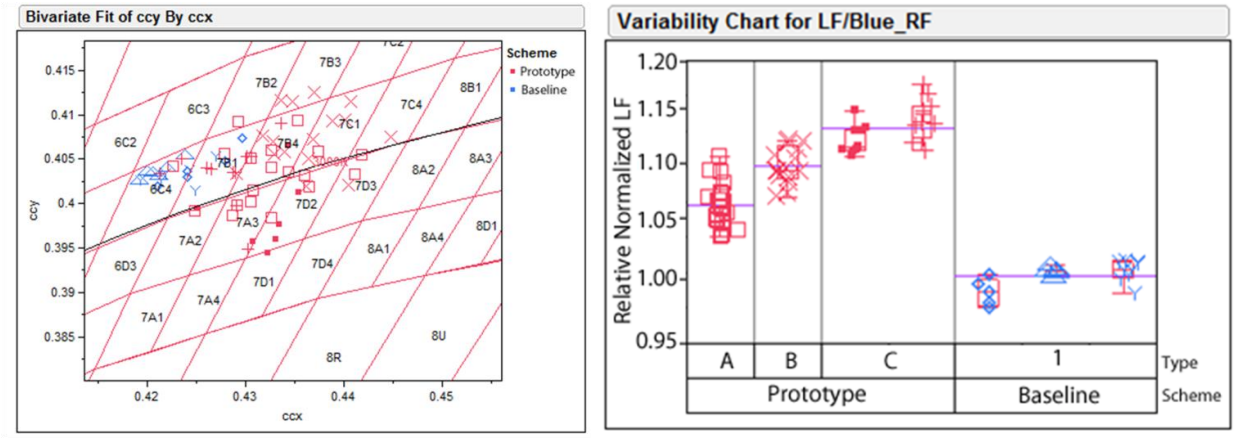

Fig 11. Left: color point distribution of LEDs with prototype and baseline downconverter configuration. Right: Relative normalized luminous flux (scaled to blue chip RF and normalized to the baseline package) for prototype vs. baseline configurations.

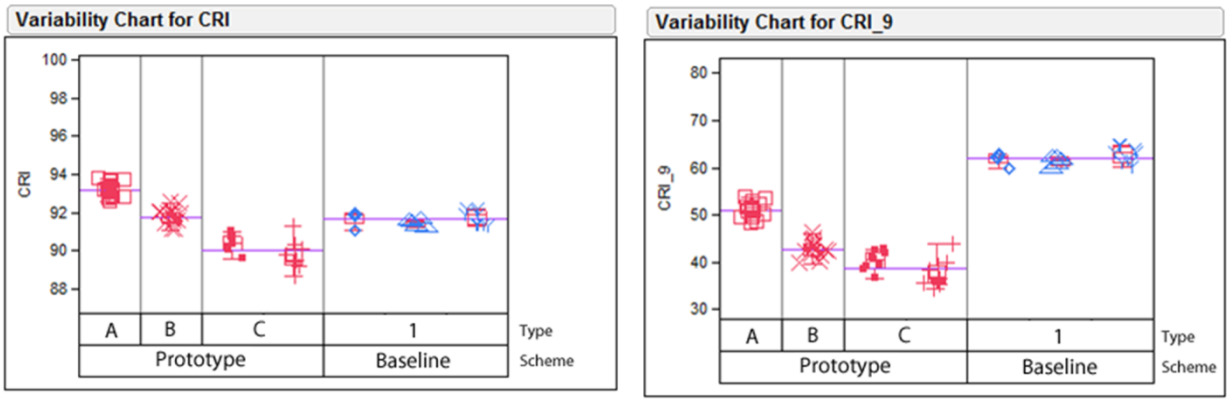

Fig 12. Left: CRI R_a (average) comparison among prototype and baseline downconverter configurations. Right CRI R_9 (deep red) index for prototype vs. baseline down-converter configurations.

Package Far-field Emission Characteristics

Prototype chip-level packages were fabricated with chips of sizes roughly equivalent to those in Cree's XQ-B and XQ-D packages. Since the prototype package lens fabrication procedure differed from that of the XQ, we performed angle-dependent luminous flux and color point measurements to establish if any changes in these characteristics resulted. As shown in Fig. 13, the far-field luminous flux distribution was quite similar to that of the XQ, with a broader width than packages with a hemispherical lens. Likewise, Fig. 14 demonstrates that the u' color point coordinate variation with far-field angle was quite similar to that of the XQ package, with some variation at high angles among downconverter configurations A, B, and C.

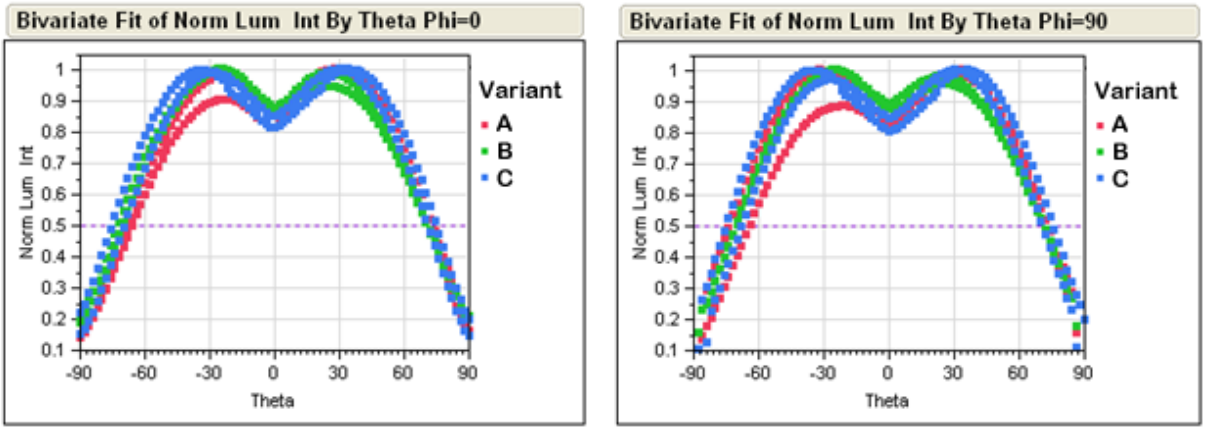

Fig 13. Far-field luminous flux of prototype LEDs at in-plane azimuth values of 0° (left) and 90° (right).

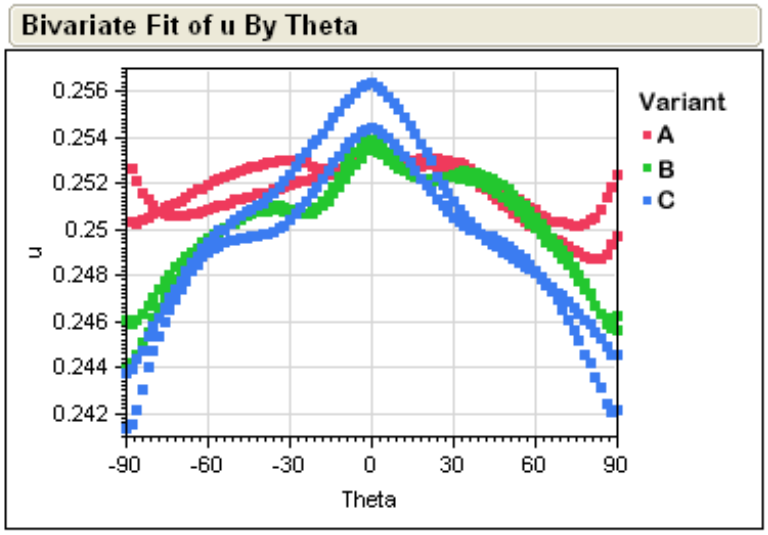

Fig 14. Far-field u' color point coordinate value of prototype LEDs at an in-plane rotation azimuth values of 0°.

Narrow-band Downconverters

In synergy with our other active Dept. of Energy SSL R&D program (DE-EE0007079) we evaluated narrow-band downconverters (NBDs) which emit in the red region of the spectrum, thereby resulting in higher net spectral efficiency. Based on spectral simulations, we expected that in most cases red-emitting NBDs should shrink the warm-white LED "efficacy gap" between 80 and 90 CRI that is typically seen with conventional red phosphors. As experimental validation, we combined a conventional yellow-green phosphor mixture with red-emitting NBDs, and by optimizing the configuration of these downconverters in the prototype package we achieved a room-temperature, "instant on" efficacy of **135.5 lm/W** at a current density of 35 A/cm^2, a color temperature of 3533K (with Duv = +0.002), and a CRI R_a value of **91**. Further improvements are expected as NBD quantum yield increases.

Task 3: Downconverter Application

One of the key development goals for the new prototype package fabrication process was to demonstrate high uniformity in downconverter application. We modified a conventional downconverter deposition process to work within this new scheme, while verifying that it should be scalable for future increases in virtual wafer size. By focusing on key process parameters such as temperature, deposition rate, and downconverter concentration, we have achieved high color point uniformity within deposition runs and also consistency from run to run. As shown for representative packages in Fig. 15, the 4-step bin yield of two successive runs was ~92%, which was an improvement on our earlier result (~85%). Process development work will likely be continued to assure that this new process is scalable and can achieve the level of reproducibility needed for a production process.

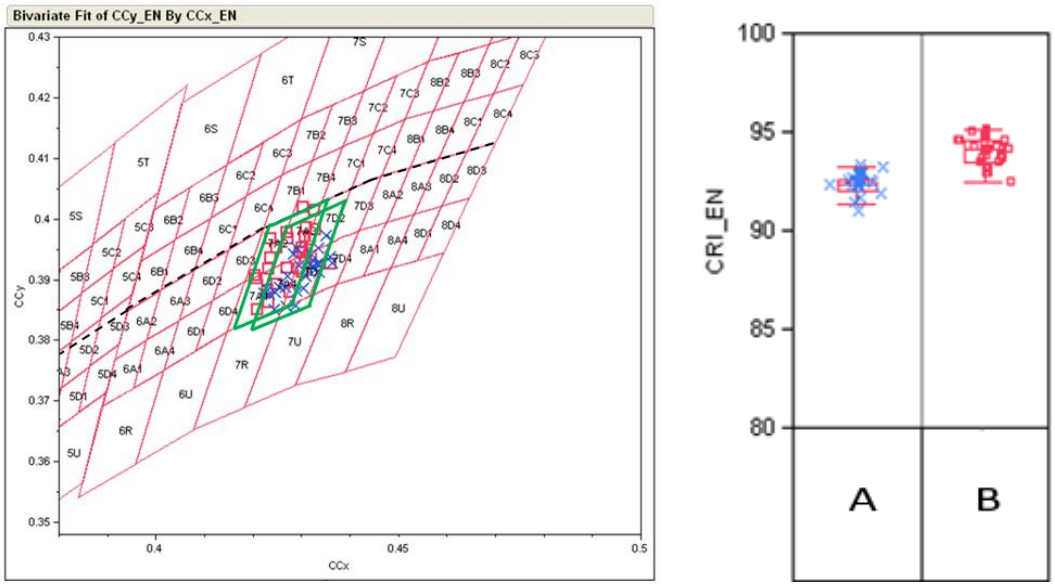

Fig 15. Left: color points of prototype packages fabricated in two successive runs, with the target 4-step bins highlighted in green for each. Right: CRI R_a values for the two runs, indicating >90 for both. The CRI R_9 values (not shown) were ~88-90.

Task 4: Encapsulant Application

A rapid and scalable method for encapsulant application was developed for the new fabrication scheme. In this step, a virtual wafer array with downconverter and reflective floor applied was uniformly coated with a clear encapsulant. We quantified encapsulant thickness uniformity by measuring the net encapsulant heights of at least 60 packages in arrays built around small (500µm) and large (1000µm) dies. The results, summarized in Fig. 16, indicated that the 3σ statistical variations from the mean (capturing 99.7% of the distribution) were 2.1% and 2.7% of the mean for the small-chip and large-chip case, respectively. These variations were lower than our target value of ±5%, demonstrating the likely suitability of this encapsulant application method for volume production.

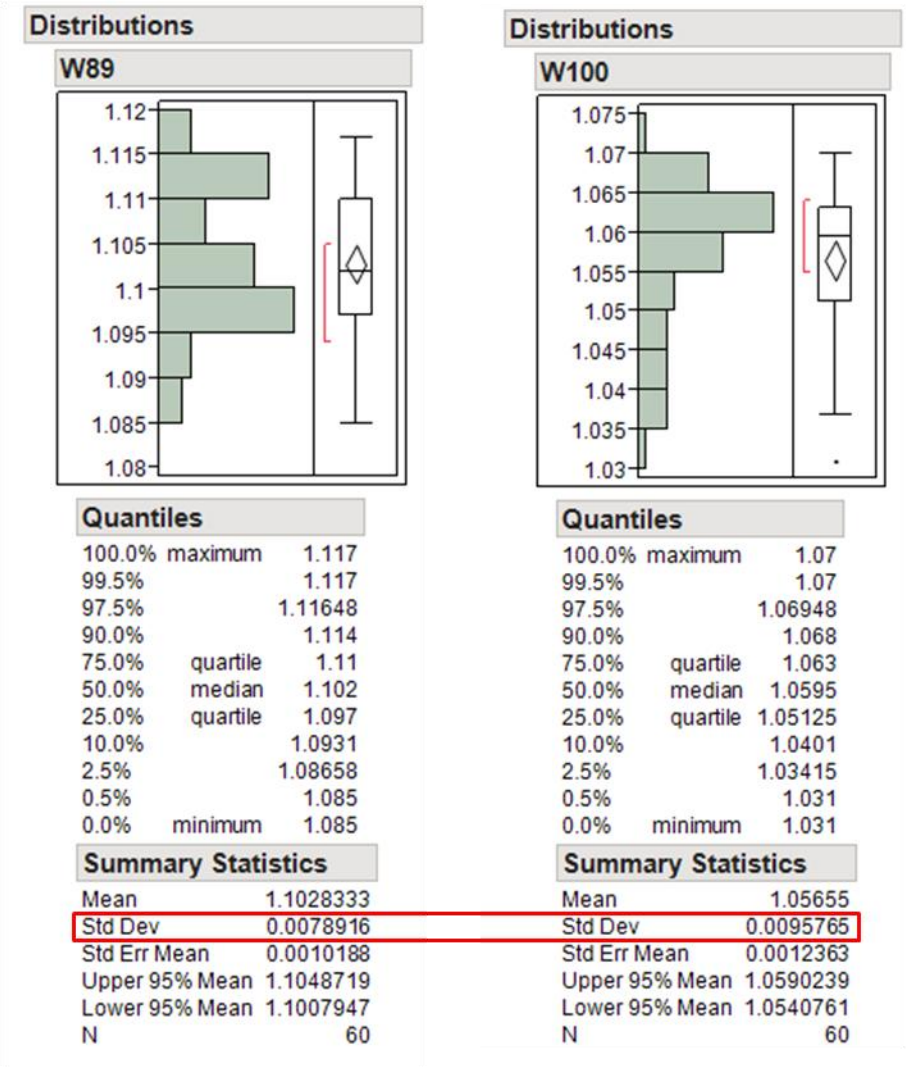

Fig 16. Encapsulant height distributions for prototype packages with small (left) and large (right) chips. The 3σ variations from the mean (capturing 99.7% of the distribution) were 2.1% and 2.7% of the mean value for the small-chip and large-chip case, respectively.

In order to verify that the prototype LED fabrication processes being developed during this program offered lower cost without an efficiency penalty, we periodically compared the luminous flux of new prototype package configurations to conventional components of similar geometry, and/or with the same chip size and type. An example is shown in Fig. 17, in which prototype LEDs were compared to Cree XQ-B LEDs fabricated from the same die sheet (for consistency in blue chip output). Here the prototype package was not only equivalent in luminous flux output vs. drive current (within the range studied), but conferred a slight efficiency advantage relative to the XQ-B baseline.

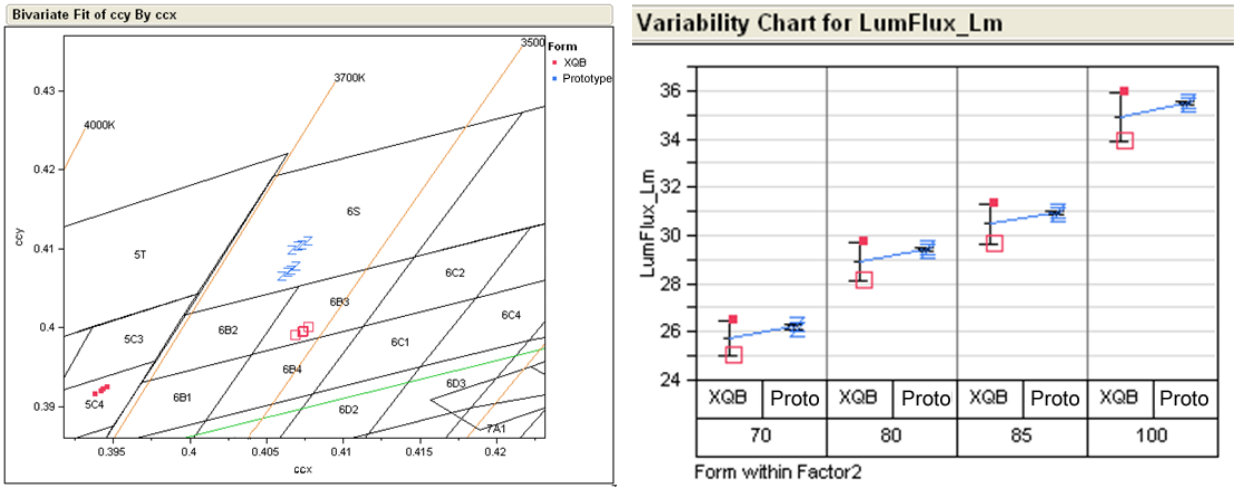

Fig 17. Left: color points of prototype & XQ-B LEDs being compared. Right: luminous flux (LF) values of XQ-B (red) and prototype packages (blue) at various drive currents, indicating the slightly increased LF of the prototype packages.

In addition to quantifying the relative encapsulation efficiency of the prototype package geometry compared to similarly sized XQ-B packages, we also compared prototype packages to much larger (9x9mm) domed MT-G packages, in which most of the light emitted from a small chip (of the same size used in the prototype package) should exit the LED encapsulant dome in a *single* pass, *i.e.* with high optical efficiency. This provided a quantitative assessment of the degree of light "recycling" (multiple bounces) within the prototype package, which directly affects luminous efficacy. A series of prototype and MT-G packages were fabricated in parallel, using chips from the same die sheet and with downconverter application optimized for proper color matching. The packages were fabricated with and without a reflective floor, to quantify its benefit for optical efficiency. As shown in Fig. 18, the color points of all packages fell around the blackbody locus at ~3000K. Relative luminous flux values (via integrating sphere measurements) revealed that the LF of the prototype package with reflective floor was on par with the MTG, while the version without the floor had ~3% lower output. This result confirmed that the optical efficiency of the prototype package geometry is high, despite its ultra-compact size and different lens geometry from conventional domed components.

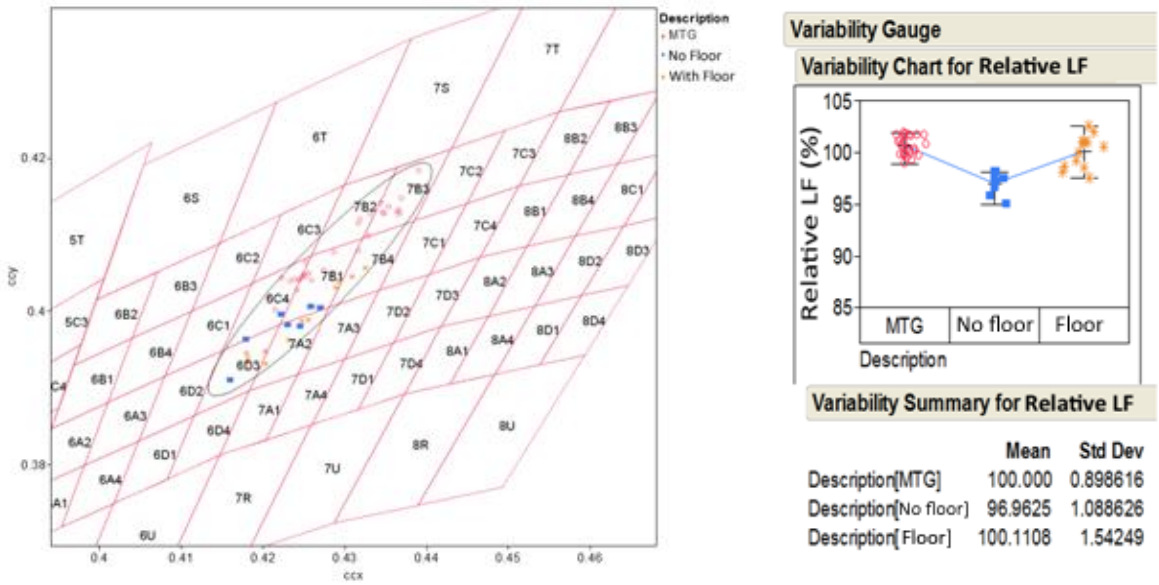

Fig 18. Left: color points of prototype and MTG packages; right: relative luminous flux comparison between MTG and prototype with and without reflective floor. The packages with reflective floor showed comparable LF to MTGs with the same chip size.

Task 5: Electrical Contact Development

From its conception, the prototype package was designed to include robust electrical contacts on the package underside. These contacts would enable electrical integration (surface mounting) of packages into luminaire systems regardless of circuit type, geometry, or substrate. The challenge was that the area of the electrical contacts on the underside of the chip at the heart of the packages was fairly small, and it was previously observed that successful die attach to typical printed circuit board (PCB) traces required a thick layer of solder paste; even then the die attach yield was not 100%.

Following the precedent of conventional surface-mount electronic devices such as diodes and transistors, we developed a solder bump process for the electrical contacts on the backside of the chips which could provide robust and reproducible package attach to the system. Solder bumps were fabricated by selectively applying solder paste directly to the chip contacts at a thickness that exceeded that of the reflective coating comprising the package floor. The packages were put through a solder reflow cycle during which the bumps formed (see Fig. 19 left). As shown in Fig. 19 right, varying solder bump thicknesses resulted from combinations of solder paste thickness and application mask opening size relative to the contacts, but the profile of all was similar (likely due to capillary forces during solder paste sintering). Groups of packages were then attached to conventional PCBs via another reflow step and the solder attach strength was evaluated using standard shear strength measurements. As shown in Table 1, the solder attach yield for chip-level packages incorporating solder bumps was 100%, relative to an 84% yield for packages without bumps. This demonstrated the utility of solder bumping for robust electrical integration of chip-level packages into the luminaire system.

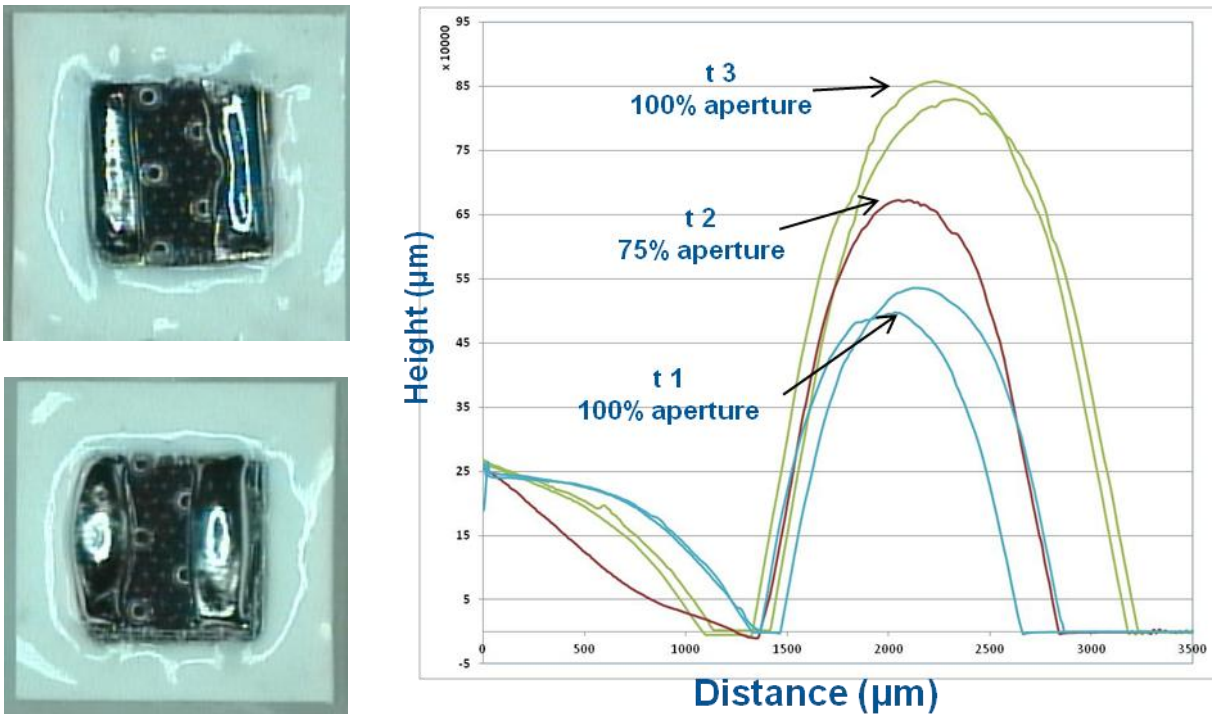

Fig. 19. Left: micrographs of reflowed solder bumps formed at two different thicknesses (t1 and t2). Right: surface profilometer scans of solder bumps at increasing thickness (t1, t2, t3) and two different mask aperture (opening) sizes.

Table 1. Solder attach yield of multiple groups of chip-level packages on standard PCBs. The attached yield of packages with solder bumps was 100%, compared to 84% for those with no bumps.

Solder Paste Mask	Reflective Coating Thickness	Solder bump height	Solder Attach Yield
No bumping	Standard	Not Bumped	13 Boards **84%** (109/130)
t1 100%	Standard	t 1	22 Boards **100%** (qty 220)
t2 100%	Standard	t 2	15 Boards **100%** (qty 150)
t2 75%	Standard	t3	15 Boards **100%** (qty 150)

The quality of the solder attach was analyzed with X-ray transmission imaging, which revealed defects not otherwise visible without shearing the packages off the PCB traces. As shown in Fig. 20, the use of solder bumps resulted in lower porosity within the solder layer than was observed for packages without solder bumps. We expected that this should result in a higher bondline shear strength, and possibly higher pad conductivity.

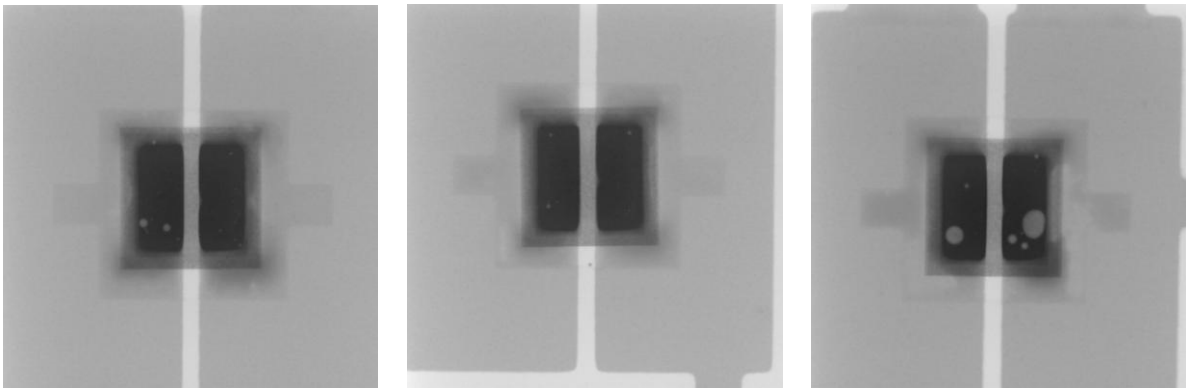

Fig 20. Transmission X-ray images of packages solder attached to PCBs with the solder bump process (left and center), vs. without solder bumps formed beforehand (right). The solder bump scheme enabled almost zero pore formation during solder reflow, which should result in higher shear strength.

Task 6: Demonstration Luminaire

The end-of-program demonstration lamp form factor was chosen based on prototype package performance characteristics as well as input from Cree product development teams. We elected to fabricate a modified version of the UR™ Series LED Upgrade Kit, since it is a cost-sensitive linear fluorescent retrofit product which could benefit from ultra-compact, low- to medium-power LEDs with low-cost potential. We designed PCBs to result in a linear prototype package array with a total lumen output which could be directly compared to the incumbent package design (*i.e.* without changes to the diffuser). See Fig. 21 for a picture of a lit demonstration UR tube. Testing and evaluation were conducted in an integrating sphere to quantify lumen output and efficacy. In Table 2 we compare the prototype-based demo tube to the commercially sold version (which employs Cree XQ LEDs). The prototype version exhibited a comparable efficacy to its commercial counterpart, despite having a higher CRI value (94 vs. 82). It was largely equivalent to the commercial version in other respects such as optical and thermal efficiency, such that it could be considered a viable "drop-in" replacement for the currently used packages in this product. Cost analysis is underway, but should prove favorable for the prototype package design relative to its conventional counterparts with comparable lumen output.

Fig 21. Photographs of the demonstration lamp with (left) and without (right) diffuser.

Table 2. Comparison of characteristics of the prototype package-based UR demo vs. its commercially sold counterpart ("baseline").

Factor	Baseline UR	Prototype UR
LED count	117	117
Color Temperature (CCT)	3520	3550
Color Rendering Index (CRI)	**82**	**94**
Lumen output (lm)	2372	2321
Efficacy (lm/W)	**123.1**	**122.8**
Optical Efficiency (%)	90	88
Electrical Efficiency (%)	86	86
Thermal Efficiency (%)	97	98

PROJECT OUTPUT

A. Publications

No project-related articles, papers, or presentations were made during this reporting period.

B. Technologies/Techniques

New technologies or techniques were developed under the Award, and are being considered for further independent development by Cree.

C. Status Reports

None.

D. Media Reports
No media articles during this reporting period.

E. Invention Disclosures
No subject inventions during this reporting period.

F. Patent Applications

No domestic or foreign patent applications arising out of subject inventions during this reporting period.

G. Licensed Technologies
No subject inventions licensed to third parties during this reporting period.

H. Networks/Collaborations Fostered
No partnerships or other arrangements were concluded with respect to the project or technology area during this reporting period.

I. Websites Featuring Project Work or Results
No web site or other internet sites that reflect the work or results of this project were established during this reporting period.

J. Other Products
No additional project output, such as data or databases, physical collections, audio or video, software or netware, models, educational aid or curricula, instruments or equipment was produced during this reporting period.

K. Awards, Prizes, and Recognition
No awards, prizes, or other recognition for project work or results, subjection inventions, patents or patent applications were received during this reporting period.