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LTCC Thick Film Process Characterization

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Abstract

Low temperature cofired ceramic (LTCC) technology has proven itself in military/space electronics, wireless communication, microsystems, medical and automotive electronics, and sensors. The use of LTCC for high frequency applications is appealing due to its low losses, design flexibility and packaging and integration capability. The LTCC thick film process is summarized including some unconventional process steps such as feature machining in the unfired state and thin film definition of outer layer conductors. The LTCC thick film process was characterized to optimize process yields by focusing on these factors: 1) Print location, 2) Print thickness, 3) Drying of tapes and panels, 4) Shrinkage upon firing, and 5) Via topography. Statistical methods were used to analyze critical process and product characteristics in the determination towards that optimization goal.

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Key words

LTCC, thin film, thick film process, shrinkage, screen print

I. Introduction

Low temperature co-fired ceramic (LTCC) is a well-established commercial technology based on simultaneous processing of glass-ceramic dielectric tape layers and noble thick film materials to yield a monolithic, multilayer structure similar to a printed circuit board. Processing steps are covered in detail in a comprehensive review [1]. The co-firing step causes the glass-ceramic tape to shrink by a defined amount. Due to dense circuitry and a design that is scaled up for production capacity, shrinkage tolerances compete with product tolerances. Thick film cover pads and filled vias must align with unique thin film features as shown in Figure 1 and they must do so *everywhere* across a 5 inch panel. The cover pads provide topographical protection over vias and the thin film pads define the circuit and provide protection to the thick film layers during soldering and subsequent use. The shrinkage tolerance for the commercial tapes is ±0.3%. On a 4.600 inch characteristic diagonal dimension, this amounts to a fired maximum positional variation of ±0.0158" (401 microns). Using a via size of 0.010" (250 microns),

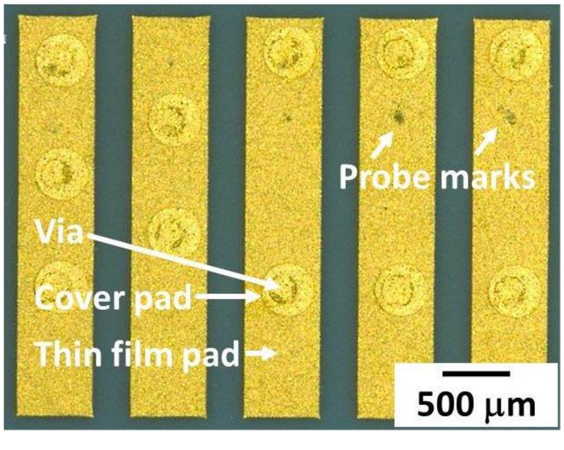

Figure 1. Acceptable thin film-to-cover pad-to via alignment is shown in this feature array.

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this could cause fixed tooling (glass masters and post-processing print screens) to be misaligned to critical features. Shape changes during the thick film processing stage can account for additional tolerance errors. Drying of filled vias on tapes can be responsible for shape changes that cause cover pads to be misaligned over vias, which increases the risk of an electrical open or short in the circuit. The process by which this shrinkage tolerance can be reduced has been examined.

II. Background

Low-temperature co-fired ceramics are substrate technology-of-choice for high frequency circuits. These materials have excellent electrical properties that allow for nearly unlimited stacking capability. Their mechanical properties support form-and-fit versatility as well as excellent mechanical performance under extreme environments.

The process flow used to make LTCC substrates is summarized below; the steps are listed in Table 1.

Table 1. Process Flow

1. Predict shrinkage/select expansion factor
2. Thermal condition and settle
3. Punch tape
4. Automated optical inspection
5. Via filling
6. Compress vias
7. Dry via filled tape
8. Print conductors side 1
9. Dry conductors
10. Remove backing
11. Print conductors side 2
12. Dry conductors
13. Remove backing on other layers
14. Collation
15. Lamination
16. Green machine
17. Cofire
18. Thin film circuit definition
    a. Physical vapor deposition (PVD)
    b. Photolithography
    c. Ion milling

The first step (1) in the fabrication is to **predict the shrinkage and set an appropriate expansion factor** for the artwork so that the unfired tape shrinks to the correct size within tolerances during the firing process. Assuring LTCC tape shrinkage begins by considering the vendor certification and in-house data to select the appropriate material lot. The lamination pressure and conductor loading, by area and thickness, are the other key process factors to control shrinkage [2, 3].

Tape is conditioned by subjecting it to a thermal profile and a hold time consisting of 1 hour at 100°C. The **thermal conditioning and settling step** (2) renders the LTCC tape dimensionally and thermally stable during downstream thick film processing. Dimensional stability is required for proper cover pad-to-via alignment and ground plane-to-via alignment. The tape remains on its backing for this treatment and a subsequent settling time of 72 hours (while vacuum-bagged). The design calls for alternating the tape casting direction between alternate layers of the circuit to further control the extent of shrinkage.

The **tape punching** (3) operation creates features such as electrical vias, cavities, shelves, alignment and registration holes. . The registration holes are used for layer-to-layer alignment. These mechanical features have critical dimensions in order to “joint up” with surface and internal conductors.

Automatic optical inspection (AOI) (4) verifies proper punching functions. Feature validation includes both its respective dimensions as well as location on the panel versus the datum.

Via-filling (5) is performed by stencil printing techniques. The vias are filled from the side with the punchable stabilization backing. Once via metallization has been properly dried, a **compression step** (6) is performed with a roller and a surface planarization step is performed through the use of a sharp edge on surfaces that will be external in the finished product. The via-filled tape is then dried (7).

The next steps (8 – 13) result in traces, cover pads, ground planes, and other circuit features screen printed on that first side of the tape to connect with the vias as called out in the design definition. All wet prints are also dried in the prescribed manner. If the design calls for features on a second side of the tape, the backing is carefully removed and those features are added to the LTCC surface. Proper filling and printing must be verified at each stage after the second-side operation, the LTCC is dried.

Collation (14) is then performed in equipment that stacks the tapes in the proper order and tacks them in place. The collated and tacked panels are exposed to the **lamination process** (15). The typical process conditions are high pressure (3000 psi); moderate temperature (70°C); and short time (10 min). This is performed in an isostatic laminator, but additional fixturing is involved, including base plates and top plates.

Additional unique physical features are introduced by milling the unfired tape in a step referred to as **green machining (16).** Green machining creates through holes, blind and stepped cavities, and valley in the laminated LTCC panel. Valleys optimize signal isolation when the alloy seal frame is subsequently mounted within it. The cavities and valleys are formed by 'sense-mode-milling,' where the milling depth is found by electrically sensing the dried ground plane through an electrically conductive milling tool. Insertion of an additional drying step prior to the sense-mode milling was required to render more consistent depth to the valleys.

The laminated panels are **co-fired** (17) using a prescribed thermal profile that accomplishes the burnout of organic binders (450°C) and sintering (850°C) of the LTCC glass/ceramic structure into a multilayer "circuit board" to be used in multichip module (MCM) applications.

The final step in Table 1 is the **thin film circuit definition** (18). This process has three primary sub-processes (a – c). The first step (a) has the LTCC surface covered with a thin film layer using physical vapor deposition (PVD) techniques, specifically, *evaporation*. Next, the conductor circuit pattern is created by photolithography (b). A photoresist covers the thin film layer. The photo resist is used to create the circuit pattern using a mask that selectively exposes the former to ultraviolet light. The photoresist is developed, which exposes selected areas of the thin film. Ion milling is then used to remove the exposed thin film. Additional details of the ion milling process are provided in reference 4.

It is important to recognize that proper shrinkage control is critical for any stage of the fabrication process when fixed artwork (thin film photolithographic glass master or thick film solder mask screen) is used to correlate surface features to themselves as well as to the internal features.

The thin film technique comes with additional challenges. First, the thin film must *completely* cover all thick film structures. Neither alignment defects nor blemishes are allowed that would expose thick film structures to molten solder during the assembly process. The thin film metalized LTCC panel consisting of multiple circuits requires a tight dimensional tolerance across the entire panel. It is necessary to minimize starting size variations as well as x/y directional shrinkage during lamination and co-firing that will assure high production yields as well as improve the long-term reliability of the final MCM assembly. This paper investigates the critical upstream thick film processes that control the variations that can occur in the co-fired panel size.

1) Co-fired panel size variation

One MCM product has several unique structural features that challenge the alignment requirement. Thick film cover pads on external vias mitigate via topography so that subsequent thin film layers can assure the robustness and reliability of the solder joints. Each cover pad must be properly aligned over it's respective via. The complicating factor is shape changes that occur in handling, heating, and, ultimately, cofiring. In turn, the cover pads must be carefully aligned with respect to the post-fired thin film layer configuration. Because the LTCC substrate is a part of a final MCM product, the former's shrinkage tolerances must dovetail with the latter's tolerances.

Product defects appear when there is improper alignment. A satisfactory alignment is shown in Figure 2a. There are no abrupt steps in the cover pad and via that would challenge the thin film coverage. On the other hand, and it is best described schematically, Figure 2b shows problems that occur with cover pad misalignment to the via (and properly aligned thin film layer). The via cover no longer

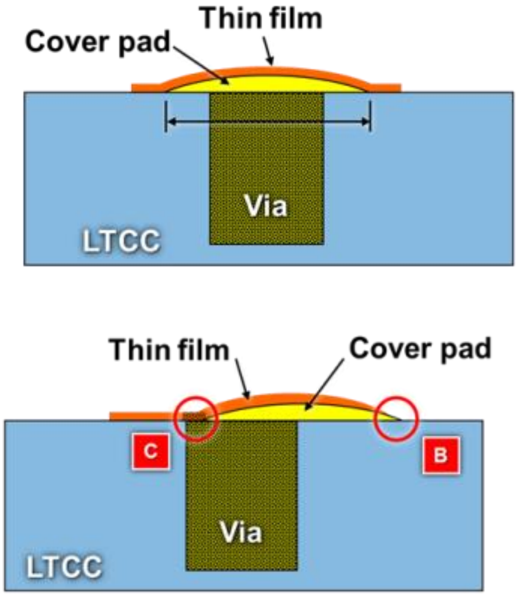

Figure 2. Role of thick film cover pads in thin film circuits.

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provides the topographical buffer over the via (location “C”). The thin film may be breached by molten solder when the via surface is too rough and is not adequately protected by the cover pad. The consequence is that the nearly pure gold (Au) via fill material can be attacked by molten solder that has breached the thin film as shown in Figure 3.

The second potential defect would occur at site “B” where the misaligned cover pad is exposed from under the thin film. Not only is there a potential degradation caused by the Au-Sn IMC reaction between molten solder and the nearly pure Au cover pad, there is also the solid-state reaction that can continue after the assembly process, which poses and increased risk to long-term reliability. Extensive studies have been performed to document these effects in order to quantitatively predict the loss of reliability by the defects observed in Figures 3 and 4.

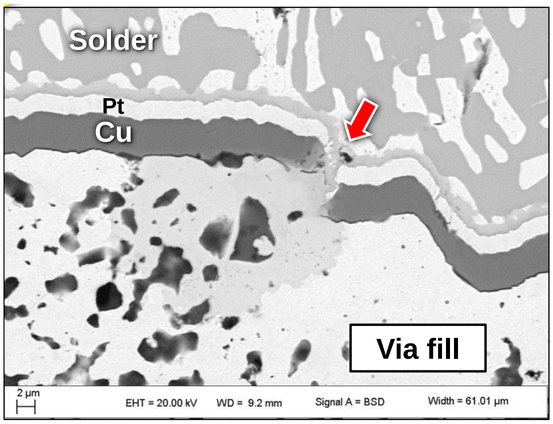

Figure 3. Breach of thin film with limited attack of the gold via fill by Sn-Pb solder

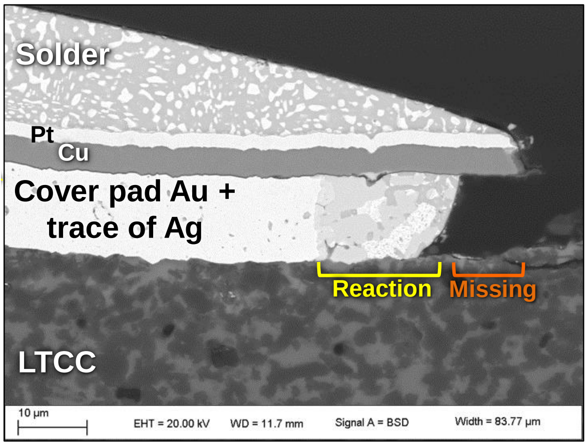

Figure 4. Attack of an exposed thick film gold cover pad edge by Sn-Pb solder.

Similarly, there was concern that via topography or the lack of a cover pad at a via boundary could lead to a breach of the thin film by solder similar to that shown in 3.

I. Discussion of Results

The thick film process was characterized with three goals in mind; 1) define the print location tolerance, 2) reduce the cofired panel size variations, and 3) improve the cover pad-to-via alignment. The characterization plan considered several process steps that affect the cofired panel size tolerance, green machining process yield, and alignment of the thin film features to those built of thick films – via and cover pads. Those process steps are: a) LTCC tape conditioning, b) Drying of via filled LTCC tape, c) Screen printing ground plane conductors. d) Drying ground plane conductors, e) Printing cover pad conductors, f) Drying cover pads conductors, g) Pre-collate drying for green machining, h) Lamination, and lastly, i) Co-firing. Several of these conditions are discussed in the following sections to exemplify the variables for, and results of, the experimental matrices.

LTCC Tape Conditioning

Design of Experiments (DoE) was conducted to quantify the impact on dimension stability of the unfired tape. The input factors are listed in Table 2.

Table 2 Input factors for conditioning experiment

1) Tape Conditioning Oven
2) Stack Count
3) Peak Temperature
4) Time at Peak

The LTCC tape was conditioned in eight experimental groups, the conditions of which are defined in Table 3. The high flow and low flow

Table 3. Experimental Factors.

Air Flow	Stack Count	Temperature (°C)	Time at Temperature (minutes)
High	10	75	45
High	1	75	60
Low	1	100	60
High	1	100	45
Low	1	75	45
Low	10	100	45
Low	10	75	60
High	10	100	60

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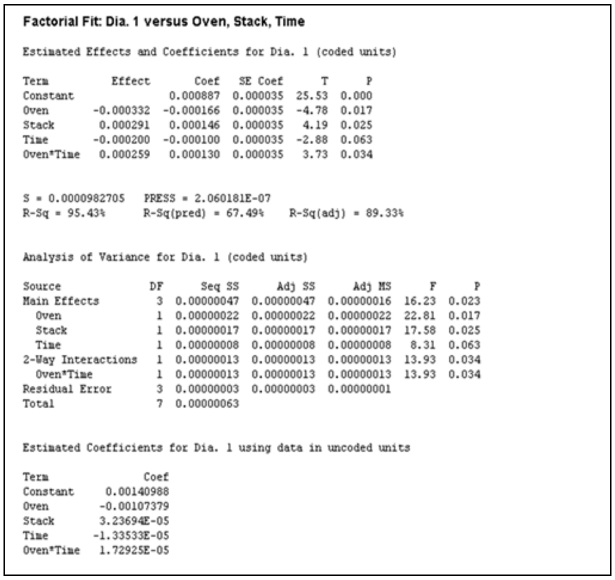
conditions were carried out in different pieces of available equipment, adding an additional factor that was scrutinized in the data analysis. While several metric dimensions were measured, only diagonal lengths are shared here in the interest of space.

Following conditioning, all tape layers were punched with a defined registration-hole pattern. The features of samples within each experimental group were measured using an optical coordinal measuring system. The samples were then processed through a belt dryer twice with a peak temperature set at 70°C (simulating two typical drying cycles: via drying and ground plane conductor drying). Then, the test samples were re-measured to determine the changes, if any, caused by the drying cycles.

The analysis of variance (ANOVA) determed that three factors caused statistically significant changes: 1) airflow, 2) stack count, and 3) time at prescribed temperature. These factors changed the diagonal dimensions of the panel following two 70°C drying cycles at the 95% confidence interval with an R-sq (adj) value of 89.33% (see Table 4).

Table 4. ANOVA data summary – LTCC tape conditioning.



Factorial Fit: Dia. 1 versus Oven, Stack, Time

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Estimated Effects and Coefficients for Dia. 1 (coded units)

Term          Effect       Coef   SE Coef       T      P
Constant                0.000887  0.000035  25.53  0.000
Oven       -0.000332  -0.000166  0.000035  -4.78  0.017
Stack       0.000291   0.000146  0.000035   4.19  0.025
Time       -0.000200  -0.000100  0.000035  -2.88  0.063
Oven*Time   0.000259   0.000130  0.000035   3.73  0.034


S = 0.0000982705   PRESS = 2.060181E-07
R-Sq = 95.43%      R-Sq(pred) = 67.49%   R-Sq(adj) = 89.33%


Analysis of Variance for Dia. 1 (coded units)

Source               DF      Seq SS      Adj SS      Adj MS      F      P
Main Effects          3  0.00000047  0.00000047  0.00000016  16.23  0.023
  Oven                1  0.00000022  0.00000022  0.00000022  22.81  0.017
  Stack               1  0.00000017  0.00000017  0.00000017  17.58  0.025
  Time                1  0.00000008  0.00000008  0.00000008   8.31  0.063
2-Way Interactions    1  0.00000013  0.00000013  0.00000013  13.93  0.034
  Oven*Time           1  0.00000013  0.00000013  0.00000013  13.93  0.034
Residual Error        3  0.00000003  0.00000003  0.00000001
Total                 7  0.00000063


Estimated Coefficients for Dia. 1 using data in uncoded units

Term              Coef
Constant    0.00140988
Oven       -0.00107379
Stack      3.23694E-05
Time      -1.33533E-05
Oven*Time  1.72925E-05
```

The minimum size change was observed when the tape was conditioned in the high air flow oven; it was stacked one layer tall; and when the tape was conditioned for 60 minutes at 100°C as shown in the interaction plot in Figure 5.

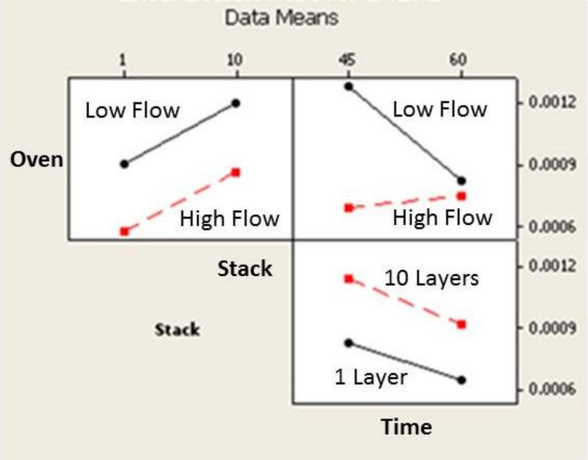

Figure 5. Interaction plots – LTCC tape conditioning experiment.

Print location

The alignment by a given printer is directly affected by the screen printer's print location repeatability (PLR). A PLR study was performed to determine the capabilities of the two different models of screen printer, a legacy screen printer (A) and a new screen printer (B) with tighter spatial controls. Intially, print alignment on Screen Printer A had a variability on the order of several thousandths of an inch, which is relativly large by today's standards for circuit miniturization. By rebuilding the theta-stage, the PLR was reduced by an order-of-magnitude so that it was similar to that of the new screen printer (B) as shown below (based on experiments having a sample size of 30):

Screen Printer (A) PLR: +/- 0.000665
Screen Printer (B) PLR; +/- 0.000792

The F-test and t-test statistics validated that the population variances and means of both screen printers are not significantly different at the 95% CI as shown in Table 5.

Table 5. PLR Statistical study.

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Ratio of standard deviations = 1.045
Ratio of variances = 1.092

95% Confidence Intervals
                                    CI for
Distribution   CI for StDev       Variance
of Data            Ratio            Ratio
Normal        (0.872, 1.250)  (0.760, 1.563)
Continuous    (0.638, 1.070)  (0.407, 1.144)

Tests
                                               Test
Method                           DF1  DF2  Statistic  P-Value
F Test (normal)                  129  111       1.09    0.634
Levene's Test (any continuous)     1  240       1.96    0.163
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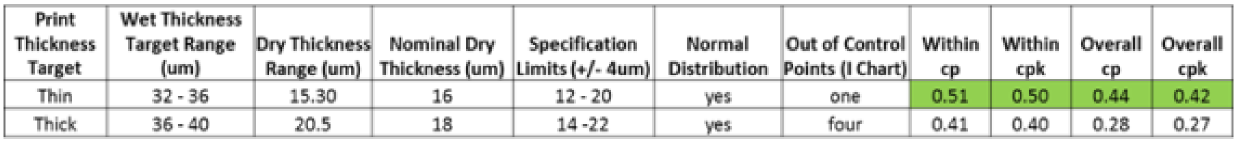
Print thickness

Print thickness and resulting LTCC panel weight has been shown to correlate with panel size (shrinkage). Based on the screen mesh selected to achieve the designed print resolution, a DOE was performed to optimize the wet and dry thickness target for a given screen mesh size opening. A 360 mesh screen having 0.5 mil emulsion was used in the process capability study. Results of the capability performed study on the existing screen printer set-up at two different wet print thickness target ranges (32 - 36um and 36um - 40um) are given in Table 6 below.

The baseline process had been 40±4 µm wet thickness and included qualitative assessments. Based on the process capability study, the lower wet print thickness target range of 32 - 36um was down-selected for non green machined thick film ground planes; Layers 1 through 6 ground plane and cover pad print thicknesses use 32–36 µm wet print thickness and the green machined ground plane Layers 7 and 8 use 36 – 40 µm wet print thickness to achieve a 32 µm minimum dry thickness. The optimum wet and dry thickness target was selected based on the minimization of the print thickness variation in the 40 um to 34um wet thickness range. The down-selected thick film printing process benefited the yield impact with respect to thin film feature alignment, mechanical dimensions, and a successful green machining feature definition.

Table 6. Screen print thickness of thick films



Print Thickness Target	Wet Thickness Target Range (um)	Dry Thickness Range (um)	Nominal Dry Thickness (um)	Specification Limits (+/- 4um)	Normal Distribution	Out of Control Points (I Chart)	Within cp	Within cpk	Overall cp	Overall cpk
Thin	32 - 36	15.30	16	12 - 20	yes	one	0.51	0.50	0.44	0.42
Thick	36 - 40	20.5	18	14 -22	yes	four	0.41	0.40	0.28	0.27

Drying tapes and panels

The drying equipment and profiles are critical, and outside of this effort, there has been significant improvements made to the drying equipment. Based on the change in tape size following one drying cycle, room-temperature drying of filled vias was chosen at the expense of schedule to ensure the best alignment of subsequently printed cover pads.

Drying has also proved critical for “green machining” of unfired panels, which occurs after lamination of a panel. Recall that this machining process uses ‘sense mode’ milling, where machining depth is determined by sensing the electrical conductivity of the buried ground plane layer. Optimum wet/dry thickness requires machining yield feedback due to minimum conductor thickness requirements for electrical sensing. Sensing errors have been a significant “in process” yield issue during process development. It was suspected that dried, but *not* fired, thick film conductors have variable electrical conductivity. Nevertheless, this conductivity is used successfully in the sense mode machining process and the drying step appears to be a contributing factor towards improved yields.

Shrinkage Variation upon Firing

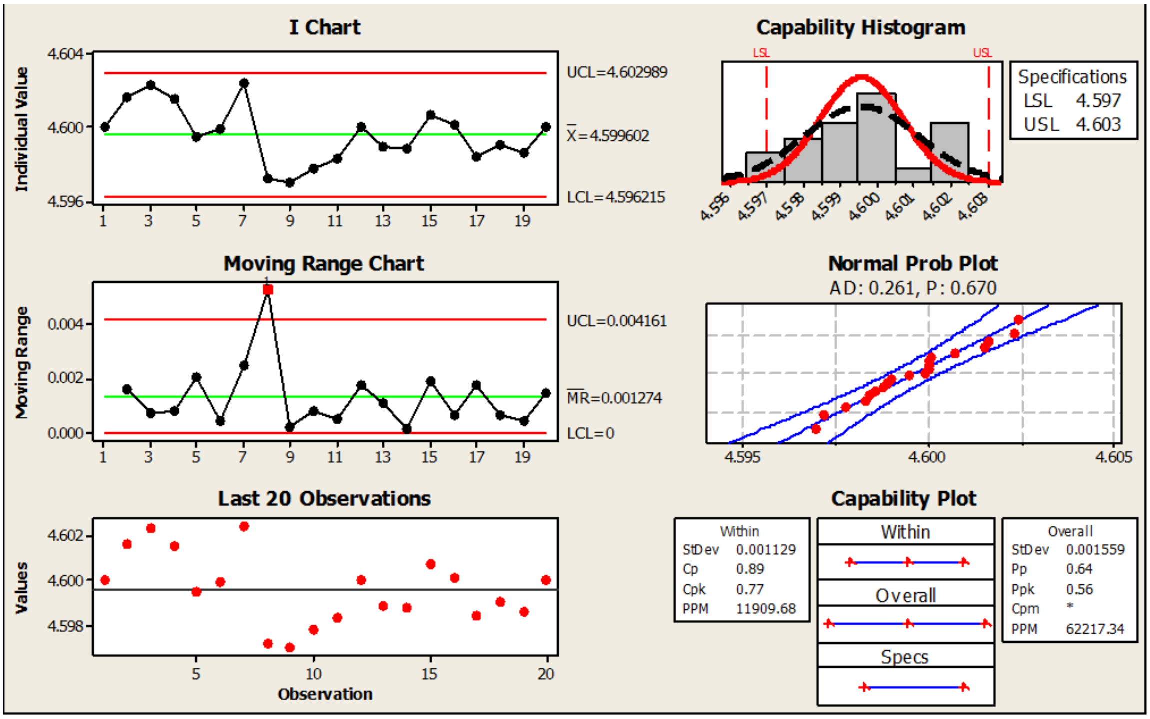
Shrinkage upon firing is a critical parameter in the design in LTCC. The shrinkage is not, itself, a problem; but, its tolerance needs to be tightly controlled in order to assure the proper alignment of surface and internal features. Panels that were 5” on a side and consisting of eight laminated layers were cofired in a ‘box’ furnace having a work zone of 12” x 14” x 18”. The peak temperature was 850°C and time interval of 45 minutes time at peak temperature. All cofire trials included a single panel positioned in the center of the furnace to eliminate any temperature gradient effects.

Based on a panel diagonal specification tolerance of 4.600” ± 0.003”, which exceeds the LTCC tape shrinkage tolerance of ± 0.3%, the cofire statistics of the baseline versus the down-selected process can be summarized in Table 7:

Table 7. Cofire statistics

Test Group	Diagonal Within cp	Diagonal Within cpk	Diagonal Overall cp	Diagonal Overall cpk
Baseline	0.54	-0.27	0.59	-0.30
DSelect	1.02	0.85	0.70	0.58

The cofire statistics of the confirmation run is shown in Figure 6.



Fiqure 6. Confirmation run of down-selected process.

Via topography

The via cover pad-to-via alignment is critical because it buffers the topography of the via fill surface to allow the thin film to build up in a contiguous manner. A contiguous thin film provides a barrier between the solder and the largely pure gold cover pad and via fill materials so that the latter are not leached by the former through breaches in the thin film. Two types of possible attack were shown in Figure 2. It was noticed that when the surface roughness of the via is reduced by the selection of alternate via fill materials, the assurance of via reliability by means of the cover pad, becomes less critical with respect to solder leaching. Some typical vias are shown in Figure 7.

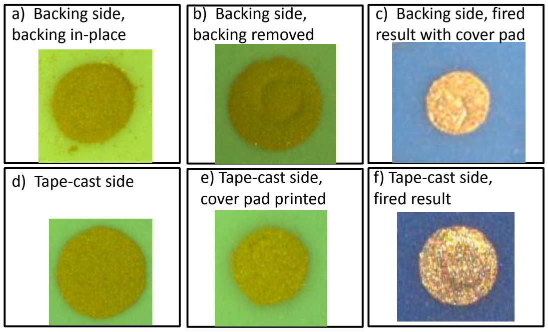


Figure 7. Origins of via topography

Because the vias are filled from the backing side and dried with the backing in place, the subsequent removal of the backing layer results in a via surface topography like that shown in 7b. Note the highly roughed surface as the via fill was disturbed by the removal process. The topography is shown in 7c that results from printing of a cover pad and firing of the LTCC panel. The opposite side is in contact with a separation layer during via fill, and removal of this separation layer leaves a smoother surface as shown in 7d. The unfired appearance of such a via covered with a cover pad is shown in 7e, and the fired result in 7f. By planning to use the smoother via surface on the external surfaces of the circuit, the safety factor for the thin film coverage is increased against solder breaching the thin film layer and leaching either the cover pad or the via fill material.

Optimized thick film process

The optimized thick film process includes the following provisions. Two-layer LTCC tape stacks are placed on perforated trays and are conditioned in box ovens at 100°C for 60 minutes. Vias are filled using a new (linear encoded print head) printer by multiple passes over electroformed stencils. Vias are compressed 30 to 45 minutes after via fill, but prior to room-temperature drying. Layers one (1) through six (6) use ground plane, trace, and cover pad prints with 32 µm to 36 µm wet print thicknesses. Layers seven (7) and eight (8), which are the reference ground planes, use thick films of 36 µm to 40 µm wet thickness. These conditions allow for realizing the required 32 µm minimum dry thickness in areas that support the 'sense-mode' green machining. Cover pads are printed prior to ground plane conductors and all printed conductors are dried at 80°C for 10 minutes. In addition, the layer one punch file is inverted so that the side defined by the stabilization backing is internally located and the coarse surface topography is eliminated from the vias. Layer 8 already benefits from this approach.

III. Conclusion

The thick film process steps that affect LTCC panel shrinkage variation have been characterized and optimized to enable improved thin film alignment with thick film surface and internal conductor features. Major steps that contributed to those benefits included a more uniform tape conditioning process; reducing the target thick film print thickness to match the capability of the required thick film screen; and defining a required print thickness tolerance. Those achievements were reflected by increases to product Cpk values from 0.39 to 1.05 with a specification tolerance ±0.003“ across a 4.600“ diagonal panel.

Independent of these process improvements, layout changes were made at the design level to increase the physical spacing between the thick film cover pad edges and the thin film features, reduction of cover pad size, and consideration for solder-free areas that are intact, but not threatened by solder interactions.

Process centering has improved through the elimination of tightening up the allowable lamination pressures. This effect was demonstrated on a lot size of 20 panels wherein fired size variations were reduced by 50%. Subsequent photolithography further amplified yields improvements at the completion of the thin film definition process.

Improvements in the green machining manufacturability and process yields included redesign of a cavity, implementation of additional thick film drying of all individual tape layers prior to collation to ensure uniform drying of the printed circuit pattern, improving the uniformity of the drying process, definition of the required thick film wet/dry circuit ground plane and reference ground plane print thicknesses.

Acknowledgment

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References

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[1] MR Gongora-Rubio, P Espinoza-Vallejos, L Sola-Laguna, JJ Santiago-Aviles, “Overview of low temperature co-fired ceramics tape technology for meso-system technology,” Sensors and Actuators A 89 (2001) 222-241.
[2] M. Girardi, G. Barner, C. Lopez, B. Duncan, L. Zawicki, “Predicting LTCC Firing Shrinkage: A Response Surface Analysis Study,” Journal of Microelectronics and Electronic Packaging Apr 2009, Vol. 6, No. 2 (April 2009) pp. 114-118.
[3] J. Kupferschmidt, M. Girardi, B. Duncan, and D. Whitlock , “Determination of LTCC Shrinkage Variations from Tape Manufacturer to Consumer.” International Symposium on Microelectronics: FALL 2014, Vol. 2014, No. 1, pp. 000668-000672.
[4] J.A. Wolf, K.A. Peterson, P.T. Vianco, M.H. Johnson, S. Goldammer, “Robustness and Versatility of Thin Films on Low Temperature Cofired Ceramic (LTCC),” 44th International Symposium on Microelectronics (IMAPS), International Microelectronics and Packaging Society, Long Beach, CA, October 9-13, 2011.