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Recommendations for Isolation Monitor Ground Fault Detectors on Residential and Utility-Scale PV Systems

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***Abstract* — PV faults have caused rooftop fires in the U.S., Europe, and elsewhere in the world. One prominent cause of past electrical fires was the ground fault detection "blind spot" in fuse-based protection systems uncovered by the Solar America Board for Codes and Standards (SolarABCs) steering committee in 2011. Fortunately, a number of alternatives to ground fault fuses have been identified, but there has been limited adoption and historical use of these technologies in the United States. This paper investigates the efficacy of one of these devices known as isolation monitoring (or isolation resistance monitoring, R_{iso}) in small (~3kW) and large (~700 kW) arrays. Unfaulted and faulted PV arrays were monitored with R_{iso} technology and compared to SPICE simulations to recommend appropriate thresholds to the maximize the range of ground faults which could be detected while minimizing unwanted tripping. Based on analytical and computational models, it is impossible to determine a trip threshold that provides fire safety and negates unwanted tripping issues. This paper mathematically demonstrates that appropriate R_{iso} trip thresholds *must* be determined on an array-by-array basis with sufficient leeway by system operators to adjust trip threshold settings for their particular usage cases.**

***Index Terms* — R_{iso}, PV safety, series and parallel faults, ground faults**

I. INTRODUCTION

PV ground faults are a shock hazard [1] and have caused many fires in the U.S. and around the world [2, 3]. In cases of faults on rooftop systems, the resulting fire can incinerate buildings and put the first responders and occupants' lives at risk. Further, publicity surrounding these fires is changing public perception of solar in harmful ways. The SolarABCs steering committee investigated ground faults and the ground fault detection blind spot [4-6] in 2011-2013. The conclusion of this work was that fuse-based GFDI (Ground Fault Detector/Interrupter) designs were vulnerable to faults to the grounded current-carrying conductor (CCC).

A GFDI is unlikely to detect a fault on the grounded CCC, which could allow unrestricted fault current flow to bypass the GFDI if a second fault is initiated elsewhere in the array. This problem has caused multiple rooftop fires in the past [2, 3, 7]. A number of alternative ground fault technologies and methods were suggested [5], including isolation/insulation monitoring (R_{iso}) [8, 9], residual current detection (RCD) [10], and current sense monitoring/relays (CSM/R) [6], but there is little experience with these technologies in the U.S.

In its simplest form (i.e. neglecting array capacitance and noise sources) R_{iso} measurements are carried out on ungrounded systems (or grounded systems which are temporary disconnected from earth ground) by injection of a voltage pulse into one of the two CCCs of the PV system by an external power source. The ground isolation can then be calculated from the current draw on the power source, represented in Eq. (1). If the isolation is measured to be below a certain threshold, the isolation monitor trips.

$$R_{iso} = \frac{V_{applied}}{I\left(V_{applied}\right) - I\left(V_{applied} = 0\right)} \qquad (1)$$

This process is carried out with both positive and negative polarity pulses on one or both CCCs. The pulse polarity and CCC should not affect the measurement of the fault as long as there is sufficient illumination to forward bias the module photodiodes. In low illumination conditions, the pulse will travel through the bypass diodes. One pulse polarity will pass through the bypass diodes and measure the fault, as long as the pulse magnitude ($V_{applied}$) is large enough to overcome the voltage drop of the multiple bypass diodes in the array. The opposite pulse polarity will be blocked by the bypass diodes, possibly leading to anomalous R_{iso} readings. The parasitic resistance of the bypass diodes will add slight position dependence in low-light conditions.

In previous work, the baseline measurements for utility-scale systems were analyzed and compared to ground fault isolation standards [8]. In this paper, we validate the Sandia ground fault SPICE model with experimental R_{iso} measurements of physical faults on two large (750 kW) PV arrays. This, in conjunction with previous [11] validation on ~3 kW arrays is used as a basis to present a theoretical understanding of fault current/power and R_{iso} trip thresholds for safe operation of PV arrays.

The detectable area of R_{iso} measurements depends on the threshold used to define the presence of a fault. Ideal detection thresholding maximizes the balance between system safety and uptime, and is essential to the performance and reliability of the PV array and the safety of those around the system. If this trip threshold is too low, there will be nuisance trip events; but if the threshold is too high, certain ground faults

will go undetected. R_{iso} methods register array leakage current (from modules or inverter) as a type of fault; therefore the detection threshold must be set above the maximum leakage current in all conditions (meteorological, configurational, and electrical) while also set low enough to detect the worst-case, lowest current faults possible in the array.

As determined in previous work [9], the array R_{iso} can be calculated in (2) and is a function of module isolation (R_{module}), inverter isolation (R_{inv}), fault resistance (R_{fault}), number of strings in the array (S) and modules in a string (M), as well as the equipment ground conductor (EGC) resistance (R_{EGC}).

$$R_{iso} = \frac{1}{\frac{S \cdot M}{R_{\text{module}}} + \frac{1}{R_{inv}} + \frac{1}{R_{fault}}} + R_{EGC} \qquad (2)$$

Further, the leakage or isolation resistance to ground depends on both PV module and inverter technology [8, 12-15] and can drastically affect the detectable region of the R_{iso} measurements space (Fig. 1). At very high values of R_{fault} (>~100 kΩ seen in a healthy systems), the array R_{iso} is dominated by the isolation of the module and other balance-of-system (BOS) components to ground. The size of the array (S, M) and the specific isolation of these components are (R_{module}, R_{inv}) can have a significant effect on fault detectability since, in general, it is not possible to detect the presence of a fault with a larger resistance than the system itself. At very low fault resistances, the R_{iso} measurement is dominated by the series EGC resistance.

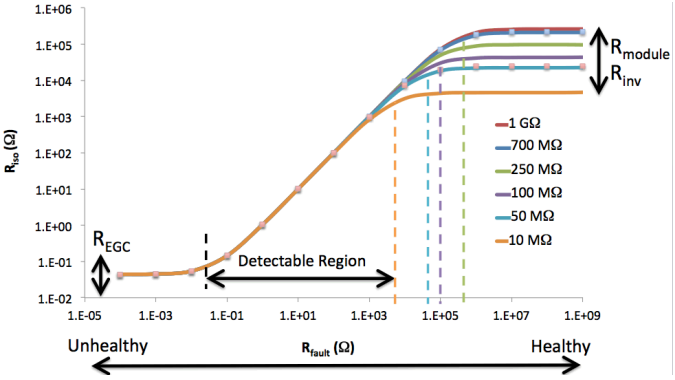

Fig. 1: R_{iso} as a function of R_{fault} for different healthy system isolations to ground. Changes in inverter or module isolation can have significant impacts on the detectability of faults.

Inverter isolation can be a significant contribution to overall system R_{iso}, especially in utility-scale arrays. Previous analysis of large PV arrays [9] have shown that modules can have several hundred MΩ to GΩ of isolation per module while inverter isolation values can be as low as tens of kΩ, even when nominally disconnected from ground. These leaky inverter pathways to ground significantly affect baseline R_{iso} readings and therefore, negatively impact the detectability of high-to-moderate impedance faults.

II. GROUND FAULT EXPERIMENTS

Ground faults were induced on two 1000 V, 1.5 MW, positively grounded PV arrays located in Riverside, CA. The arrays consisted of 336 and 408 strings (Array 01 and 02, respectively) of ten E20-435-COM SunPower modules per string. 0.1, 2.6, and 5 kΩ faults were induced at the positive CCC (1+), one module into the array (1-), and five modules into the array (5-) as measured from the nominal positive CCC. After fault initiation, the array was ungrounded and a Bender isoPV-3 unit with coupling box (AGH-PV-3) was used to obtain array R_{iso}. The results of each test are shown in TABLE I.

TABLE I
RESULTS OF FAULT INSTALLATION ON TWO 1.5 MW PV ARRAYS

Time	Fault Location	Fault Impedance (kΩ)	Inverter	isoPV Reading (kΩ)
7:28 AM	1+	5.0	INV02	3.8
8:45 PM	1+	2.6	INV01	2.4
9:05 PM	1-	2.6	INV01	7.2
9:25 PM	5-	2.6	INV01	7.7
Morning	None	None	INV02	19
1:25 PM	1-	0.10	INV01	<0.2
5:30 AM	None	None	INV02	19
5:38 AM	1-	5.0	INV02	8.4
Morning	1-	5.0	INV01	3.9

It should be noted that the morning checks indicated the unfaulted array R_{iso} was low at 19 kΩ. As with previous testing on utility-scale arrays [9], the inverter was found to be a low-impedance pathway to ground, even when nominally disconnected from the ground bond. When the inverter is physically disconnected from the array, Array 01 registered a non-faulted isolation of 769 kΩ (2.6 GΩ/module) while Array 02 had a non-faulted isolation of 126 kΩ (0.5 GΩ/module). In these arrays, the low-impedance pathway to ground through the inverter accounts for 97.6% of Array 01 and 86.5% of Array 02 of the overall R_{iso} value. This poor isolation significantly affects the ground fault protection system.

The results of the experimental data from TABLE I compared to the predicated values from the SPICE simulations are shown in

The measured array R_{iso} does have a significant dependence on location of the fault in the array. The value of R_{iso} matched theory when the fault was on the CCC (1+). However, when the fault is at 1+, the measured value of R_{iso} increases by 300% and 215% for Array 01 and 02, respectively.
Fig. 2 for both Array 01 and 02. In general, the experimental results match very well with the predicted outcome of the

model. Interestingly, although the component of module isolation to R_{iso} differs widely (769 kΩ for 01 and 126 kΩ for 02), the low-impedance pathway to ground through the inverter dominates the entire array R_{iso} and the individual R_{iso} curves for each array are indistinguishable.

This low impedance pathway through the inverter decreases the detectability region when the inverter is connected to the array (and nominally ungrounded). However, it also decreases array-to-array variability and may make determining proper thresholds module insensitive (at least when the inverter is the significant low-impedance path to ground).

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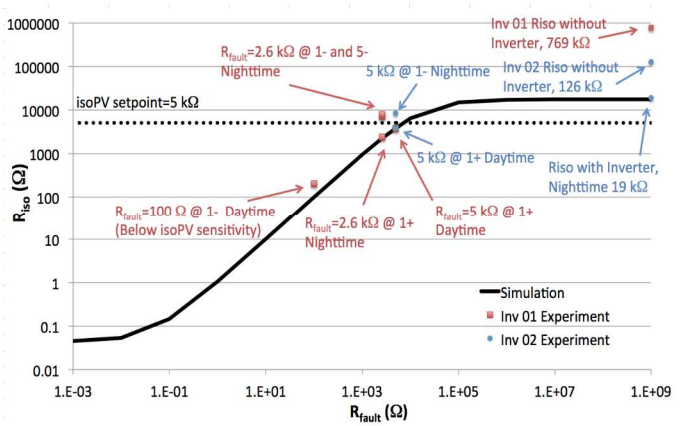

Fig. 2: Experimental data of measured R_{iso} for Array 01 (red) and 01 (blue) compared to simulations (black line). The threshold for this array is set at 5 kΩ and is denoted by the hashed line.

While the presence of the fault on the CCC is sufficient to decrease the measured array R_{iso} below the trip threshold (5 kΩ in this case, shown as a dashed line in Fig. 2), the larger measured R_{iso} for faults internal to the array are actually above the trip threshold and could subsist indefinitely in the array. Also, interestingly, there is no subsequent increase (just 7% for Array 01) when the fault is moved from 1- to 5-). This dependence of R_{iso} on array location during nighttime R_{iso} measurements is the result of the bypass diodes conducting the voltage pulse.

To measure R_{iso}, the isoPV unit injects a 50 V pulse into one of the CCCs. Fig. 3 shows the pulse injected into the positive CCC, although the measurement unit uses pulses applied to both the positive and negative CCCs for error correction (however the exact nature of the measurement is immaterial as the array is more or less symmetric and either of the CCCs can be used). If the R_{iso} measurement is taken at night, the photodiodes in the modules are not forward biased and cannot conduct the voltage pulse. Therefore, the pulse must travel through the bypass diodes in order to interrogate the fault.

When the fault is at 1+, both the positive and negative pulse polarities give the same value of around 2.27 kΩ (see TABLE II) since neither of the pulses have to traverse any bypass diodes. If, however, the fault is internal to the array, the bypass diodes block the positive polarity pulse and the measurement unit will not "see" the fault inside the array. Therefore, the positive pulse will measure R_{iso} to be approximately equal to the inverter isolation (around 18 kΩ) while the positive pulse will measure R_{iso} to the correct value. The isoPV unit then averages the R_{iso} results from the positive and negative pulses to get a final result for array R_{iso}.

When certain pulse polarities are blocked by the bypass diodes, the R_{iso} isolation measurement is (1) increased by several kΩ when the fault is not on the CCC. This accounts for similar R_{iso} increases when fault is moved from the CCC to 1- or 5-, as the difference between 1- and 5- is only from the small parasitic voltage drop across the bypass diodes.

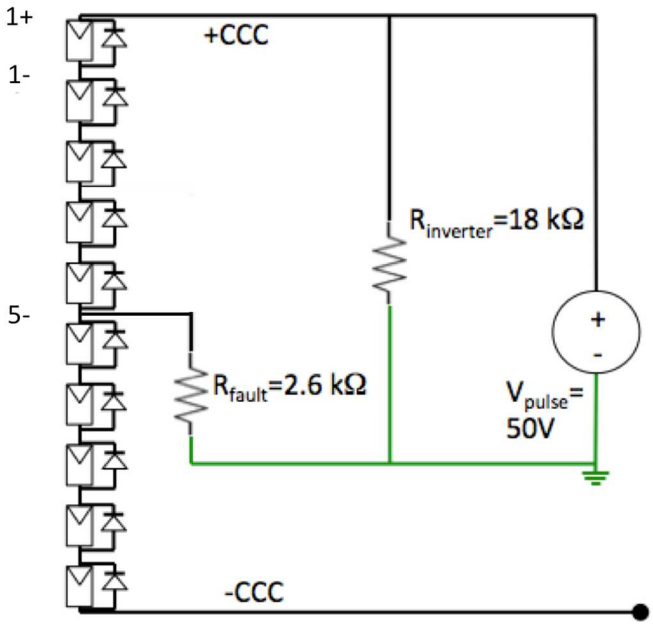

Fig. 3: Schematic of a R_{iso} measurement on the positive CCC.

TABLE II
THEORETICAL NIGHTTIME R_{ISO} RESULTS

	CCC	Pulse Polarity	+ CCC	1 mod. in	5 mod. in	- CCC
Simulation	+	-	2.26 kΩ	2.39 kΩ	2.39 kΩ	2.78 kΩ
	+	+	2.27 kΩ	17.5 kΩ	17.6 kΩ	17.9 kΩ
	Average		**2.27 kΩ**	**9.95 kΩ**	**10.0 kΩ**	**10.34 kΩ**
Experiment			2.4± 0.4 kΩ	7.2± 1.1 kΩ	7.7± 1.2 kΩ	

At night, the bypass diodes block half the polarity pulses from interrogating a fault internal to the array. The R_{iso} measurement unit then incorrectly measures the system isolation. The location dependence of the fault is from the

unit averaging the fault resistance (measured with the polarity that can pass the bypass diodes) with the inverter isolation.

III. TRIP THRESHOLD RECOMMENDATIONS

In order to determine the maximum allowable trip thresholds for an array, it is necessary to solve for the fault current and define an allowable fault current/power below which the array can still be considered to exist in a safe condition. In general, the fault current for an arbitrary location in an array is not analytically solvable. However, the worst-case scenario (fault at a current carrying conductor) has an analytical form since the inverter acts as a current divider circuit with resistance R_{mp}: part of the array supply current, I_{mp}, flows through the fault, with the rest flows through the inverter. The fault current can be described for both ungrounded and grounded arrays by Eqs. (3) and (4), respectively.

$$I_{fault} = \frac{V_{oc}}{2 \cdot \left(R_{iso} + R_{fault} \right)} \tag{3}$$

$$I_{fault} = I_{mp} \left[1 - \frac{R_{fault}}{R_{mp} + R_{fault}} \right] \leq \frac{V_{oc}}{R_{fault}} \tag{4}$$

It is apparent from the equations plotted in Fig. 4 that grounded arrays provide significantly more fault current than ungrounded arrays. This is due to the "clamping" effect of ungrounded systems where the available fault current is limited. That is, when a well behaved ($R_{iso} \rightarrow \infty$) ungrounded system develops a fault condition, the array becomes referenced to ground at the point of the fault and it, effectively, turns into a grounded system.

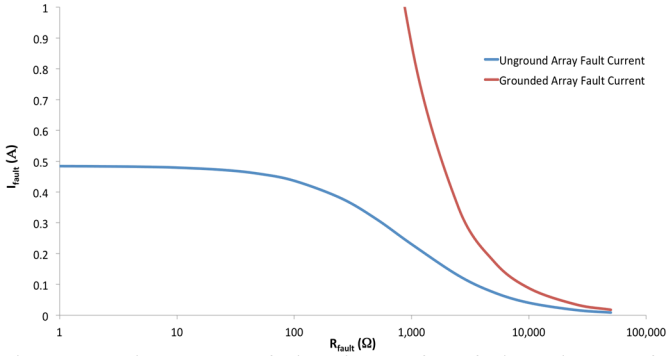

Fig. 4: Fault current vs. fault resistance for a fault on the CCC for an ungrounded (blue) and grounded (red) array of a 1000V, 1.5 MW array.

Since grounded systems provide much more available power to the fault, they are *significantly* more dangerous than ungrounded systems. As a matter of safety, the threshold for an array should be set for the worst-case fault: a grounded system faulted at the ungrounded CCC.

From IEC 60364-4-42 [16], the maximum power that can be dissipated safely through an enduring fault without risk of a fire is 70 W. For a 1000 V system, this would correspond to a fault current of 70 mA. For a grounded array, this would be caused by an R_{fault} value of 14.3 kΩ based on (4). A system designer, with knowledge of the specific array configuration (S, M), module leakage (R_{module}), and inverter isolation (R_{inv}) could then use (2) to find the proper R_{iso} threshold for the array in question (R_{EGC} is assumed to be zero for thresholding purposes). For the arrays presented in this work, Array 01 would require a threshold of 7.89 kΩ and Array 02 would require a threshold of 7.48 kΩ.

Unfortunately, for standards purposes and other bodies such as inverter manufacturers without detailed knowledge of specific array configuration, it is not ideal to describe necessary trip thresholds based on array configuration (S, M). It is possible to remove the array configuration aspects from (2) and completely describe R_{iso} with array electrical information and allowable fault power.

The number of modules in an array (S•M) is a function of the power of the array (P_{inv}), power of a module (P_{mod}), and DC-to-AC ratio (P_{DC}/P_{AC}) as seen in (5).

$$S \cdot M = \frac{P_{inv}}{P_{\text{mod}}} \cdot \left(\frac{P_{DC}}{P_{AC}} \right) \tag{5}$$

There also exists an implicit assumption in R_{module} on the number of modules (more specifically, in the area of modules present, as module isolation is limited by IEC 61215 [17] to no less than 40 MΩ•m^2). The module area (A) is a function of module power (P_{mod}) and module efficiency (η) as shown in (6).

$$A = \frac{P_{\text{mod}}}{1000 \cdot \eta} \tag{6}$$

By inserting (5) and (6) into (2), the value of R_{iso} can be described only in terms of the electrical state of an array (7).

$$R_{iso} = \frac{1}{\dfrac{P_{inv} \cdot \left(\dfrac{P_{DC}}{P_{AC}} \right)}{R_{\text{module}} \cdot 1000 \cdot \eta} + \dfrac{1}{R_{inv}} + \dfrac{P_{fault}}{V_{oc}^2}} \tag{7}$$

This equation can be used to determine an array threshold. Let us assume that a standards-making body wants to set a R_{iso} threshold to limit fault power (P_{fault}) to 70 W. A conservative estimation of R_{iso} threshold would be assume a worst-case situation for the array in which large area, leaky modules (40 MΩ, 5% efficiency) with a low inverter impedance to ground (15 kΩ) are installed on an 500 kW, 1000 V system. In this

case (shown as the blue curve in Fig. 5) the unfaulted array would have a R_{iso} value of 2.58 kΩ with a trip threshold calculated using (7) to be 2.2 kΩ.

If, however, a system designer installs significantly better modules (20% efficient, red curve in Fig. 5), the unfaulted R_{iso} would increase to 5.95 kΩ. This increase would increase the detectability for faults; however, the trip setting calculated for the less efficient modules (2.2 kΩ) would yield a fault power of 285 W, resulting in a hazardous condition where a fault dissipating over 70 W could exist in the system without detection. Therefore, assuming very poor quality modules as a worst-case condition actually decreases system safety.

Conversely, if it is assumed that high-isolation modules are installed ($R_{module} \rightarrow \infty$) then the array isolation is only a function of fault impedance (purple line in Fig. 5). In this case, the threshold would be set at 14 kΩ. If a system designer installs more leaky modules (red line in Fig. 5), then there will be nuisance tripping issues as even the R_{iso} of the healthy array case (5.95 kΩ) is below the determined trip threshold.

In general, without some knowledge of the array configuration or module quality, it is impossible to determine a trip threshold that provides safety and prevents unwanted tripping issues. Appropriate R_{iso} trip thresholds *must* be determined on an array-by-array basis with sufficient leeway by system operators to adjust trip threshold settings for their particular usage cases.

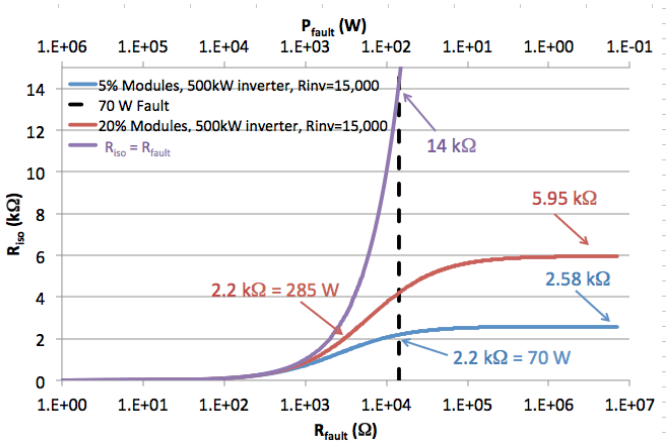

Fig. 5: Riso vs. Rfault for different module technologies based on (7) ranging from very leaky modules (blue line) to slight better modules (red line) to non-leaky modules (purple line). In general, with regard to a priori calculation of Riso trip settings, changes in module efficiencies and isolations result in either safety or unwanted tripping issues.

CONCLUSIONS

Faults were installed on two 1000 V, 1.5 MW, positively grounded PV arrays. SPICE simulations were found to match well with the field R_{iso} measurements. Slight deviations from theory were found for nighttime measurements in the interior of the array due to voltage pulses travelling through bypass diodes as opposed to the module photodiodes.

I_{fault} and R_{iso} theoretical equations were derived for grounded and ungrounded arrays, which can be used to determine appropriate trip thresholds based on allowed fault power. Equations were also developed to allow the calculation of trip threshold without knowledge of the specific array topology. However, in this case, selection of the default R_{iso} value for leaky modules (low R_{module}/η) leads to potential safety issues if well-isolated modules are installed; while using well-isolated modules to select the default R_{iso} trip threshold leads to possible unwanted tripping issues in systems with leaky modules. Said another way, a default R_{iso} value cannot be determined for a given PV inverter because leaky systems will have unwanted tripping and highly-isolated systems will not trip before a fire hazard.

Therefore, it is apparent that any *a priori* calculation of trip threshold cannot mitigate both fire risk and unwanted tripping issues for all possible arrays. Some system knowledge is necessary for the determination of trip points. In general, there is no *one-size-fits-all* solution and standards bodies may have to determine a *range of values* that can be set by array operators based on specific details of the array. In general, correct thresholds should be determined on a case-by-case basis, most likely as part of array commissioning.

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