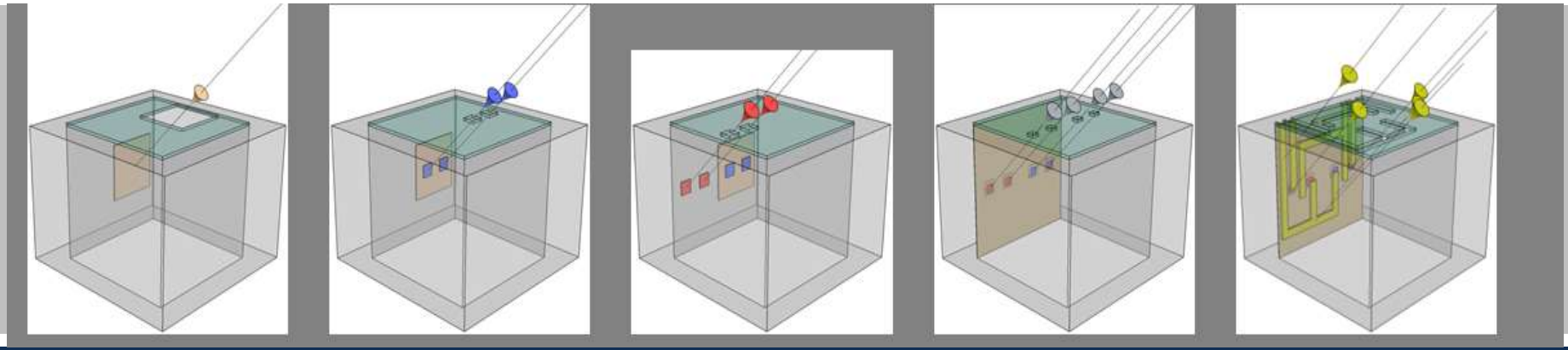
Exceptional service in the national interest

SAND2015-4648C



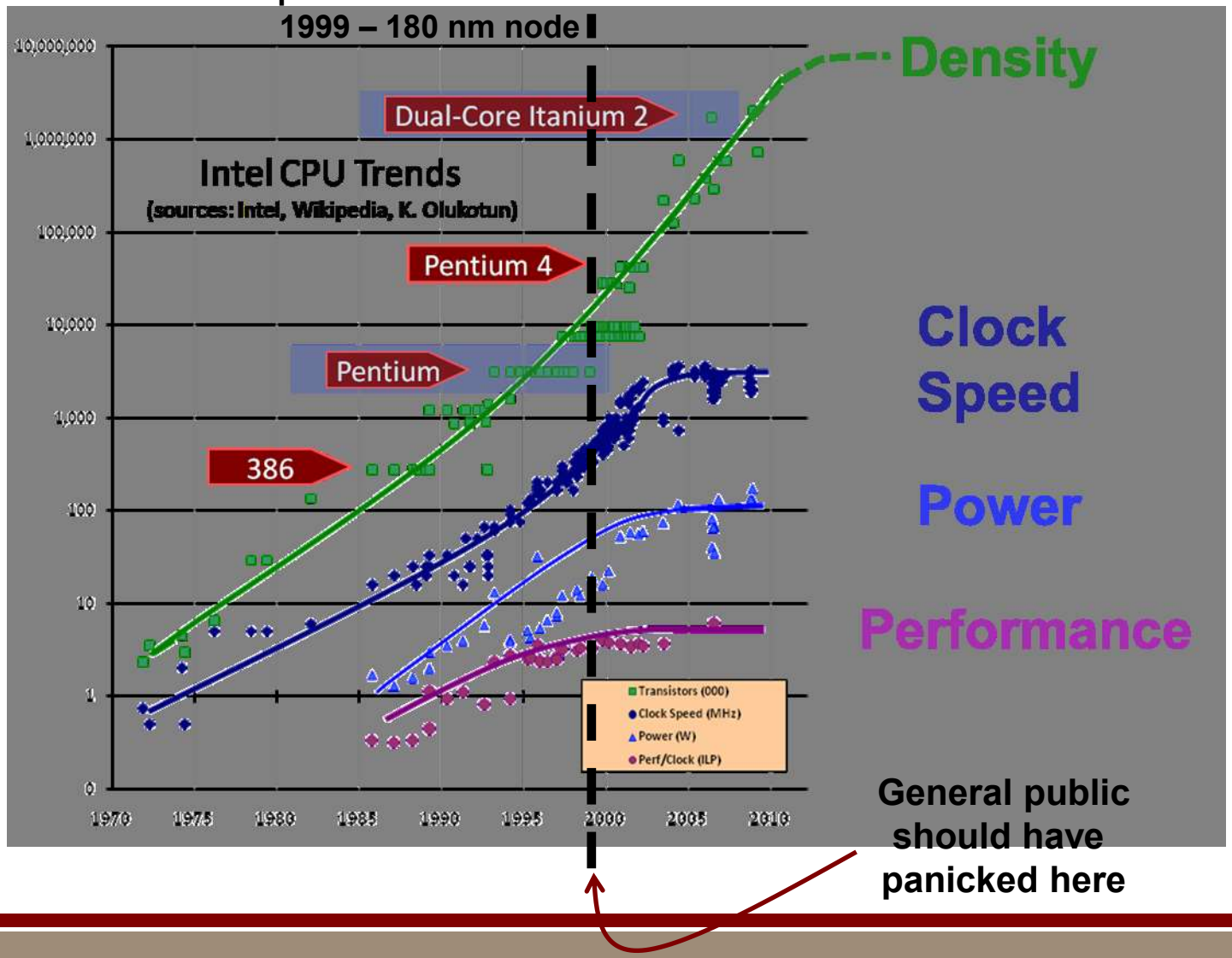
Device Level 3-D Integrated Circuits

D. Bruce Burckel, Paul J. Resnick, Bruce L. Draper, Patrick S. Finnegan, and Paul Davids

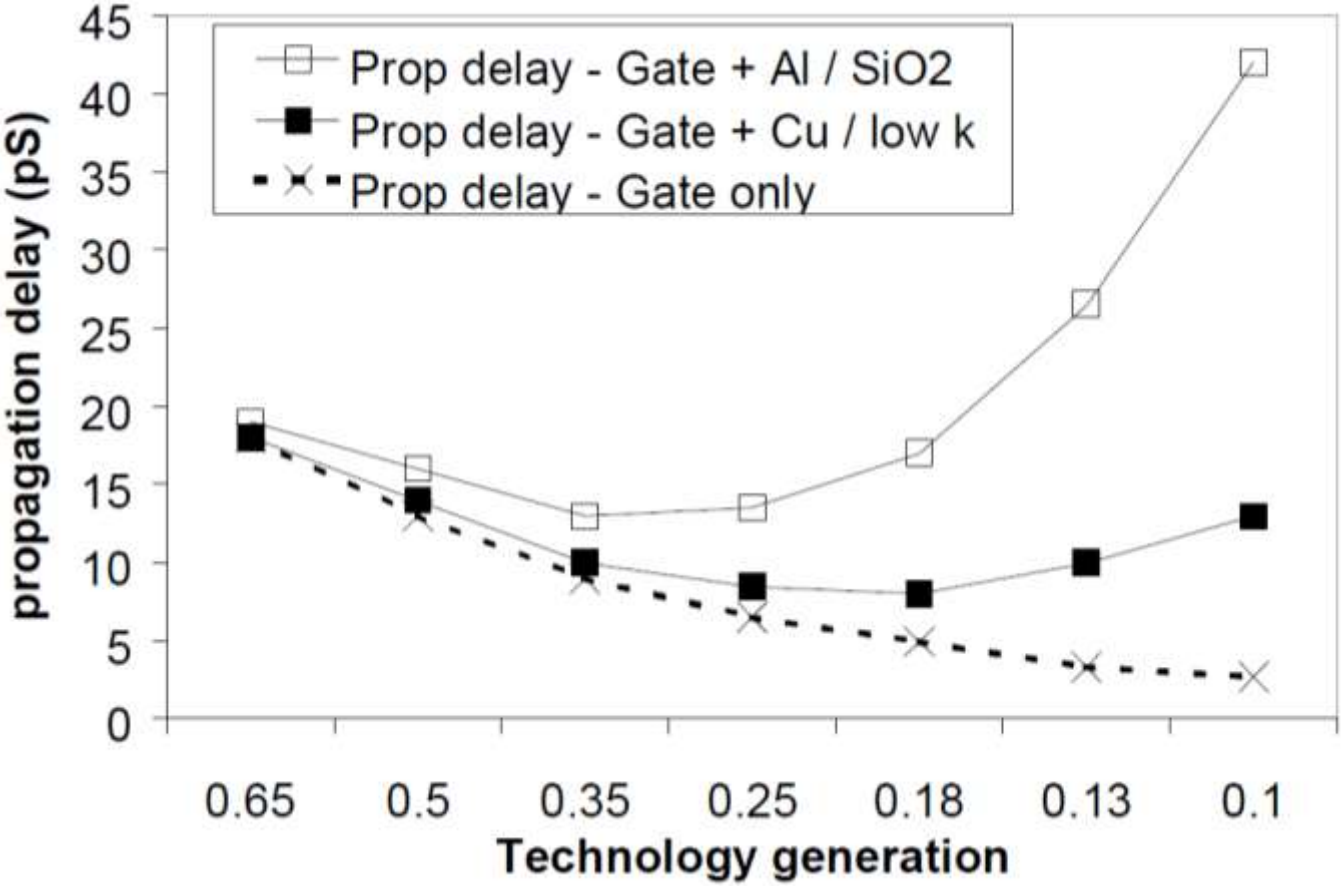
dbburck@sandia.gov

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND NO. 2011-XXXXP

Moore's Law in Several Variables



IC Performance Dominated by Interconnect Issues

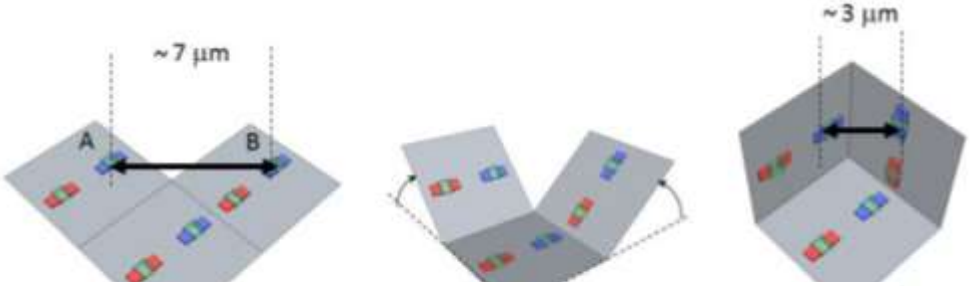


Key Technology Innovations and Drivers

Technology	Node	Driver	Type of Change
AlSi alloy	1.0μm	Contact reliability (leakage/spiking)	Material
AlSiCu alloy	0.8μm	Line reliability (EM)	Material
TiN /TiW barrier	0.5μm	Contact reliability (Rc; spiking)	Material
W-plug	0.5μm	Scaling – straight sidewalls in contacts & vias (step coverage)	Material
TiN-AlCu-TiN Metal lines	0.5μm	Reliability – hillocks Top ARC provision	Material
Contact silicide	0.35μm	Scaling – junction depth	Material
CMP	0.35μm	MLM lithography Global dielectric planarisation	Process
Cu metallisation	0.18μm	R-C propagation delay	Material
Dual damascene	0.18μm	Lithography – global planarisation Cu RIE process	Process
Zero overlay line-via	0.18μm	scaling	Process
Low k dielectric	0.13μm	R-C propagation delay	Material

Keith Buchanan, "The evolution of interconnect technology for silicon integrated circuitry," GaAs MANTECH Conference, (2002)

3D-ICs Reduce Interconnect Length



Reduction in *L* by a factor of ~ 2.3

Rent's rule and wire length estimation

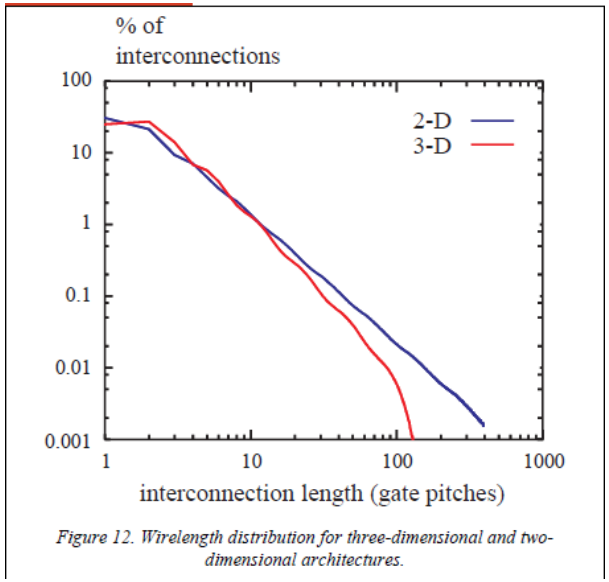
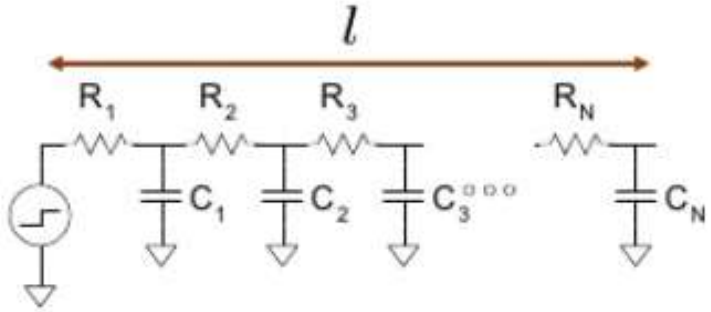


Figure 12. Wirelength distribution for three-dimensional and two-dimensional architectures.

D. Stroobandt, "Recent advances in system-level interconnect prediction," *IEEE Circuits and Systems*, **11**, pp3-20, (2000).

Treating Interconnects as distributed circuit elements :

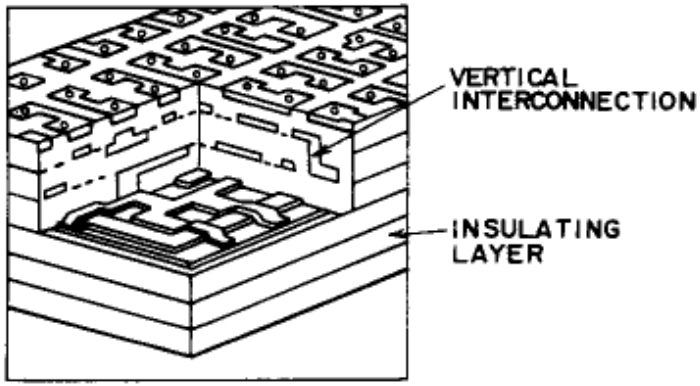


R_i = resistance per unit length
C_i = capacitance per unit length

$$\text{RC delay} \propto L^2$$

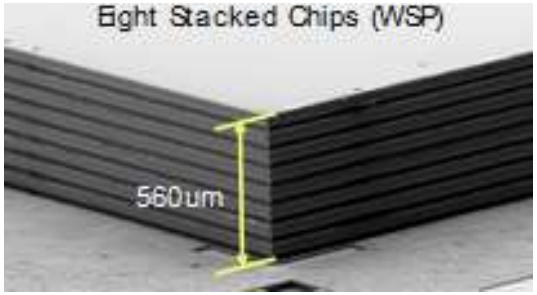
$$\text{Joule Heating} \propto L$$

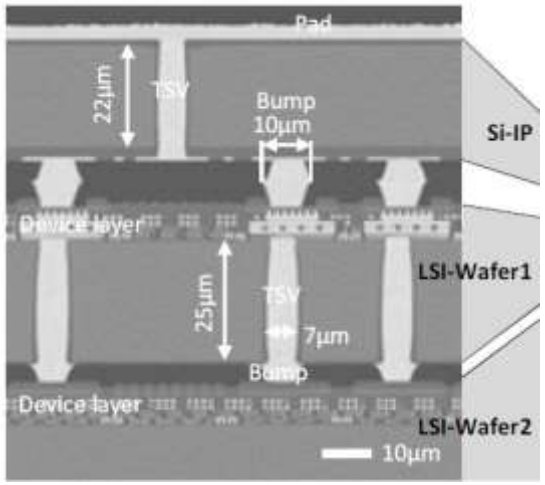
Predominately 3DIC = TSVs



Y. Akasaka, "Three-Dimensional IC Trends," Proc. IEEE, 74, pp1703-1714, (1986)

DARPA MTO
3D-ICs Portfolio

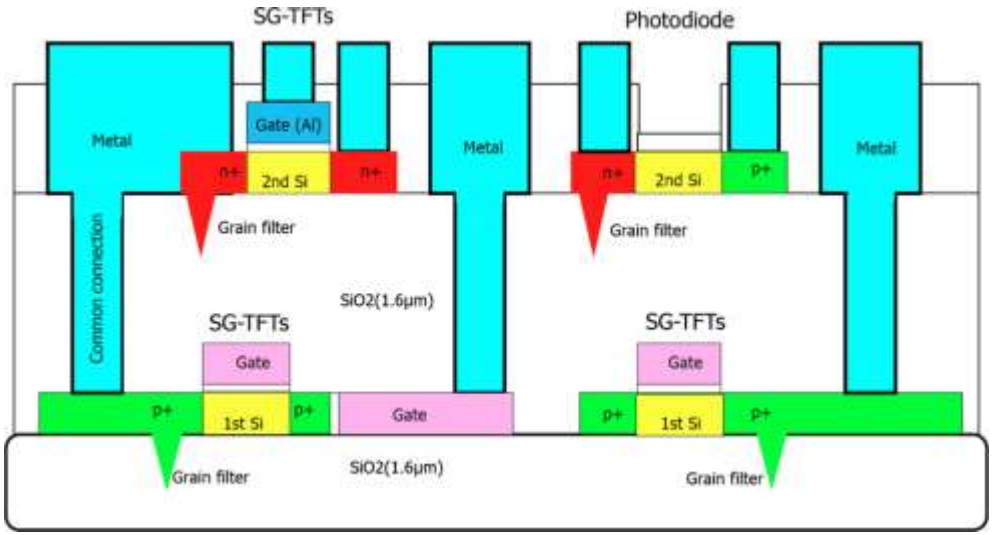


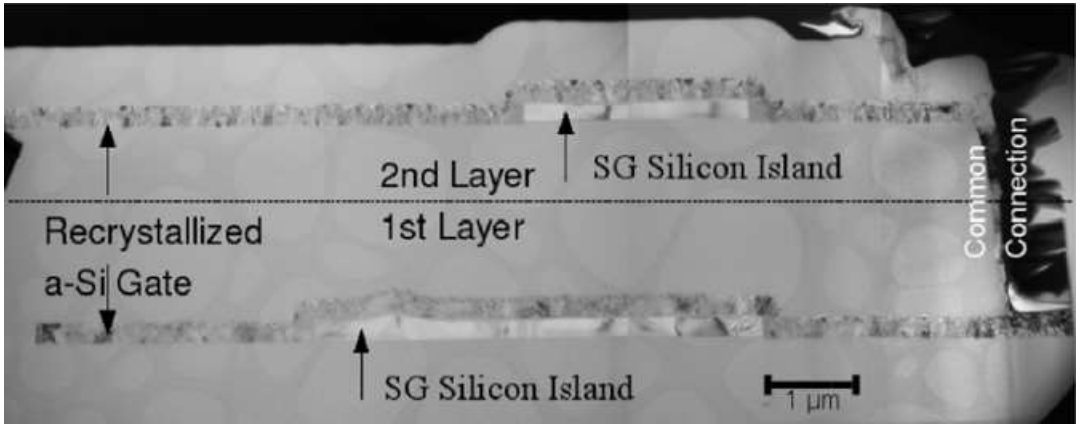


Solid State Technology

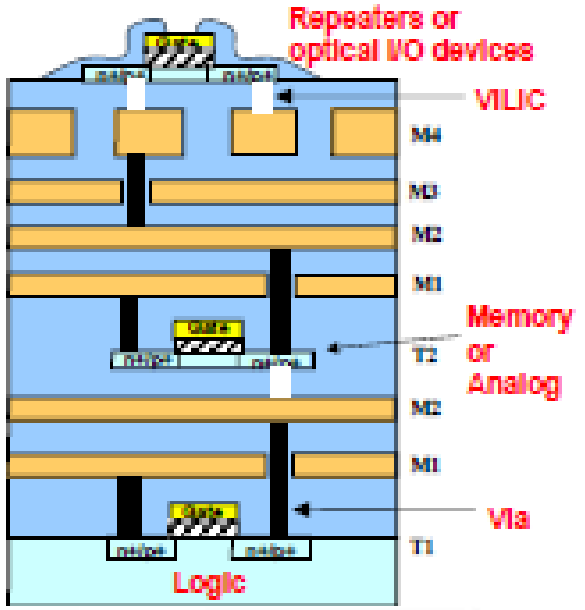
IFTLE 176 2013 IEDM; Micron, TSMC, Tohoku Univ., NC State, ASET

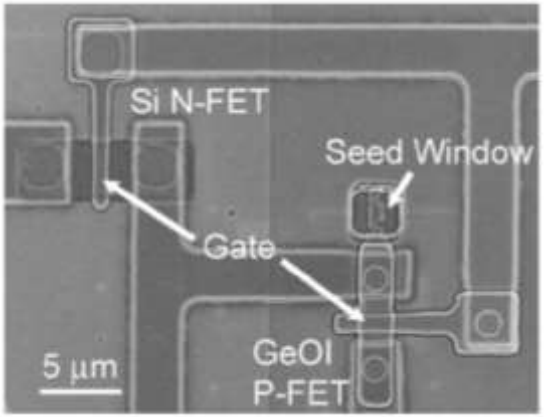
Some Work On Monolithic 3D-ICs





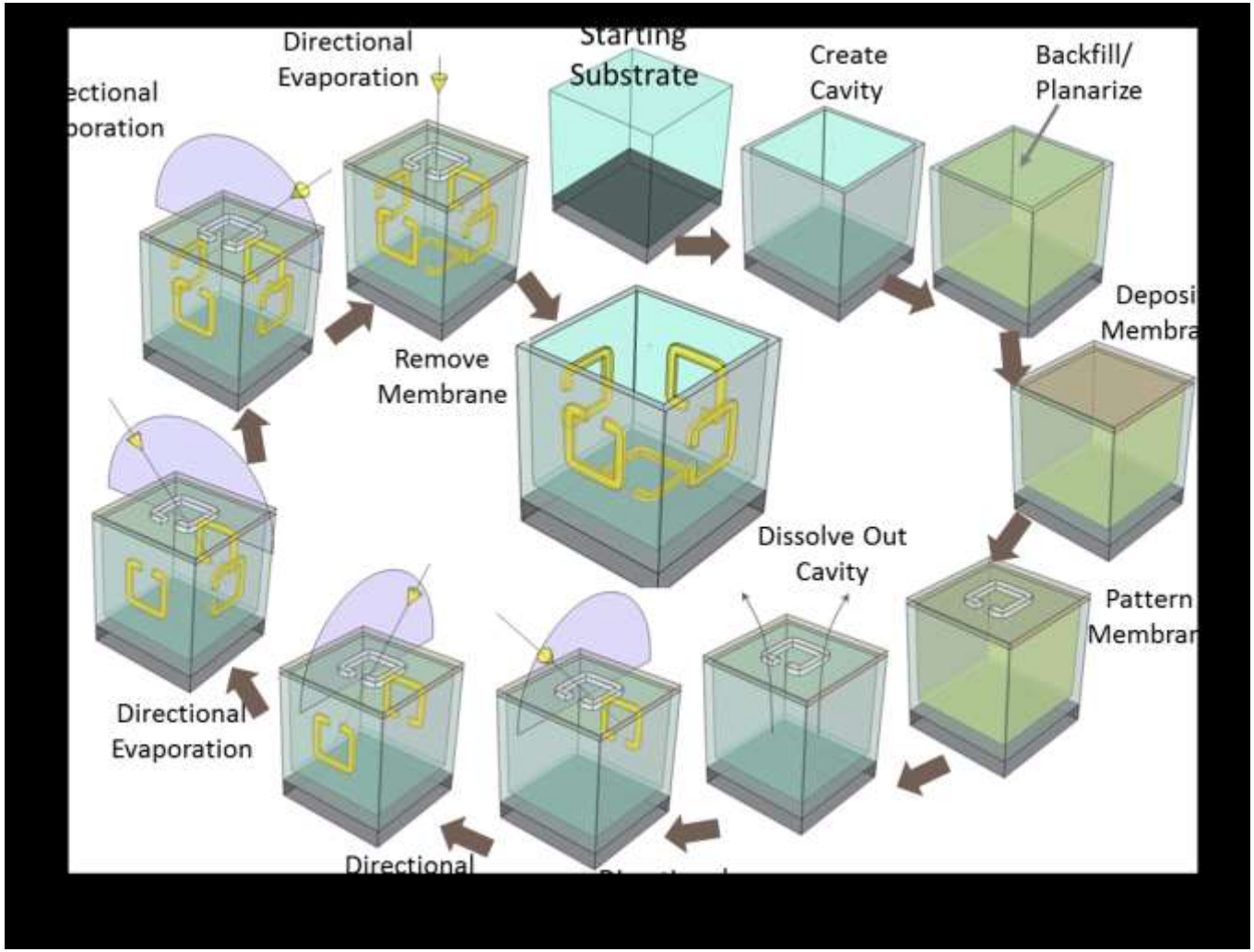
Ishihara et. al., "Monolithic 3D-ICs with single grain Si thin film transistors," Solid State Electronics, 71, pp. 80-87, (2012).



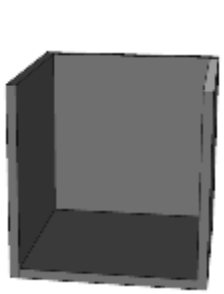


Wong et. al., "Monolithic 3D Integrated Circuits," IEEE VLSI TSA, 1-4244-0585-8/07, (2012).

Micron-scale 3D Fabrication: Membrane Projection Lithography

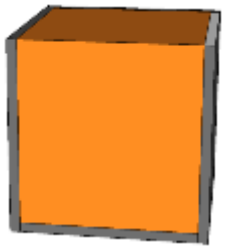


Polymer Based MPL Process Flow



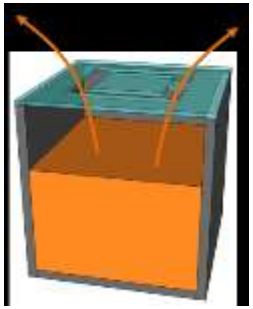
Create Cavity

Sacrificial Backfill

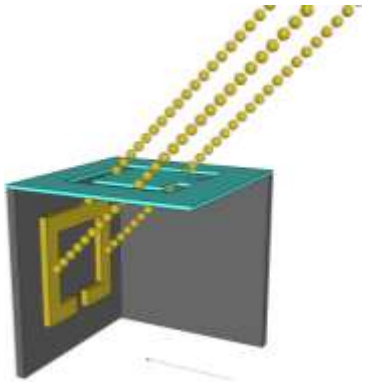


Planarize Backfill

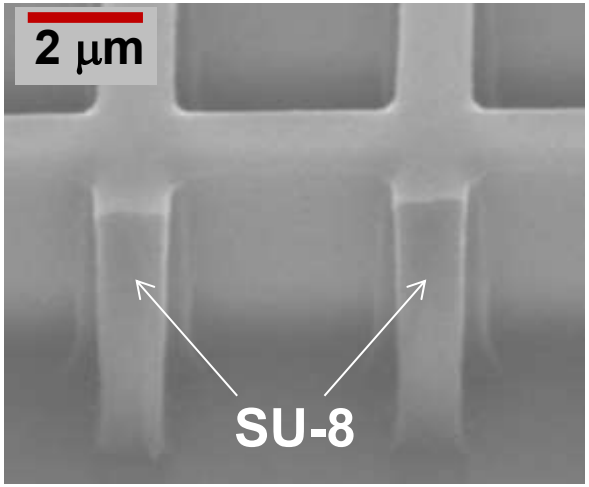
Deposit/Pattern Membrane



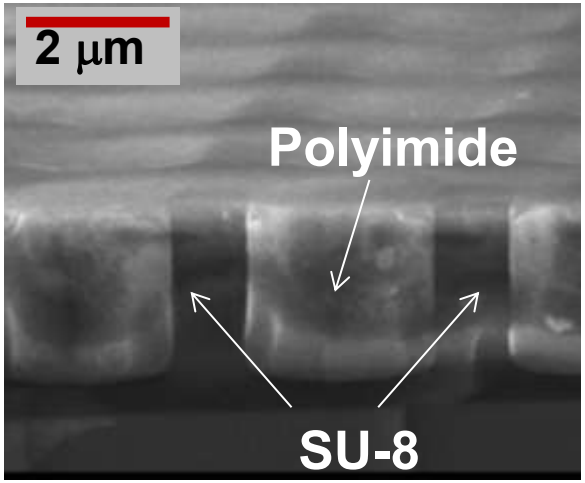
Dissolve Out Backfill



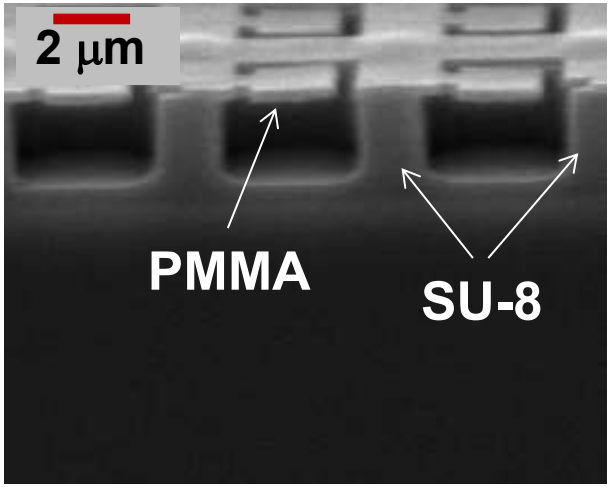
Directional Processing



Create Cavity

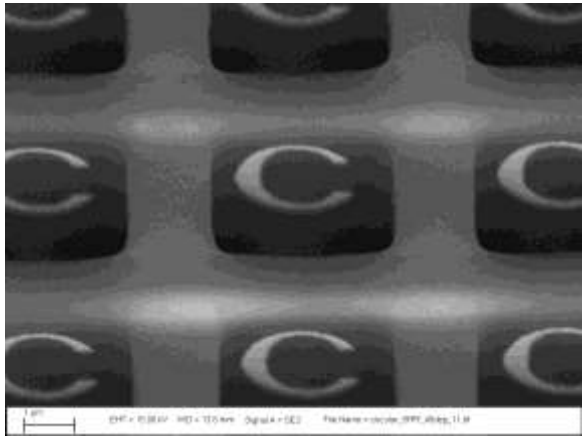


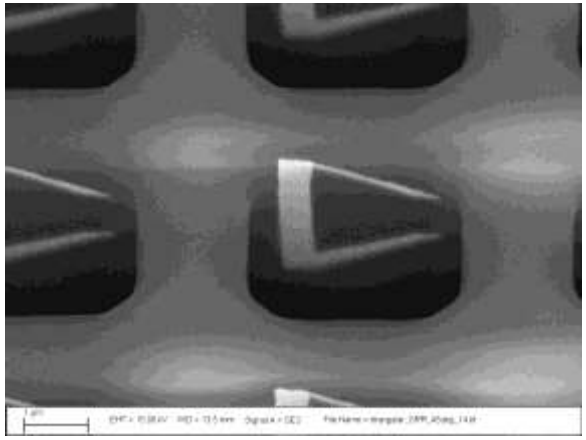
Planarize Backfill

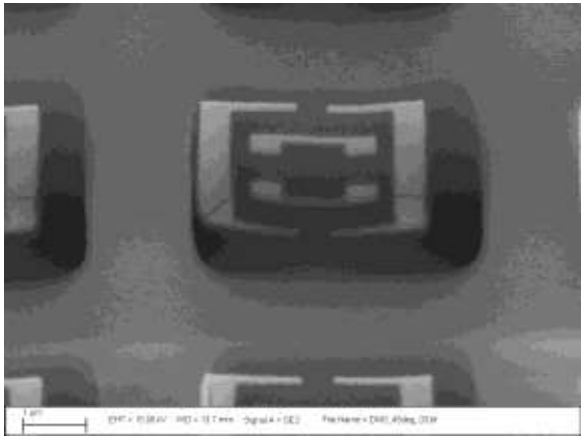


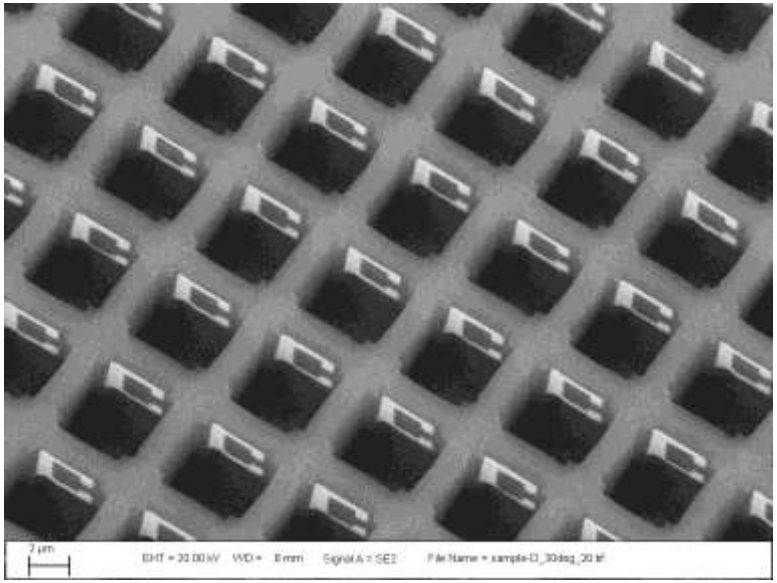
Dissolve Out Backfill

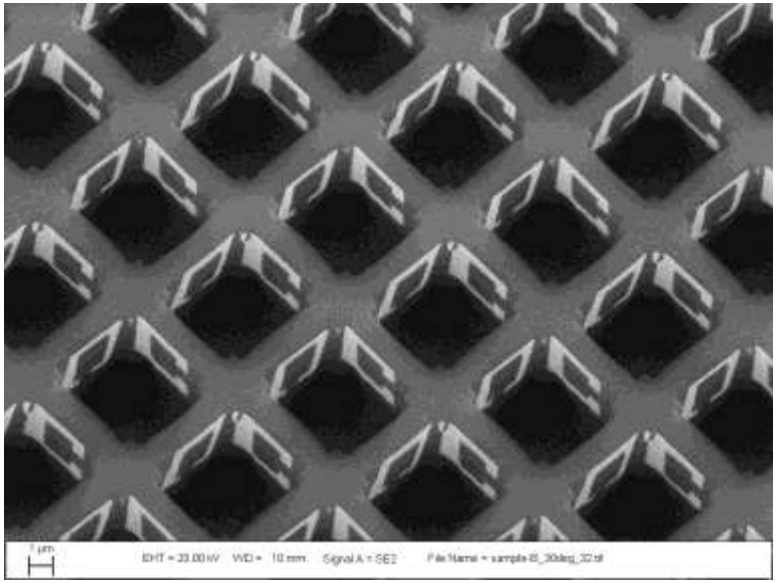
Polymer-Based MPL Structures







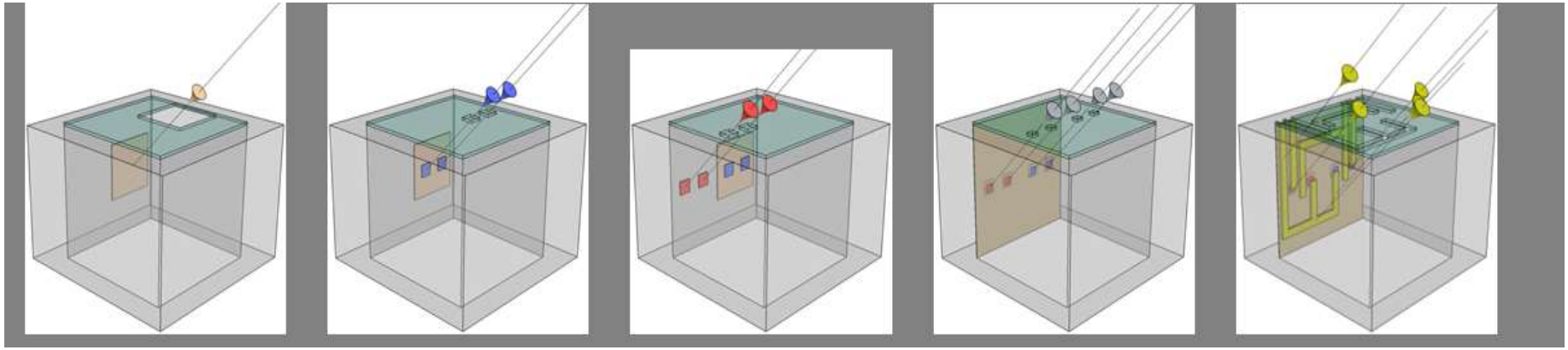




Can MPL Process Be Generalized?

Question: Can we generalize MPL to include ion implantation and dry etching, as well as deposition in a CMOS compatible material system?

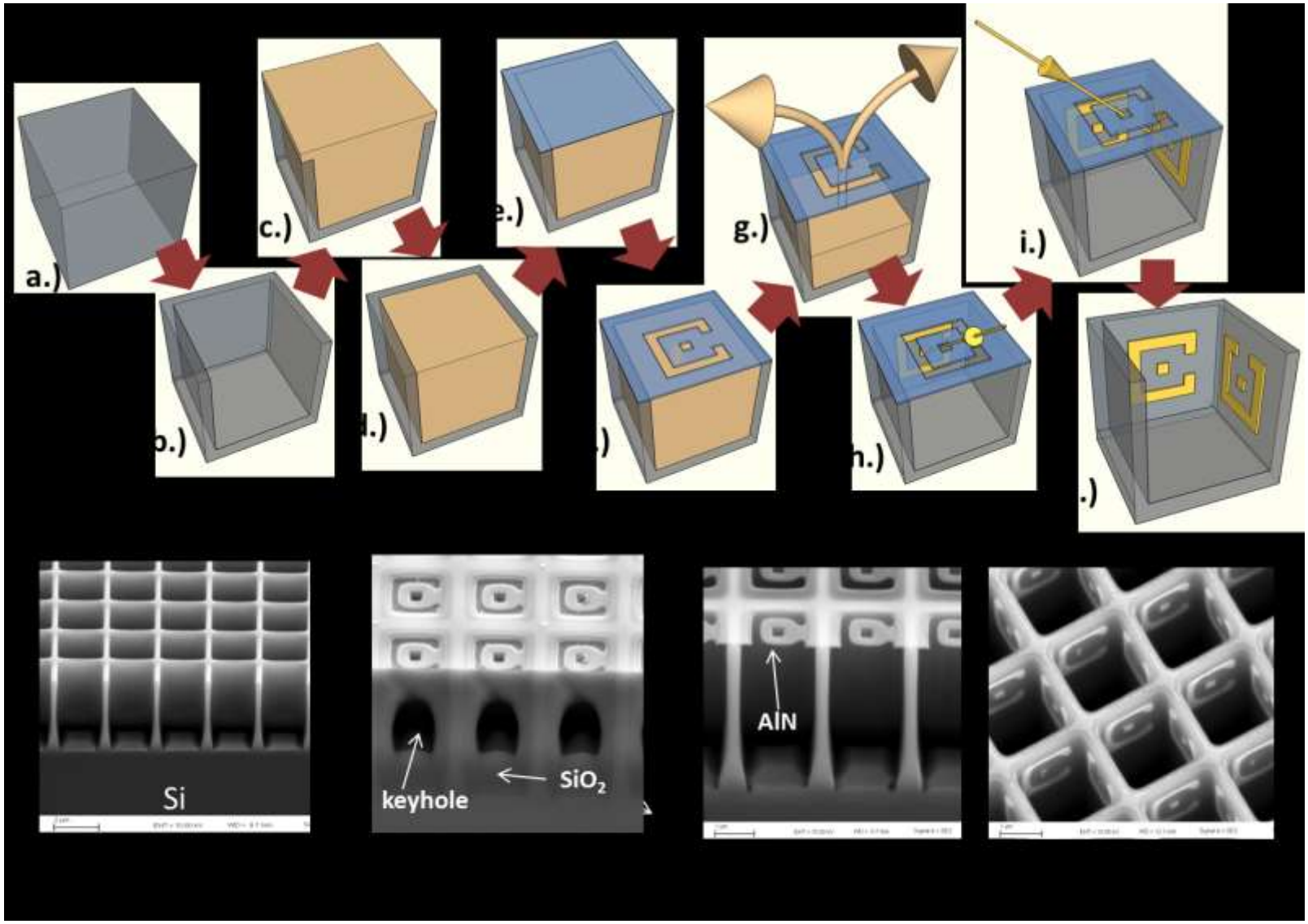
Long Channel Metal Gate CMOS



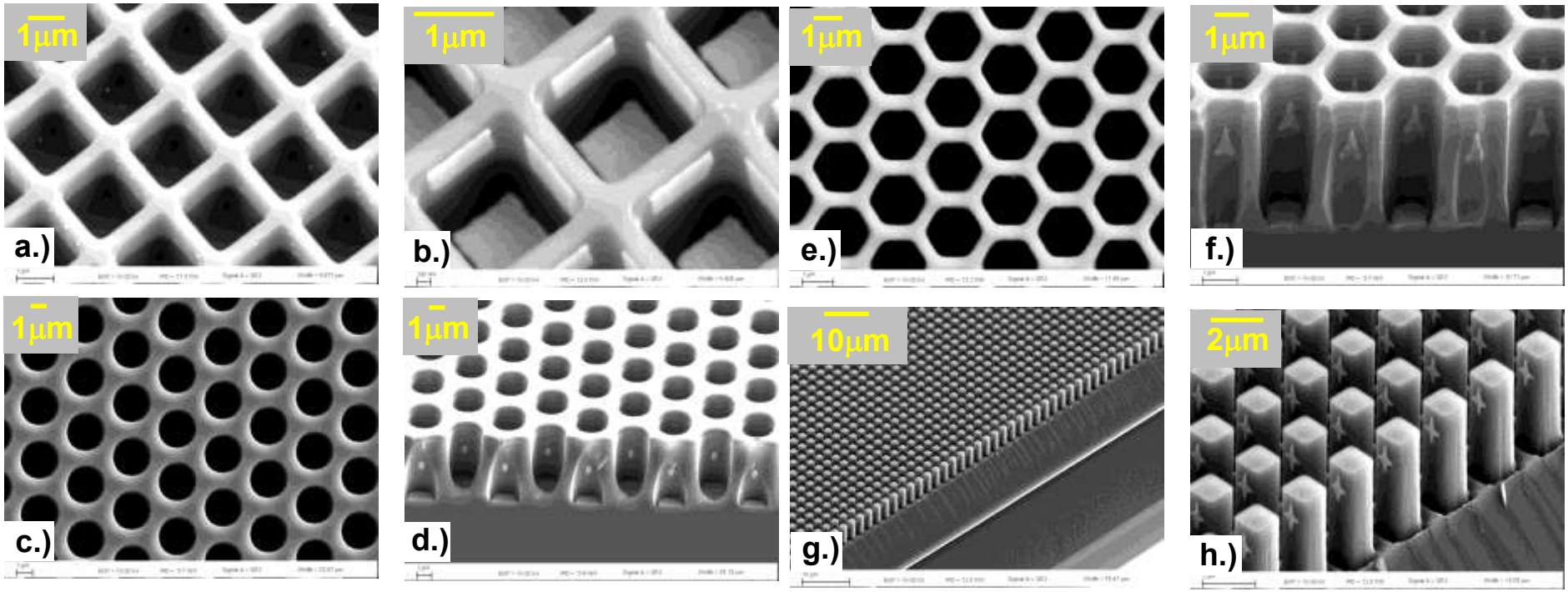
Well Implant	PMOS Source/Drain Implant	NMOS Source/Drain Implant	Contact Cuts	Metal 1 Deposition

Deposition:
CMOS Compatible Material Set

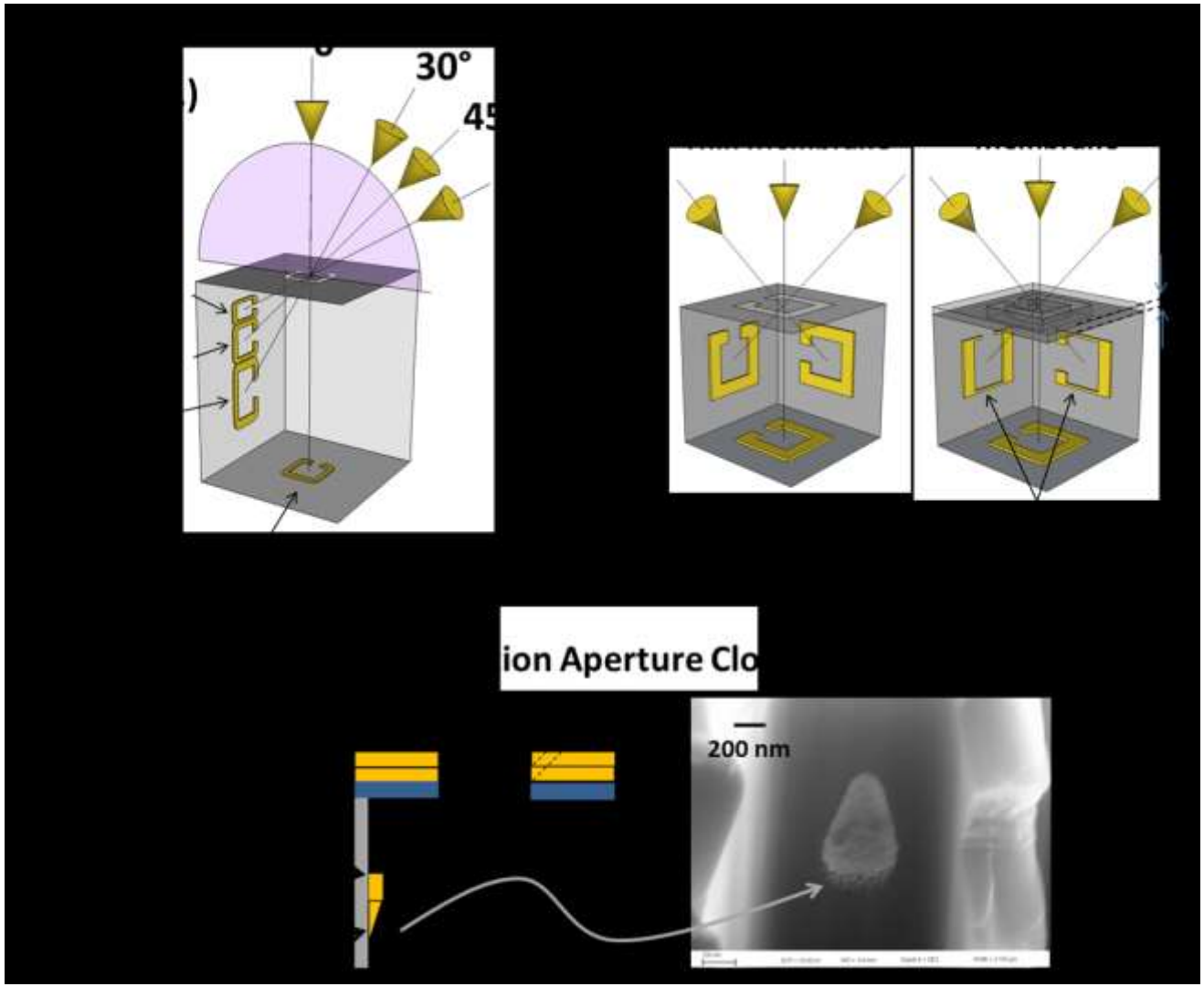
CMOS Compatible MPL - Deposition



Examples of CMOS-Compatible MPL: Deposition



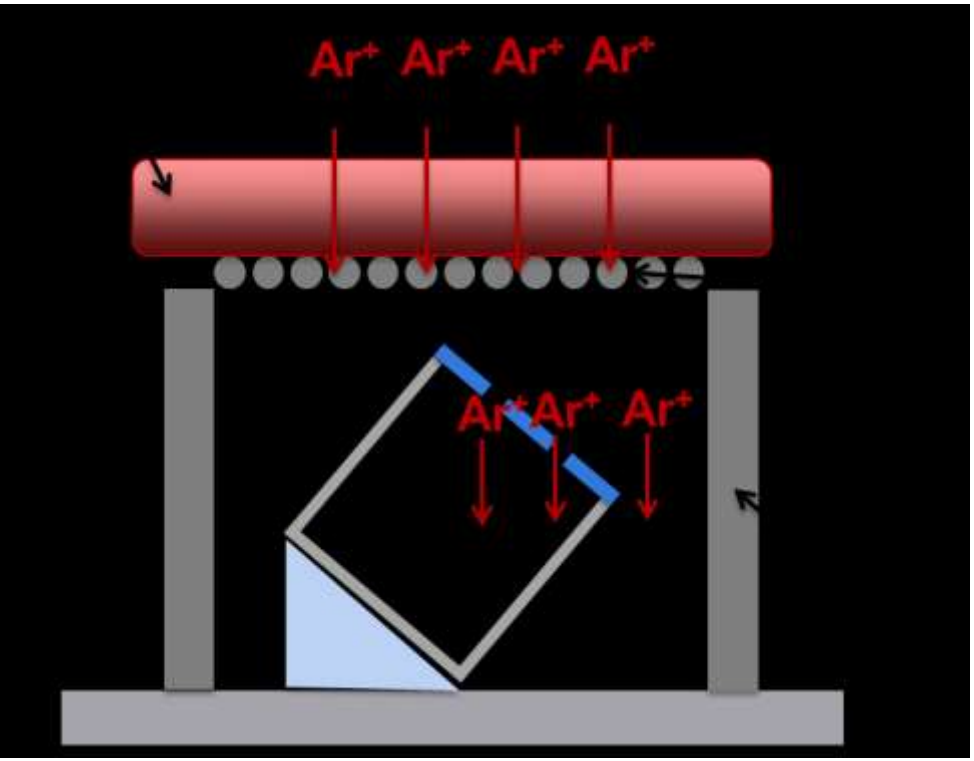
Sources of MPL Distortion



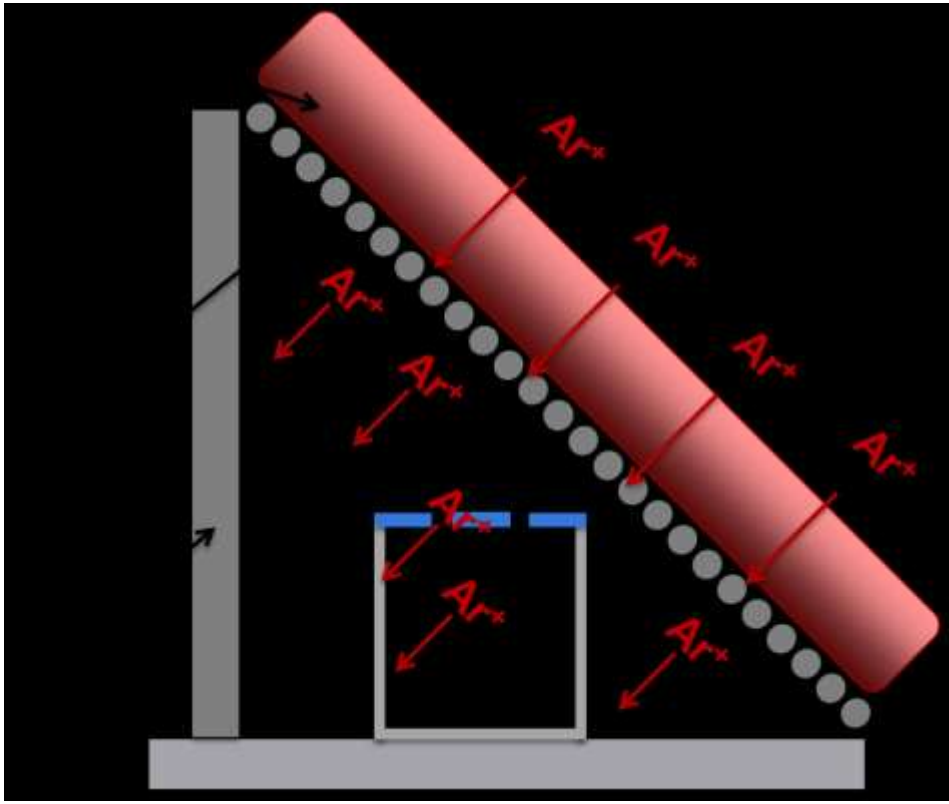
Directional Etching
Secret ingredient: Faraday Cage

Use Faraday Cage to Reorient The Plasma Sheath

Planar Faraday Cage



Tilted Faraday Cage

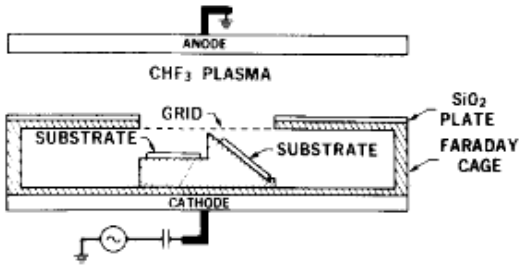


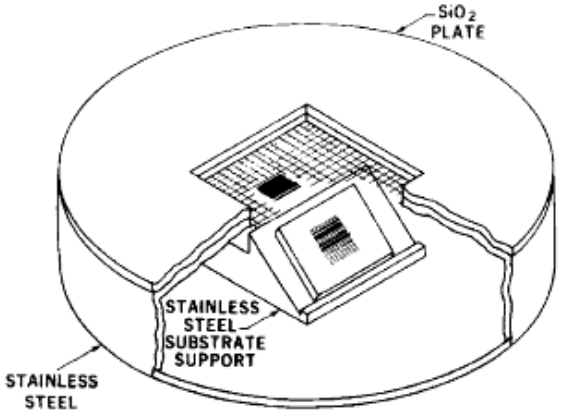
Oblique Directional Etching in the Literature

Directional reactive ion etching at oblique angles

G. D. Boyd, L. A. Coldren, and F. G. Storz
Bell Laboratories, Holmdel, New Jersey 07733

(Received 13 December 1979; accepted for publication 24 January 1980)

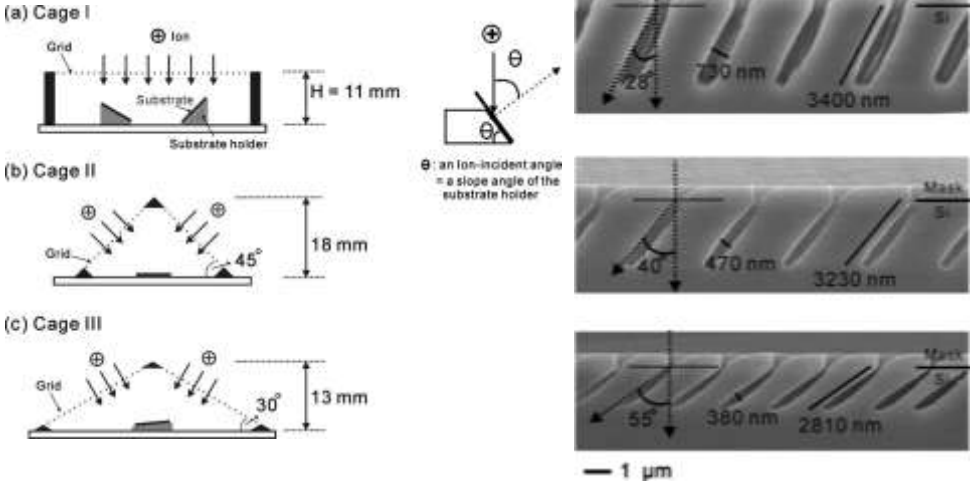


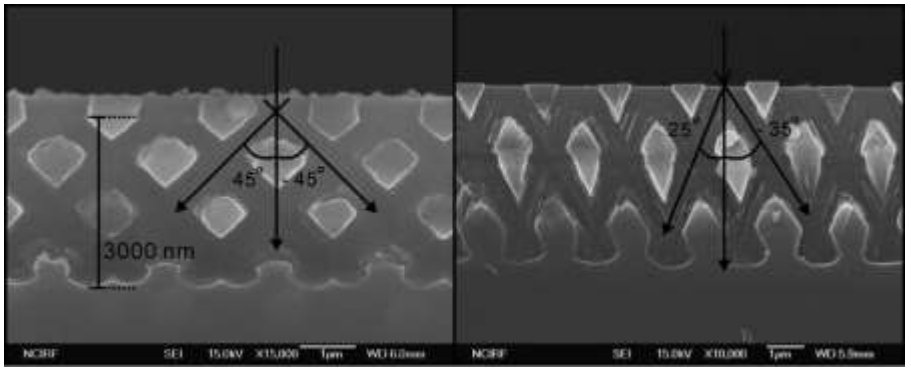


D222 *Journal of The Electrochemical Society*, **156** (7) D222-D225 (2009)
0013-4651/2009/156(7)/D222/4/$25.00 © The Electrochemical Society

Oblique-Directional Plasma Etching of Si Using a Faraday Cage

Jin-Kwan Lee,[a] Seung-Haeng Lee,[a] Jae-Ho Min,[a] Il-Yong Jang,[a] Chang-Koo Kim,[b,*] and Sang Heup Moon[a,z]



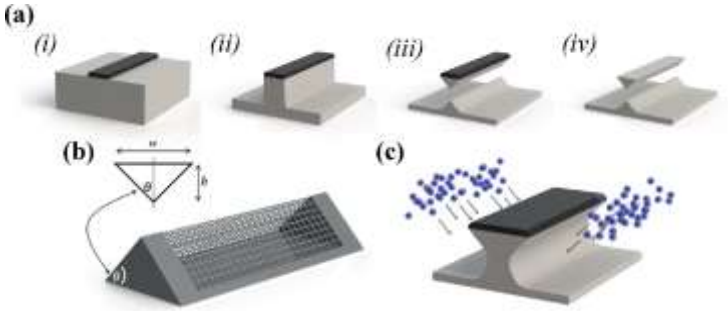


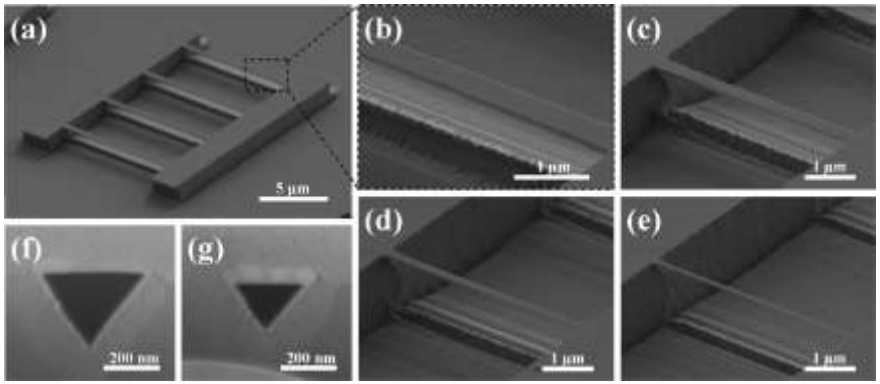
Oblique Directional Etching in the Literature

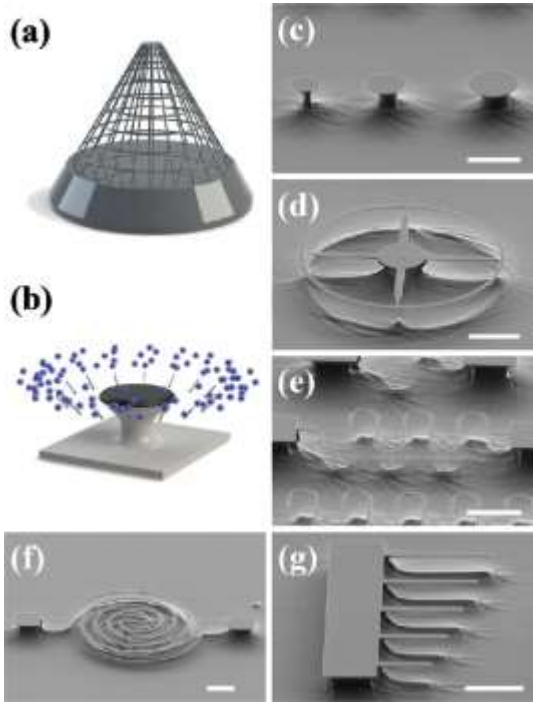
NANO LETTERS
Letter
pubs.acs.org/NanoLett

Free-Standing Mechanical and Photonic Nanostructures in Single-Crystal Diamond

Michael J. Burek,[†] Nathalie P. de Leon,[‡,§] Brendan J. Shields,[‡] Birgit J. M. Hausmann,[†] Yiwen Chu,[‡] Qimin Quan,[†] Alexander S. Zibrov,[‡] Hongkun Park,[†,§] Mikhail D. Lukin,[‡] and Marko Lončar*,[†]







Monolithic Faraday Cage

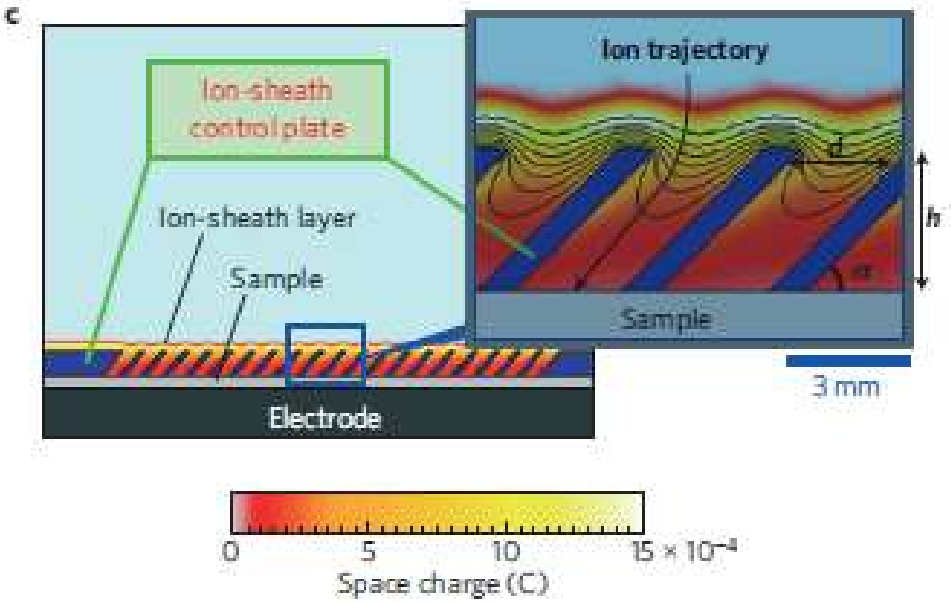
nature materials

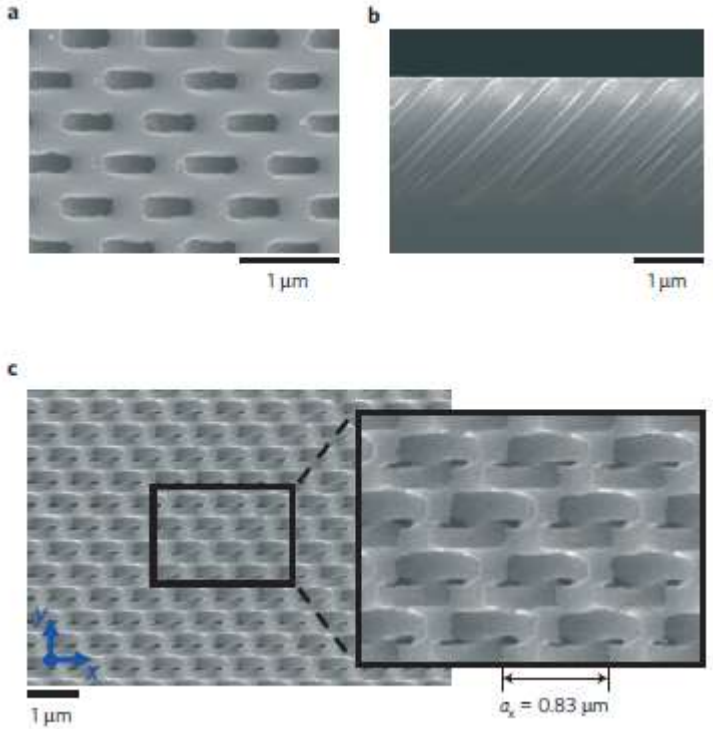
LETTERS

PUBLISHED ONLINE: 9 AUGUST 2009 | DOI: 10.1038/NMAT2507

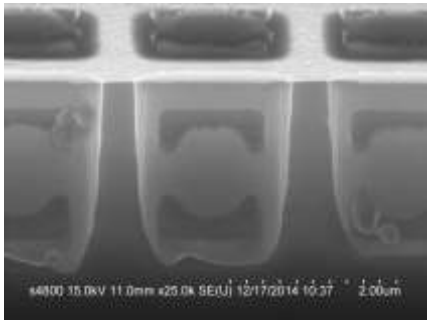
Direct creation of three-dimensional photonic crystals by a top-down approach

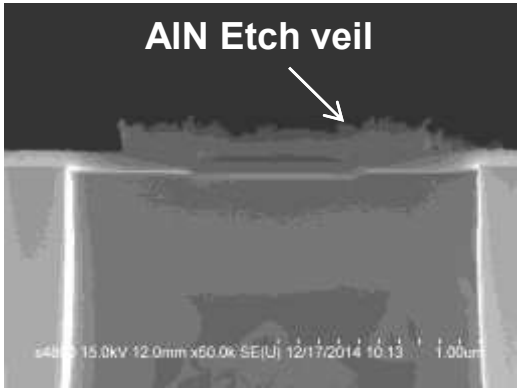
Shigeki Takahashi*, Katsuyoshi Suzuki*, Makoto Okano, Masahiro Imada, Takeshi Nakamori, Yuji Ota, Kenji Ishizaki and Susumu Noda†

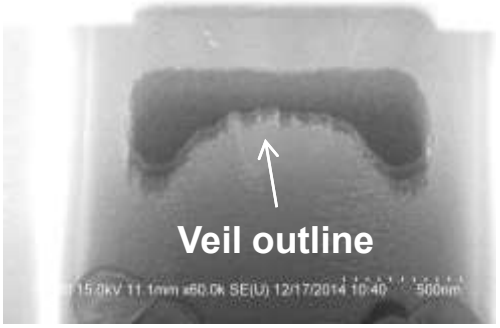


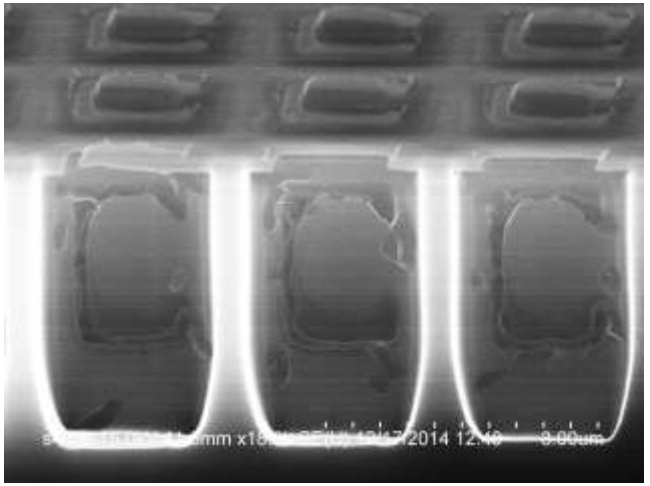


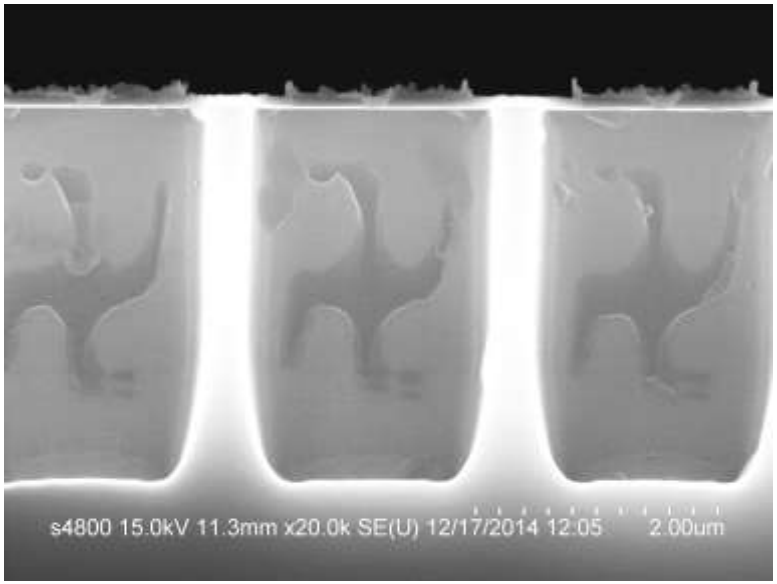
Example SEMs of vertical patterned etches



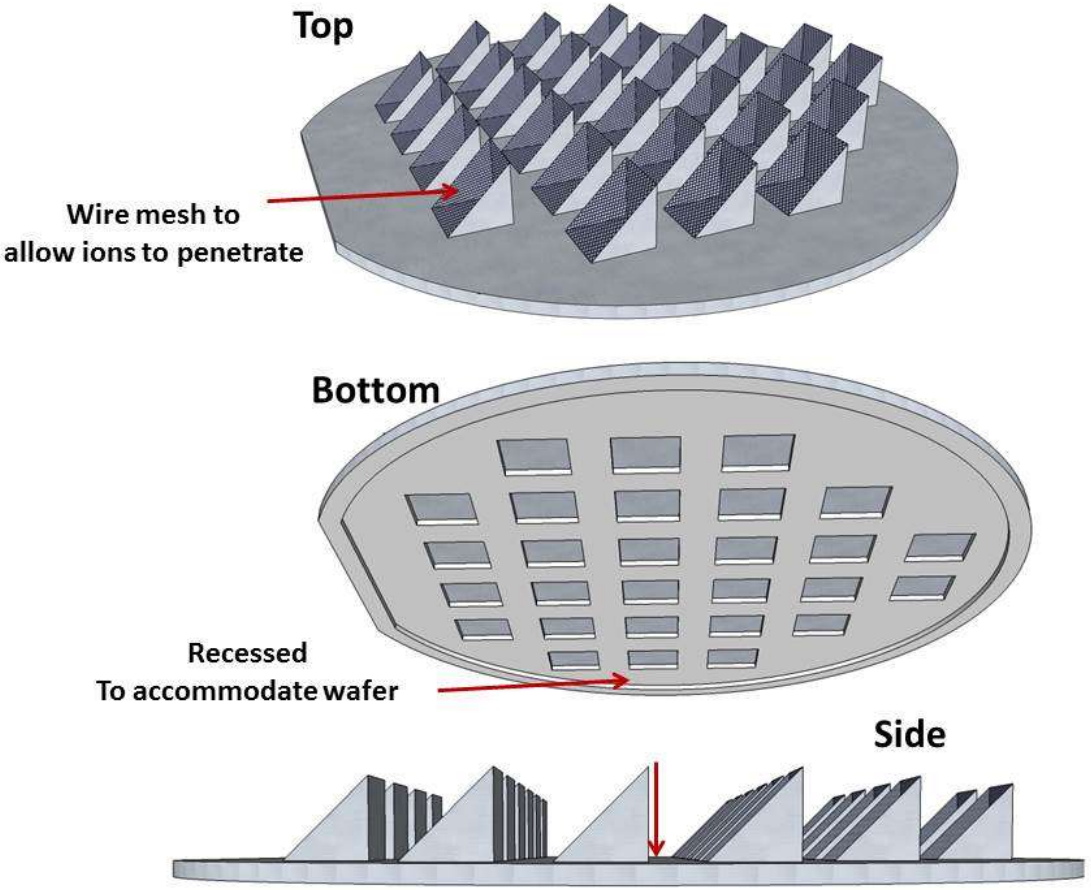




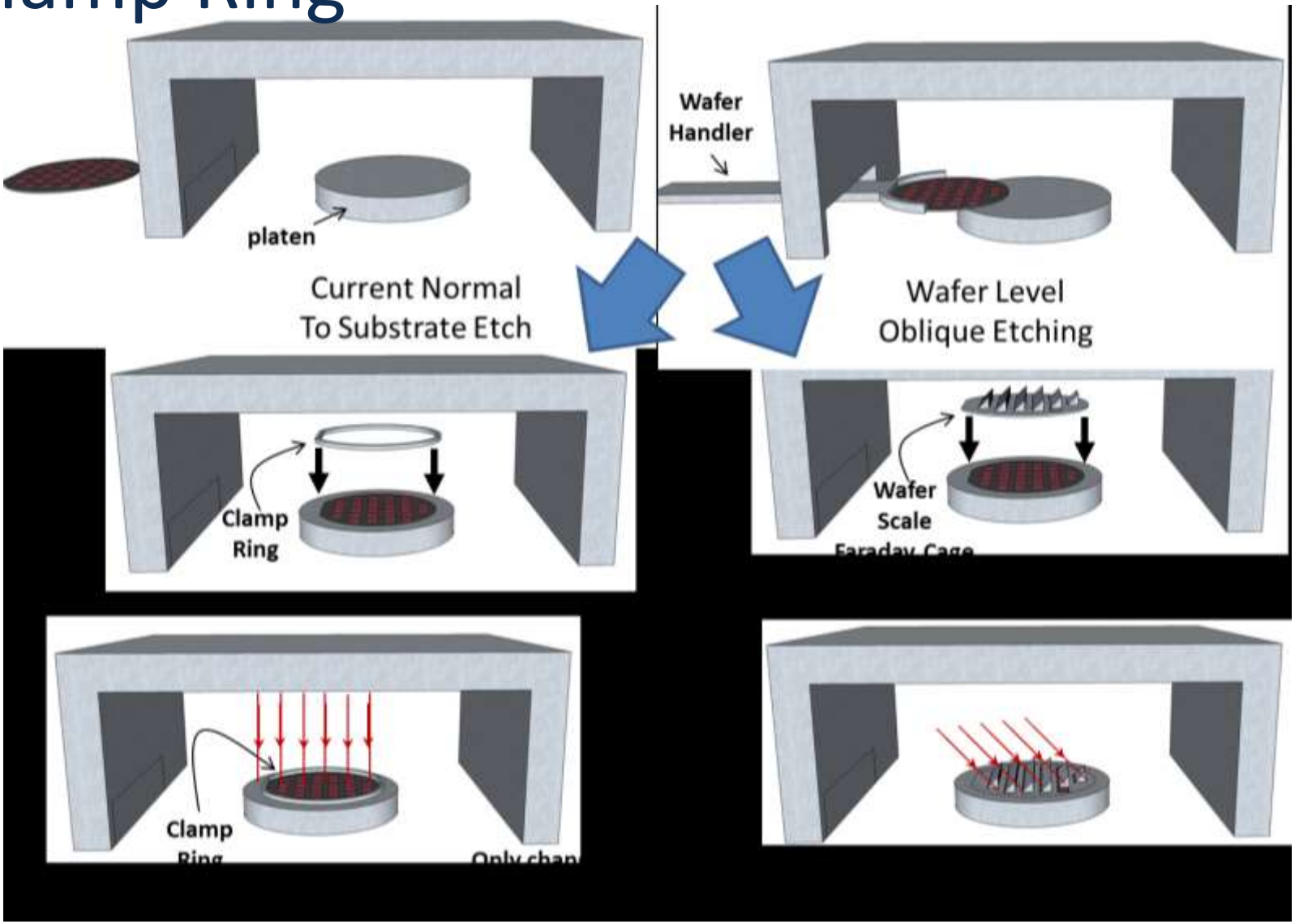




Wafer-level Faraday Cage Clamp Ring

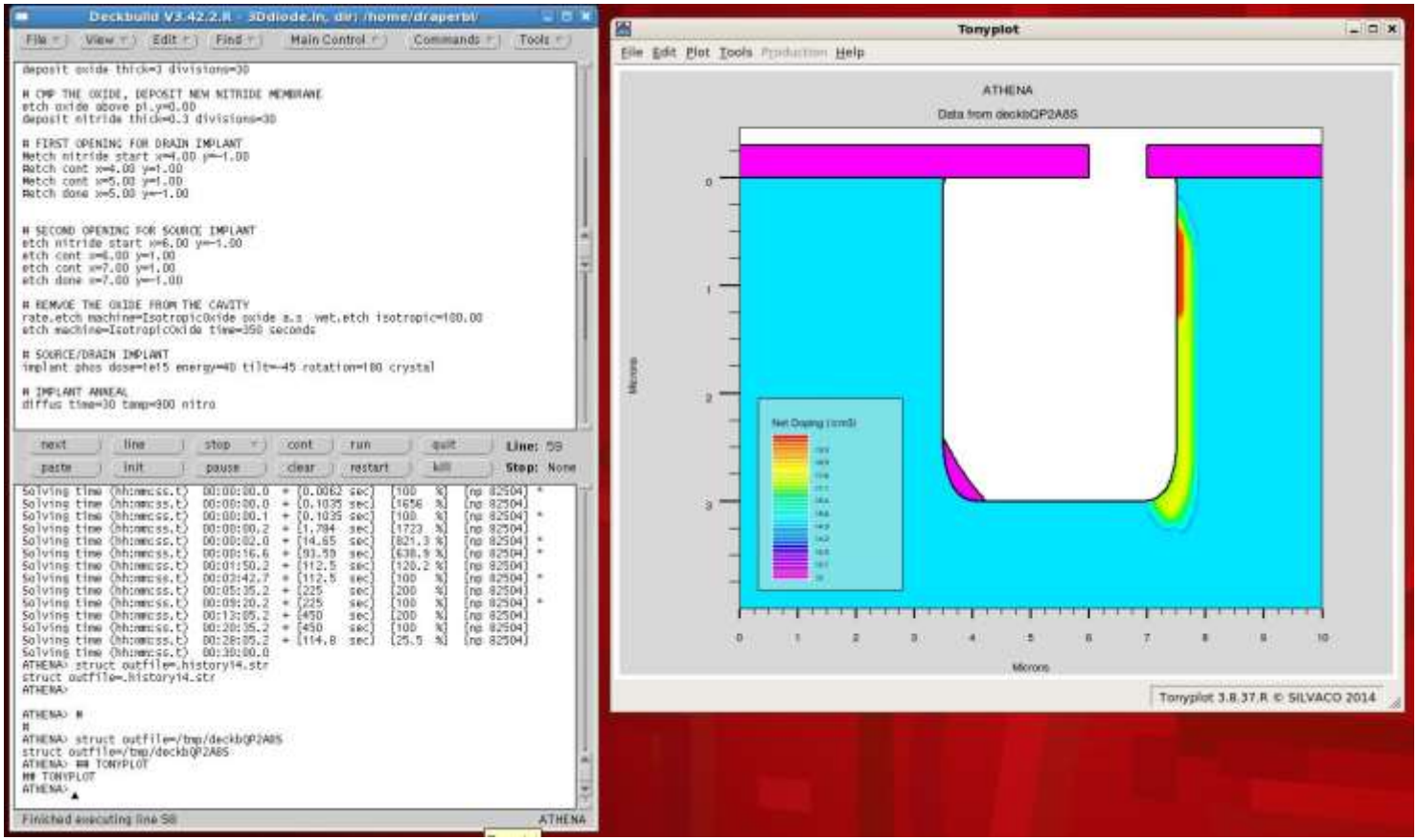


Wafer-level Faraday Cage Clamp Ring



Directional Implantation:
Currently in HVM → Halo implants

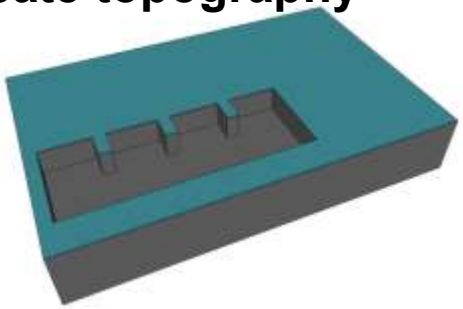
Process Sim Modeling: Angled Implantation



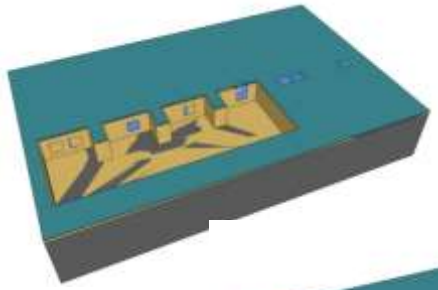
1000 Å Nitride membrane possess enough stopping power

Currently in Fabrication

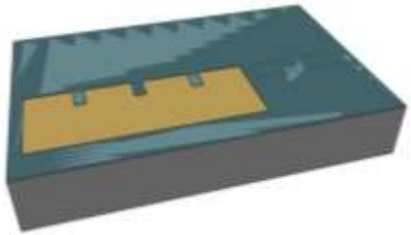
Create topography



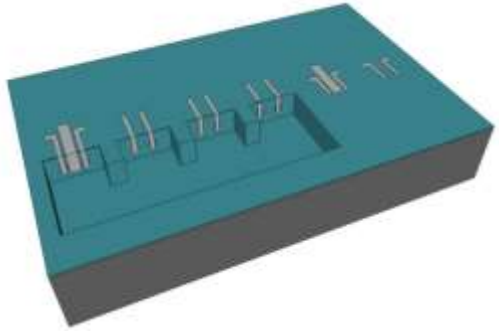
Grow/Deposit Gate Oxide



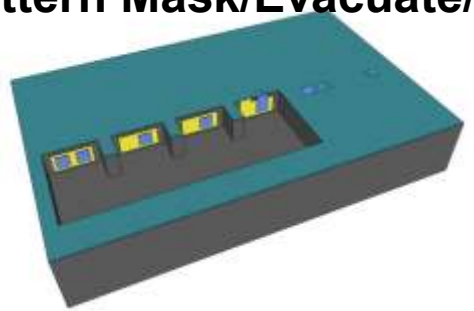
Backfill and CMP



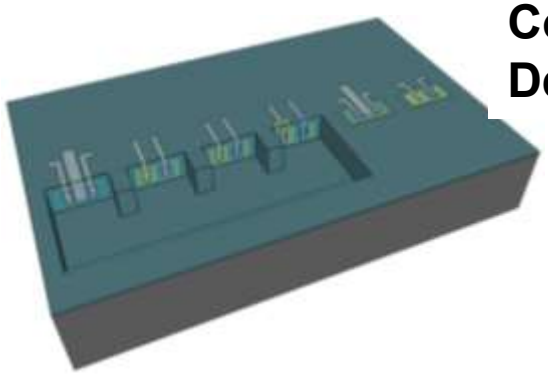
Deposit Metal Gate And SD Contacts



Pattern Mask/Evacuate/Implant



Completed Devices



Conclusions

- Device level 3D ICs can potential reduce interconnect lengths by factors (compared to % by improving materials)
- MPL is a general fabrication technique for patterning 3D structures in CMOS compatible materials.
- CMP-flatness of membrane – high NA immersion stepper compatible.
- MPL requires only fixturing changes to current SOA semiconductor processing equipment.
- Fabrication of device-level 3D-ICs underway to demonstrate proof of concept long-channel metal gate CMOS.

QUESTIONS?

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