Chemical Vapor Deposition of Refractory Ternary Nitrides for Advanced Diffusion Barriers

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Refractory ternary nitride films for diffusion barriers in microelectronics have been grown using chemical vapor deposition. Thin films of titanium-silicon-nitride, tungsten-boron-nitride, and tungsten-silicon-nitride of various compositions have been deposited on 150 mm Si wafers. The microstructures of the films are either fully amorphous for the tungsten based films, or nanocrystalline TiN in an amorphous matrix for titanium-silicon-nitride. All films exhibit step coverages suitable for use in future microelectronics generations. Selected films have been tested as diffusion barriers between copper and silicon, and generally perform extremely well. These films are promising candidates for advanced diffusion barriers for microelectronics applications.

The manufacturing of silicon wafers into integrated circuits uses many different process and materials. The manufacturing process is usually divided into two parts: the front end of line (FEOL) and the back end of line (BEOL). In the FEOL the individual transistors that are the heart of an integrated circuit are made on the silicon wafer. The responsibility of the BEOL is to wire all the transistors together to make a complete circuit. The transistors are fabricated in the silicon itself. The wiring is made out of metal, currently aluminum and tungsten, insulated by silicon dioxide, see Figure 1. Unfortunately, silicon will diffuse into aluminum, causing aluminum spiking of junctions, killing transistors. Similarly, during chemical vapor deposition (CVD) of tungsten from WF_6, the reactivity of the fluorine can cause "wormholes" in the silicon, also destroying transistors. The solution to these problems is a so-called diffusion barrier, which will allow current to pass from the transistors to the wiring, but will prevent reactions between silicon and the metal.

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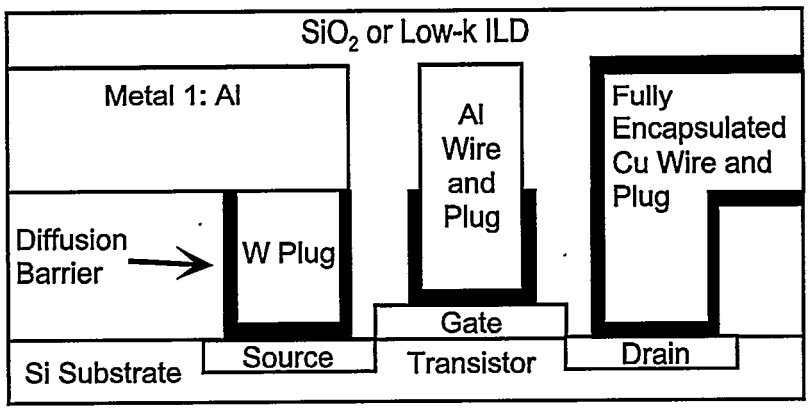

Figure 1. General integrated circuit metallization scheme. On the left is the current industry standard of tungsten vias and aluminum alloy wires. The gate contact shows the potential replacement of the tungsten with aluminum. On the right is the future with Cu completely encapsulated by a diffusion

There are a number of requirements for a diffusion barrier for silicon microelectronics, which have often been reviewed in the literature (*1-6*). As device dimensions shrink, the demands on diffusion barrier performance and processing reliability increase. One set of demands is on the composition and microstructure of the barrier material. The barrier must keep the silicon and metal apart. First, the barrier must remain macroscopically intact as a layer between the silicon and metal layers. This can be accomplished in several ways. A variety of "reactive" barriers have been investigated which will react with the silicon or the metal, although the reaction is self-limiting and part of the barrier will remain intact for the lifetime of the device. As devices get smaller, the barrier must shrink proportionately, so it is more difficult to find materials that continue to work. Second, the barrier can be made of a material that remains in thermodynamic equilibrium with both silicon and the metal. Because of the reactivities of silicon and most metals, this can dramatically limit the choices of materials.

In addition to having to remain intact to keep the silicon and the metal from interacting, the barrier must also keep either one of them from diffusing through and reacting with the other. Bulk diffusivities tend to scale with the melting point (*7*), so materials with a high melting point are preferred. In addition, it is important to consider high diffusivity paths, such as grain boundaries (*7*). If a single grain boundary crosses the thickness of the barrier, it may provide a ready diffusion pipe for the silicon or the metal, bypassing the bulk of the barrier. It is almost impossible to grow single crystal layers of materials in microelectronics processing, so eliminating grain boundaries requires using an amorphous material. Thus, an amorphous refractory material is a obvious candidate for a diffusion barrier.

A third set of demands on the diffusion barrier is related to the deposition method. There are two common methods for depositing films in microelectronics. The first is sputtering, where a target material is eroded by a plasma and transported to the silicon wafer, possibly reacting with the plasma gases along the way. The second method is chemical vapor deposition (CVD), where gas or vapor phase precursors flow over the wafer and react to grow the film. Sputtering has the advantage of being a low temperature, simple process. Since the diffusion barrier is

deposited after the transistors are formed and, possibly, after some metal layers have already been deposited, the allowable thermal budget is very small. However, CVD processes are more effective at coating the sides or bottoms of vias, leading to better step coverage. This issue of step coverage is critical since via sizes are rapidly approaching 0.18 μm with an aspect ratio of 10:1 or greater.

Finally, several electrical parameters are required of the barrier. The first is that the barrier material conduct electricity. The requirement is not as stringent as for the metal wires, since the barriers are much thinner than the length of the wiring. So, although a resistivity of 2.4 μΩ cm for Al wires is considered high relative to 1.6 μΩ cm for Cu, it is generally accepted that future diffusion barriers can have resistivities up to 1000 μΩ cm and still be useful. The second electrical parameter is the contact resistance of the barrier to the silicon or the metal. Contact resistance is caused by the presence of an interface (and, possibly, contamination) between materials. A desirable contact resistance for future barriers is 1 $n\Omega/cm^2$. For a square 0.15 μm contact, the contribution to the resistance per contact from a bulk resistivity of 1000 μΩ cm and a contact resistance of 1 $n\Omega/cm^2$ are equal, and as the contact size decreases, the contact resistance rapidly becomes larger than the bulk resistance.

Currently, the most widely used diffusion barrier for microelectronics metallization is sputtered TiN. As device sizes continue to shrink, two major problems arise with sputtered TiN: poor step coverage and the columnar polycrystalline microstructure. The poor step coverage will not allow TiN to fully line the aggressive via geometries of future devices, while the columnar microstructure will limit the barrier performance by providing grain boundaries that act as fast diffusion paths across the barrier (*1*). Chemical vapor deposition of TiN has the potential to produce highly conformal films. Films grown from $TiCl_4$ and NH_3 exhibit excellent step coverage, but are deposited at relatively high temperatures (450 to 700°C) and are contaminated with chlorine, particularly at low temperatures, which can cause corrosion in the aluminum metallization (*8*). The deposition temperature can be reduced by using metalorganic precursors such as tetrakis(dimethylamido)titanium (TDMAT), with or without NH_3, but these films generally exhibit either poor step coverage or film resistivities that are too high for metallization applications (typically caused by C impurities) (*9-11*). More recent work has focused on improving the quality of films grown with TDMAT by post-deposition treatments with nitrogen plasmas or silane exposure (*12, 13*). Titanium nitride films grown from tetrakis(diethylamido)titanium (TDEAT) and NH_3 exhibit good step coverage and lower resistivities (*11*). Regardless of the deposition chemistry, the problem of grain boundary diffusion remains for CVD TiN.

To eliminate grain boundary diffusion, several groups have investigated amorphous or nanocrystalline materials (*14-17*). The most promising materials for microelectronics are films consisting of a refractory metal (e.g., Ti or W), nitrogen, and a third constituent, typically Si, such as titanium-silicon-nitride (Ti-Si-N) (*16*). These ternaries have high crystallization temperatures, so they retain their microstructure after thermal cycling, and tend to be thermodynamically stable in contact with either Si or the metal lines. Excellent barrier properties have been

demonstrated for sputtered Ti-Si-N, W-Si-N, and other similar combinations (*16-18*). However, the poor step coverage of the sputtering process remains an obstacle to their application in ULSI devices.

In this report we describe the development of chemical vapor deposition (CVD) processes for three refractory ternary nitrides, Ti-Si-N, W-B-N, and W-Si-N. These materials do not react with either Si or Cu (*19*), and are either amorphous or contain small nanocrystals in an amorphous matrix, and do not crystallize at normal BEOL processing temperatures. The CVD processes described here are performed at low temperatures, generally near 350°C, and the step coverages for the processes are sufficient for future device geometries. The materials have resistivities below 1000 μΩ cm, suitable for use in metallization. These characteristics make them viable candidates for ULSI diffusion barriers.

Experimental

Titanium-silicon-nitride films were grown in an MRC Phoenix CVD system. This system consists of a single-wafer process chamber attached to a central robotics hub with a vertical-cassette elevator for batch wafer loading. The system was based on MRC's beta-test version of their $TiCl_4$ TiN CVD system, with modifications to deliver metalorganic precursors as well as an additional mass flow controller for silane. The metalorganic precursors were delivered using a heated (65°C) bubbler and N_2 as the carrier gas. The system at Sandia used nitrogen (N_2), ammonia (NH_3), silane (SiH_4), and a metalorganic precursor in nitrogen carrier gas. The only metalorganic precursor used in these experiments was TDEAT. Experiments performed using $TiCl_4$ are detailed elsewhere (*20*).

The MRC process chamber was designed to be similar to a rotating disc reactor (*8*). The 150 mm wafers sit on a susceptor that can be heated (20 - 800°C) and can rotate at 0 to 1500 rpm. All depositions were performed at a pressure of 20 Torr. The walls were warmed to 125-150°C to prevent condensation of TDEAT. A gas injection showerhead lies ≈3 cm above the susceptor. As delivered, all the reactants were injected into the showerhead plenum, allowed to mix, and then flowed down out of the showerhead to the wafer below. The showerhead, although passively cooled with a heat pipe, was warm enough that TDEAT would react with the other precursors while still in the showerhead. This resulted in the growth of highly C contaminated films. Therefore, the showerhead was modified to include a separate "piccolo tube" for injection of TDEAT. This tube hung slightly below the showerhead (which was moved up to accommodate the modifications) and extended along a radius from near the center of the showerhead out to the edge of the wafer.

Tungsten-based films were grown in a Vactronics CVD system, a single wafer, manual loading tool. The 150 mm wafer holder was heated to 300 - 450°C. The showerhead was custom designed and included three separately plumbed injection rings located 10 cm above the wafer. The gases used in film deposition were WF_6, NH_3, N_2, Ar, and a pyrophorics line used for B_2H_6, SiH_4, or Si_2H_6. The deposition pressure was typically 500 to 700 mTorr.

The weight gain during deposition was correlated with cross section SEM measurements of film thickness. These results were used to estimate the film thicknesses of other samples by using only the mass gain of the wafer. The sheet resistance of films deposited on oxide was measured using a 4-point probe, and converted to film resistivity using the estimated film thickness. Plan view or cross section high resolution TEM was performed on selected Ti-Si-N, W-B-N, and W-Si-N films to determine the microstructure of the material. Rocking curve X-ray data was taken on various films before and after thermal annealing to monitor microstructure changes. Film composition was measured with 3.5 MeV He^+ Rutherford backscattering spectrometry (RBS) and 28 MeV Si^{5+} elastic recoil detection (ERD) (*21*). Film stress was determined from wafer curvature measurements.

Ternary films were deposited over test structures to determine step coverage. These structures consisted either of trenches patterned through polysilicon down to silicon dioxide (for feature sizes down to 0.5 μm), or trenches were cut into crystal silicon and then thermally oxidized to narrow the trenches down to feature sizes of 0.1 μm. Films were also deposited over large area (250 × 250 μm) diodes for testing their effectiveness as diffusion barriers. Finally, several films were used in contact chain structures to monitor integration effects.

Titanium-Silicon-Nitride from TDEAT

Titanium nitride can be deposited by CVD at temperatures down below 250°C with metalorganic precursors such as TDMAT or TDEAT (*22*). We chose to focus on using TDEAT as the titanium precursor. TDMAT reacts more easily than TDEAT, which leads to two problems. The first is that TDMAT and NH_3 react quickly in the gas phase (*23*), which can lead to gas phase nucleation of particles. The reaction rate for TDEAT is more than two orders of magnitude lower than for TDMAT (*24*). Second, silane and disilane are much less reactive at low temperatures, so Si incorporation will be harder at lower temperatures where TDMAT is commonly used. This suggested that the deposition temperature might have to be relatively high by metalorganic CVD standards. However, it is known that TDMAT-based TiN can have high carbon levels, increasing the film resistivity, as the deposition temperature rises above 300°C (*11*). These constraints limited the choice to TDEAT as the titanium precursor.

Titanium-silicon-nitride films can be grown under a wide range of conditions using TDEAT, NH_3, and SiH_4 (*25*). The film compositions that have been deposited from 300 to 450°C are shown in Figure 2 on the Ti-Si-N ternary phase diagram (*26*). At these deposition temperatures, this chemistry can incorporate a wide range of Si in the films (0 to >25 at.%). The Ti-Si-N films lie along the TiN-Si_3N_4 tie line and are generally N rich. This is not surprising as MOCVD TiN is also found to be N rich (*11, 23*). Since TiN is known to have a broad composition range from 30 to over 54 at.% N (*27, 28*), the TiN-Si3N4 "tie line" is actually a two phase region that may encompass all of these films.

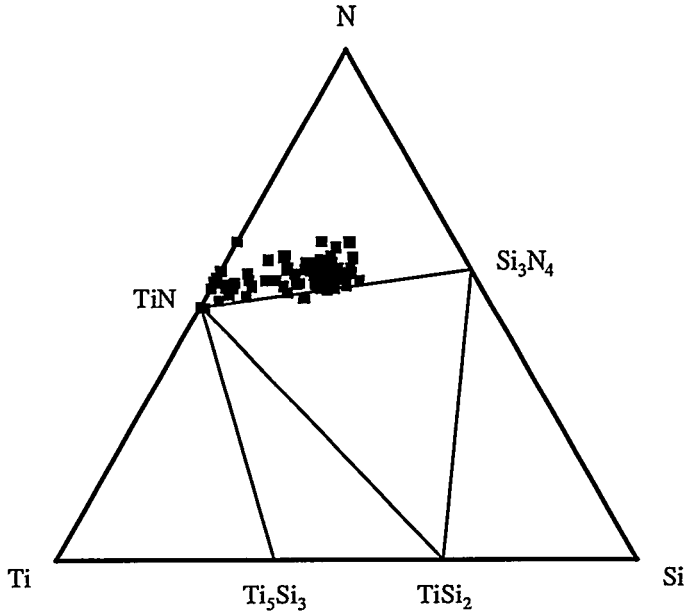

Figure 2. The compositions of films grown from TDEAT, SiH_4, and NH_3 are shown on a Ti-Si-N ternary phase diagram. The films lie near the TiN - Si_3N_4 tie line, and are generally nitrogen rich. The phase equilibria are tentative, since they are not known at these temperatures.

The question arises as to how Si is incorporated in the Ti-Si-N films. It is well known that SiH_4 and NH_3 do not react with each other at these low temperatures. This leaves three possibilities. The first is that the silane reacts with TDEAT, although TDEAT and SiH_4 do not react without NH_3 being present, i.e., we have not been able to deposit titanium silicides using these precursors. However, the reaction of silane may be catalyzed by an intermediate in the reaction of TDEAT and NH_3. TDEAT undergoes a transamination reaction in which the diethylamine groups surrounding the central Ti atom are replaced with NH_2 from the ammonia (*29, 30*). The more compact amine may reduce stearic hindrance (*31*), and allow the SiH_4 access to the Ti atom to undergo the reaction. A second reaction path is that the decomposition of SiH_4 is catalyzed by a metallic surface. That is, a thin film of TiN grows first, and then SiH_4 could decompose on the surface and be incorporated in the growing film. The third possibility is that diethylamido complexes with silicon are formed in either the gas phase or on the surface. These complexes react to form Si_3N_4 at lower temperatures than required for the SiH_4-NH_3 reaction (*32*), but it is not known if they will react below 450°C. Further experiments, such as mass spectrometry of the exhaust gases of the system, are needed to identify the Si reaction mechanism.

Although the mechanism for incorporation of Si in the Ti-Si-N films is not known, the amount of Si found in the films is a well behaved function of precursor flows. As shown in Figure 3, the relative concentration of Si found in a film is a monotonically increasing function of the ratio of SiH_4 to TDEAT in the precursor flow, divided by the total gas flow in the system. A similar plot is obtained for the simpler cases of either the ratio of SiH_4 to TDEAT or SiH_4 to total gas flow on the abscissa. The increase in Si content with increasing SiH_4 flow is expected. The

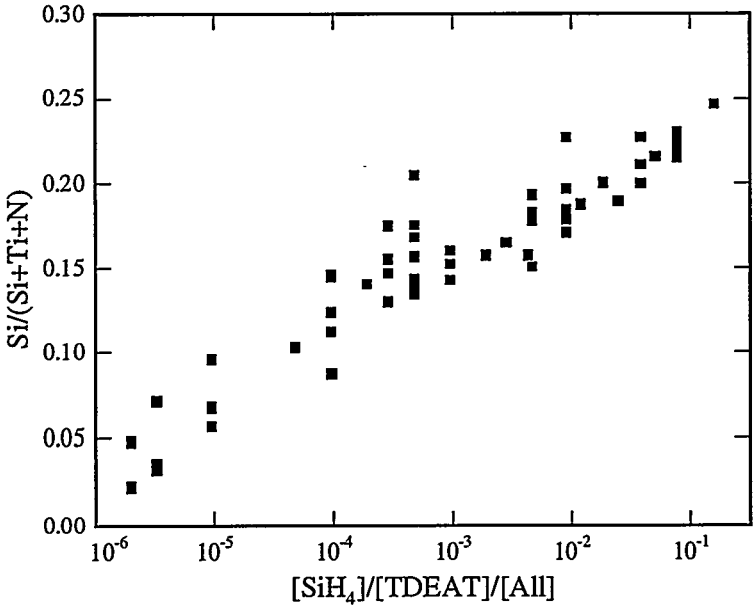

Figure 3. The Si content of Ti-Si-N is shown vs the ratio of SiH_4 to TDEAT divided by the total gas flow, which establishes the gas residence time in the reactor. Si incorporation increases logarithmically with the gas flow ratios. The spread is caused by changing parameters such as the temperature.

decrease in Si content as the total gas flow is increased, and hence the SiH_4 residence time in the reactor decreases, is also normal. An increase in TDEAT flow could result in a decrease in the Si content if the major effect of higher TDEAT flows is to grow more TiN, lowering the relative amount of Si in the film. Two other points should be noted. First, very low SiH_4 flows are required to incorporate some Si into the films (typical SiH_4 flow rates where below 1 sccm). Second, the incorporation of Si into the films saturates relatively quickly with SiH_4 flow. That is, we could not access compositions near the Si_3N_4 side of the tie line.

Figure 4 shows the resistivity of Ti-Si-N films as a function of the Si content. The resistivity of TiN (no Si) grown from TDEAT and NH3 ranges from about 100 to 1000 μΩ cm. This spread is normal for this deposition chemistry, and reflects a range of TiN stoichiometries (*33*). The addition of silicon to the films increases the resistivity exponentially, eventually exceeding 1 Ω-cm at 25 at.% Si (not shown). In order to remain below the 1000 μΩ-cm level, the films must have a composition with less than approximately 4 at.% Si.

The lowest resistivity at a given Si composition is found for films deposited at 350°C. Here, the film resistivity varies predictably from ≈ 400 μΩ cm for TiN to nearly 1 Ω cm for Ti-Si-N with 25 at.% Si. Films grown at 300, 400, or 450°C have higher resistivities at a given Si composition. These systematic variations in film resistivity with deposition temperature correlate well with the "excess" nitrogen incorporated in the films, that is, how far the films lie from the ideal TiN-Si_3N_4 tie line. Films deposited at 350°C have the lowest resistivities and lie closest to the tie line, having an average of only 1.5 at. % excess N. Films deposited at 300 or 400°C have ≈ 8 at.% excess N, resulting in higher resistivities. The 450°C films have the

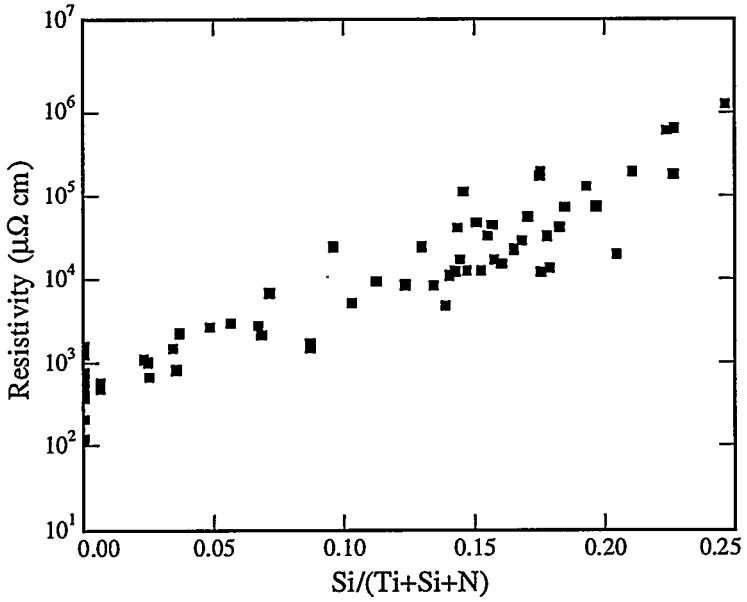

Figure 4. The resistivity of Ti-Si-N films is shown as a function of the Si content. The wide spread in resistivity at a given Si content is caused primarily by variations in the N content of the films, i.e. how far the films lie from the ideal TiN - Si_3N_4 tie line. Only films with low Si content have low resistivities.

greatest amount of excess N, ≈ 15 at.%, and the highest resistivities. This is similar to MOCVD TiN films deposited at atmospheric pressure, which have resistivities that are sensitive to stoichiometry and display an increase in resistivity at temperatures above and below 350°C (*33*).

High resolution cross-section TEM of Ti-Si-N show that, as-deposited, the film consists of small nanocrystals, ≈ 6 nm in diameter, embedded in an amorphous matrix (*25*). The rings in the electron diffraction pattern index to TiN, with no evidence of any other phase. Therefore, the nanocrystals observed are TiN embedded in an amorphous matrix. The volume fraction of amorphous material is much larger than can be accounted for by Si_3N_4 alone, so the amorphous material must also contain a significant fraction of Ti as well. The microstructure found for these CVD Ti-Si-N films is similar to that of sputtered Ti-Si-N films, which are known to be excellent diffusion barriers (*16*). X-ray diffraction indicates that annealing below 750°C does not significantly change the microstructure.

The Ti-Si-N films are smooth and featureless as deposited, and have good step coverage (*25*). For example, a $Ti_{0.46}Si_{0.03}N_{0.51}$ film (with impurities of 1 at.% C and 8 at.% H) deposited at 350°C has step coverages of 60% on 0.2 μm lines with an aspect ratio of 6:1, 75% on 0.35 μm lines at 3:1, and 35% to 40% even for 0.1 μm lines at 10:1. It should be noted that the conformality of this CVD Ti-Si-N film is better than that previously observed for optimized TDEAT-based CVD TiN films (85% for 0.8 μm lines with an aspect ratio of 1.2:1) (*11*).

Ti-Si-N films were integrated into a standard MDL test chip, a 16 kilobyte static random access memory surrounded by various test structures. A twelve wafer lot was split three ways at the via liner process. One split received the standard via

liner, consisting of sputtered Ti, a rapid thermal anneal (RTA) step to resilicide the contacts and getter impurities into the Ti, and sputtered TiN. The second split was processed through sputtered Ti, RTA, and then CVD Ti-Si-N. The final split consisted of using just CVD Ti-Si-N alone with no sputtered Ti. It was found that CVD tungsten nucleated differently on the CVD Ti-Si-N than on sputtered TiN.

After completing the rest of the needed processing (tungsten deposition, CMP, and metal deposition and patterning), all wafers went through electrical test. The resistivity of chains of 2986 contacts from metal 1, through a tungsten plug (with Ti/TiN or CVD Ti-Si-N liner) to n+ Si, and then back up through a plug to metal 1 were measured to determine the average resistance per contact. The four wafers with the standard Ti/TiN process yield an average resistance per contact of $13.6 \pm 3.6\ \Omega$ (251 total good die). Only one CVD Ti-Si-N wafer survived processing because of tungsten nucleation problems, and it had an average resistance per contact of $13.8 \pm 4.0\ \Omega$ (63 good die). The mixed process, sputtered Ti and then CVD Ti-Si-N, showed much higher resistances of about 56 Ω, which was attributed to the exposed Ti absorbing impurities, primarily oxygen, while waiting for the CVD Ti-Si-N film. Comparing the standard Ti/TiN process vs the CVD Ti-Si-N liner shows no statistically significant difference in contact resistance.

Several different Ti-Si-N films were evaluated as diffusion barriers against copper or aluminum. Arrays of large area diodes (250×250 μm) isolated by oxide were fabricated on 150 mm wafers. After depositing a blanket barrier film, the Ti-Si-N was patterned so that it covered the diode area and some 10 μm of oxide on all sides. Thick photoresist was used to pattern sputtered copper or aluminum using a lift-off process. The diodes could then be annealed in vacuum at different temperatures, and the diode characteristics, particularly the reverse leakage current, used as a measure of barrier effectiveness.

With Al metallization, all of the Ti-Si-N barriers survived anneals up to 30 min at 350°C, but all of them fail after annealing at 400°C. Experiments on sputtered Ti-Si-N barriers against Al typically perform better than these CVD films (*34*). However, all of the sputtered films that were tested had higher Si contents than these CVD Ti-Si-N films. For Cu metallization, no increase in reverse current, indicative of barrier failure, is observed for anneals up to 500°C. After annealing at 550°C, most barriers are still good, and it is only at 600°C that all barriers fail. This performance should be suitable for use in future ULSI generations.

Tungsten-Boron-Nitride

Tungsten-boron-nitride films were deposited in the Vactronic CVD system (*35*). The precursors used for the film were WF_6, SiH_4, NH_3, and 30 % B_2H_6 in N_2. Argon was used as a carrier gas. Tungsten is incorporated in the film through reduction of WF_6, which thermodynamically prefers to react with the silane. Because B_2H_6 is unstable at room temperature, boron is most likely incorporated in the film through simple decomposition of B_2H_6. Nitrogen is incorporated through the reaction of ammonia with tungsten on the hot wafer surface (*36*). The only

impurities detected by RBS or ERD in these films was Si (less than 5 at.% maximum) and H (typically 5 at.%).

The compositions grown with this chemistry are shown in Figure 5 on a W-B-N ternary phase diagram. Since the ternary phase diagram has only been assessed at much higher temperatures (*26*), the tie lines shown are tentative. The main discrepancy with published diagrams is the possible tie lines between BN and the different tungsten nitrides, many of which are thermodynamically unstable (*37*), but are easily grown by CVD. The compositions lie roughly in a band from WB_4 to W_2N. We were unable to increase the tungsten fraction in the film by changing the relative gas flows. Films grown with high WF_6 partial pressures have little or no detectable hydrogen in them, compared with 5 at.% H for most of the films shown on the diagram. This indicates that for sufficiently high WF_6 flows the growing surface switches from being H-terminated to being F-terminated, which has been observed in the WF_6-SiH_4 system (*38*). This change in the surface state may limit W incorporation in the film.

As-deposited W-B-N films are amorphous as measured by x-ray diffraction. The resistivities of these films range from 200 μΩ cm for films rich in tungsten and boron to 20,000 μΩ cm for films close to the W-N side of the ternary system. The resistivity as a function of N content is shown in Figure 6. Films with less than about 20 at.% N have resistivities below 1000 μΩ cm.

The step coverage of a $W_{0.24}B_{0.66}N_{0.10}$ film grown over 1.5 μm wide trenches with an aspect ration of 5.5 is 40%, which is good but not exceptional. However, the large surface area caused by having a high density of these structures across the entire wafer may have resulted in reactant depletion which would limit the coverage. It is possible that the step coverage on samples more typical of microelectronics metallization might be better.

All ternary W-B-N films investigated with Read camera x-ray diffraction were amorphous as deposited. High resolution TEM (not shown) on a film with the

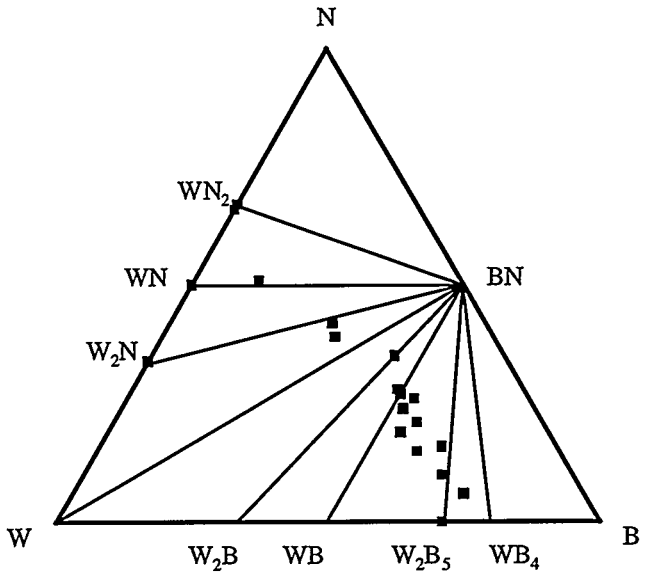

Figure 5. The compositions of films grown at 350°C from WF_6, B_2H_6, and NH_3 (with SiH_4 to reduce the WF_6) are shown on a W-B-N ternary phase diagram.

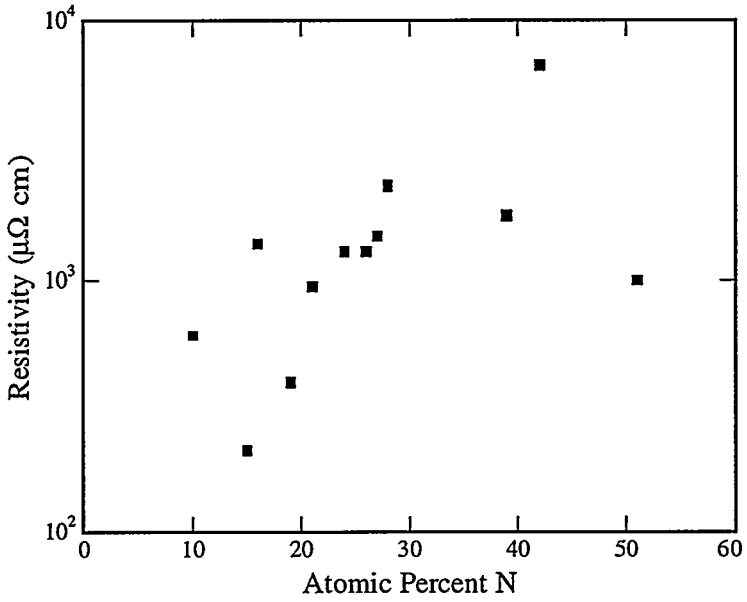

Figure 6. The resistivity of W-B-N films is shown as a function of the N content. Several different compositions have resistivities below 1000 μΩ cm, required for use as diffusion barriers.

composition of $W_{0.24}B_{0.52}N_{0.24}$ revealed some small diffracting regions some 1.5 to 2 nm in size. However, the volume fraction of these crystallites was estimated to be below 5 vol.%. Films were then subjected to one hour anneals until some crystallization was detected in the x-ray diffraction patterns. Many compositions did not begin to crystallize until 700°C or higher.

These films were also tested as diffusion barriers using 100 nm films deposited on 250 × 250 μm diodes. These diodes had Cu sputtered on them, and the diode characteristics were monitored as a function of anneal temperature in vacuum. Failure of the barrier was defined as an increase in reverse current of a factor of ten. All of these films were good diffusion barriers up to at least 500°C for 30 min, with many composition exceeding 600°C.

Tungsten-Silicon-Nitride

Tungsten-silicon-nitride films were also deposited in the Vactronics CVD system (*35*). The precursors used were WF_6, SiH_4 or Si_2H_6, and NH_3. Argon was used as a diluent. The deposition pressure was typically 500 to 700 mTorr, and the wafer temperature was 350°C. Little if any silicon was incorporated in the film when SiH_4 was used. However, using Si_2H_6 did result in Si incorporation. The deposition rates are adequate for diffusion barrier applications at 5 to 500 nm/min, depending on flow conditions. The films were smooth and featureless both visually and by SEM. The only impurity detected in the films was H, present at levels below 5 at.%.

A range of compositions can be grown from WF_6, Si_2H_6, and NH_3 as indicated in Figure 7. In general, the compositions form an arc from WN_2 to WSi_2, passing over a number of possible tie lines. As in the cases of Ti-Si-N and W-B-N, the ternary phase diagram has only been assessed at much higher temperatures (*26*),

so the tie lines shown are tentative, particularly for the W-N compounds. The film resistivity as a function of Si content is shown in Figure 8. Almost all films have resistivities below 1000 μΩ cm. Films with stoichiometries corresponding to WN_2 (i.e. no silicon) have resistivities in excess of 20,000 μΩ cm.

The step coverage of these films is exceptional. Even over reentrant 0.25 μm, 4:1 aspect ratio features the step coverage is 100%. Films with a composition of $W_{0.47}Si_{0.09}N_{0.44}$ have been tested as diffusion barriers with copper on large area diodes. The reverse leakage current of the diodes increased only after a 30 min anneal at 700°C. This film composition shows signs of crystallization by x-ray diffraction at 700°C as well. High resolution TEM on as-deposited $W_{0.49}Si_{0.10}N_{0.41}$ films shows no evidence for crystallinity in bright field, dark field, or electron diffraction imaging modes.

Conclusions

Processes for chemical vapor deposition of three different amorphous refractory ternary materials have been developed. Titanium-silicon-nitride was deposited using TDEAT, NH_3, and SiH_4. The Ti-Si-N films from TDEAT consisted of nanocrystals of TiN in an amorphous matrix. Growth of tungsten-boron-nitride was accomplished with a mixture of WF_6, SiH_4, B_2H_6, and NH_3, while tungsten-silicon-nitride was deposited from WF_6, Si_2H_6, and NH_3. The tungsten-based ternaries were completely amorphous as-deposited. Each film offers step coverages and film resistivities well within the range needed for future ULSI generations. In addition, they are excellent diffusion barriers to copper, with barrier failure temperatures as high as 700°C. These characteristics make them promising candidates for advanced diffusion barriers in microelectronics applications.

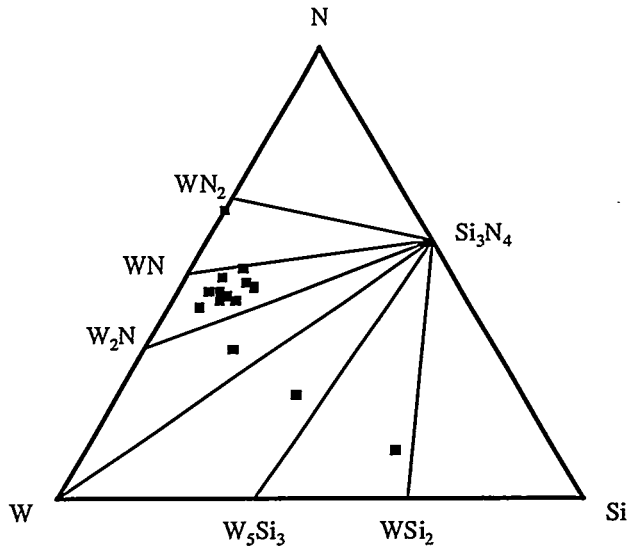

Figure 7. The compositions of films grown at 350°C from WF_6, Si_2H_6, and NH_3 are shown on a W-Si-N ternary phase diagram. The tie lines are tentative. Most films lie in a composition range from WSi_2 to WN.

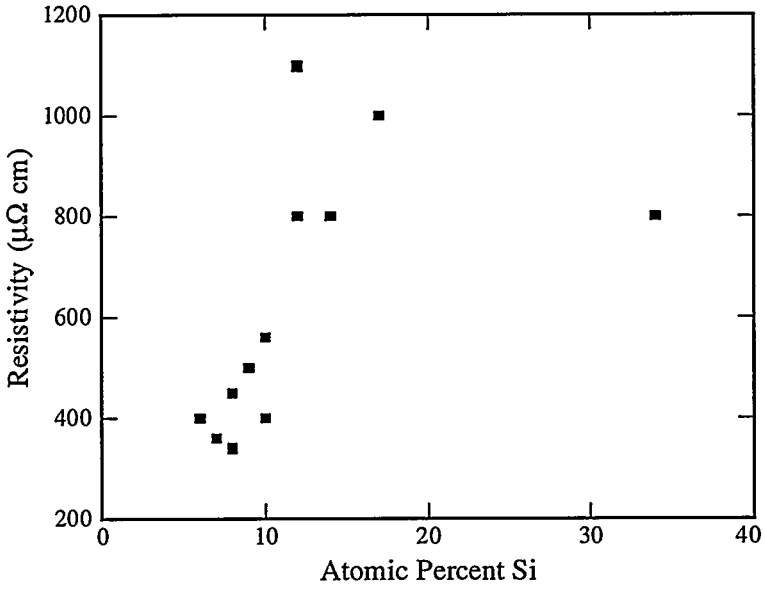

Figure 8. The resistivity of W-Si-N films is shown as a function of the Si content. Most films have resistivities below 1000 μΩ cm, required for use as diffusion barriers.

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