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Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation

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***Abstract*-- This study examines the single-event response of the Xilinx 20 nm Kintex UltraScale Field-Programmable Gate Array irradiated with heavy ions. Results for single-event effects on configuration SRAM cells and Block RAM memories are provided.**

I. Overview

This study examines the static single-event effects susceptibility of the Xilinx Kintex UltraScale Field-Programmable Gate Array (FPGA). The UltraScale is Xilinx's first product offering built using TSMC's 20 nm 20SoC process [1]. This part has also been previously tested for the purpose of estimating terrestrial neutron upset rates [2] and to determine susceptibility to direct ionization by low-energy protons [3]. The purpose of this work is to determine the flight-worthiness and feasibility of utilizing these parts in space environments where heavy ions are present.

The part was irradiated with heavy ions at effective LETs from 0.98 to 63.91 MeV-cm^2/mg in May 2015. This paper presents measured single-event upset (SEU) results for the FPGA configuration memory and the user-accessible block random-access memory (Block RAM).

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II. Test Description

A. FPGA Device Under Test

The Kintex UltraScale family is offered in various configurations with different numbers of logic blocks, Block RAM, supplemental functional features (such as high-speed transceivers, digital signal processing blocks, clock management tiles, and others), speed grade, temperature grade, packaging, and I/O pin count. UltraScale devices operate with a nominal 0.95 V main core voltage, an auxiliary voltage of 1.8 V, and programmable I/O pins at voltages from 1.2 V up to 3.3 V [4]. The configuration memory in these parts is comprised of an array of highly robust CMOS configuration latches that behave similarly to a static random-access memory (SRAM) [5]. This configuration memory controls the behavior of the various internal components and the programmable interconnect.

The specific part tested was the XCKU040-2FBVA1156E, which is a mid-range, extended temperature-grade, flip-chip Kintex UltraScale device.

The UltraScale device-under-test (DUTs) were attached to commercially available KCU105 evaluation boards. The package lid was removed from the device and the silicon substrate was thinned to approximately 68 μm. The board was verified against the OEM built-in self-test, which provided assurance that the thinned parts were functional following the part preparation steps. The prepared board is shown below in Figure 1.

Fig. 1. KCU105 board with UltraScale DUT mounted.

B. Hardware Setup

A JTAG controller developed by Brigham Young University based on the Xilinx programmable SOC ZYNQ device was the configuration monitor for this experiment. This board connected to the KCU105 through JTAG and would perform initial configuration and periodic readback of the FPGA configuration memory state.

The KCU105-based DUT board was powered through a single 12V input by an external power supply. The DUT board is equipped with Maxim power controllers with a PMBUS interface, allowing a USB PMBUS interface pod to monitor and control the power regulators on the KCU105. This method allowed individual control and monitoring of each of the power rails connected to the UltraScale FPGA.

The temperature of the part was monitored both through the embedded Xilinx Analog-to-Digital Converter (XADC) module and with a package-mounted thermocouple.

A picture of the SEU test setup is below in Figure 2.

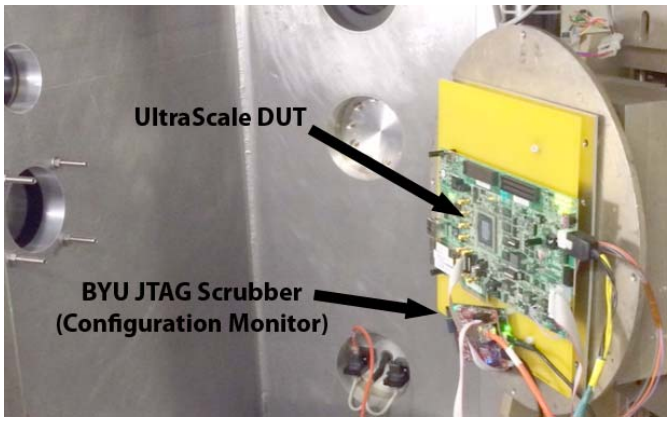

Fig. 2. Test setup inside LBL vacuum chamber.

C. Particle Beam Properties

The Kintex UltraScale DUTs were irradiated in vacuum at the Lawrence Berkeley Laboratory (LBL) 88-inch Cyclotron. Utilizing a variety of ions and angles from 0 to 65 degrees, effective LETs ranging from 0.98 to 63.91 MeV-cm^2/mg were obtained.

D. SEU Test Procedure

The goal of SEU testing is to examine the static SEU response of the configuration memory cells and the Block RAM in the UltraScale. During irradiation, the clock is stopped, which masks most dynamic effects typically caused by single event transients. The post-irradiation state of the DUT compared to the starting state to yields static upset counts. SEU testing was conducted at ambient temperature and nominal voltage biases.

In order to obtain Block RAM upset rates, the FPGA design loaded into the DUT included all available Block RAM primitives in the device. The initial values of these Block RAM primitives were divided into thirds consisting of all-1s, all-0s, and checkerboard patterns.

Following FPGA configuration, the clock was stopped and the part was irradiated to a specified fluence or until conditions arose that required stopping the beam, for example when SEU contention caused the die temperature to rise beyond safe thresholds.

During irradiation, readback of the configuration memory state occurred frequently (on average, every 15 seconds) in order to minimize the possibility of masking coincident SEUs on one memory cell.

III. Results

A. Configuration Memory Cell SEU

The Weibull curve illustrating the configuration memory cell cross-section is shown in Figure 3. These curves are generated with the SERET software tool, which takes the experimental data points and fits Weibull curves and generates space rate estimates using CREME96-like algorithms.

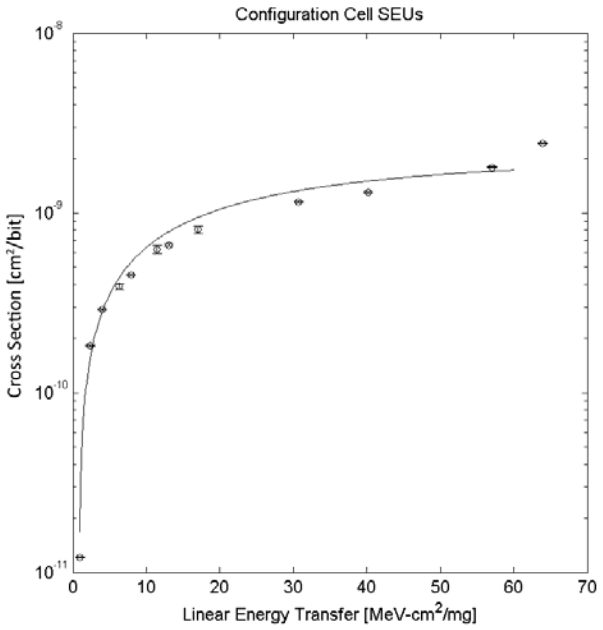

Fig. 3. Weibull curve for configuration memory cell upsets. L_{th}=0.8 [MeV-cm^2/mg], σ_{sat}=2.0e-9 [cm^2/bit], W=27.0 [MeV-cm^2/mg], S=0.88.

B. Block RAM SEU

Block RAM event analysis is ongoing, but preliminary results are shown below in Figure 4. One effect noted during Block RAM SEU testing was a reset-like event that would affect clusters of approximately 1024 bits per event. These large reset events were removed from the data set below in order to limit the analysis to SEU effects at the bit level.

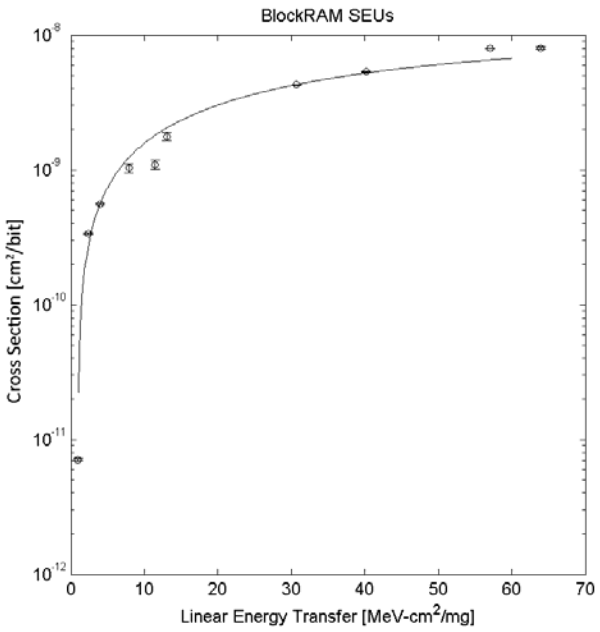

Fig. 4. Block RAM SEU Weibull curve. L_{th}=0.9 [MeV-cm^2/mg], σ_{sat}=1.0e-8 [cm^2/bit], W=53.0 [MeV-cm^2/mg], S=1.0.

C. Simulated Proton Sensitivity

There are several models that estimate proton sensitivity without testing the microcircuit of interest with protons, when heavy ion data is available. One such model, the Edmonds model, estimates the upper bound proton sensitivity cross-section. This model uses a generic charge collection efficiency function to calculate upper bound proton SEE cross sections from heavy ion data. There are several methods by which this can be accomplished, as described in [6]. We have chose to calculate the estimated upper bound using Method 3, whereby the heavy ion cross-section curve is integrated over LET values. The Weibull parameters provided the captions of Figures 3 and 4 above were used in the calculation.

TABLE I
EDMONDS MODEL PROTON ESTIMATES

	Configuration Memory	Block Ram
Upper Bound Proton Estimate Cross Section (cm^2/bit)	1.87E-15	4.74E-15

The values calculated in Table I correlate well to measured values presented in [3].

D. SEL Results

Although the testing performed so far was not specifically investigating single-event latch-up, the current consumption on each power rail was still monitored to look for current increases of any magnitude. The current was monitored primarily through the PMBUS communications with the Maxim power regulators.

The only current increases observed during this testing were attributed to contention within the device caused by upsets to the configuration memory. No latch-up-like current steps of any magnitude were observed on any power rail during this testing. However, a dedicated latch-up test is still needed to validate this part as a latch-up-free device.

E. Event Rates

The event rates from CREME96 [7] are listed below in Table II, assuming a GEO orbit, solar minimum conditions, and 100 mils of aluminum shielding.

TABLE II
EVENT RATES FOR SEU EVENTS

	Configuration Memory	Block RAM
per bit, per day	7.54E-09	2.48E-08
per device, per day	7.75E-01	6.26E-01

F. Heavy Ion Scaling Trends In Xilinx Configuration Memory

For reference we provide a plot in Figure 5 of scaling trends of Xilinx FPGA configuration memory including 0.13µm Xilinx Virtex-II [8], 90nm Xilinx Virtex-4 [9], 65nm Xilinx Virtex-5 [10], 28nm Xilinx Virtex-7 [11], and 20nm Xilinx UltraScale. Table III below provides Weibull parameters and rate calculations. Again, the event rates from CREME96 assume a GEO orbit, solar minimum conditions, and 100 mils of aluminum shielding.

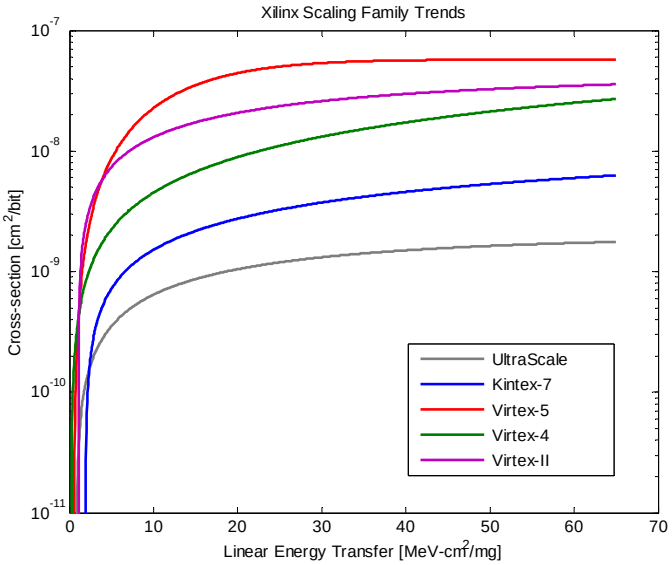

Fig. 5. Weibull fits for Xilinx configuration memory scaling Xilinx Virtex through Xilinx UltraScale devices.

TABLE III
SCALING FITS AND RATE CALCULATIONS

	Configuration Memory Rates	Weibull Parameters				
	per bit, per day	Node	Onset	Limit (cm^2/bit)	Width	Power
Virtex-II	3.99E-07	130 nm	1	4.37E-08	33	0.8
Virtex-4	2.63E-07	90 nm	0.2	1.76E-07	400	0.98
Virtex-5	4.23E-07	65 nm	0.5	5.73E-08	15	1.5
Kintex-7	1.41E-08	28 nm	1.9	1.43E-08	125	0.8
UltraScale	7.56E-09	20 nm	0.8	2.00E-09	27	0.88

IV. Conclusion

The Kintex UltraScale FPGA parts were tested for SEU performance in heavy ions at LBL at effective LETs from 0.98 to 63.91 MeV-cm^2/mg.

SEU cross sections are presented and performance of the part yielded very good results consistent with expectations derived from combining previous Xilinx FPGA family SEU performance with transistor feature size scaling. No SEL signatures were observed during testing, but test conditions and beam energies were not optimal for inducing potential SEL effects.

Further testing is needed to perform a full SEL test and obtain additional SEU data. A future test in June 2015 should be able to provide SEL data, and possibly additional configuration, Block RAM, and possibly user flip-flop data.

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