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Square Pulse LTD Based Injector for ARIA and / or DARHT I

Michael G. Mazarakis, Michael E. Cuneo, Mark Hess. Mark D. Johnston,
Mark L. Kiefer, Josh Leckbee, Tim J. Webb

My Message

- **A Linear Induction Voltage Adder (LTD) can be multi-pulsed because of its inherent modularity.**
- **However, only the square pulse LTD with less than 1% voltage variation flat top can be considered as a DARHT I or ARIA injector.**
  - **Multi-pulsing options**
  - **Square pulse LTD**

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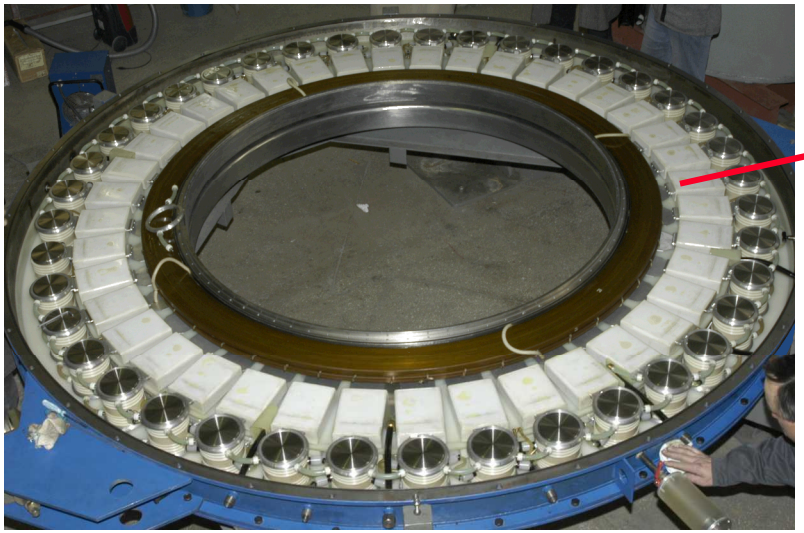
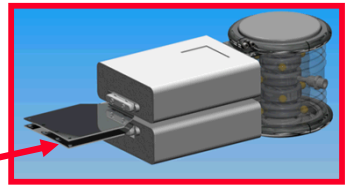
LTD Cavity Architecture
(a reminder)

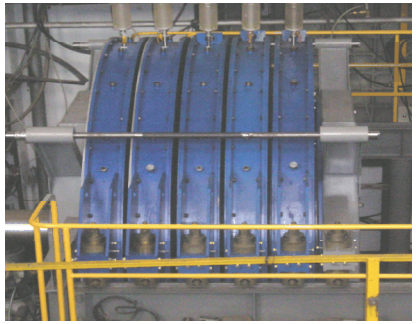
- The LTD cavity is an induction cavity enclosing the pulse-forming network.
- The enclosed capacitors are charged in series and discharged again in series.
- Together with its pulse blocking cores the LTD is nothing else but a one to one transformer. This explain the name tossed by the Russians.



The 1-MA LTD MYKONOS cavity encloses 40 identical bricks.



one brick



1- MA 5 LTD cavity IVA

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Multi-pulsing an LTD inductive voltage adder (Method 1: Triggering a number of cavities and/or bricks per pulse)

- The modular construction of the LTD cavities offer the option of multi-pulsing a Linear Transformer Driver (LTD) Induction Voltage Adder (IVA).
  - The cavity bricks of an LTD can be triggered individually or divided into groups of different numbers to produce a train of pulses of equal output voltage to a diode load. We already proposed this technique in 2001 in a beam weapon report: " Particle Beam Directed Energy for Ship Defense" SAND 2001-3568 (OUO)
  - French researchers in the Centre d'Edude de Grammat already succeeded in multi-pulsing. They double-pulsed first a single LTD cavity and most recently a 10 LTD cavity IVA. (Results will be presented at the 2015 Pulsed Power Conference).
  - This can be tested with our 23 cavity radiographic LTD IVA Ursa Minor.
- A conventional IVA or LIA can of course be multi-pulsed by triggering only part of the cavities per pulse.
  - The main difference between LTD IVA or LIA and a conventional induction device is that all LTD pulses can be designed to be of the same voltage output and equal to the single pulse operation. However, in a conventional IVA or LIA the voltage per pulse would be equal to the sum of the individual cavity voltages simultaneously triggered per pulse.

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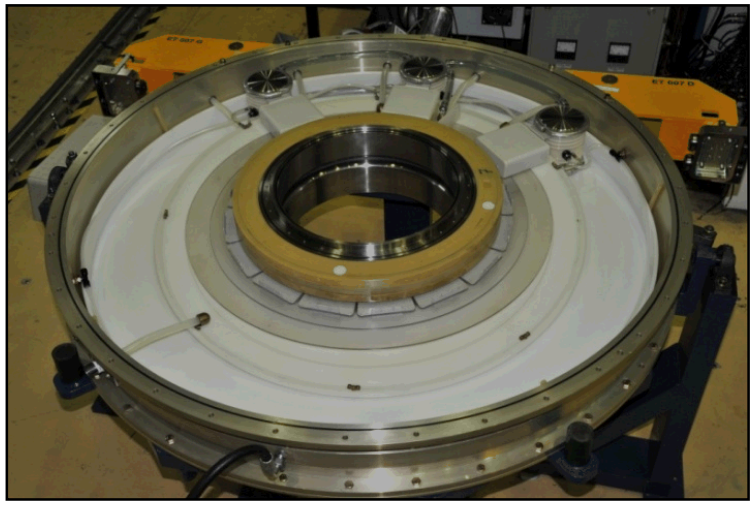
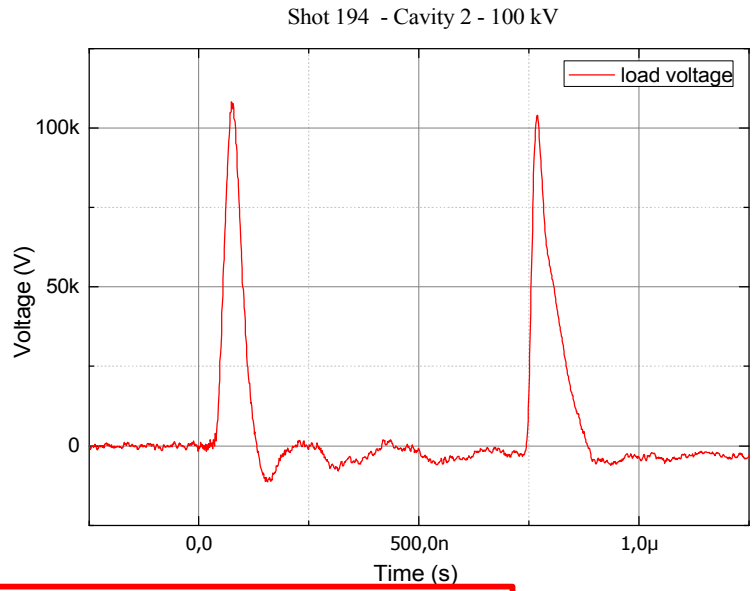
The CEA cavities have been modified to produce two high-voltage pulses

- Bricks triggered at two different times.
- Two pulses obtained on resistive load.
  - 100 kV – 8 kA – 45 ns
- The delay between the two pulses can be adjusted from 200 ns to 2 µs with no change on the 2nd pulse





Results will be presented by CEA staff at the 20th Pulsed Power Conference 2015 in Austin, Texas.

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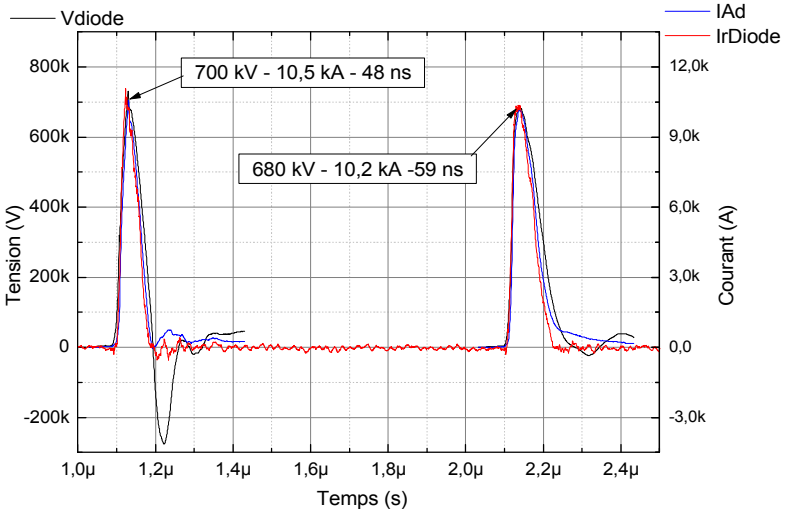
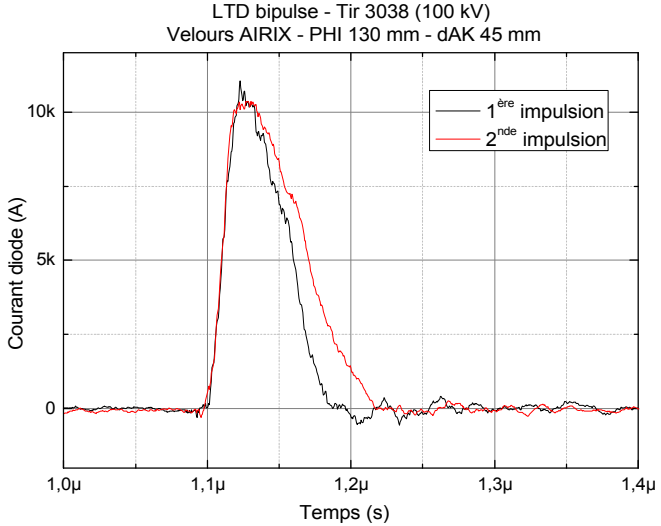
Double- pulsing tests on the 10-cavity accelerator are in progress

- **Two ~ 700 kV pulses were obtained at the load with the CEA accelerator.**
- **As for a single LTD cavity, the delay between the two pulses could be adjusted from 200 ns to 2 µs.**
- **These first results demonstrate that LTD is a versatile architecture for pulse power technology.**



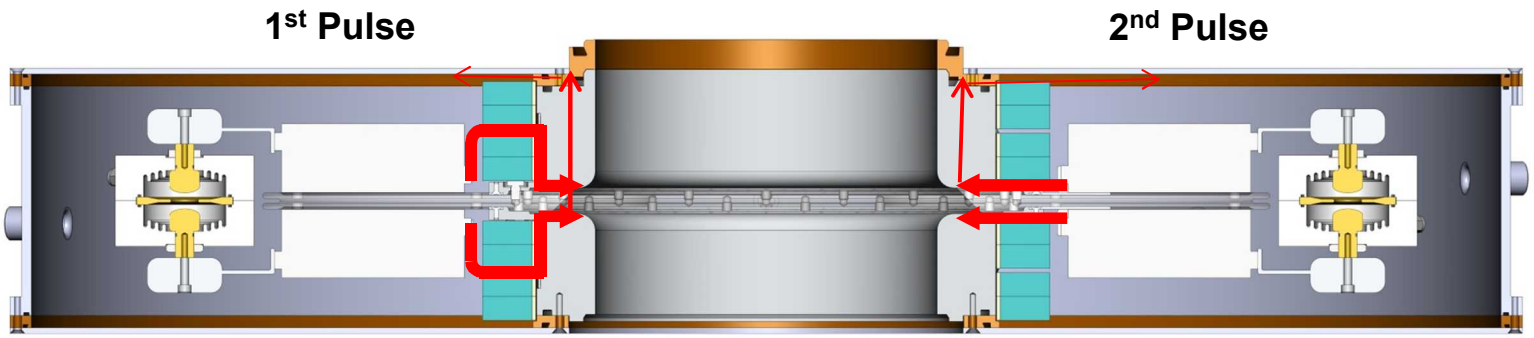


Results will be presented by CEA staff at the 20th Pulsed Power Conference 2015 in Austin.

Double-pulsing method 2: Core Isolation*

- Method # 2 the idea ;The output connection for the first pulse encircles only half of the core material. The cores for the first pulse are sized to saturate at the end of the pulse. The output connection for the second pulse encircles all of the core material. This way, when the second pulse bricks fire, there is unsaturated core material separating the first and second pulse bricks. If designed properly, the first and second pulses should be identical, even with identical drive circuits.

- We have designed and already ordered hardware to allow a demonstration of this pulse method # 2 on an Ursa Minor cavity. This will be the quickest and most affordable way to demonstrate this concept.

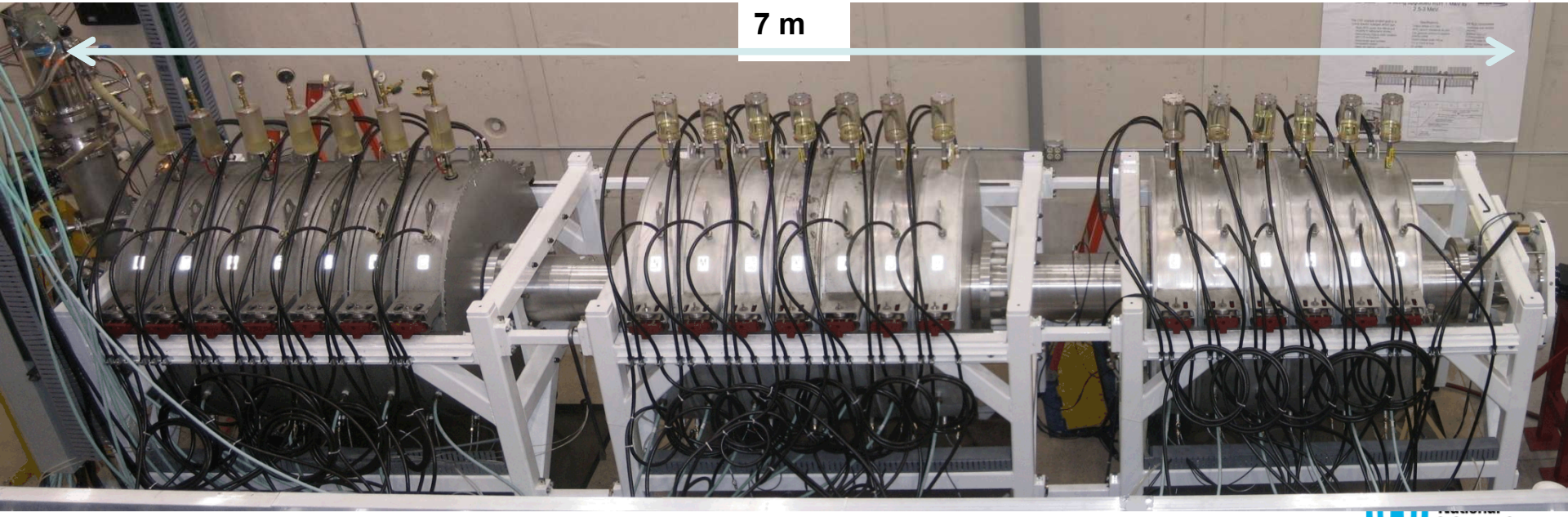


* The method # 2 was first proposed in 2007 in an LDRD Idea proposal by Josh Leckbee

* Engineering design by M. Sceiford

Ursa Minor could be converted into a two pulse injector test bed

- Could provide a test bed for cathode development beginning later this fiscal year.
- Could be used full time for multi-pulse cathode R&D. (method 1 and later method2)
- Availability of extensive plasma diagnostics routinely fielded on RITS
  - High speed optical cameras (single frame and multi-frame)
  - Optical streak cameras
  - Spectroscopy
  - High sensitivity optical fiber arrays



Multi-pulsing a 3-4 MV Square Pulse LTD IVA Injector

- 30 to 40 square pulse LTD cavities connected in series could provide 3 to 4 MV 50 ns or shorter flat top pulses.
- The voltage flat top must be regulated to vary less than ±1%
- The length of the injector voltage adder will be 6 to 8 meters utilizing presently available components.
- We can envisage multi-pulsing the voltage adder. We consider three possible options:
  - Firing half of the cavities per pulse. Then each pulse will be 1.5 to 2 MV.
  - Firing a number of the bricks of all cavities per pulse. Then each pulse could be 3 to 4 MV.
  - Firing half of the cavities and ~half of the bricks per pulse This way we can have a train of four pulses of 1.5 to 2 MV per pulse.
- It is possible to reduce the number of the cavities by the usage of a voltage transformer or by overmatching the diode load. In this case the ringing in the inter-pulse intervals may be a problem.

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Square Pulse LTD: Theory and Experimental Verification

PHYSICAL REVIEW SPECIAL TOPICS - ACCELERATORS AND BEAMS **15**, 040401 (2012)

Square pulse linear transformer driver

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The linear transformer driver (LTD) technological approach can result in relatively compact devices that can deliver fast, high current, and high-voltage pulses straight out of the LTD cavity without any complicated pulse forming and pulse compression network. Through multistage inductively insulated voltage adders, the output pulse, increased in voltage amplitude, can be applied directly to the load. The usual LTD architecture [A. A. Kim, M. G. Mazarakis, V. A. Sinebryukhov, B. M. Kovalchuk, V. A. Vizir, S. N Volkov, F. Bayol, A. N. Bastrikov, V. G. Durakov, S. V. Frolov, V. M. Alexeenko, D. H. McDaniel, W. E. Fowler, K. LeCheen, C. Olson, W. A. Stygar, K. W. Struve, J. Porter, and R. M. Gilgenbach, Phys. Rev. ST Accel. Beams **12**, 050402 (2009); M. G. Mazarakis, W. E. Fowler, A. A. Kim, V. A. Sinebryukhov, S. T. Rogowski, R. A. Sharpe, D. H. McDaniel, C. L. Olson, J. L. Porter, K. W. Struve, W. A. Stygar, and J. R. Woodworth, Phys. Rev. ST Accel. Beams **12**, 050401 (2009)] provides sine shaped output pulses that may not be well suited for some applications like *z*-pinch drivers, flash radiography, high power microwaves, etc. A more suitable power pulse would have a flat or trapezoidal (rising or falling) top. In this paper, we present the design and first test results of an LTD cavity that generates such a type of output pulse by including within its circular array a number of third harmonic bricks in addition to the main bricks. A voltage adder made out of a square pulse cavity linear array will produce the same shape output pulses provided that the timing of each cavity is synchronized with the propagation of the electromagnetic pulse.

DOI: 10.1103/PhysRevSTAB.15.040401 PACS numbers: 84.70.+p, 84.60.Ve

I. INTRODUCTION

The linear transformer driver (LTD) [1,2] is a new method for constructing high current, high-voltage pulsed accelerators. The salient feature of the approach is switching and inductively adding the pulses at low voltage straight out of the capacitors through low inductance transfer and soft iron core isolation. LTD based drivers are considered for many applications including future very high current *z*-pinch inertial confinement fusion drivers like *ZX*, *z*-pinch inertial fusion energy drivers, and x-ray radiography. High currents can be achieved by feeding each core with many capacitors connected in parallel in a circular array. High voltage is obtained by inductively adding many stages in series. In addition to the relative compactness, LTD has a number of very significant advantages compared to the Marx-and-water-line technology. However, the applicability of the LTD drivers could be greatly enhanced if we could change the output pulse shape according to the requirements of the various applications. For instance, the radiographic accelerators would be greatly benefited if the voltage applied to the x-ray diode had a square or even flattop shape. The square pulse LTD cavity described, built, and analyzed in this paper accomplishes exactly that.

The idea of the square pulse LTD is based on the Fourier theorem, which states that any waveform can be reproduced by the superposition of a series of sine and cosine waves. In particular, the constant function $f(x)$ for $0 \leq x \leq \pi$, defined as

$$f(x) = \frac{\pi}{4}, \tag{1}$$

can be reproduced as follows:

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Square Pulse LTD (continue)

The idea of the square pulse LTD is based on the Fourier theorem, which states that any waveform can be reproduced by the superposition of a series of sine and cosine waves. In particular, the constant function $f(x)$ for $0 \leq x \leq \pi$, defined as

$$f(x) = \frac{\pi}{4}, \tag{1}$$

can be reproduced as follows:

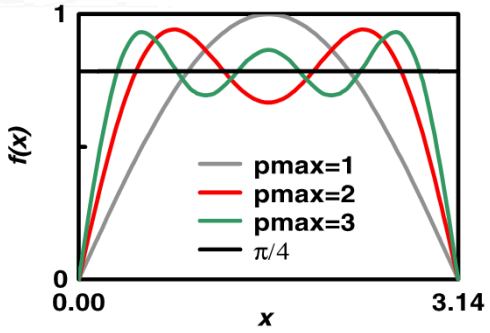
$$f(x) = \sum_{p=1}^{p_{\max}} \frac{\sin(2p-1)x}{2p-1}, \tag{2}$$

where $p_{\max} = \infty$. Figure 1 demonstrates the difference between Eqs. (1) and (2) depending on $p_{\max}$. (next viewgraph)

For $p_{\max} = 2$, Eq. (2) can be represented in the form

$$f_2(x) = \sin x + \frac{1}{a}\sin 3x, \tag{3}$$

In order to analytically evaluate the output of the square pulse LTD circuit we make the following two approximations:



IG. 1. The functions $f(x)$ given by Eq. (2) for $p_{\max} = 1$ to 3 ompared with $f(x) = \pi/4$.

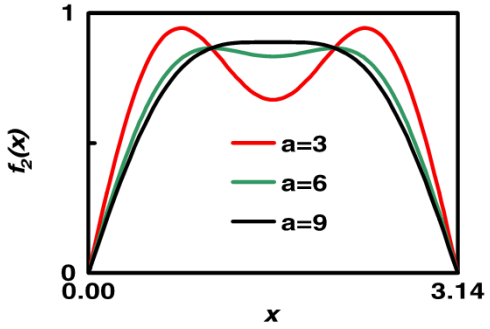
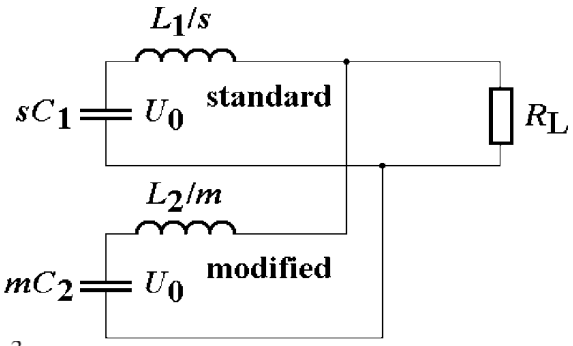


FIG. 2. The function $f_2(x)$ at $a = 3, 6, 9$.

$$\alpha \sim 1.65\frac{s}{m} \sim \frac{I_1}{I_2}$$



Here ***S*** is the number of standard fundamental frequency bricks and ***m*** the number of modified bricks . We assume that ***s>m*** then:

$$\sqrt{\frac{L_1/s}{sC_1}} = \frac{1}{s}\sqrt{\frac{L_1}{C_1}} = \frac{1}{s}\rho_1 \approx R_L$$

First approximation

$$\rho_1 = \sqrt{\frac{L_1}{C_1}}$$

The circuit frequency of the modified brick of the 3rd harmonic must be 3 times that of the standard brick, resulting in:

$$\sqrt{L_1 C_1} \sim 3\sqrt{L_2 C_2}$$

$$L_1 \sim L_2$$ **Second approximation**

Then $$C_2 \sim \frac{1}{9}C_1$$

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Square LTD Cavity Results with only Fundamental and 3rd Harmonic

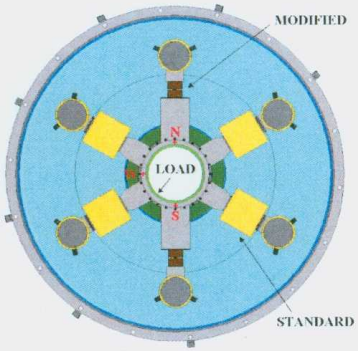
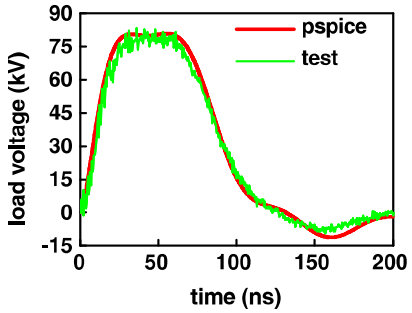
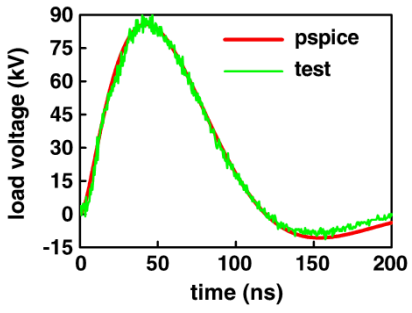


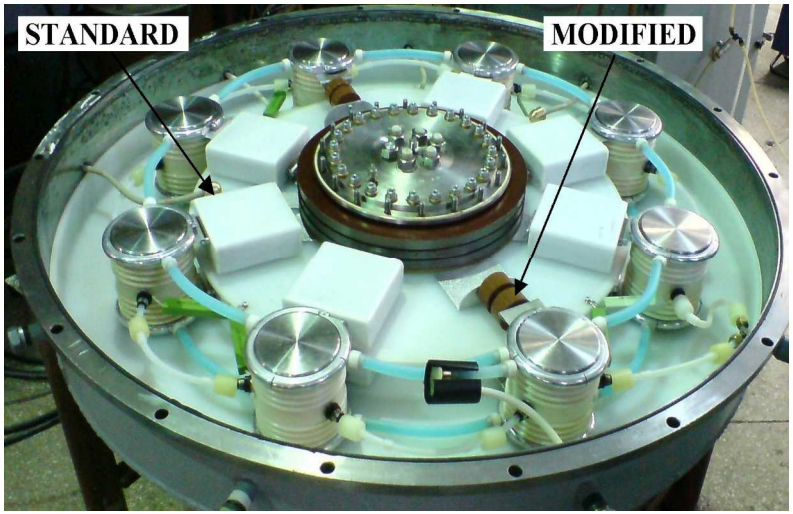
FIG. 4. (COLOR) Square pulse LTD with 4 standard and 2 modified bricks. The outer diameter of the cavity is 140 cm. The location of the cavity core is indicated in dark green.



Recorded and simulated data. Only fundamental and third harmonic. R_L=1.6 Ohm



Recorded and simulated load voltage with only the standard bricks



Square pulse cavity LTD with 6 fundamental (standard) and 2 third harmonic (modified) bricks.

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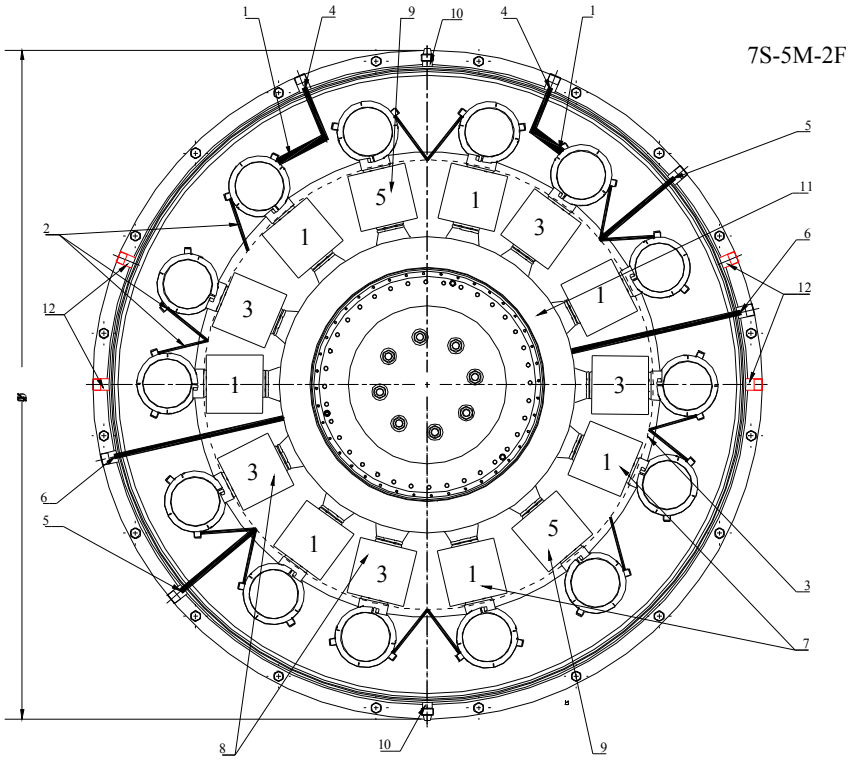
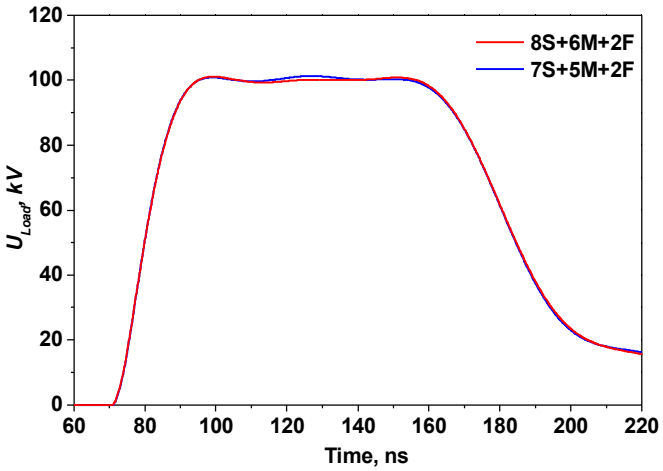
We have already built a LTD cavity with 3rd and 5th harmonic. We are awaiting the GA capacitors to start testing it.





Simulation results for two brick variations.

LTD cavity top view with 7 fundamental (1), 5 third harmonic (3) and 2 5th harmonic bricks.

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Required tolerances on the LTD components to achieve ± 1% voltage flat top variation.

- We are currently evaluating the LTD component manufacturing precision and exploring compensation techniques to achieve the required voltage pulse top flatness at the end of a 30 or 40 cavity voltage adder. Namely:
  - Switch jitter
  - Capacitor value accuracy
  - Inductance of each brick
  - Trim the capacitance and inductance of each cavity brick to achieve the required voltage pulse at the end of 30 to 40 cavity voltage adder.
  - Compensate the capacitance and inductance variation of the bricks by varying the charge voltage of each harmonic brick.
  - Make the first half of the cavities to ramp the voltage up and the second half to ramp down so the superposition of both to produce the required perfect flat top pulse.
  - Other possible options

Switch Jitter effect on the voltage flat top of the square pulse (work in progress)

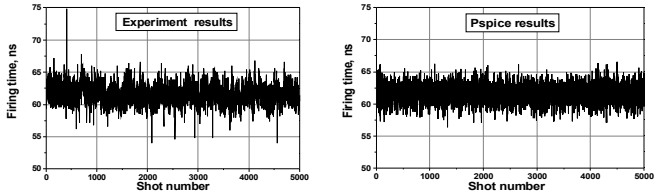

Fig. 3. Scatter of the switch firing (a) in the experiment, and (b) in the simulation at σ_1 = 1.49 ns (b).

The top of the output pulse of the Square Pulse LTD with three harmonics could be inclined as desired by shifting the firing of the bricks generating one of the harmonics. An example is shown in Fig. 7, which presents the load voltage traces simulated in 400 runs in the case the mean firing time of the standard bricks is shifted for 3 ns before all other bricks.

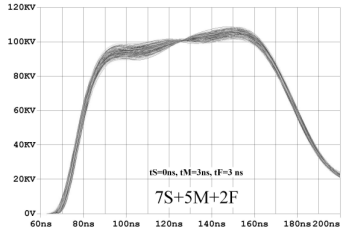

Fig. 7. Rising-top output pulse simulated in 7S+5M+2F configuration. The mean firing time of the standard bricks in these runs is shifted for 3 ns before all other bricks

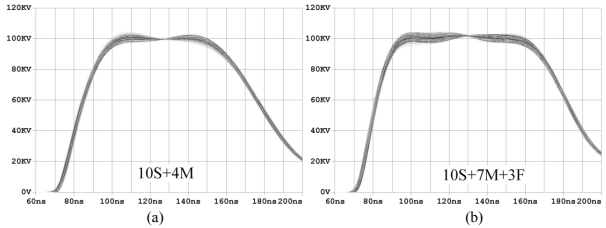

Fig. 5. Load voltage pulses simulated in 400 runs by taken into account the switch statistics in LTD's with (a) two, and (b) three harmonics.

The comparison of the load voltage traces simulated in 400 runs in 8S+6M+2F and 7S+5M+2F configurations is given in Figs. 6(a) and 6(b). The statistical distortion of the pulse top is almost the same, though in 8S+6M+2f it is slightly less because of larger total capacitance of the capacitors.

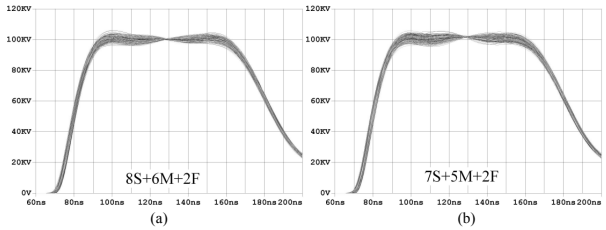

Fig. 6. Load voltage traces simulated in 400 runs in (a) 8S+6M+2F, and (b) 7S+5M+2F configurations.

Data from: "V .M. Alexeenko, S. S. Kondratiev, S. V. Vasiliev, V. A. Syneebryukhov, A. A. Kim, M.G. Mazarakis, J. Leckbee, M. L. Kiefer Proceeding of the 18h International Symposium on High Current Electronics, September 21-26, 2014, Tomsk, Russia, UDC: 621.3"

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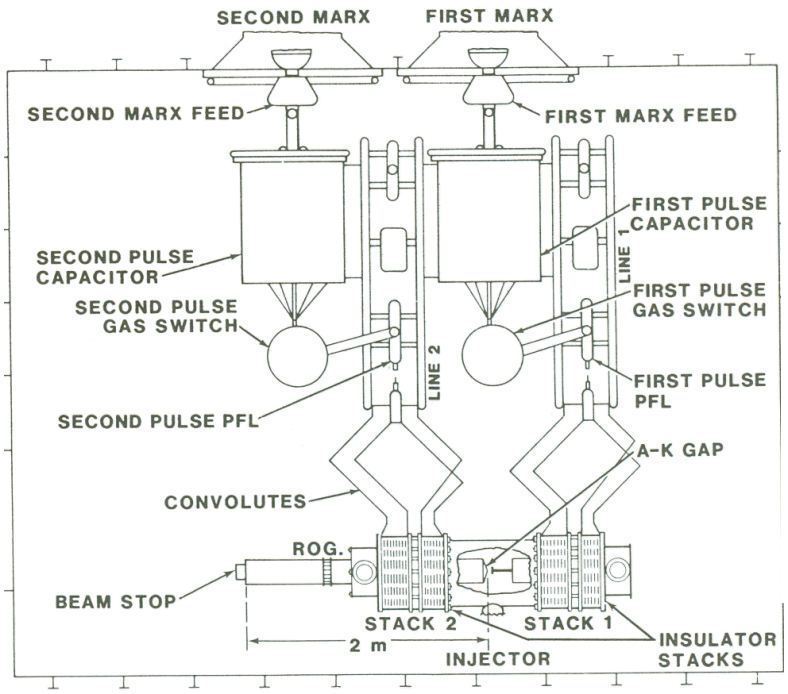
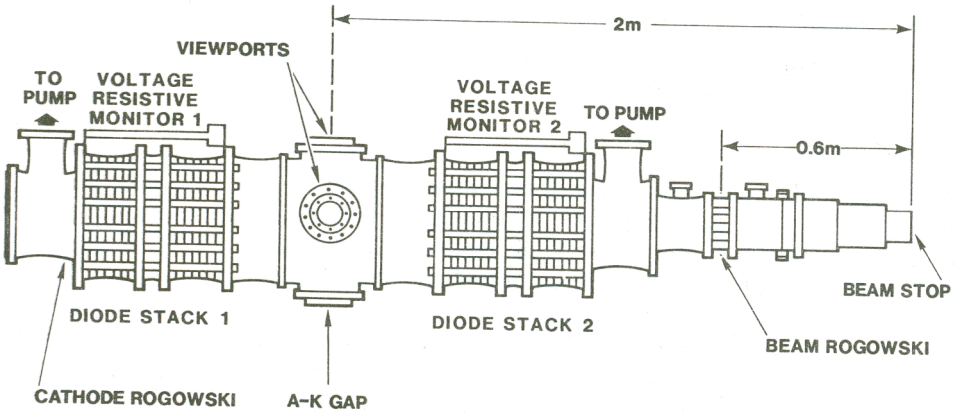
The Square Pulse LTD with 5th Harmonic Injector could in principle meet most of the wishes of the Radiographic Community.

- (a) Number of pulses: one initially; upgradable to 2, 3, or 4.✔
- (b) Inter-pulse time: variable.✔
- (c) Electron-beam current: 2 kA.✔
- (d) Peak voltage: at least ~2 MV.✔
- (e) Voltage-pulse shape: flat-top square pulse.✔
- (f) Voltage variation over the flat top: ± 1%.✔
- (g) Voltage-pulse rise and fall times: ~25 ns.✔
- (h) Voltage-pulse width: ~50 ns✔

We have double-pulsed the RIIM (RADLAC) LIA injector with a magnetically immersed foilless electron diode.



RIIM double pulse accelerator



RIIM beam line

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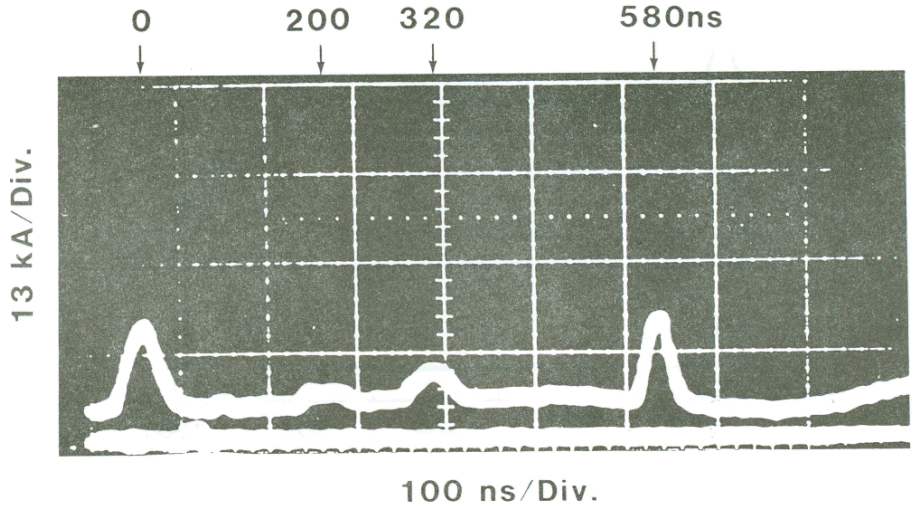
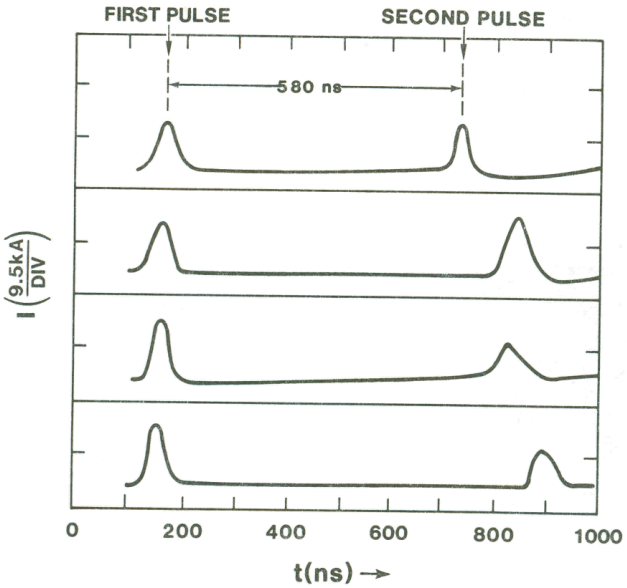
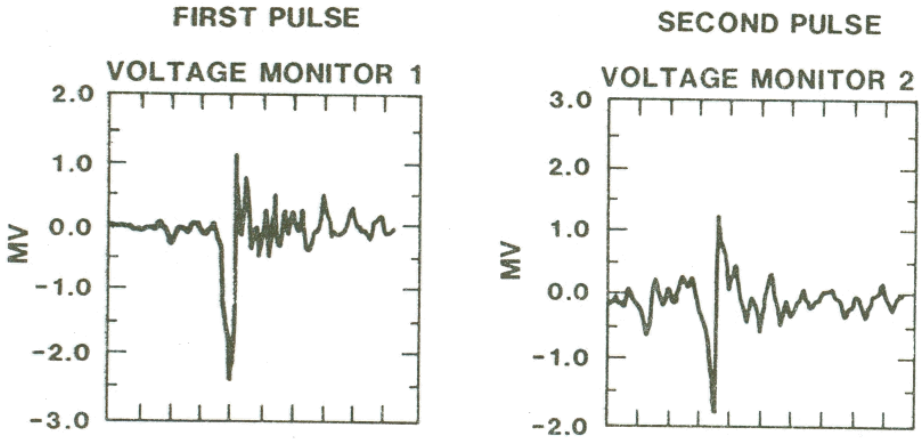
Double pulse experiment results

Beam currents



Beam current





Diode Voltage

M. G. Mazarakis *et al.,* Applied Physics 64 part I pp. 4815, (1988)

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We have designed and operated several high voltage electron diodes .

- We have designed and built magnetically immersed foilless diodes for the LIAs ; RADLAC II, RIIM, and HERMES III and SABER IVAs for radiography.

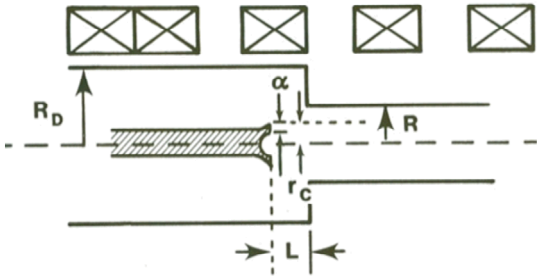
- We have also built planar diodes for Sandia's Recirculating Linear Accelerator (RLA) and have done a number of low emittance early diode studies for the radiographic DARHT I accelerator.

- The following viewgraphs show some examples.

BACK UP SLIDES

Foilless diodes.

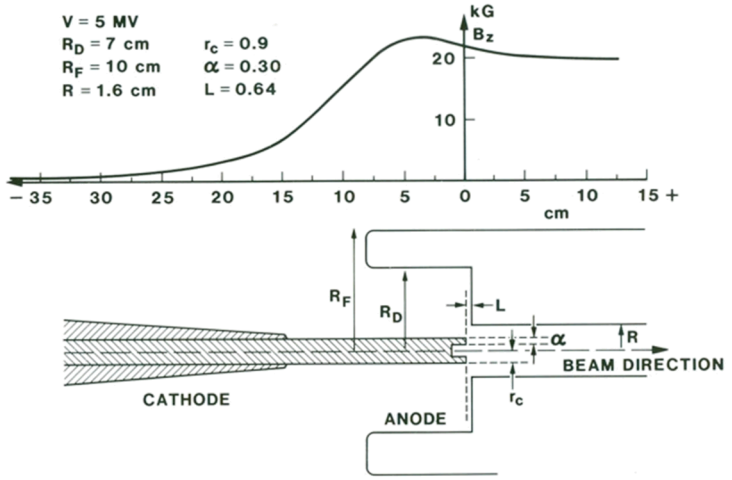
IBEX FOILESS DIODE PARAMETERS



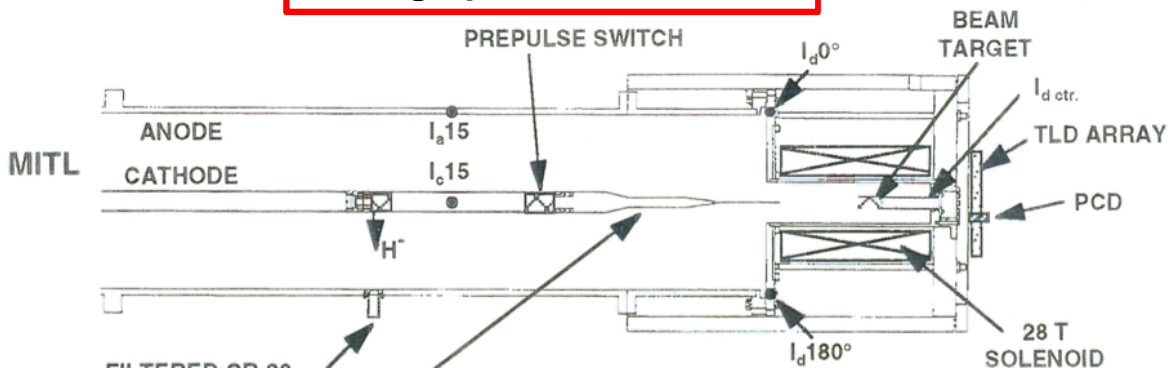
$16 \geqslant B_z \geqslant 6$ kG
R = 2.9 cm
r_c = 1.3 cm (variable)
α = 2 mm (variable)
L = 3.2 cm (variable)
R_D = 7.3 cm

V_D = 4 MV
I_B = 20-30 kA
Z_D = 95-130 Ω
Z_L = 195 Ω

RADLAC II Foilless diode



Radiographic foilless diode



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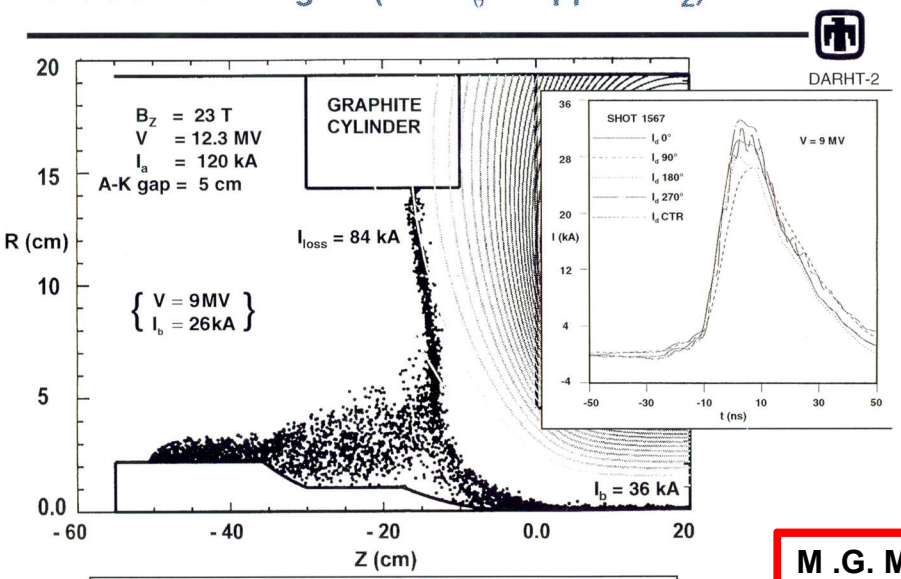
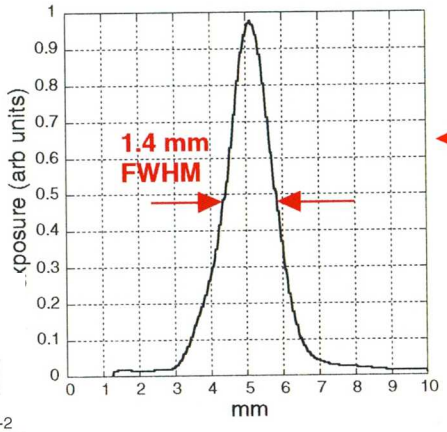
Radiographic foilless diode results.

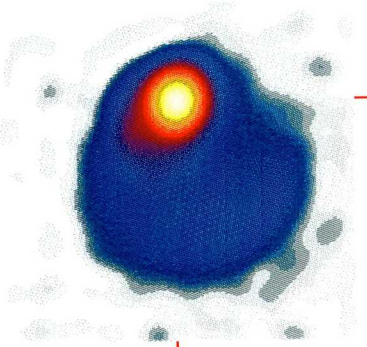
The sheath electrons are diverted to the anode at the transition region (self B_θ to applied B_Z)

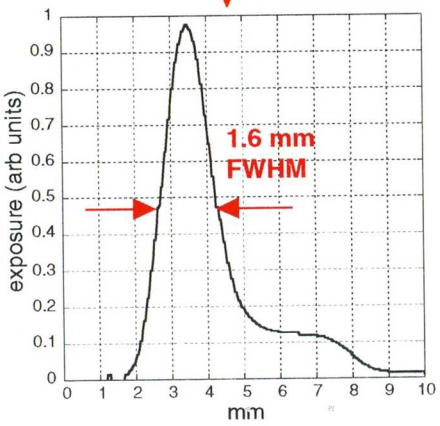


Measured currents agree with TWOQUICK predictions.



time integrated X-ray pinhole camera image deconvolution





M .G. Mazarakis *et al.*, Applied Physics Letters, 7, pp. 832 (1996)

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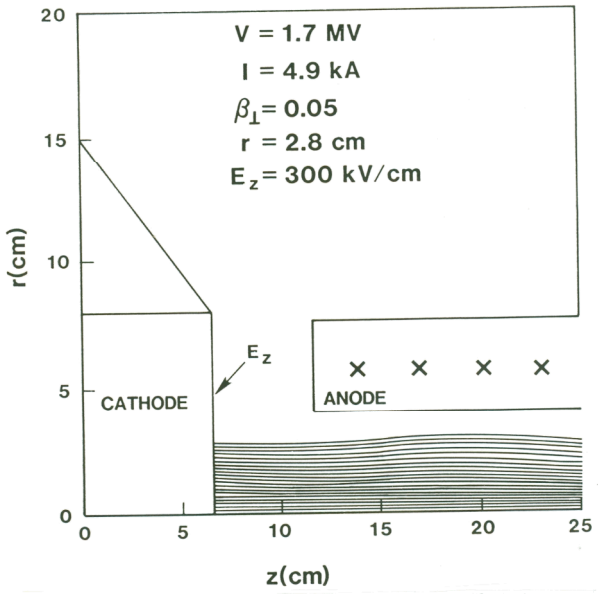
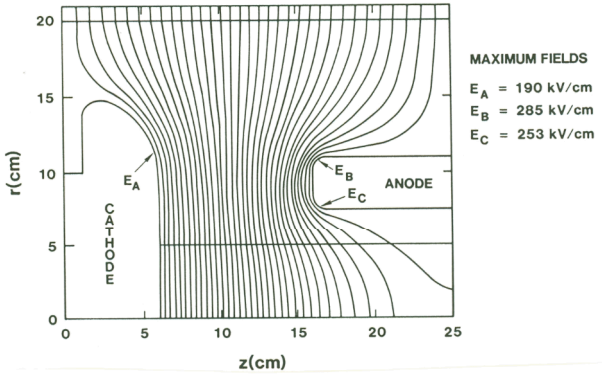
We have experience in designing and operating low emittance, low current velvet diodes for LIA injectors.

ELECTRON TRAJECTORIES

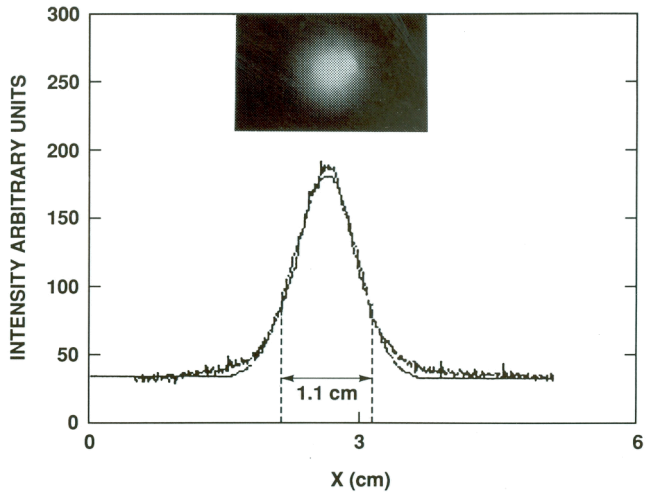


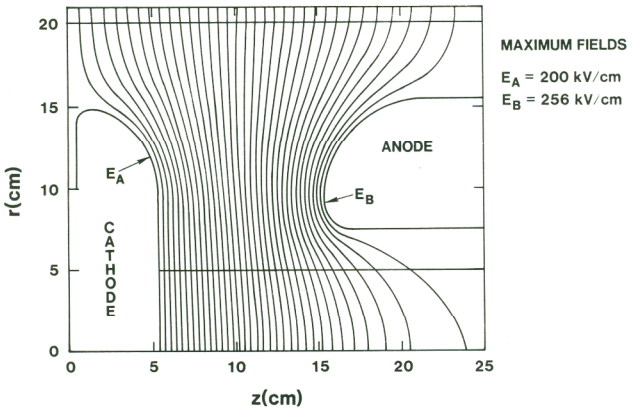
2. Non-immersed foilless diodes can produce very cold beams.

EQUIPOTENTIAL PLOT 1.7 MV ANODE VOLTAGE



3. Equipotential plots obtained with the JASON code. The cathode shape is optimized to reduce the electric field stresses on the surface.





Both the anode and cathode surface shapes are optimized for minimum electric field stresses.

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Back- shot of RADLAC electron beam

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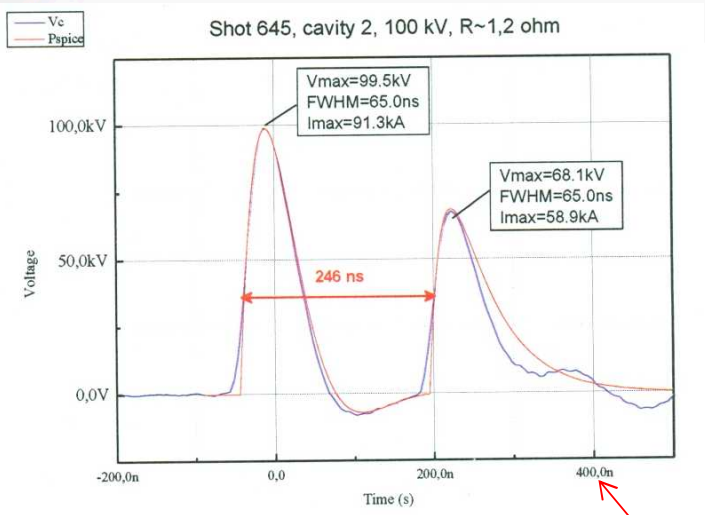
The Centre d' Etude de Grammat experimental results.



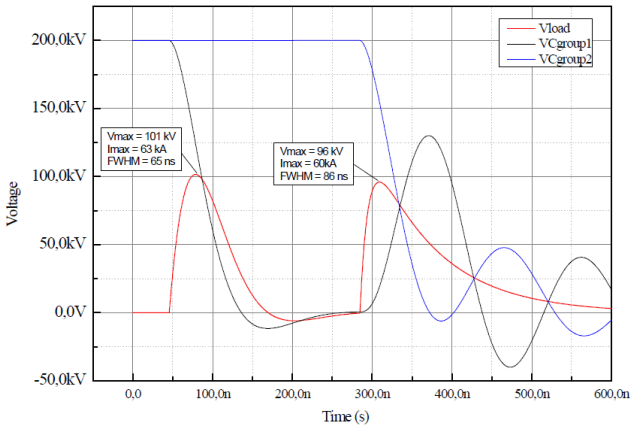
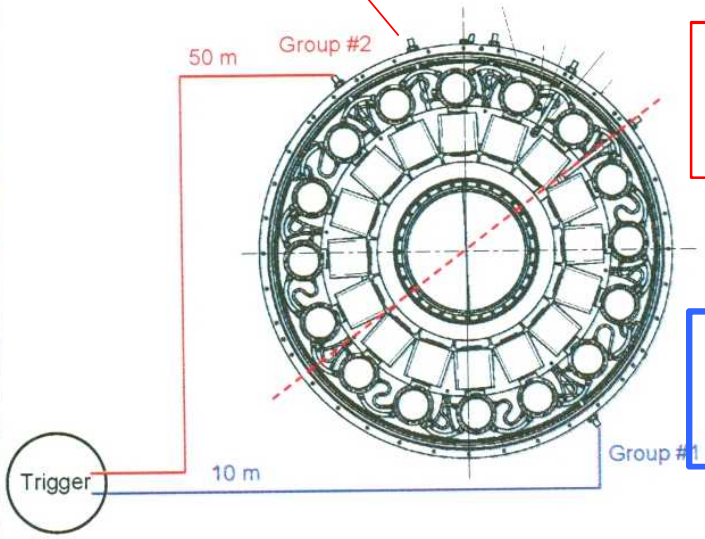


Figure 11. Simulation of a two pulses test with a first group of 6 bricks and a second group of 10 bricks.



The two pulses can be of equal amplitude if for the first pulse we trigger less number of bricks

M. Toury, et. al., "Two pulses tests with a single LTD cavity," in Proc. Beams Conf. 2012.

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