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University Center of Excellence for Photovoltaics Research and Education: Annual Report

A. Rohatgi, G. Crotty, L. Cai, P. Sana, A. Doolittle,
M. Ropp, T. Krygowski, and S. Narasimha

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ABSTRACT

This is the second annual report since the University Center of Excellence for Photovoltaics Research and Education was established at Georgia Tech. The major focus of the center is crystalline silicon, and the mission of the Center is to improve the fundamental understanding of the science and technology of advanced photovoltaic devices and materials, to fabricate high-efficiency cells, and develop low-cost processes, to provide training and enrich the educational experience of students in this field, and to increase U.S. competitiveness by providing guidelines to industry and DOE to achieve cost-effective and high-efficiency photovoltaic devices. This report outlines the work of the Center from July 1993-June 1994.

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SUMMARY

High efficiency and low cost are the keys to large scale applicability of photovoltaic systems. Current cost of PV modules is about $4/watt, which needs to come down by a factor of 2 to be competitive for utility peak shaving, and a cost reduction of about a factor of 3-4 will be necessary for base load applications. No PV material or technology has yet met the cost and efficiency targets simultaneously to produce electricity at a rate of 6-10¢/kWh. As research and development continue on various materials, it is becoming increasingly obvious that crystalline silicon will remain the most reliable and widely used PV material for many years to come. In 1994, out of the 25.6 MW of PV modules sold by companies in the U.S., 23.2 MW came from single and multicrystalline silicon. The remaining 2.4 MW was produced from thin film panels, primarily amorphous silicon.

In spite of the significant progress made in single crystalline and multicrystalline silicon solar cell efficiencies in the last decade, a large gap still remains between the cost of generating power from PV and fossil fuels, as well as between the current and theoretical efficiencies of solar cells made from silicons. This is why basic research toward low-cost, high-efficiency crystalline silicon cells is important for PV to become a cost-effective and environmentally clean source of electrical energy for the next generation.

The objective of single and multicrystalline silicon materials and device research at Georgia Tech is two-fold. One track pursues basic understanding of the efficiency limiting defects and mechanisms that affect material quality and device performance. The second track seeks to develop processes, cell designs, and methodologies that will enhance material quality, reduce cell processing time and cost, and lead to higher cell efficiencies.

We have made significant progress toward understanding the lifetime and efficiency limiting

mechanisms in cast and sheet multicrystalline (mc-Si) materials. This understanding has enabled process optimization to achieve higher quality surface passivation, longer bulk carrier lifetimes, and higher efficiency cells on single crystal and multicrystalline silicon materials.

Aluminum and phosphorus gettering are important and highly compatible with multicrystalline silicon cell processing. A detailed investigation of quality enhancement techniques such as aluminum and phosphorus diffusion for defect and impurity gettering was conducted on several promising multicrystalline silicon materials. These defect passivation techniques were found to be quite beneficial in enhancing the performance of multicrystalline silicon cells. However, these effects were found to be material specific. It was found that for multicrystalline silicon from Sitix Corp., 930°C is the optimum temperature for phosphorus diffusion. In order to take advantage of intense phosphorus gettering without the harmful effects of an emitter dead layer, a deep phosphorus diffusion at 930°C was performed followed by a partial etch-back of the n^+-region. It was found that this treatment is optimum for emitter formation in multicrystalline silicon cells, and results in high bulk lifetime without significant penalty from the heavy doping effects. The optimum aluminum treatment for Sitix multicrystalline silicon solar cells included 1.2 μm thick Al deposition followed by 850°C, 35 min drive-in. This resulted in 1.4% increase in absolute cell efficiency primarily due to Al gettering-induced bulk lifetime enhancement. It was shown that the Al treatment forms a back surface field (BSF) and improves bulk lifetime but reduces back surface reflection because of the rough Al-Si alloyed back surface. Beneficial effects of Al on silicon solar cell performance were found to be material specific. Float-zoned (FZ) cells showed less than 1% increase in cell performance, exclusively due to the Al back-surface field effect with little or no gettering and passivation. Heat- exchanged method (HEM) cast multicrystalline silicon cells showed about 1.6% increase in absolute cell efficiency primarily due to Al gettering-induced diffusion length enhancement. Finally, aluminum diffusion on the back side increased the edge-defined film-fed

growth (EFG) cell efficiency by 1.7% (absolute) due to Al process-induced gettering.

During this study it was found that defect passivation by forming gas-anneal (FGA) is also highly material specific. In contrast to the EFG cells, the forming gas treatment had virtually no effect ($< 5\%$) on the Sitix and HEM cast multicrystalline silicon cells. This is probably because higher quality cast mi-Si materials do not have enough of those defects that can benefit from hydrogen passivation. However, in materials like EFG and Astropower-Si thin film, which consist of a high concentration of active dislocations or grain boundaries, FGA showed a very significant effect on bulk diffusion length and cell performance.

After developing and optimizing gettering and passivation techniques, we integrated them into a process sequence that does not increase the cell fabrication cost by much. This process starts with intense phosphorus diffusion, followed by an etch-back. Then 1 μm thick aluminum is evaporated, followed by a three-step drive-in: the first five minutes in oxygen at 850°C to grow a passivating oxide, next, thirty minutes in nitrogen at 850°C for aluminum gettering and BSF, and finally a two-hour forming gas anneal (FGA) at 400°C. Then the grid pattern was defined by photolithography and, finally, the cells were capped with a two-layer antireflection (AR) coating. This advanced process sequence gave a record high efficiency for mc-Si of 17.8%. It should be noted that through this study, impressive progress has been made in multicrystalline silicon cells with an efficiency approaching 18%, which is less than 1% shy of CZ cells and about 1.5% shy of float zoned (FZ) cells, when fabricated without texturing.

After in-depth characterizations, cell model calculations were performed by ignoring the grain boundary effects, but using a measured effective excess lifetime in the cell. A good correlation was found between the measured and calculated cell parameters of the high- efficiency multicrystalline silicon cells. Model calculations were extended to outline an approach toward achieving greater than 20% efficient multicrystalline cells, which emphasizes the need for surface texturing, reduced back-

surface recombination velocity, and reduced base resistivity without paying too much penalty for lifetime.

Significant progress was made during the past year on the development of plasma enhanced chemical vapor deposition (PECVD) of SiO_x and SiN_x films for surface and bulk defect passivation, in addition to AR coatings. We demonstrated that the (PECVD) SiO_2/SiN AR coating gives much greater improvement in cell parameters, when compared with thermally evaporated MgF_2/ZnS coatings, for cells without thermal oxide passivation. For cells that have thin thermal oxide passivation, the improvements in efficiency are comparable for the two AR coatings. We have also demonstrated that thin SiO_2 (~100Å) deposited on single crystal silicon by direct PECVD at 250°C on high resistivity wafers, and annealed using an optimized rapid thermal anneal (RTA) in forming gas at 350°C, results in very low surface recombination velocity (<2cm/s). This low temperature process also resulted in very high effective carrier lifetimes (>5ms) and low interface state density (D_{it}), in the range of 1-4x10^{10} $cm^{-2}eV^{-1}$ near the midgap of silicon. The best D_{it} value achieved in this study was 1.1x10^{10} $cm^{-2}eV^{-1}$. This is the lowest D_{it} value reported to date for PECVD oxides.

It is shown for the first time that plasma-enhanced chemical vapor deposition (PECVD) passivation, which involves low-temperature PECVD of ~100 Å SiO_2 and ~600 Å SiN followed by photoassisted anneal, is very effective for both surface and bulk defect passivation in multicrystalline-Si materials. It is found that PECVD coatings can increase the effective recombination lifetime by a factor of 2-10 depending upon the multicrystalline material. The bulk and surface passivation effects were quantified and decoupled by a combination of internal quantum efficiency measurements and computer modeling. The PECVD passivated OTC multicrystalline solar cells from Osaka Titanium Corp. (OTC) showed an increase in bulk lifetime from 10 to 20 μs, and a decrease in surface recombination velocity from 2x10^5 to 5x10^4 cm/s.

The effective surface recombination velocity (S_{eff}) at the PECVD. SiQ -Si interface was

The effective surface recombination velocity (S_{eff}) at the PECVD. SiO_2-Si interface was measured by PCD method in conjunction with the bias voltage via transparent ITO gates. A theoretical analysis based on the measured $D_{it}(E)$ distribution in the band gap was performed to obtain S_{eff} as a function of the surface band bending, from which the electron and hole capture cross sections for the PECVD Si_2-Si interface states were estimated to be $\sigma_{nD}=4X10^{-15}$ cm^2, $\sigma_{pD}=1X10^{-17}$ cm^2, $\sigma_{nA}=3X10^{-17}$ cm^2, and $\sigma_{pA}=3X10^{-16}$ cm^2. Model calculations were extended further to investigate the relationship between S_{eff}, Q_{ox}, D_{it}, and injection level. It was found that Q_x should be roughly 10 times larger than the midgap D_{it} value in order to reduce S_{eff} below 10 cm/s for 5 Ω cm (100) p-type Si. These results prove the effectiveness of PECVD SiO_2 for passivation of mi-Si surfaces and its application for devices like solar cells.

A combination of rapid thermal processing (RTP) and PECVD coatings was used to reduce cell fabrication cost and time. By developing an RTP temperature/time cycle consisting of an *in-situ* anneal for simultaneous front and back diffusion with suitable τ_b and J_o, silicon solar cell efficiencies of ~17% and diffusion lengths > 200 μm were achieved on FZ without any furnace treatment. Use of low temperature PECVD SiN/SiO_2 coatings further speeds up the process in addition to providing bulk defect and surface passivation in conjunction with excellent antireflection properties. The RTP/PECVD process resulted in cell efficiencies of 16.4% on Czochralski silicon, 14.9% on dendritic web, and 14.8% on multicrystalline silicon. We are currently trying to incorporate screen-printed contact technology as an alternative to photolithography to reduce the cell fabrication time to less than two hours. The combination of RTP, PECVD, and screen-printing will make the process extremely rapid and industrially attractive.

Other major accomplishments include the establishment of close industry interaction, and development of state-of-the-art characterization and testing facilities. We have also developed powerful and user-friendly modelling capabilities to optimize any region of the cell, in addition to

designing high efficiency solar cells and PV systems. We have established two separate solar cell fabrication laboratories that routinely produce cell efficiencies in the range of 18-21% on single crystal FZ silicon. The above research has resulted in about 50 technical papers and three patents (filed) in the last two years.

In the area of education and training, we have completed the establishment of the educational support program (ESP) lab and have started providing hands-on training to undergraduate and graduate students. We have also developed a three credit hour course on solar cells, which is taught once a year and covers PV materials and devices, efficiency limiting mechanisms, modelling, design and fabrication of silicon cells.

In summary we have made record high-efficiency silicon cells in a number of categories, developed and optimized RTP/PECVD technology for low-cost high-efficiency cells, established state-of-the-art characterization, modelling and silicon cell fabrication facilities, established the ESP lab, developed laboratory and classroom courses for training undergraduate and graduate students, and last but not least, establish a good working relationships with the PV industry and national laboratories.

EXECUTIVE SUMMARY

In spite of progress made in the efficiencies of single-and multicrystalline silicon solar cells in the last decade, the cost of generating power from photovoltaics is still higher than from fossil fuels, and the actual and theoretical efficiencies of solar cells made from silicon continue to differ. For these reasons, basic research such as that carried out at Georgia Tech toward low-cost, high-efficiency crystalline silicon cells is important so that photovoltaics can become a cost-effective source of electricity that is also environmentally clean.

This annual report covers our work from July 1993 to June 1994, during which time record-high-efficiency solar cells were made, rapid thermal processing/plasma-enhanced chemical vapor deposition technology for low-cost, high-efficiency cells was optimized, state-of-the-art characterization, modelling, and silicon cell fabrication facilities were established, an educational support program laboratory was established, laboratory and classroom courses for training graduate and undergraduate students were developed, and a good working relationship was established with industry and the national labs.

More specifically, significant progress was made during this year toward understanding the lifetime- and efficiency-limiting mechanisms in cast and sheet multicrystalline materials, leading to an optimization of the process to achieve higher quality surface passivation, longer bulk carrier lifetimes, and higher efficiency cells on single- and multicrystalline silicon materials.

The report describes a detailed investigation of quality enhancement techniques, which were found to be beneficial in enhancing the performance of multicrystalline silicon cells, but were quite material specific. A review is given of how gettering and passivation techniques were optimized and integrated into a process sequence that does not greatly increase the cost of cell fabrication. Cell model calculations were made and extended to outline an approach toward achieving greater than 20% efficient multicrystalline cells that emphasizes the need for surface texturing, reduced back-surface recombination velocity, and reduced base resistivity without paying too much penalty for lifetime.

The progress made on developing plasma-enhanced chemical vapor deposition is described, and its passivation is for the first time shown to be effective for surface and bulk defect passivation in multicrystalline silicon materials.

Included is a report on how a combination of rapid thermal processing and plasma-enhanced chemical vapor deposition coatings was used to reduce the time and cost of cell fabrication. Other accomplishments outlined here are a close interaction with industry, development of state-of-the-art testing and characterization facilities, development of powerful, user-friendly modelling capabilities to optimize any region of the cell, and establishment of two solar cell fabrication laboratories capable of routinely producing cells with efficiencies of 18-21% on single-crystal FZ silicon. This research has resulted in two patents and about 50 technical papers in the last two years.

CHAPTER 1. INTRODUCTION

This is the second annual report since the inauguration of the University Center of Excellence for Photovoltaics Research and Education (UCEP) at Georgia Tech. The major focus of the UCEP at Georgia Tech is crystalline silicon. The mission of the Center is to improve the fundamental understanding of the science and technology of advanced Photovoltaic devices and materials, to fabricate high-efficiency cells and develop low-cost processes, to provide training and enrich the educational experience of students in this field, and to increase U.S. competitiveness by providing guidelines to industry and DOE for achieving cost-effective and high efficiency PV devices.

These objectives are to be accomplished through a combination of research and education. In addition to teaching solar cell courses and providing practical training to students at Georgia Tech, a new Educational Support Program (ESP) laboratory has been built from scratch. This lab will support university-level educational PV programs in the nation through collaboration and technical assistance. The fabrication laboratory will provide a baseline capability to fabricate 18%-20% efficient silicon solar cells on single crystal float-zoned (FZ) wafers. The fabrication laboratory will fabricate silicon solar cells according to run sheets and materials submitted by other universities. The second major objective of this program is to conduct basic and applied research to advance the science and technology of silicon solar cells and materials. This work is expected to assist the PV industry in cost-effective development of silicon solar cells and give the USA a competitive edge in the field by setting the pace and trajectory of research and development. This program will produce well-trained graduate and undergraduate students to continue the much-needed development of cost-effective and high-efficiency PV devices. Research thrusts involve development and optimization of cost-effective processes for use in the fabrication of solar cells, gettering and passivation of impurities and defects, modeling and design of high efficiency cells, and fabrication and testing of high-

efficiency one-sun cells on monocrystalline and multicrystalline silicon substrates. Major research milestones at the end of the second year include (a) fabrication of high-efficiency cells on low-cost multicrystalline cells with a target efficiency of 17%, (b) fabrication of single crystal silicon cells with target efficiency of 22%, (c) development of high- efficiency, rapidly processed RTP/PECVD cells and (d) publication of three journal articles.

Photovoltaic education milestones were to establish the ESP lab to assist other university and industry PV programs in the USA, provide national focus for silicon PV research, establish a baseline process which will consistently produce > 18% efficiency cells on FZ silicon in the ESP lab, document run sheets, teach a course on solar cells, and provide hands-on training to graduate and undergraduate students in fabricating high efficiency silicon solar cells.

A number of faculty members from various academic units, including ECE, MSE, ME, ChE, Chemistry and Physics have contributed to the success of this program. In addition to the faculty members, a large number of talented research engineers have also made contributions to the PV program, and most of all 12 Ph.D. students and some undergraduate students and visiting scholars have also made significant contributions to the PV research at the Center.

The Center has established state-of-the-art facilities for PV materials and device characterization and has all the necessary tools to troubleshoot, test and analyze solar cells. Modelling and design are very important components of our PV program. To add depth to our research we have developed and assembled a library of 12 user-friendly computer models to design and analyze various regions of solar cells. For example, using these models we have designed and optimized AR coatings, surface texturing, SRV, grid patterns, bulk resistivity and lifetime, in addition to designing and fabricating high- efficiency cells.

The most difficult aspect of this program was to establish and operate a silicon solar cell fabrication facility. We now have two complete fabrication laboratories -- one is exclusively for

research and the other is for education, training and research. This program provides the opportunity for students and scientists to conduct theoretical and experimental research and a mechanism for technology transfer to the PV industry.

Significant progress was made last year in the area of research and education in photovoltaics. This report summarizes the technical accomplishments. Chapter 2 describes modeling, processing and characterization of cast multicrystalline silicon solar cells. Attempts were made to quantify and improve the fundamental understanding of the beneficial effects of oxide passivation, Al diffusion, and forming gas anneal, which resulted in the fabrication of a record high 17.8% efficient cell on Oseka Titenium Corporation (OTC) multicrystalline silicon, in addition to cell efficiencies in the range of 16-17 % on a number of other multicrystalline silicon materials. Accomplishments on single crystal include fabrication of ~20% efficient flat cells and ~21% efficient textured monocrystalline cells. These results are described in Chapter 3. The development of a novel PECVD SiN/SiO_2 AR coating that also provides good bulk and surface passivation is discussed in Chapter 4. Chapter 5 describes the development of record high- efficiency, (17%) rapidly processed RTP/PECVD cells. Finally, Chapter 6 describes our educational activities and accomplishments, which include construction and completion of the educational support program lab, hands-on training in the ESP lab, and course offerings on solar cells.

CHAPTER 2. HIGH-EFFICIENCY MULTICRYSTALLINE SILICON SOLAR CELLS

2.0 Introduction

Low-cost and high-efficiency are the keys for large-scale applicability of photovoltaic systems. Unfortunately, the cost of solar cell modules is about a factor of 4 too high to be attractive for very large-scale utility applications in the USA. However, given the fact that in the 1970's this factor was about 100, there is reason for optimism that photovoltaics will become a cost-effective source of electrical energy in the near future. Photovoltaic modules today cost about $4/watt, which can produce electricity at a rate of about 25¢/kWh. A factor of 2 in cost reduction will make PV attractive for peak-power load applications, and a reduction by a factor of 3 or 4 would make it extremely competitive with conventional energy sources for base load utility applications.

Figure 2.1 shows that a DOE goal of producing PV-generated electricity at 6 ¢/kWh can be realized by various combinations of module efficiency and cost. This is why research is being conducted today on various materials ranging from high-cost high-efficiency single crystal GaAs to low-cost low-efficiency materials like amorphous silicon thin films. No material or technology has yet achieved the cost and efficiency goals simultaneously. Large- grain multicrystalline silicon, which is the focus of this section, is a strong contender for cost-effective PV because of low material cost and potential for high-efficiency cells. Low-cost crystal growth techniques, such as casting, reduce the cost of multicrystalline silicon but at the same time introduce defects, impurities and grain boundaries, which can degrade cell performance. However, by implementing appropriate gettering and passivation techniques, and clever cell designs, it is possible to mitigate the impact of defects and impurities and reduce the gap between single and multicrystalline cell efficiency. This is why enhancement in multicrystalline silicon cell efficiency has become an area of very active investigation.

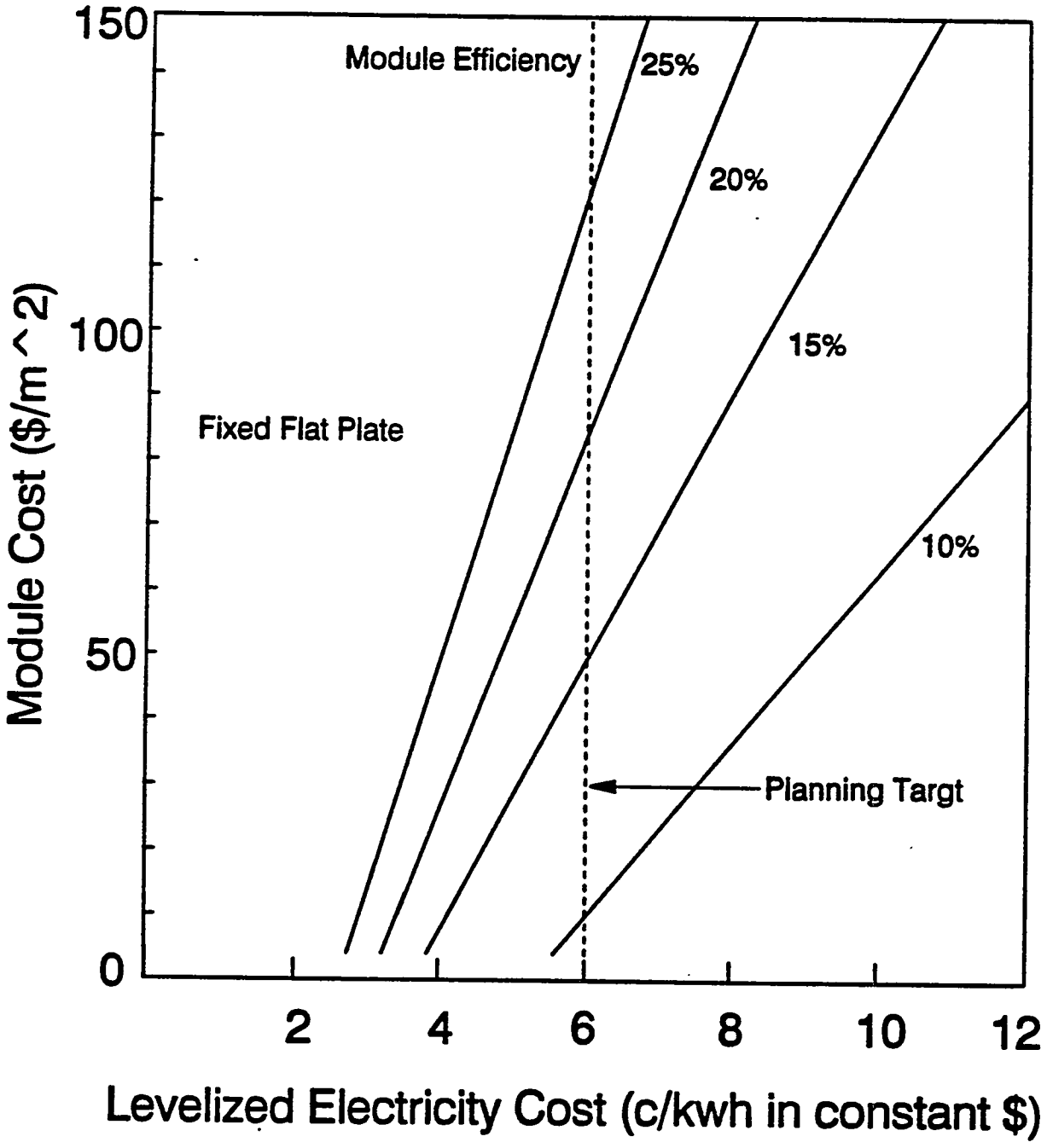


Figure 2.1. Module costs and efficiencies versus 30-year levelized electricity costs for flat-plate photovoltaic systems.

The overall goal of this section is to design and fabricate a record-high-efficiency multicrystalline silicon cell through fundamental understanding of defects and quality enhancement techniques in multicrystalline silicon materials.

2.1 Fabrication of Multicrystalline Silicon Solar Cells Without Gettering and Passivation Techniques; Simple Base-line Process Sequence

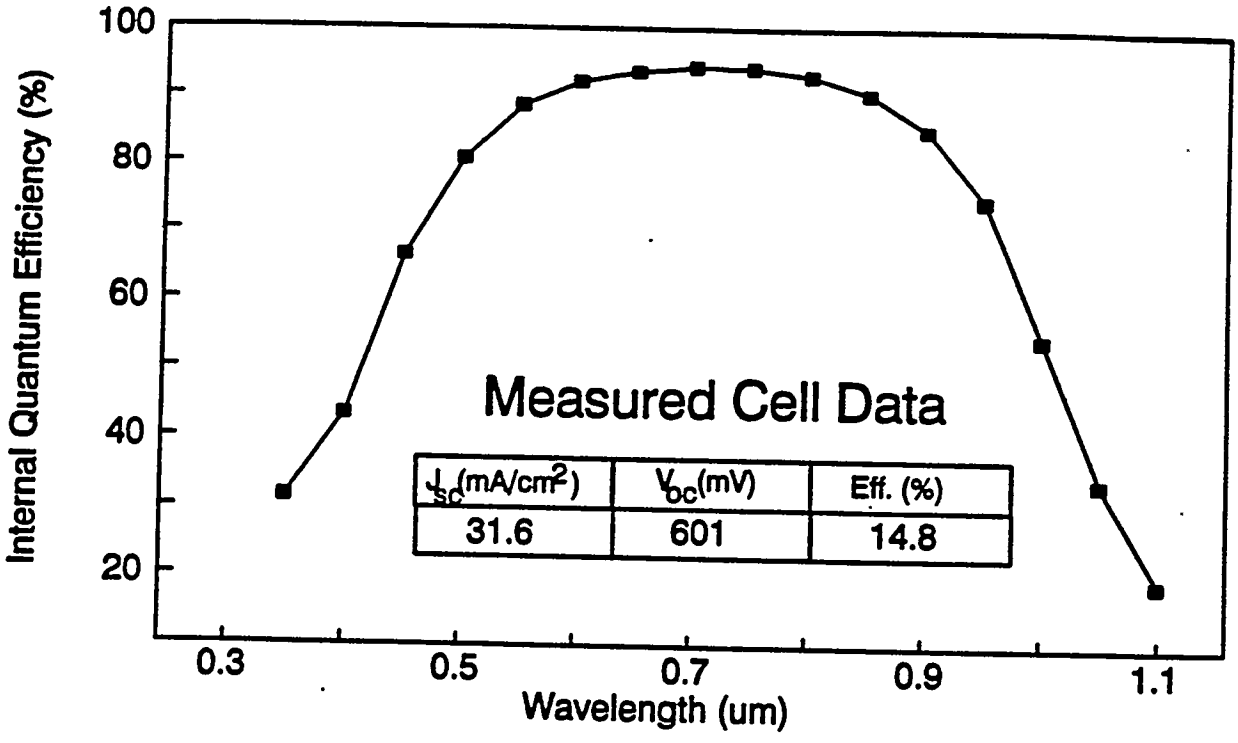
At the beginning of the research, cast multicrystalline silicon material from Sitix (formerly OTC) was selected for cell fabrication. Figure 2.2 shows that when a simple process sequence (Figure 2.3) is used to fabricate n^+-p solar cells, which involves unoptimized phosphorus gettering, no Al gettering, no oxide surface passivation, and no surface and bulk defect passivation by forming gas anneal (FGA), we were only able to achieve 14-15% efficient cells. Diffusion length (L) obtained by internal quantum efficiency analysis was only 200 μm (lifetime of ~14 μs). Model calculations (Figure 2.2) were performed to show that this cell design with L of 200 μm can only give a 14-15% efficient cells. However, if bulk lifetime increased to 25 μs, we can achieve ~16.5% efficient cells. IQE response of these cells in Figure 2.2 also suggests that the performance of the cells can be improved if front and back surface recombination velocities can be reduced by incorporating front-surface oxide passivation and BSF, respectively. Therefore the next step was to change the design to n-p-p^+ structure and incorporate these gettering and passivation techniques that became an integral part of the cell process sequence, rather than using additional steps, so that cell performance could be increased without appreciably influencing the cell fabrication cost.

2.2 Understanding and Optimization of Phosphorus Gettering on Multicrystalline Silicon Solar Cells

Phosphorus gettering is an integral part of cell fabrication because it also forms the n^+ emitter on p-silicon. In this investigation phosphorus gettering was performed for 25 min, using P_2O_5 solid sources. The phosphorus diffusion temperature was varied in the range of 880-1030°C to find the optimum. Since phosphorus gettering is expected to improve bulk lifetime by extracting impurity or defects from the bulk by providing a sink due to the formation of misfit dislocations at surface, open circuit voltage decay lifetime on the phosphorus diffused n^+-p samples was used as an indicator for gettering efficiency or process optimization. Table 2.1 clearly shows that there is an optimum phosphorus diffusion temperature (~930°C) for this cast mc-Si material, which gives and optimizes OCVD lifetime of ~9 μs.

Table 2.1. The effect of phosphorus diffusion temperature on measured OCVD OCVD lifetime

Phos. Diffusion Temperature (°C)	OCVD Lifetime (μsec)	Sheet Resistance(Ω/□)
880	6.0 (±1.0)	25
930	9.0 (±1.0)	16
980	2.0 (±0.5)	12
1030	1.0 (±0.5)	8



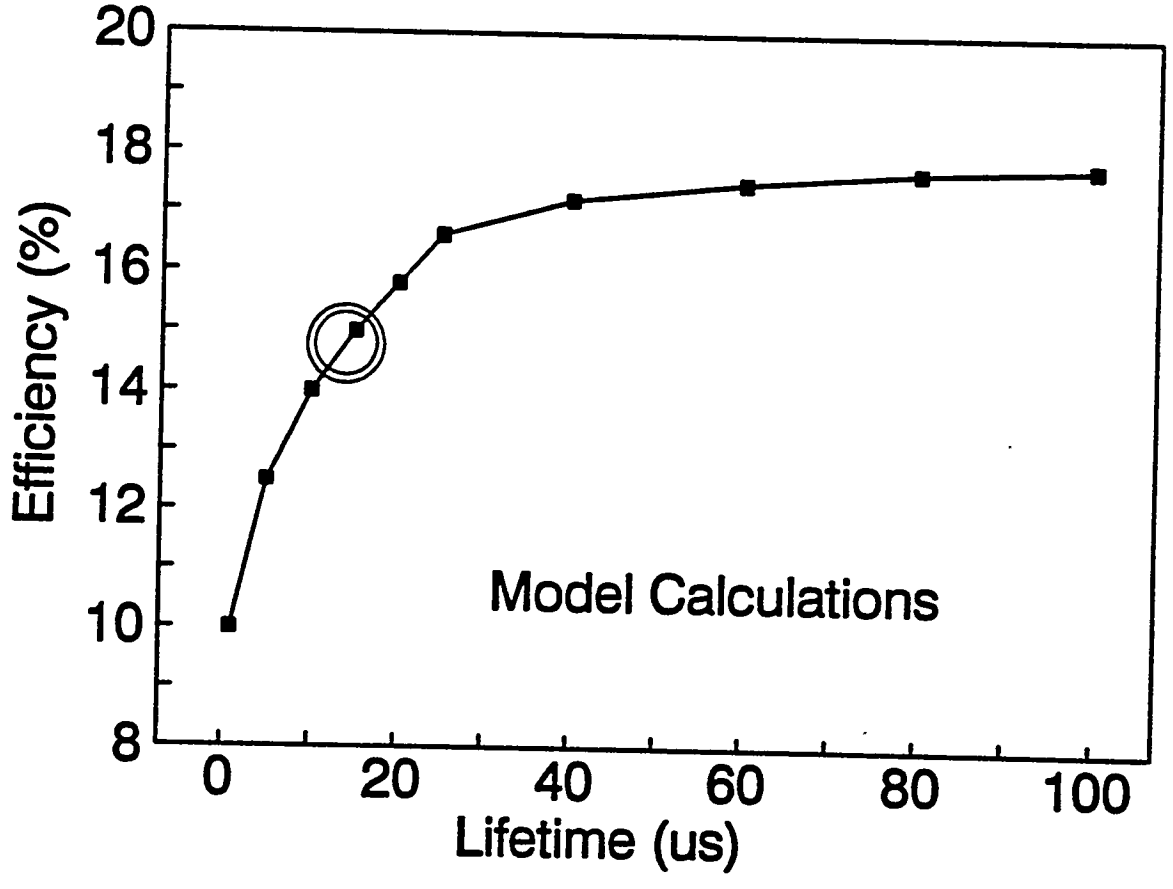


Figure 2.2. Measured cell data and model calculations for the simple base-line cells.

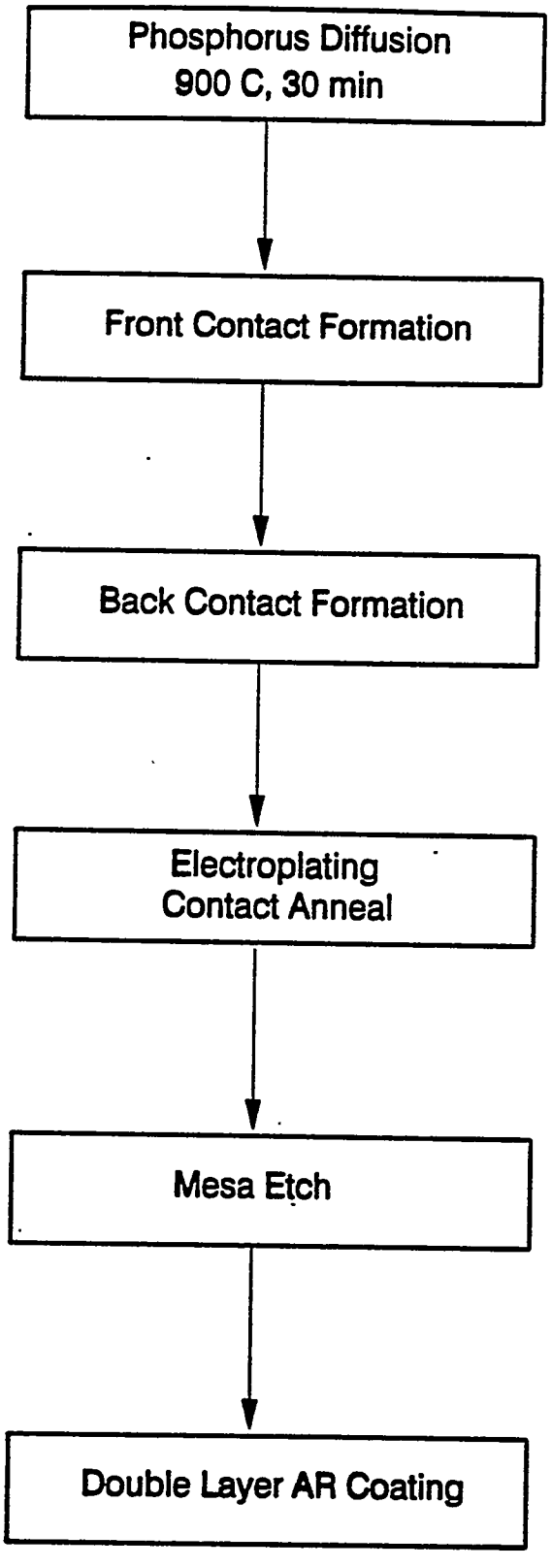


Figure 2.3. Simple base-line process sequence.

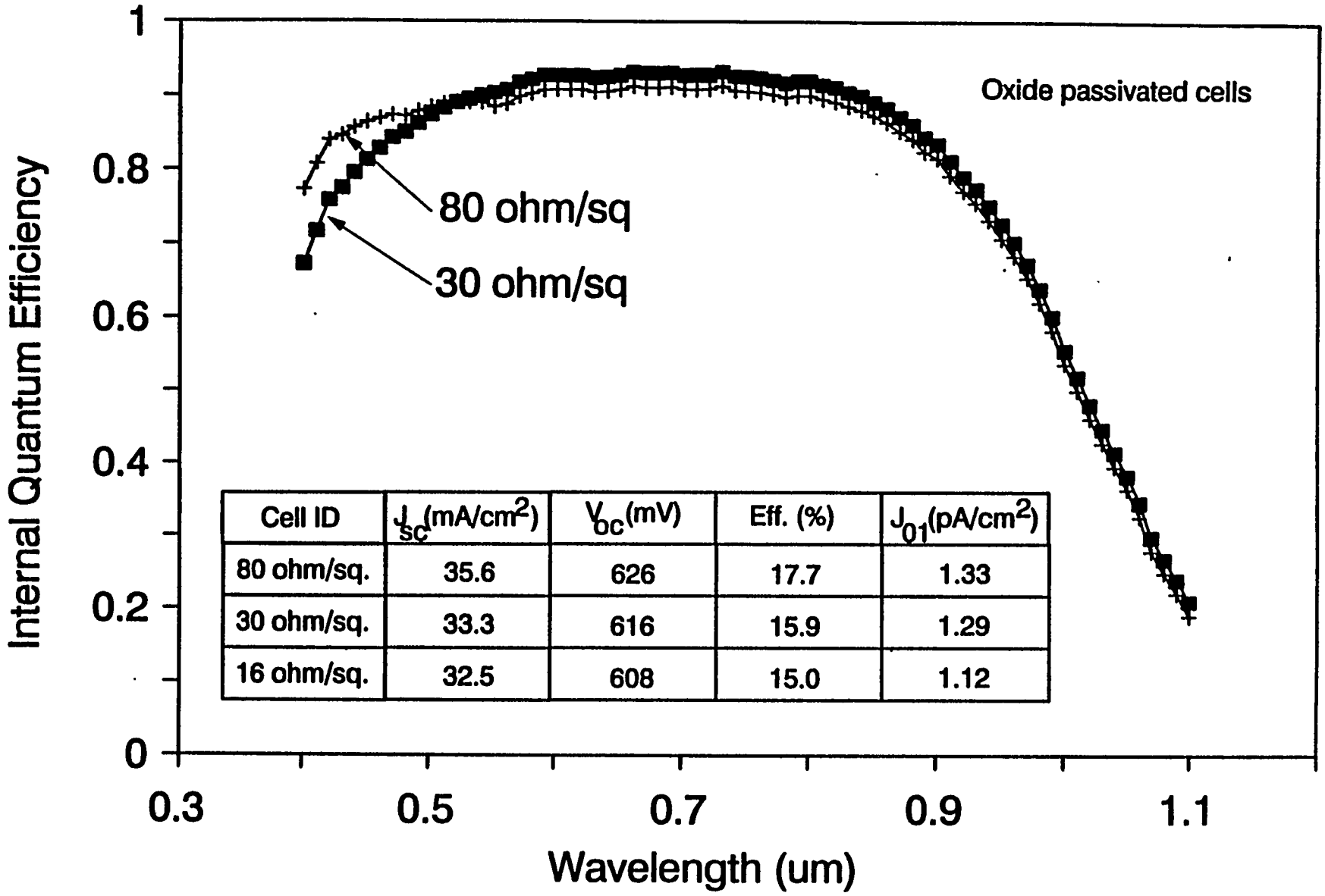
Cost-effective gettering and passivation techniques passivate surface and bulk defects to improve the bulk lifetime and surface recombination velocities. When the diffusion time was varied from 15-45 min at 930°C no appreciable change was observed in the bulk lifetime. Optimum gettering temperature is the result of competition between gettering of impurities and formation of process-induced defects. The latter is due to the fact that mc-Si has grown-in defects and impurities; at high temperatures these defects can migrate and form lifetime- limiting defect complexes, or some defects can get decorated with impurities. Generally, defective materials cannot stand high-temperature processing without lifetime degradation. This is why the phosphorus diffusion temperature was intentionally kept below 1000°C to prevent process-induced lifetime degradation [1], but was kept above 850°C for intense gettering (Table 2.1). It has been suggested [2] that the phosphorus gettering mechanism involves substitutional impurities in the bulk to become interstitial which then diffuse into the n^+-region due to the sink provided by misfit dislocations in the n^+-region. During phosphorus diffusion, a high phosphorus concentration is generated near the surface, which exceeds the solubility limit. Precipitates of SiP are formed and due to the molar volume expansion, the formation of SiP precipitate generates an excess of self interstitials, which are injected in to the bulk. Gettering sites could also be created by the dislocation network that is produced by the stress introduced by the atomic radius difference between phosphorus and silicon atoms. In addition, the n^+ doped region contains a large density of vacancies, which can trap interstitial metal atoms.

2.3 The Effect and Understanding of Partial Emitter Etch Back on the Performance of Multicrystalline Silicon Solar Cells

Spreading resistance data showed that the 930°C/25-min diffusion, which is optimum for phosphorus gettering of Sitix material, gave 16 Ω/□ sheet resistance, with ~1μm thick, very heavily

doped n^+ emitter. This gave lower cell performance because of the thicker dead layer and heavy doping effects, such as Auger recombination and bandgap narrowing. Therefore, an emitter etch-back technique was attempted to partially remove the heavily doped n^+-region, thus raising sheet resistance and thinning the emitter. Figure 2.4 shows a comparison of cells fabricated after two different emitter etch-back depths, resulting in a sheet resistance of 30 and 80 Ω/□. The cells with high emitter sheet resistance of 80 Ω/□ gave the highest V_{oc}, J_{sc} and cell efficiency while the 16 Ω/□ cells, with no emitter etch back, gave the lowest cell efficiency. No attempts were made to increase the sheet resistance beyond the 80 Ω/□ because the grid design used in this study was not suitable for greater than 100 Ω/□ sheet resistance.

V_{oc} of a solar cell is a strong function of J_0 ($V_{oc} = kT/q \cdot \ln J_{sc}/J_0$) while J_{sc} depends strongly on the IQE. The above cells were also analyzed by the reverse saturation current (J_{01}) and internal quantum efficiency (IQE) measurements. J_{01} consists of emitter and base components ($J_{01} = J_{01e} + J_{01b}$). J_{01b} should be independent of emitter etch-back; therefore, any measured difference in the J_{01} with emitter etch-back will reflect the change in the J_{01e} provided the J_{01e} is an appreciable component of the J_{01}. A comparison of the J_{01} of the oxide passivated cells, Figure 2.4, shows that an increase in the sheet resistance from 30 to 80 Ω/□ had virtually no effect on the J_{01}, indicating that the J_{0e} plays a negligible role in dictating the J_{01} or V_{oc} of these gettered and oxide passivated multicrystalline cells with effective bulk lifetimes of 25 μsec. Figure 2.4 shows that, unlike J_{01}, the emitter etch-back from 30 to 80 Ω/□ enhanced the quantum efficiency of the multicrystalline cells in the short wavelength range by reducing the heavy doping effects and absorption in the dead layer. This resulted in about 2.3 mA/cm^2 increase in J_{sc}.



Cell ID	J_{sc}(mA/cm^2)	V_{oc}(mV)	Eff. (%)	J_{01}(pA/cm^2)
80 ohm/sq.	35.6	626	17.7	1.33
30 ohm/sq.	33.3	616	15.9	1.29
16 ohm/sq.	32.5	608	15.0	1.12

Figure 2.4. The effect of emitter etch back on the performance of multicrystalline silicon solar cells.

The observed increase in cell performance after the emitter etch back could result either from removal of the contaminated n^+ region, where gettered impurities end up, or from the reduction in heavy doping effects such as Auger recombination and bandgap narrowing. Therefore model calculations were performed to understand and quantify the effect of emitter etch back. Measured emitter profiles were fed into the device modeling program (PC-1D). Model calculations showed that the 2.5 mA/cm^2 increase out of the observed 3.0 mA/cm^2 increase in J_{sc} came from the reduction in heavy doping effect. The remaining 0.5 mA/cm^2 can be attributed to better surface passivation due to reduced surface doping concentration. Thus, intense phosphorus gettering followed by an etch back is an ideal way to form an emitters in mc-Si cells because you retain the benefit of phosphorus gettering without the penalty of the heavy doping effects.

2.4 Optimization and Fundamental Understanding of Multiple Effects of Al Treatment on MC-Si Cells

2.4.1 Effect of Al Gettering Temperature on Cell Performance

In order to conduct a controlled investigation of Al gettering, cells were fabricated with one-half of each wafer covered with Al on the back side (Al-diffused cells with p^+-BSF) while the other half was kept bare (Al-sintered cells with no BSF) during the Al drive-in (Figure 2.5). The drive-in temperature in this study was varied in the range of 800-925°C to find the optimum. Improvement in V_{oc} contains the information about the gettering-enhanced bulk lifetime as well as the BSF effect. BSF tends to reduce the back surface recombination velocity (BSRV) at the p-p^+ interface which manifests itself in the form of higher effective lifetime, J_{sc}, and V_{oc}; therefore, V_{oc} and cell

efficiency were used as the indicator for process optimization. Figure 2.6 shows that for this Sitix multicrystalline silicon material, Al drive-in temperature in the range of 850-900°C gives the highest V_{oc} and efficiency. An optimum Al gettering temperature is related to the competition between gettering and thermally-induced defect generation, as also seen in the case of phosphorus gettering. Figure 2.7 shows that at each temperature, Al-diffused solar cells showed better performance compared to those with no Al BSF. Below the 850°C drive-in, the V_{oc} increased with increasing drive-in temperature because of two reasons: first the Al gettering efficiency increases with temperature, and second, the thickness and effectiveness of the BSF also increase with the temperature. The decrease in V_{oc} beyond 900°C is probably due to the fact that defective materials like multicrystalline silicon cannot stand very high temperature processing without lifetime degradation due to defect generation or defect complex formation. This hypothesis was confirmed by IQE and diffusion length (L) measurements (Figures 2.8 and 2.9). Figure 2.8 clearly shows that low Al-drive-in temperature does not improve L, at intermediate temperatures (850-900°C) L increases rapidly due to gettering and BSF, but at high temperatures (> 900°C) L decreases again due to process-induced defects. This fact is also reflected in the IQE of the cells with and without Al treatment at different drive-in temperatures. Table 2.2 shows a comparison of cell data for the Al-diffused and Al-sintered Sitix cast multicrystalline silicon. Cast multicrystalline cells showed an appreciable increase in the effective diffusion length from 195 to 261 μm and a corresponding absolute cell efficiency improvement of 1.4% due to the Al process, Table 2.2. PC-1D device modeling was performed for the best cell (efficiency of 17.8%) to understand the multiple effects of Al treatment. Model calculations showed (Table 2.3)

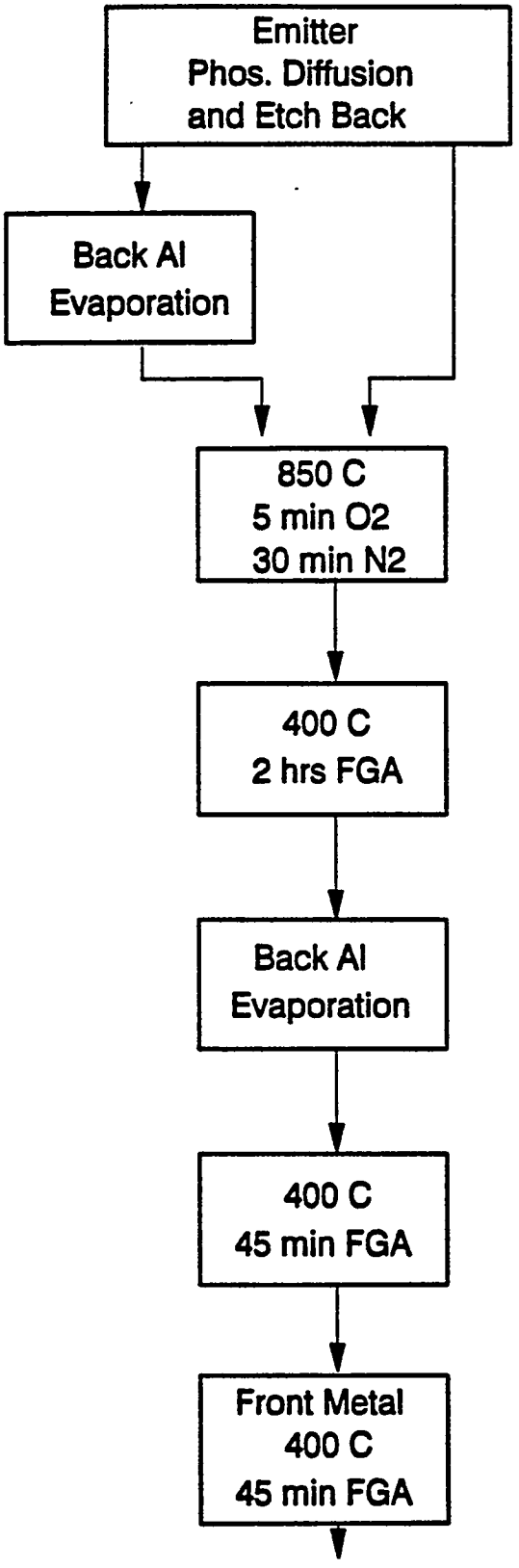


Figure 2.5. Process sequence to decouple the effect of Al diffusion.

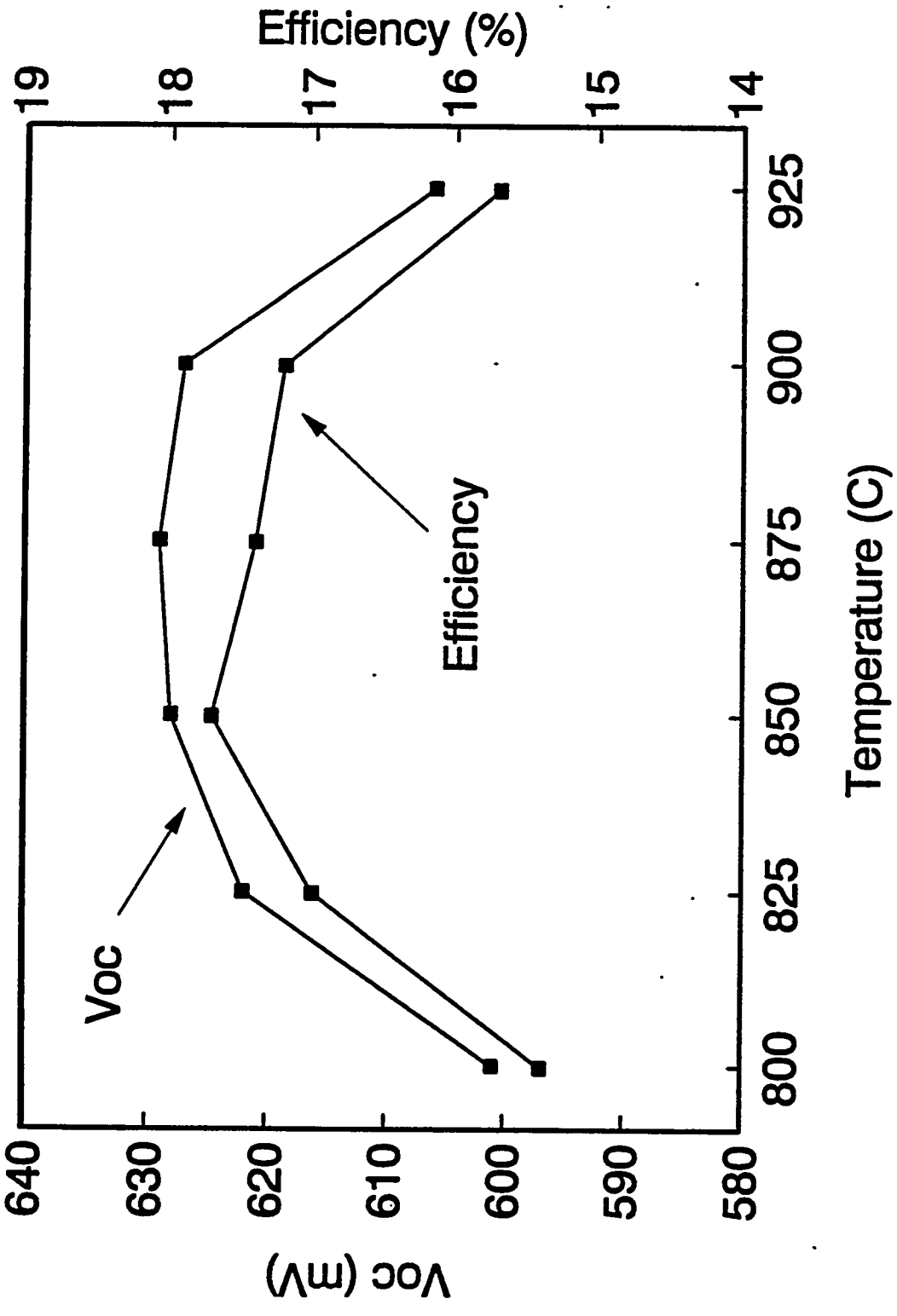


Figure 2.6. The effect of Al drive-in temperature on the cell performance.

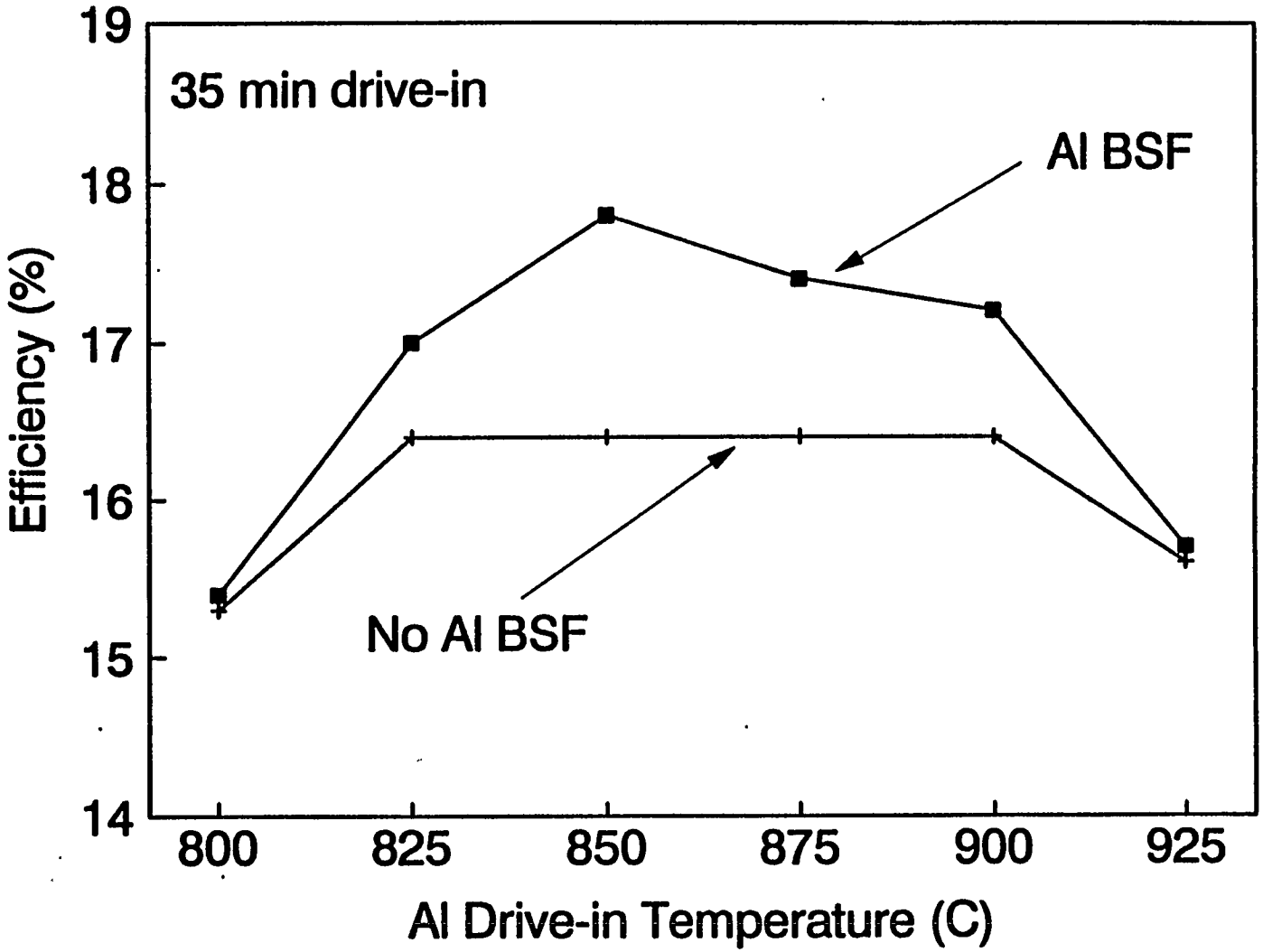


Figure 2.7. The effect of Al drive-in temperature and Al BSF on the cell performance.

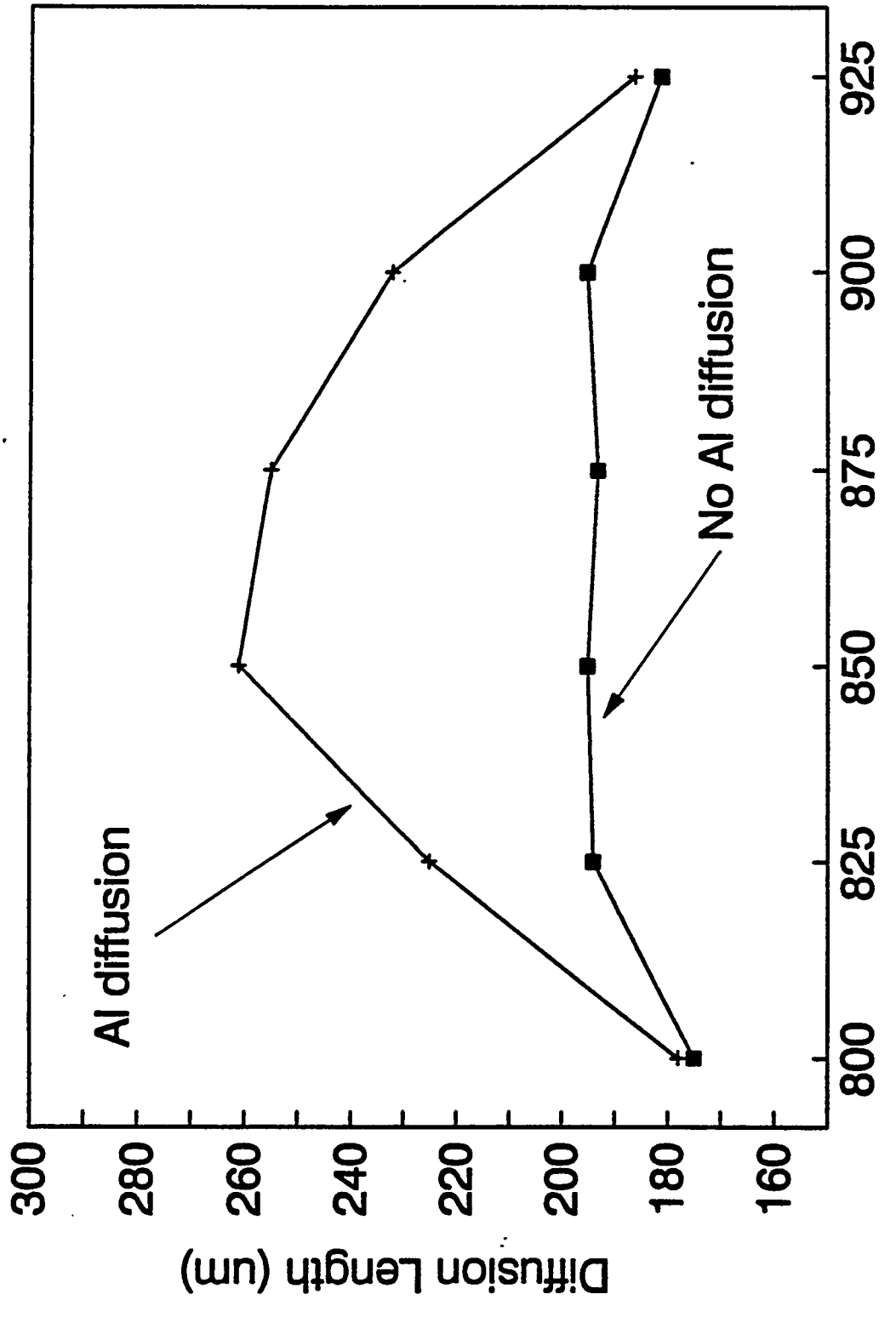


Figure 2.8. The effect of Al gettering temperature and Al BSF on bulk diffusion length.

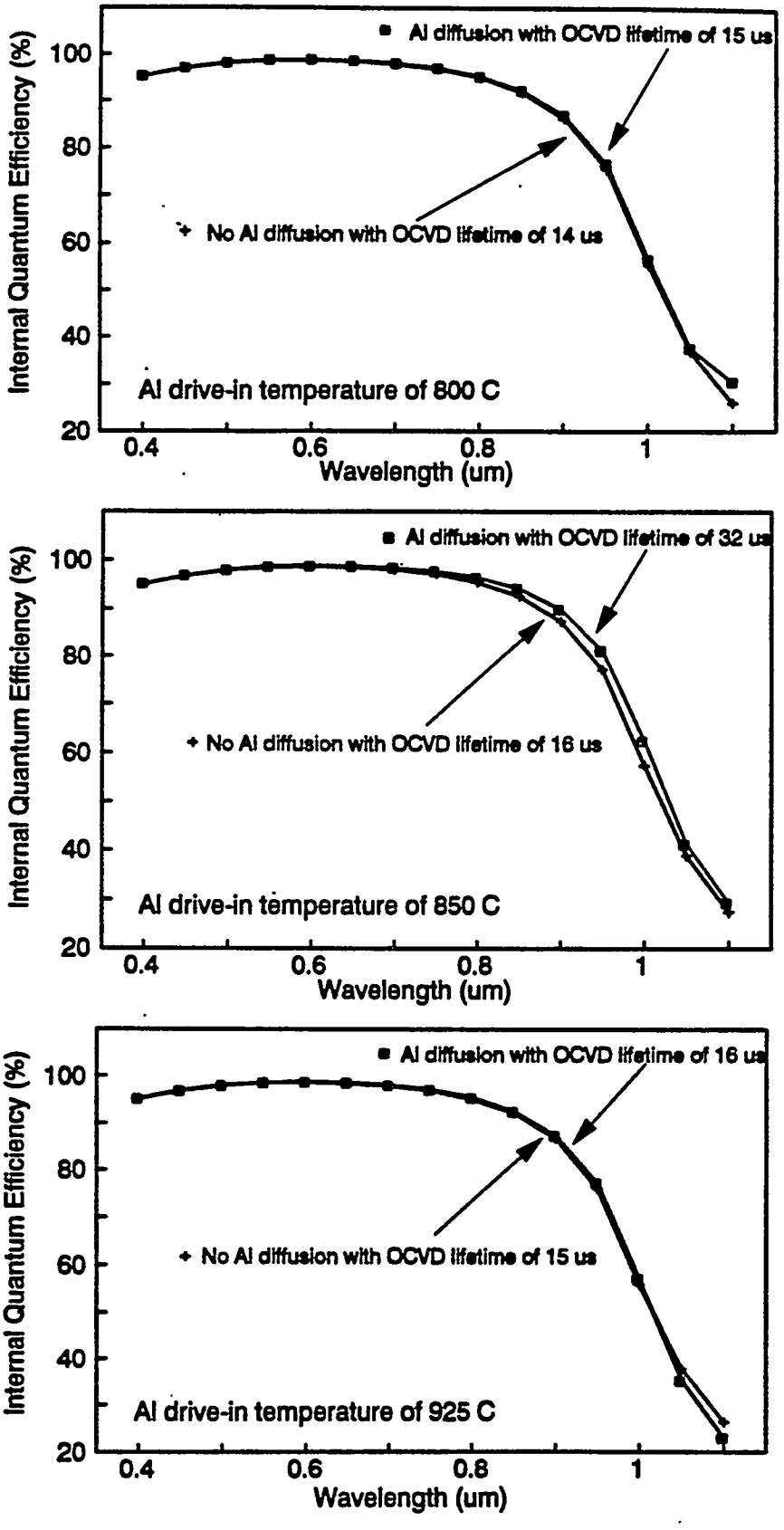


Figure 2.9. The effect of Al gettering temperature on IQE of solar cells.

that in the 400 μm thick Sitix polysilicon cells with 195 μm diffusion length, Al BSF can only produce an efficiency improvement of ~0.3%. Detailed model calculations also showed that the observed 1.4% increase in cell efficiency in this case results from the multiple effects of Al treatment. In addition to the BSF and gettering effects, the Al treatment roughens the back surface, which reduces the back surface reflectance and introduces some light trapping. Detailed cell analysis showed a reduction in BSR (back surface reflectance) from 87% to 75% and path length enhancement by a factor of 1.4 due to back texturing in these cells. Model calculations in Table 2.3 revealed that Al treatment increased J_{sc} by 0.3 mA/cm^2 due to BSF, decreased J_{sc} by ~0.1 mA/cm^2 due to reduced BSR, and increased J_{sc} by 1.7 mA/cm^2 due to lifetime enhancement and light trapping, accounting for the observed increase of 2.1 mA/cm^2 in J_{sc} in these cells. Thus, even though there are multiple effects of Al, the majority of the improvement results from the Al-gettering-induced increase in lifetime.

Table 2.2. Effect of aluminum treatment on multicrystalline silicon cell performance

	Aluminum Diffused and Gettered				Aluminum Sintered with no Al Gettering			
MCS ID	V_{oc} (mV)	J_{sc} (mA/cm^2)	Efficiency (%)	Diff. Length (μm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	Efficiency (%)	Diff. Length (μm)
Sitix	628	36.2	17.8	261	618	34.1	16.4	195

Table 2.3. The multiple effects of Al gettering, the observed change in J_{sc} is 2.1 mA/cm^2

	ΔJ_{sc} (mA/cm^2)	Δ Efficiency (%)
Lifetime	1.0	0.7
BSF	0.3	0.1
BSR	- 0.05	< 0.1
Perfect Back Texture	0.7	0.3

2.4.2 LBIC Response of Al-gettered Multicrystalline Silicon Solar Cells

In order to support the above conclusion that Al treatment performs gettering, light beam induced current (LBIC) measurements were performed on Sitix cells, with and without the Al treatment, to investigate if bulk diffusion length enhancement results from Al-gettering inside the grains or at the grain boundary. Samples covered with 1-μm thick Al on the back-side followed by 850°C drive-in were processed as a solar cells. They were divided into four groups: no Al gettering, 1-min, 35-min, and 120-min Al drive-in, respectively. LBIC measurements were performed in a region with the same microstructure on all four neighboring samples. The light beam spot size was 125 μm for a LBIC-map, and 25 μm spot size was for the scans over grain boundary to obtain a higher resolution. To generate carriers deeper in the bulk, a light beam with a wavelength of 975 nm was used. The LBIC maps for these four samples are shown in Figure 2.10. It is clearly seen that LBIC response is significantly enhanced by longer Al gettering time, with strong enhancement within the grains, but with not much change at grain boundaries.

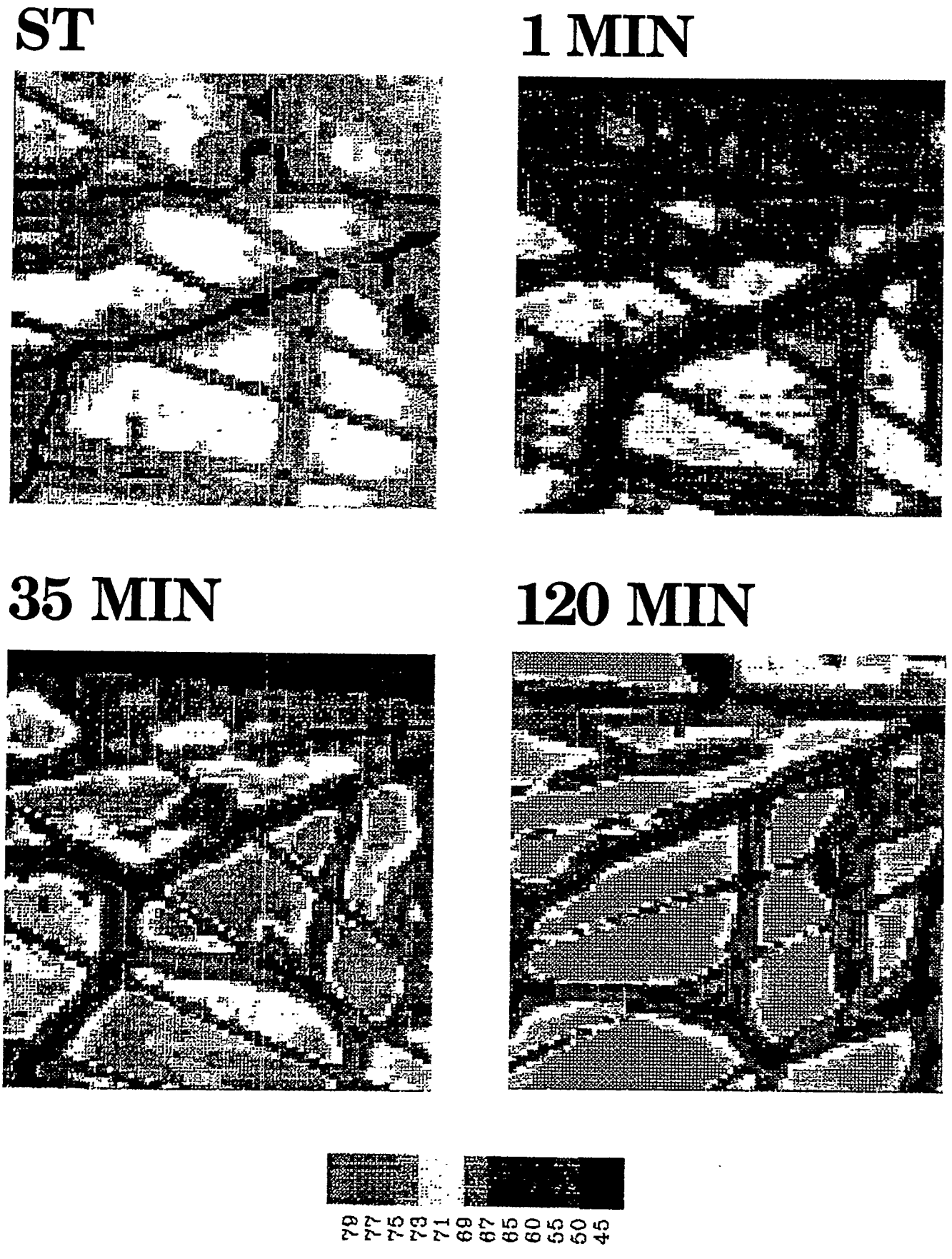
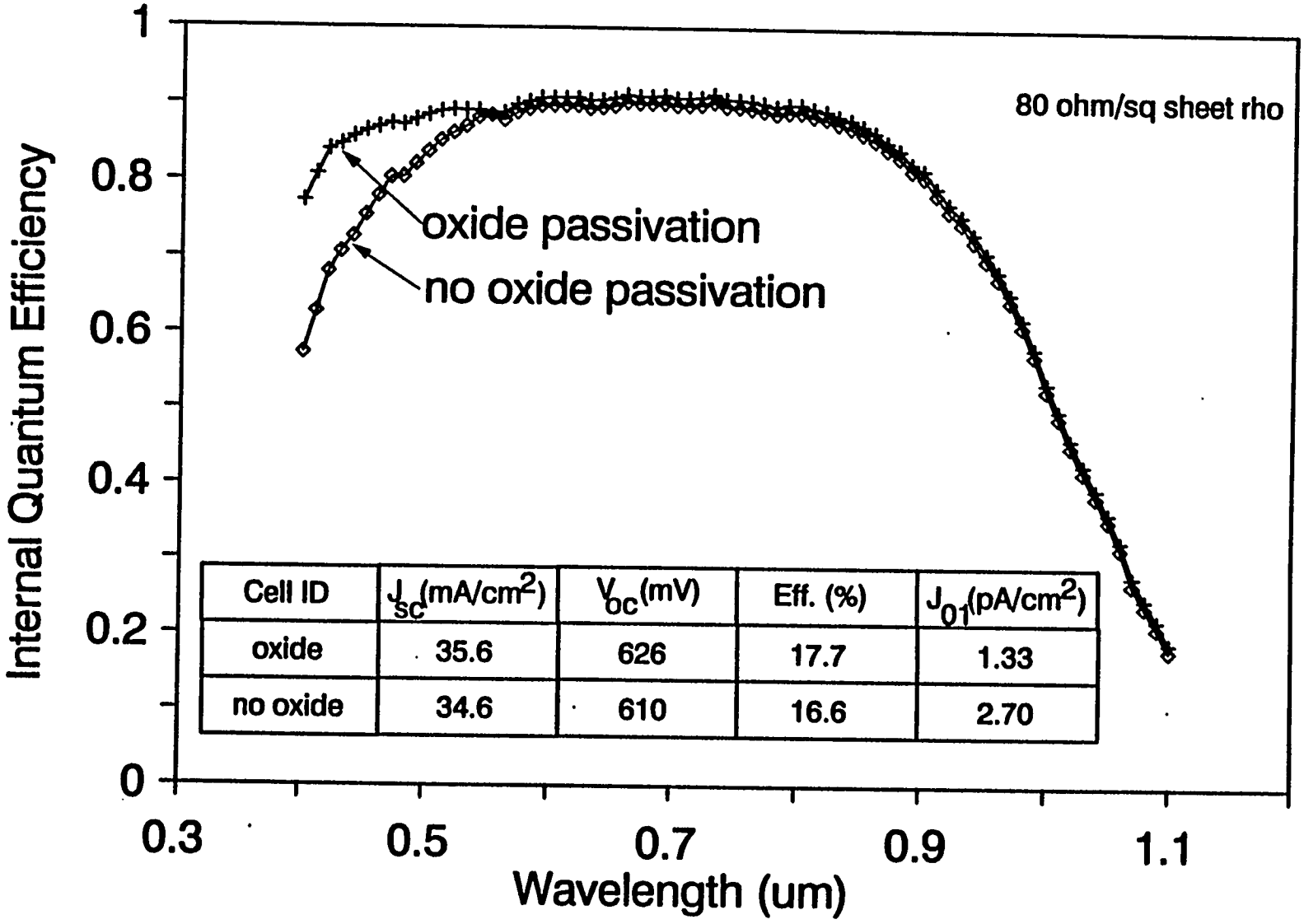


Figure 2.10. LBIC map of the Al-treated multicrystalline silicon wafers.

2.5 Understanding the Impact of Emitter Oxide Passivation on the Performance of Multicrystalline Silicon Solar Cells

In addition to bulk lifetime, the front surface recombination velocity plays an important role in determining the J_0, V_{oc}, J_{sc}, and cell performance. Therefore an attempt was made to passivate the emitter surface during the Al drive-in. This simplifies the process and maintains the cost effectiveness of the process sequence. After Al evaporation on the back surface, wafers were inserted at 850°C in the oxygen ambient to first grow ~100 Å thick passivating oxide on top of the n^+ emitter region on the front. After 5 minutes of oxide growth, the gas ambient was switched to nitrogen for an additional 30- minute Al drive-in. Similar to phosphorus gettering and emitter etch-back, oxide passivation was found to be quite beneficial for the multicrystalline silicon cells. Figure 2.11 shows that oxide passivation resulted in about 1.0 mA/cm^2 improvement in the J_{sc} and 1% increase in absolute efficiency of the Sitix multicrystalline cells. This increase in J_{sc} is supported by the appreciable increase in the short wavelength response of the multicrystalline cells due to the oxide passivation (Figure 2.11). Dark I-V analysis in Figure 2.11 shows that the oxide passivation of these multicrystalline cells also reduced the J_{01} by a factor of ~2. This combination of increased J_{sc} and reduced J_{01} should result in an increase of 18 mV in V_{oc} [V_{oc}=KT/q. ln(J_{sc}/J_0 + 1)]. This agrees fairly well with the observed increase of 16 mV in V_{oc}. Thus oxide surface passivation can be quite beneficial in properly gettered high-lifetime multicrystalline cells.



Cell ID	J_{sc}(mA/cm^2)	V_{oc}(mV)	Eff. (%)	J_{01}(pA/cm^2)
oxide	35.6	626	17.7	1.33
no oxide	34.6	610	16.6	2.70

Figure 2.11. The effect of emitter oxide passivation on the multicrystalline silicon cell performance.

2.6 Bulk Defect Passivation by Forming Gas Anneal in Multicrystalline Silicon Cells

Bulk defects, such as dislocations, grain boundaries etc., are an integral part of mc-Si. These defects are electrically active and provide sites for recombination of photogenerated carriers to reduce bulk lifetime and cell performance. Atomic hydrogen has been used successfully to passivate such defects. Forming gas, which contains 10% molecular hydrogen, can provide a source of atomic hydrogen if it can be dissociated. Therefore an attempt was made to use forming gas anneal (FGA) to passivate defects in this research. The process sequence in Figure 2.12 shows that we incorporated two forming gas treatments at 400°C in our cell fabrication, one directly after the 850°C Al drive-in step and the other after the Al back contact deposition. This was done intentionally to enhance the beneficial effect of FGA, phosphorus diffused region, Al metal, and Al/Si alloy layers can assist in generating atomic hydrogen by interacting with the 10% molecular H_2 in the forming gas. We selected EFG mc-Si, which is known to respond quite favorably to hydrogen passivation, to investigate the effect of FGA. In order to investigate and decouple the effects of Al gettering and FGA passivation in one experiment, we fabricated four kinds of cells. Figure 2.13 shows that incorporation of Al gettering treatment and first and second FGA for defect passivation resulted in an EFG cell efficiency of ~13.8-14.1% [3], which is comparable to good EFG cells made by intentional hydrogen ion implantation [4]. If the Al diffusion is eliminated by fabricating Al sintered cells, then a significant drop in IQE and cell efficiency, from 13.8 to 12.4%, is observed. This indicates that Al treatment-induced gettering alone improves the EFG cell efficiency by ~1.5%. Figure 2.13 shows that if the Al or alloyed Al layer interaction with forming gas is turned off by replacing the second FGA by nitrogen anneal in the case of sintered cells, then the IQE drops further and the EFG cell efficiency decreases from 12.4 to 11.2%.

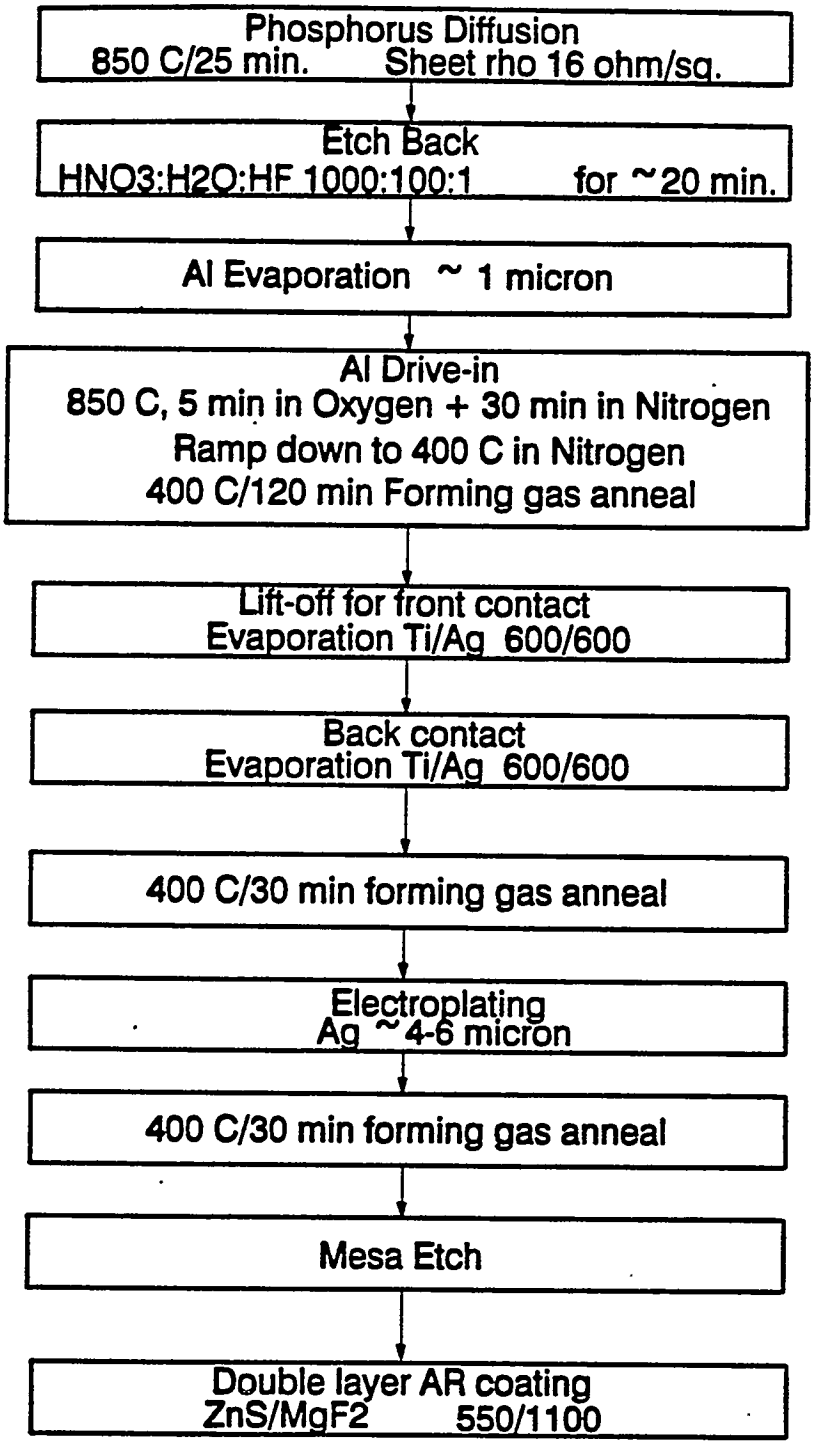
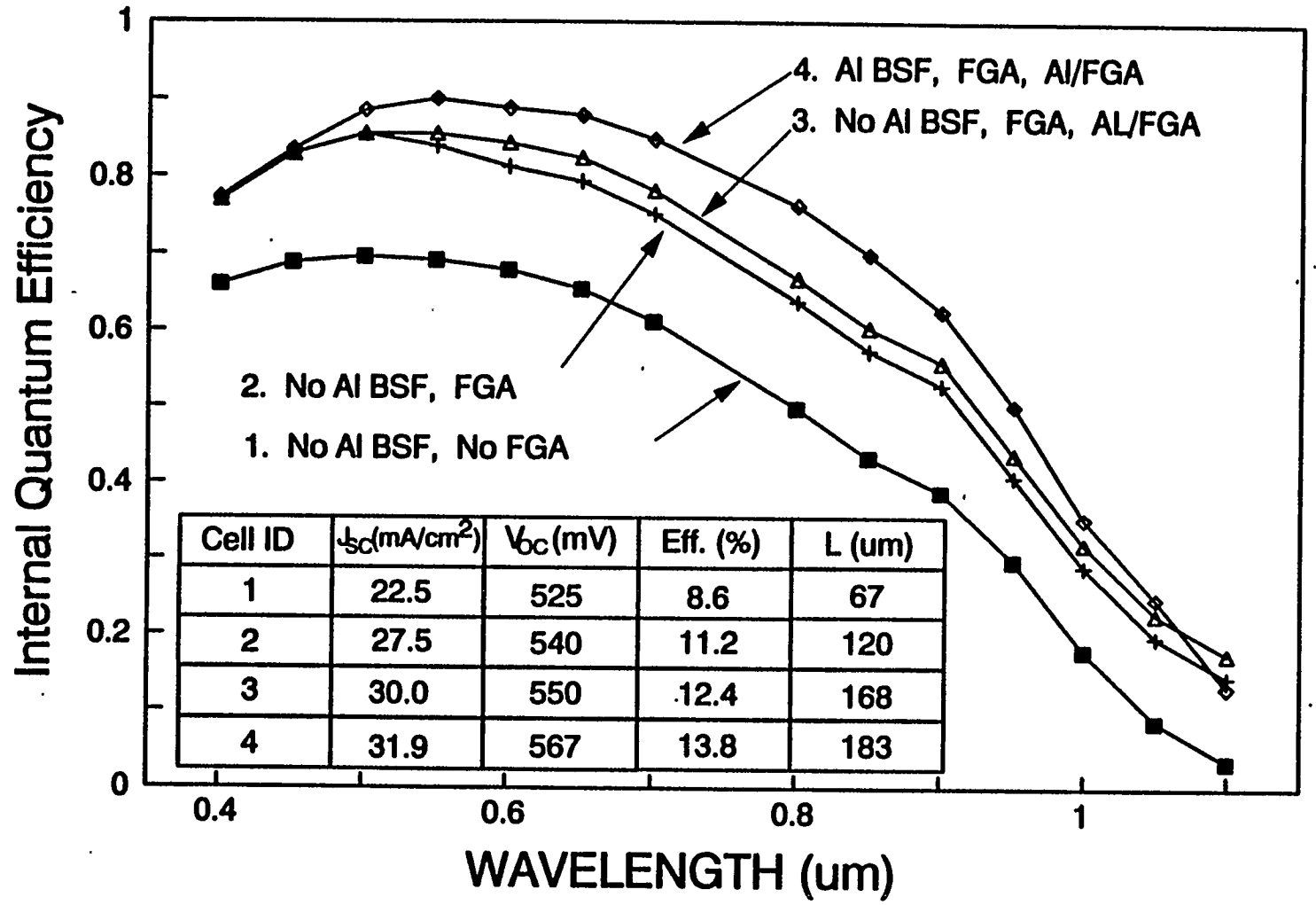


Figure 2.12. Process sequence for fabricating high-efficiency multicrystalline silicon solar cells.



Cell ID	J_{SC}(mA/cm^2)	V_{OC}(mV)	Eff. (%)	L (um)
1	22.5	525	8.6	67
2	27.5	540	11.2	120
3	30.0	550	12.4	168
4	31.9	567	13.8	183

Figure 2.13. The effect of FGA and forming gas/Al on the performance of multictrystalline silicon solar cells.

This suggests that Al or Al doped p^+ region/FGA interaction leads to some hydrogenation and defect passivation in the EFG material. Finally if both the 400°C forming gas anneals are replaced by nitrogen anneals, then the EFG cell efficiency drops significantly to 8.6%, which indicates that the first FGA alone does significant defect passivation in the EFG material. Thus EFG material not only benefits from Al gettering but also from FGA-induced defect passivation.

In order to prove that the FGA-induced improvement is related to hydrogenation, after the 400°C/2hr FGA, the temperature was raised to 600°C and the ambient gas was switched to nitrogen to drive out the incorporated hydrogen. Indeed it was found that the cell efficiency decreased from 14% to 10%, shown in figure 2.14, suggesting that hydrogen passivation is the most likely mechanism for the FGA effect.

In an attempt to further investigate the interaction of molecular hydrogen in forming gas with surface defects, n^+ and p^+ regions, a systematic study was conducted using EFG silicon without the cell fabrication. It was found that FGA alone increases the diffusion length of EFG silicon from 61 to 95 μm, Al diffusion alone increases it to 153 μm, and phosphorus diffusion alone increases the EFG diffusion length from 61 μm to 173 μm (Figure 2.15). However FGA after the phosphorus or Al diffusion results in much greater enhancement in diffusion length (> 300 μm), suggesting that FGA is not only beneficial by itself but in the presence of Al metal, n^+, and p^+ regions, it becomes even more effective. This could be because surface defects, such as dislocations and grain boundaries, can dissociate molecular hydrogen into atomic hydrogen and provide paths for hydrogen diffusion into the bulk. This could explain why FGA by itself is so effective in defective mc-Si. Phosphorus and Al diffusions tend to create more surface defects, stress, and vacancies, which can increase the solubility of hydrogen and facilitate the formation of rapidly diffusing hydrogen-vacancy pairs near the surface [5]. This could explain why the FGA effect is magnified in the presence of n^+ or p^+ regions. The exact mechanism behind the FGA-induced passivation is not yet fully understood.

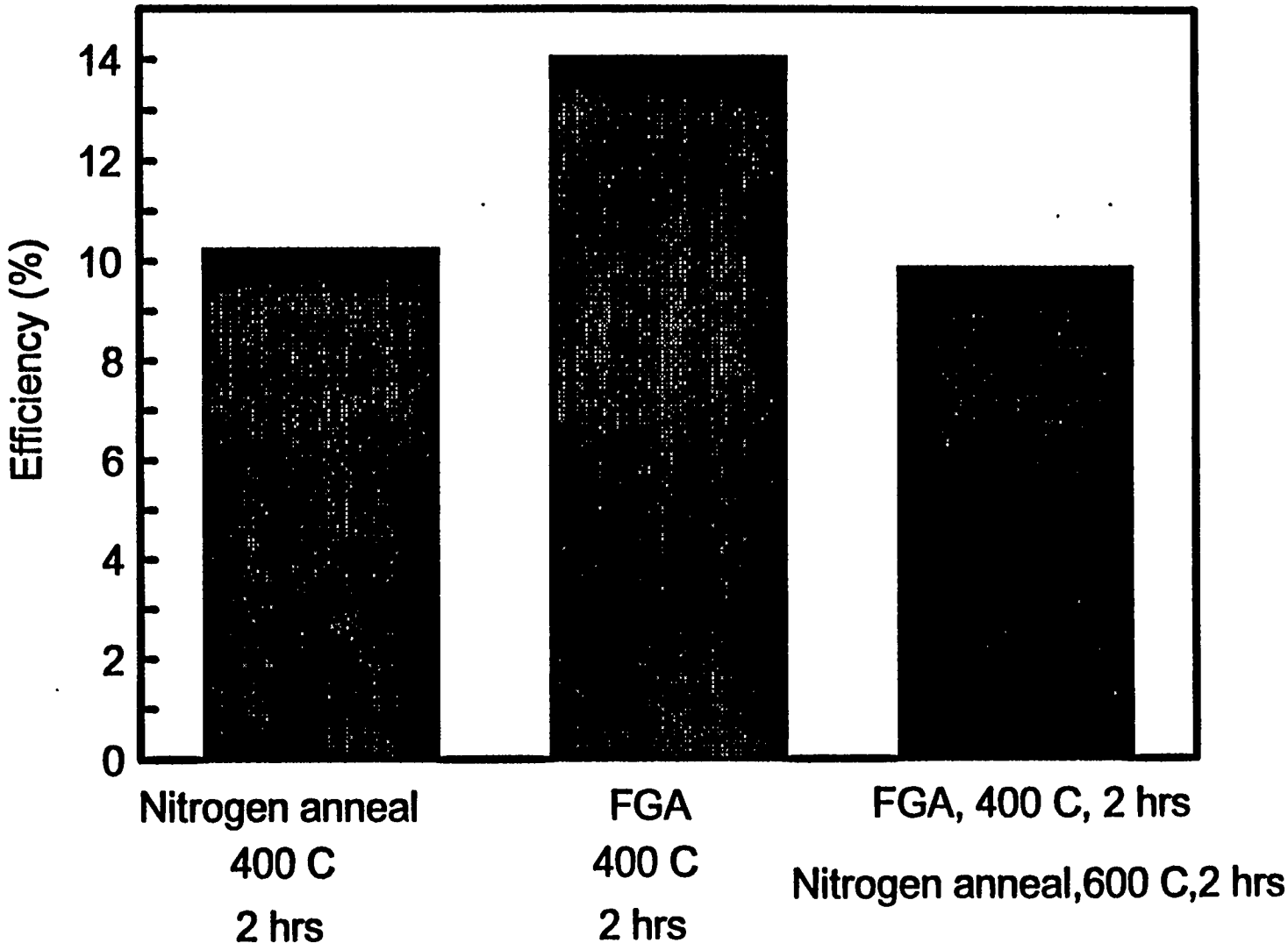


Figure 2.14. The effect of nitrogen anneal on the performance of forming gas annealed cells.

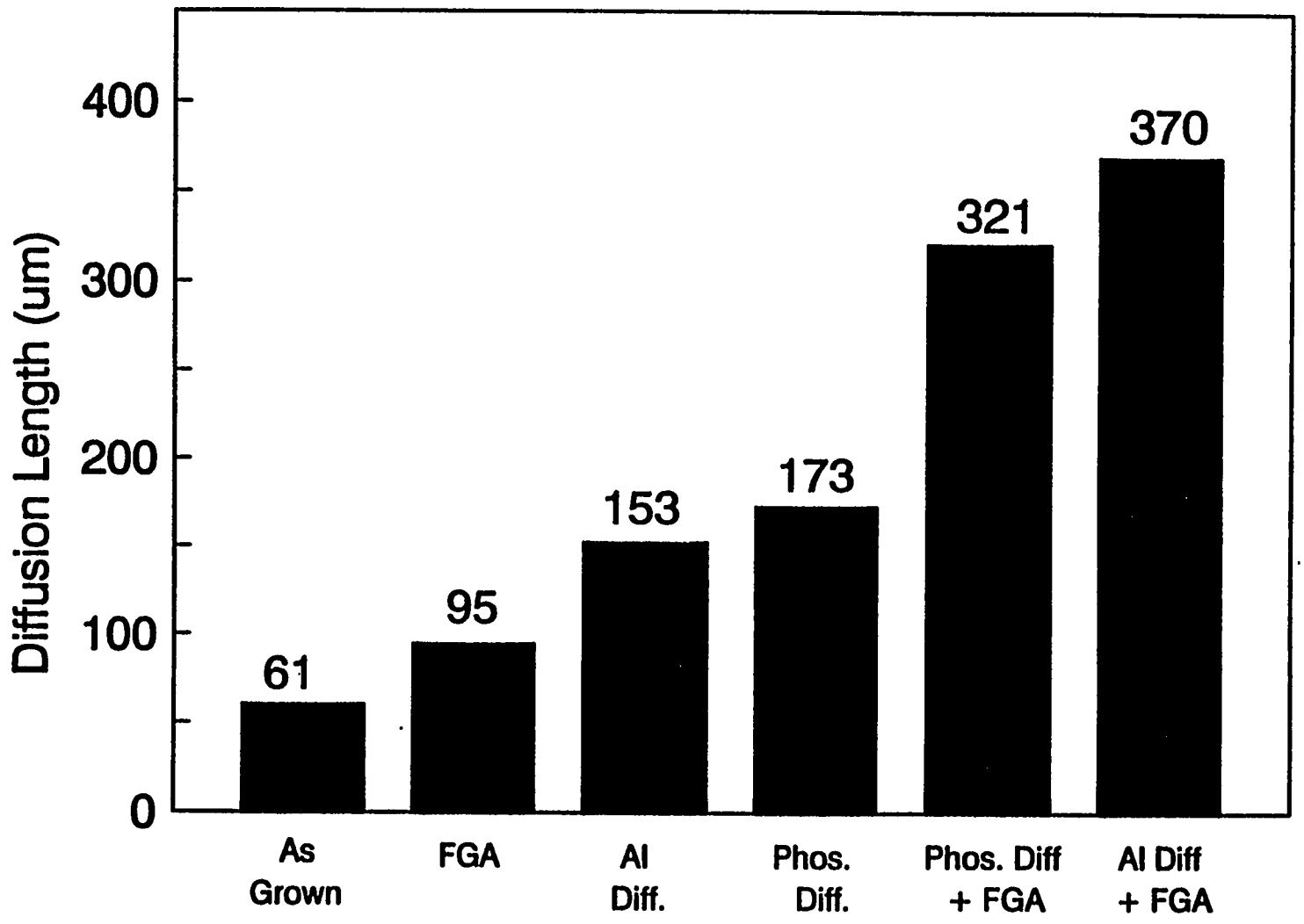


Figure 2.15. The effect of different treatment on the diffusion length of EFG wafers.

Figure 2.16 shows that defect passivation by FGA is highly material specific. In contrast to EFG cells, the forming gas treatment had virtually no effect (< 5%) on the Sitix and HEM cast multicrystalline silicon cells. This is probably because higher quality cast multicrystalline silicon materials do not have defects that can benefit from hydrogen passivation. However, in materials like EFG and AP-Si thin film, which consist of a high concentration of active dislocations or grain boundaries, FGA has a very significant effect on bulk diffusion length and cell performance, as seen in figure 2.17.

We have been trying to develop a physical model for hydrogen dissociation and diffusion. Based on the literature, H_2 solubility in silicon at 400°C is very small, on the order of 10^{-16}, cm-3. According to the literature, if H_2 diffuses in silicon via an interstitial plus trapping mechanism, then it should not get beyond 1 or 2 μm at 400°C. However in mc-Si cells we see a substantial increase in long wavelength response. We think the FGA effect can be explained by the following model (Figure 2.18). First, both phosphorus and Al diffusion lead to stress and surface damage. Phosphorus diffusion introduces misfit dislocations, and Al treatment results in stress-induced voids and surface damage. It has been shown [6] that such surface damage can increase the solubility of molecular hydrogen by orders of magnitude.

Phosphorus and Al treatments also introduce near-surface defects like vacancies, interstitials and dislocations, which can dissociate molecular hydrogen [7] resulting in a huge source of atomic hydrogen. Mc-Si materials not only have vacancies to begin with but the Al and phosphorus diffusions also generate vacancies near the surface, and this enhances the possibility of formation of H-V pairs that can diffuse in silicon more rapidly than interstitial hydrogen. This explains why we see FGA defect passivation so deep in the bulk. At this point this explanation is just a hypothesis, and more work needs to be done in this area to prove or disaprove it.

2.7 Fabrication of Record High-Efficiency Multicrystalline Silicon Solar Cells

After developing, optimizing, and improving the fundamental understanding of the above gettering and passivation techniques, we designed and fabricated high-efficiency mc-Si cells by integrating these techniques in a process sequence. Attempts were made to fabricate 1cm x 1cm high-efficiency multicrystalline solar cells using the optimized phosphorus and aluminum gettering conditions, oxide passivation, FGA, and an evaporated double layer ZnS/MgF_2 antireflection coating. Sitix silicon was selected for this task, since it was one of the best mc-Si available at that time. Figure 2.19 shows the model calculations for a 400 μm thick n^+-p-p^+ silicon cell, with a junction depth of ~0.5 μm, a BSF thickness of ~1.5 μm, and a two layer AR coating. Notice that in order to achieve high- efficiency (> 17%) cells, a bulk lifetime of more than 20 μs is required. Bulk lifetime in the as-grown Sitix material is only 6-10 μs. Thus, gettering and passivation techniques will have to play a significant role to achieve the high-efficiency record. First 30-40 μm silicon was removed from each side by a chemical etch in order to remove the saw damage from the as-received multicrystalline wafers. After the chemical polishing, the substrate thickness was reduced to about 400 μm. The emitter region was formed by 930°C/25 min phosphorus diffusion followed by an etch-back to 80 Ω/□. Then 850°C oxide passivation and Al drive-in were performed. As shown in the previous sections, these treatments not only constitute the best phosphorus and Al gettering conditions but also give desired n^+ and p^+ regions with 0.5 and 1.5 μm thickness, respectively. The front grid contact was formed by evaporation of Titanium/Silver (600 Å/600 Å) and the lift-off technique. The back contact was formed by evaporating 500 Å Ti/ 500 Å Ag on the top of the Al BSF region. Contacts were annealed in a forming gas ambient for 30 minutes at 400°C. About 5 μm thick silver was plated on the front grid pattern to reduce the series resistance. Finally, a 550 Å ZnS/1100 Å MgF_2 double layer AR coating was deposited by thermal evaporation on the

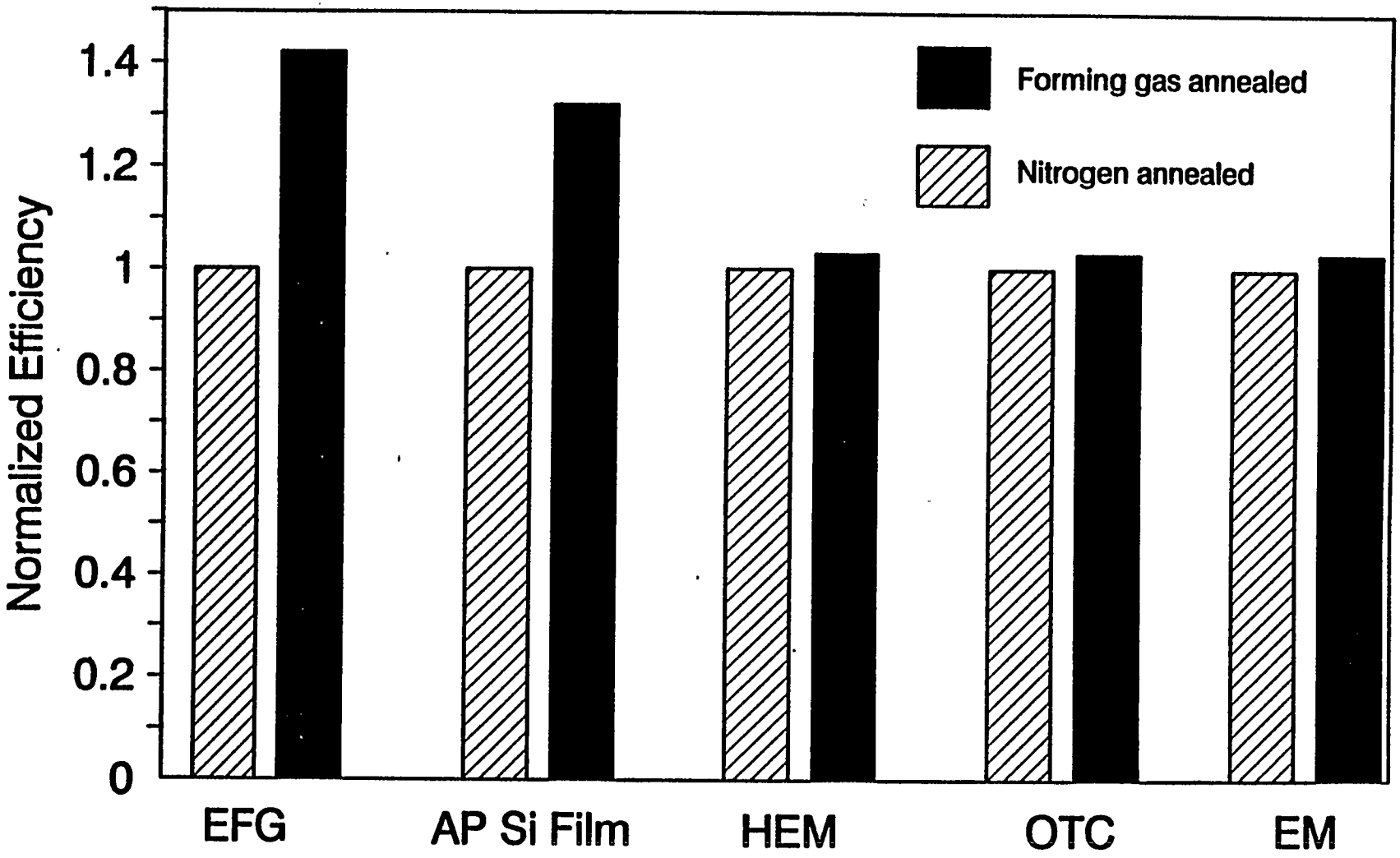


Figure 2.16. The effect of FGA on the performance of solar cells made on different substrates.

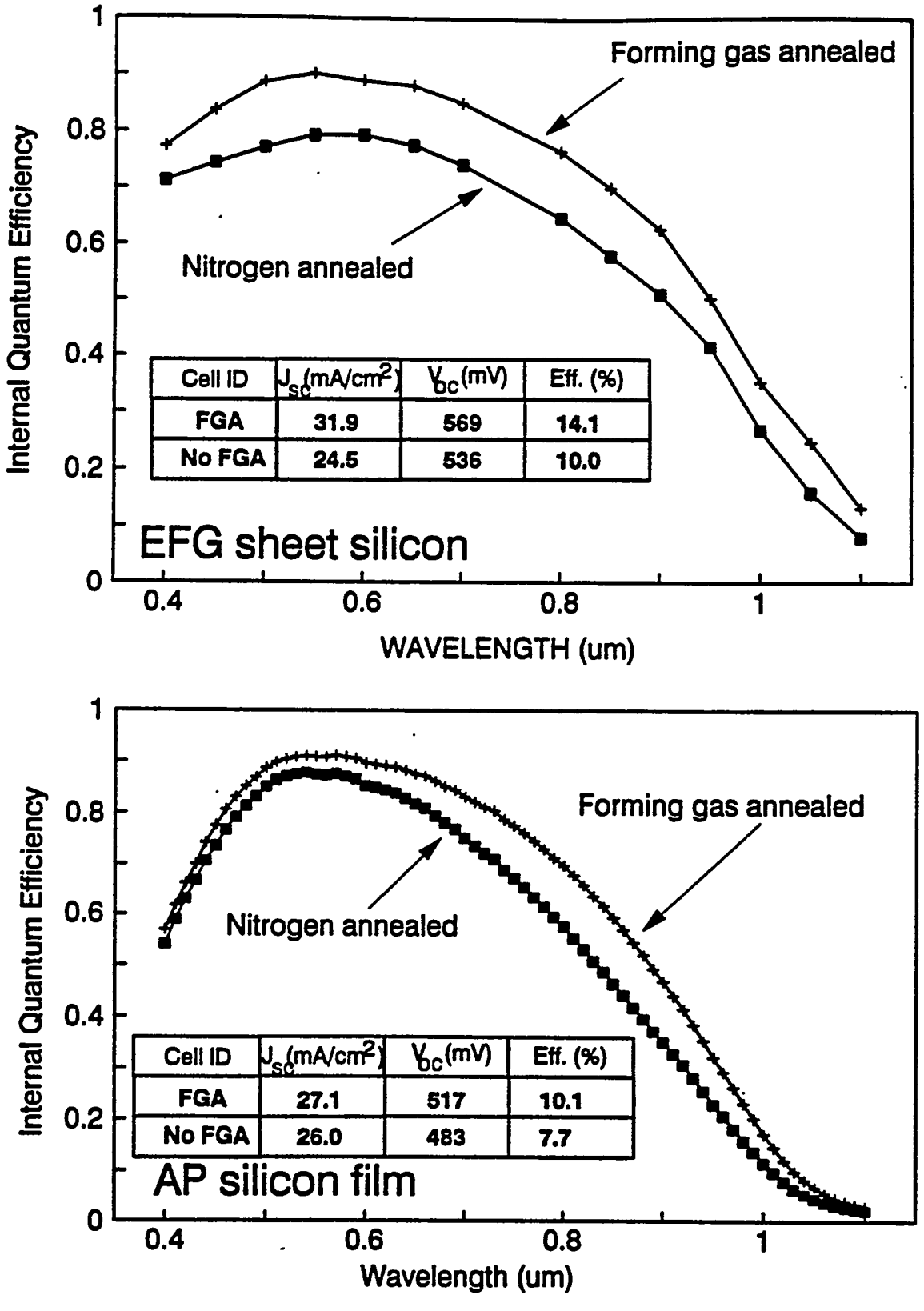


Figure 2.17. The effect of FGA on EFG Sheet ribbon and AP thin film silicon.

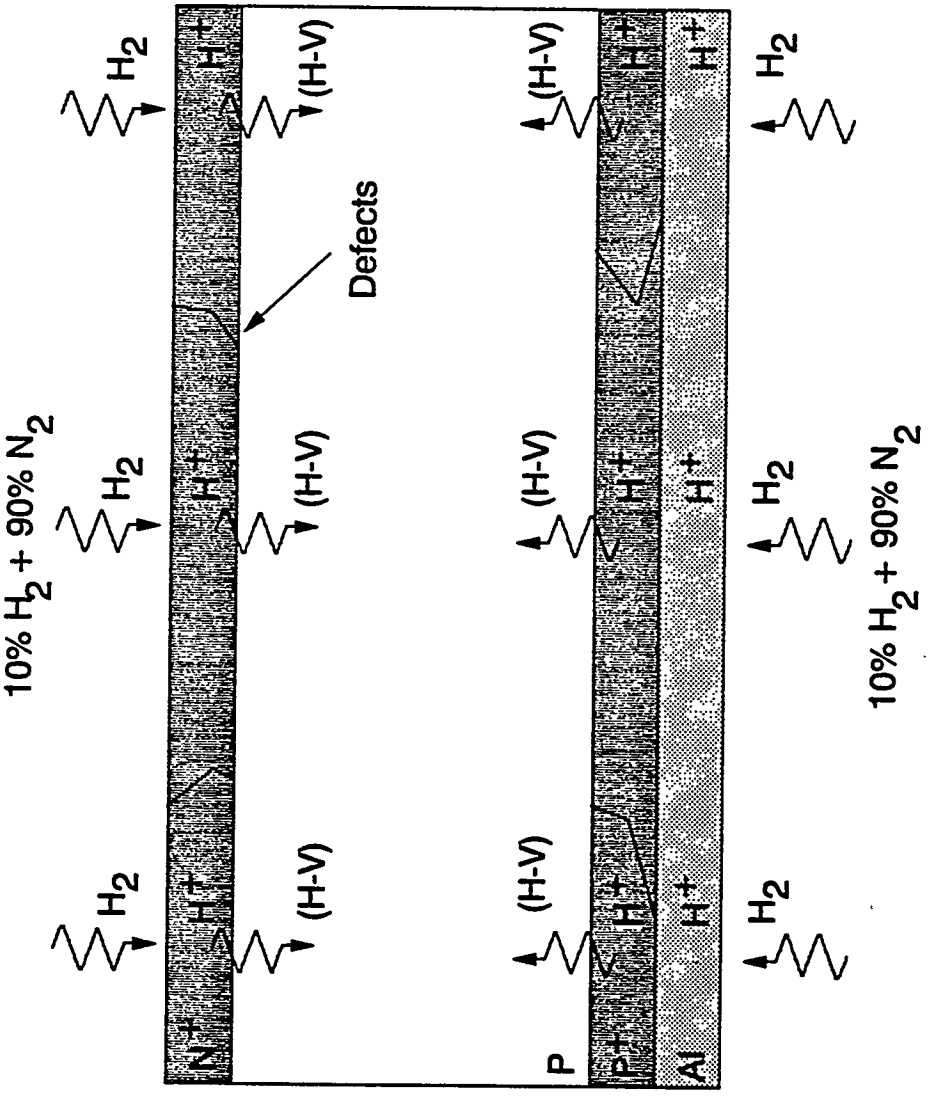


Figure 2.18. Model of hydrogen passivation by forming gas anneal

thermal evaporation on the cells. Figure 2.20 shows that the optimized process sequence indeed resulted in a record high efficiency of 17.8% for a mc-Si cell (tested and verified by Sandia) with V_{oc} of 628 mV and J_{sc} of 36.2 mA/cm^2. Dark I-V analysis gave a reverse saturation current density of 1.33×10^{-12} A/cm^2 and a series resistance of 0.45 Ω-cm^2. Open circuit voltage decay (OCVD) lifetime measurements gave an effective carrier lifetime of 32 μs measured at V_{oc}, which is quite respectable for such low resistivity (0.8 Ω-cm) multicrystalline silicon. As shown in section 2.1, without the optimized gettering conditions, passivation, and cell design, we were able to achieve only 14.8% efficient cells on this material. Figure 2.20 also shows the reflectance and internal quantum efficiency of the 17.8% efficient cell. Table 2.4 shows all the mcs cells we have fabricated so far with efficiencies greater than 17%. It should also be recognized that an optimum process sequence for multicrystalline silicon may be material specific because of the large variation in the material quality, grain size, and impurity and defect content of multicrystalline materials.

It should be noted that the efficiency distribution (Figure 2.21) was in the range of 16.8%-17.8% (tested and verified at Sandia). This difference in cell efficiency is partly due to nonuniform defect distribution in the Sitix mc-Si material. Figure 2.21 also shows the efficiency distribution on the wafer that produced a 17.7% efficient cell (all tested at NREL).

Table 2.4. High-efficiency multicrystalline silicon solar cells fabricated at Georgia Tech

Cell ID	Substrate	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	Efficiency (%)	Measured at
OPS-21	OTC	36.2	628	0.785	17.8	Sandia
GIT125-23	OTC	35.6	626	0.792	17.7	NREL
OPS-31	OTC	36.0	626	0.783	17.6	Georgia Tech
OPS-13	OTC	35.7	626	0.783	17.5	Sandia
GITCS205	OTC	35.7	612	0.800	17.5	NREL
GITCS106	HEM	36.2	614	0.782	17.4	NREL
NPS1-24	OTC	34.5	629	0.801	17.4	Sandia
OPS-12	OTC	35.6	625	0.782	17.4	Georgia Tech
OPS-11	OTC	35.6	625	0.781	17.4	Georgia Tech
GITCS110	HEM	35.9	613	0.791	17.4	NREL
GITCS207	OTC	35.0	615	0.805	17.3	NREL
GITCS108	HEM	34.7	618	0.802	17.3	NREL
GITCS109	HEM	35.9	616	0.782	17.3	Georgia Tech
GITCS101	HEM	35.7	613	0.790	17.3	Georgia Tech
GITCS203	OTC	34.9	615	0.803	17.2	Georgia Tech
GITCS111	HEM	35.8	615	0.781	17.2	Georgia Tech
NPS2-12	OTC	34.8	627	0.790	17.2	Sandia
OPS-22	OTC	35.4	621	0.781	17.2	Georgia Tech
GT125-43	OTC	34.8	627	0.790	17.2	Sandia
GITCS111	HEM	35.8	615	0.781	17.2	NREL
GITCS210	OTC	35.1	614	0.798	17.2	NREL
GITCS214	OTC	35.2	614	0.798	17.2	NREL
GIT225	HEM	34.3	626	0.790	17.0	Sandia
NPS2-24	OTC	34.7	622	0.786	17.0	Sandia
GITCS206	OTC	33.5	612	0.783	17.0	Georgia Tech
GITCS208	OTC	34.8	611	0.796	17.0	Georgia Tech
STPS3-32	OTC	34.9	622	0.782	17.0	Sandia
OPS-32	OTC	35.4	622	0.771	17.0	Georgia Tech

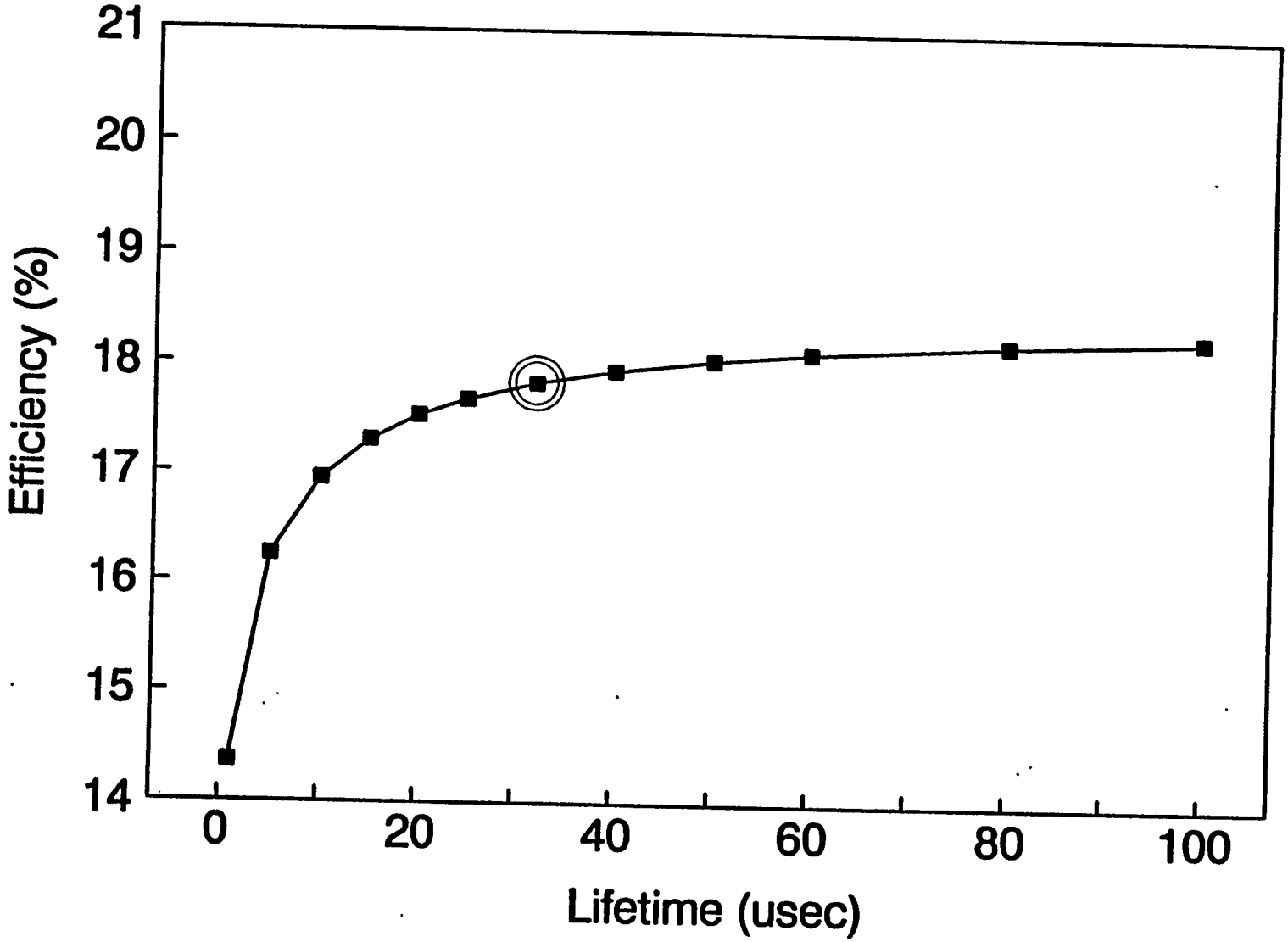


Figure 2.19. The effect of lifetime on the performance of the cells modelled by PC-1D.

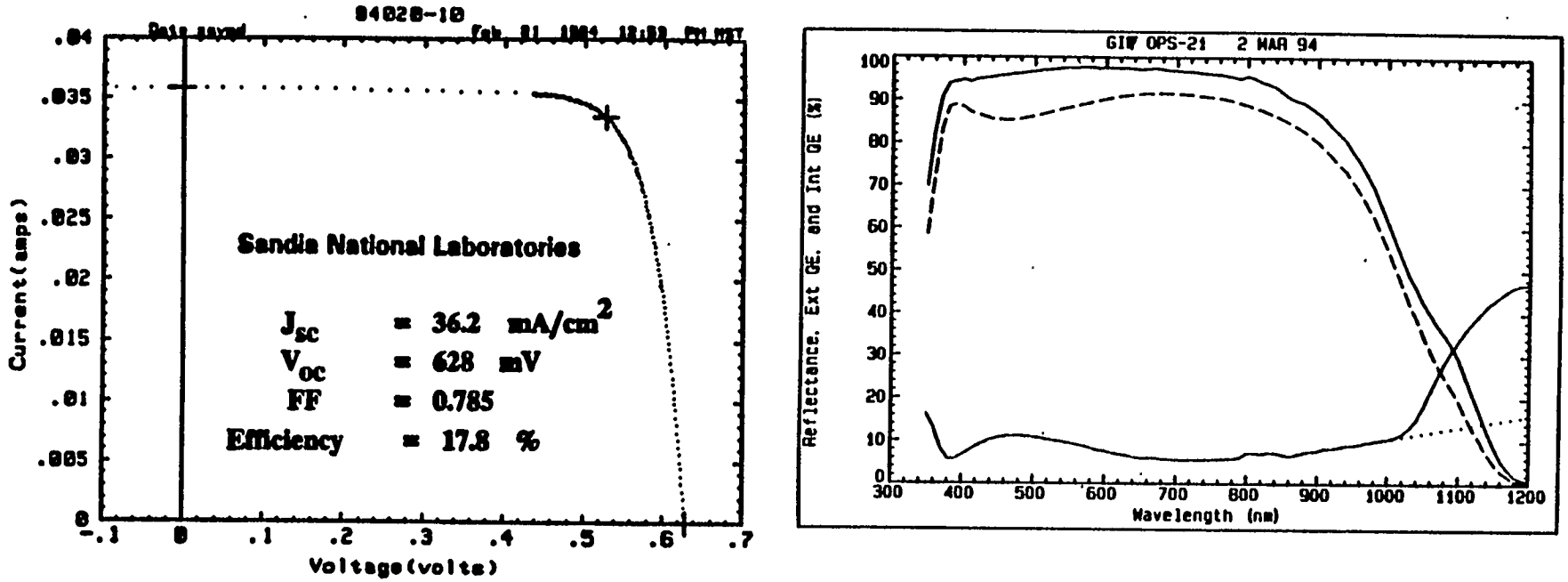


Figure 2.20. Reflectance and internal quantum efficiency of the 17.8% efficient Sitix multicrystalline cell.

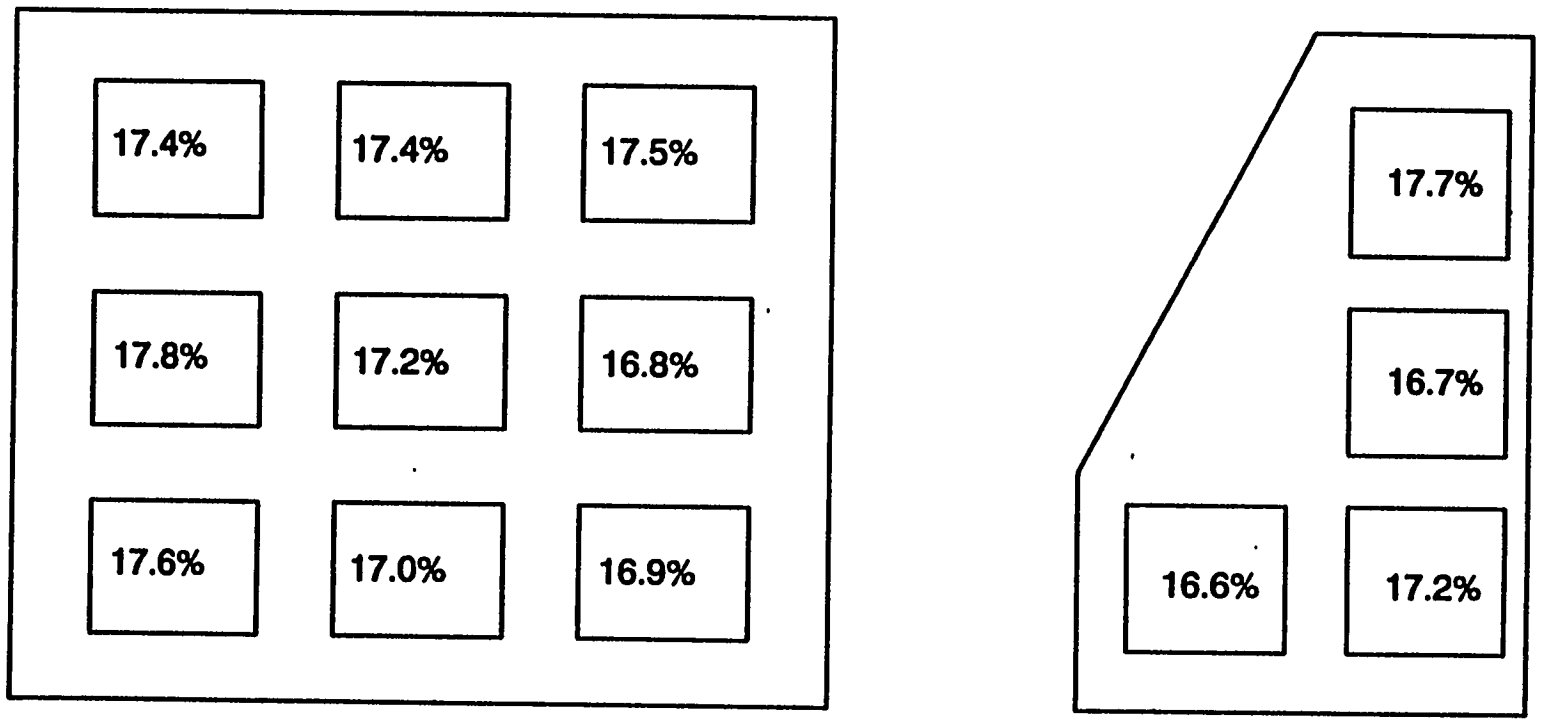
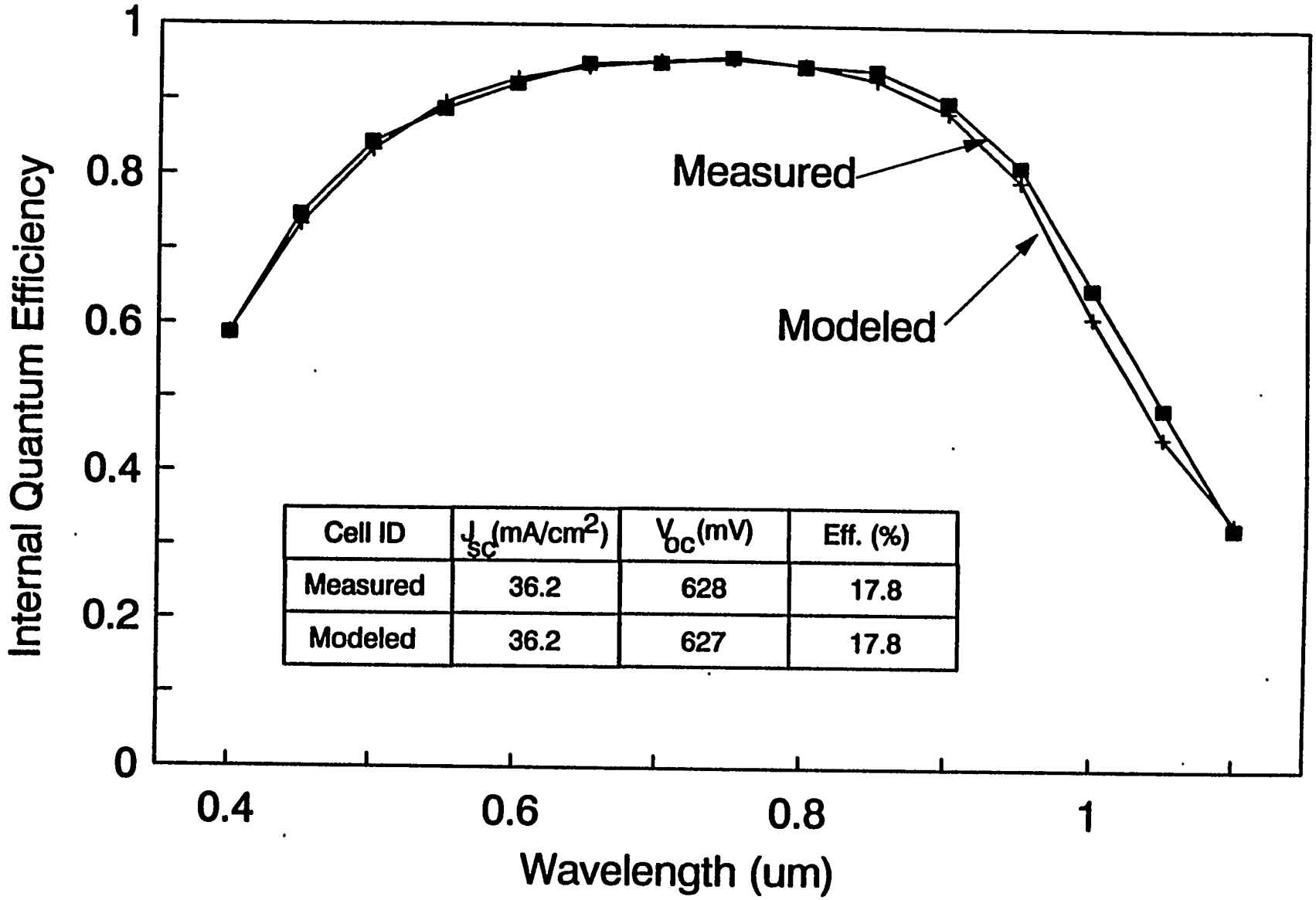


Figure 2.21. Cell efficiency distribution on the wafers produced 17.7% and 17.8% efficient cells.

2.8 Detailed Characterizations and Analysis to Model the Performance of the Record High Efficiency Multicrystalline Silicon Solar Cell

Solar cell modeling and characterization were performed to match the performance of the best cells obtained in this study and to provide guidelines for achieving greater than 20% efficient cells. Solar cell efficiency calculations were performed using the PC-1D model [8] in a mode that allows external input files for the doping profile and front surface reflectance. PC-1D is a software package for personal computers that uses finite-element, drift-diffusion analysis to solve the fully-coupled, two-carrier, semiconductor transport equations in one dimension [9]. Grain boundary defects and effects were ignored. Instead the measured bulk diffusion length was used as the input to assess whether grain boundary or intragrain defects dominate the cell performance. A good match between the measured and calculated cell parameters and IQE would suggest that intragrain defects dominate it. A significant mismatch would indicate the importance/dominance of grain boundary defects on the cells. Model calculations were performed to match the performance of the 17.8% efficient cell using the PC-1D program with the input parameters shown in Table 2.5. Figure 2.22 shows that the model calculations are in reasonably good agreement with the experimentally measured cell parameters, in spite of ignoring the grain boundary defects and effects. Figure 2.22 shows a very good match between the measured and calculated IQE for the 17.8% efficient cell. A measured OCVD effective bulk lifetime of 32 μs was used in the model calculation. This indicates that in properly-gettered, large-grain multicrystalline cells, intragrain defects are probably more important than the grain boundary defects in dictating the cell performance.



Cell ID	J_{sc} (mA/cm^2)	V_{oc} (mV)	Eff. (%)
Measured	36.2	628	17.8
Modeled	36.2	627	17.8

Figure 2.22. Comparison of the calculated and measured cell parameters and IQE for the high efficiency multicrystalline silicon cell.

2.9 Guidelines for Achieving 20% Efficient MC-Si Cells

After matching the measured cell parameters of the 17.8% efficient multicrystalline cell, attempts were made to change the cell design and material properties, such as R_{series}, cell thickness, front and back SRV, BSF thickness, lifetime, and surface texturing, to provide guidelines for achieving even higher efficiencies. Table 2.6 shows quantitatively the effect of changing some of the design parameters on the performance of the cell. Table 2.6 shows that a change in FSRV has very little effect on the cell efficiency for this cell structure. An increase in the carrier lifetime from 32 to 100 μsec increases the absolute efficiency by 0.5% (case d) for this cell design with ~1.5 μm deep unpassivated BSF. Therefore additional gettering will not do much for this cell unless the BSF or BSRV are improved. Figure 2.23 shows that initial gettering was very important for this cell, because the efficiency increases rapidly with lifetime (τ) up to a lifetime value of about 40 μs. Beyond τ= 40 μs, relative improvement in cell efficiency becomes very small. Model calculations show that even with the increase in the bulk lifetime value up to 1 ms, an efficiency of only 18.5% can be realized with this cell structure. Since J_{01} is dominated by base or J_{0b} in this cell, reduced FSRV from 6000 to 50 cm/sec also has very little effect on the performance of this cell (case b). However a significant gain in the performance, from 17.8% to 18.5%, can be realized by reducing the BSRV alone from 10^6 to 500 cm/sec by growing a passivating oxide on the back surface (case g). Similarly surface texturing alone (case f), using slats or grooves with a pitch of 100 μm and slat angle of 60°, can also raise the efficiency of this cell to 18.5% (Figure 2.23). Such surface texturing can be achieved by a dicing machine [10], [11] or laser grooving [12]. A combination of reduced BSRV and front surface texturing can produce 19.1% efficient cells (case h). Finally a combination of texturing, reduced BSRV, and increase in lifetime up to 100 μs can raise the efficiency of the cell to 20.2% (case i). It should be noted that there could be some inaccuracy in the absolute values of

Table 2.5. Input parameters to PC-1D for model calculations

- Cell area of 1 cm^2.
- Cell thickness of 400 μm.
- p-type base with resistivity of 0.8 Ω-cm.
- External doping file, 16 Ω/□ Erfc doping etched to 80 Ω/□ sheet resistance, junction depth of ~0.5 μm.
- Erfc doping profile with surface concentration of $5x10^{18}$ cm^2 for ~1.5 μm thick Al BSF
- Measured bulk lifetime of 32 μs.
- FSRV of 6000 cm/s.
- BSRV of 10^6 cm/s at metal-silicon contact.
- Measured J_{02} of $4.37x10^{-7}$ A/cm^2 and ideality factor of 2.8.
- Measured series resistance of 0.45 Ω-cm^2.
- External input file for the measured front surface reflectance.
- 75% efficient back surface reflectance.
- 81% front internal reflectance.
- Flat front and textured back surface.
- Spectrum AM1.5 Global.

Table 2.6. Modeling the effect of selected design parameters on performance of the 17.8% efficient cell

Changed Parameters	J_{sc} (MA/cm^2)	V_{oc} (mV)	FF	Efficiency (%)
a: Cell thickness = 250 μm	36.9	636	0.785	18.4
b: FSRV = 50 cm/sec	36.5	629	0.785	18.0
c: R_{series} = 0.1 Ω-cm^2	36.2	627	0.809	18.4
d: Lifetime (τ) = 100 μs	36.7	634	0.785	18.3
e: BSF thickness = 10 μm	36.7	631	0.788	18.2
f: Front surface texturing	38.2	618	0.784	18.5
g: BSRV = 500 cm/sec	37.2	634	0.785	18.5
h: Front surface texturing and Reduced BSRV (f+g)	39.0	624	0.785	19.1
i: Lifetime of 100 μsec, Front surface texturing, and Reduced BSRV (d+f+g)	40.0	644	0.784	20.2

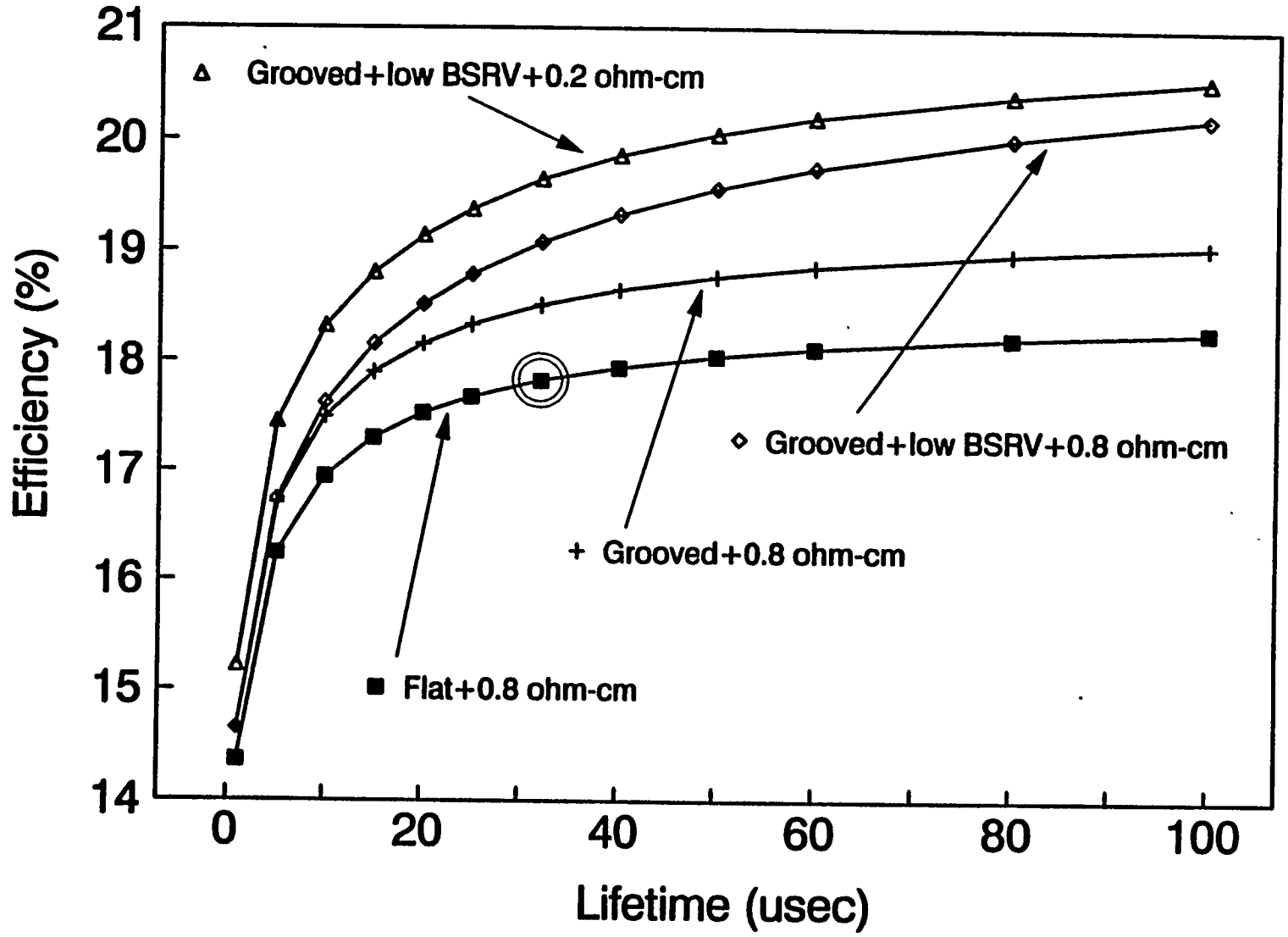


Figure 2.23. The effects of lifetime and surface texturing on multicrystalline cell performance.

the calculated cell parameters due to assumptions; nevertheless, these model calculations provide useful guidelines for achieving 20% efficient multicrystalline silicon cells

2.10 Surface Texturing of MC-Si Wafer for Light Trapping

We have shown [13] that multicrystalline silicon solar cells with efficiencies close to 18% can be achieved on cast material by a combination of improvement in casting technology and in cell fabrication process. For highly efficient crystalline silicon solar cell devices some form of surface texturization has to be implemented in order to enhance the optical path length within the material and to reduce the reflection losses. Different light trapping schemes have been developed for monocrystalline silicon solar cells using a combination of photolithography and anisotropic alkaline etching relies on the regular crystallographic structure of the crystalline silicon to improve single crystalline cell performance. Regular inverted pyramids [14], random texturing and V-grooves are some examples of successful texturing schemes for single crystalline silicon. Pyramidal or grooved microstructures are composed of facets of <111> crystallographic planes. In multicrystalline silicon, the above the methods are rather ineffective due to the irregular distribution of crystal orientations. The overall spectral reflectance for a multicrystalline substrate after anisotropic alkaline etching is not as good because the substrates has grains with different crystal orientations. Due to the lack of a cost- effective texturing process, commercial multicrystalline silicon wafers are often lightly textured by chemical etching prior to cell processing and antireflection coating. Therefore, there is a strong need for an orientation-independent, cost-effective and efficient texturing method that can be implemented in an industrial environment.

Several approaches for texturing multicrystalline silicon wafers have been considered but none are suitable for commercial production at this time because of perceived development and/or

processing costs. Laser-beam texturing [15] is costly and requires a high-energy laser and long exposure time. Reactive ion etching has been used to texture multicrystalline silicon wafers with an oxide mask. Results have been promising, producing 20% more short-circuit current. This etching process is suitable for large-scale production, however the mask is formed photolithographically and requires additional processing steps. For the purpose of reducing the surface reflectance and introducing light trapping in multicrystalline silicon solar cells, several investigators have recently begun to use a dicing machine for mechanical grooving of the multicrystalline silicon substrate. This technique offers maximum flexibility for changing groove depth, shape and pitch. It provides very good antireflection and light trapping properties and is independent of the structural quality of the starting material.

We have made some attempts to mechanically groove mc-Si by a dicing saw. The average integrating sphere measurements on an uncoated wafer with 200 μm depth grooves and 100 μm spacing gave a reflectance of 3.8% (from 400 to 1100 nm), which represents the lowest reflectance reported to date on uncoated multicrystalline silicon. The minimum reflectance for this sample was 3.3% at 770 nm. After, using a double layer ZnS/MgF_2 antireflection coating, the average reflectance went down to 1.5%, with a minimum of 0.87% at 540 nm (Figure 2-24). Because of the very low reflectance of an uncoated grooved wafer, a double-layer AR coating does not show a significant improvement. Instead we found that a single-layer AR coating (SiO_2 or SiN) results in almost the same reflectance as a double-layer coating on these grooved samples. Because of the high surface recombination velocity of the grooved surface, a single-layer SiO_2 or SiN AR coating may be more advantageous due to better surface passivation characteristics (which is crucial in grooved cells).

In conclusion, a new mechanical texturing scheme with a conventional blade followed by a chemical etching resulted in the record-low average reflectance of 3.8% on bare-grooved-

multicrystalline silicon. Such low reflectance allows the use of a thick SiO_2 single-layer AR coating, which can be more beneficial for grooved multicrystalline cells because of its lower surface recombination velocity.

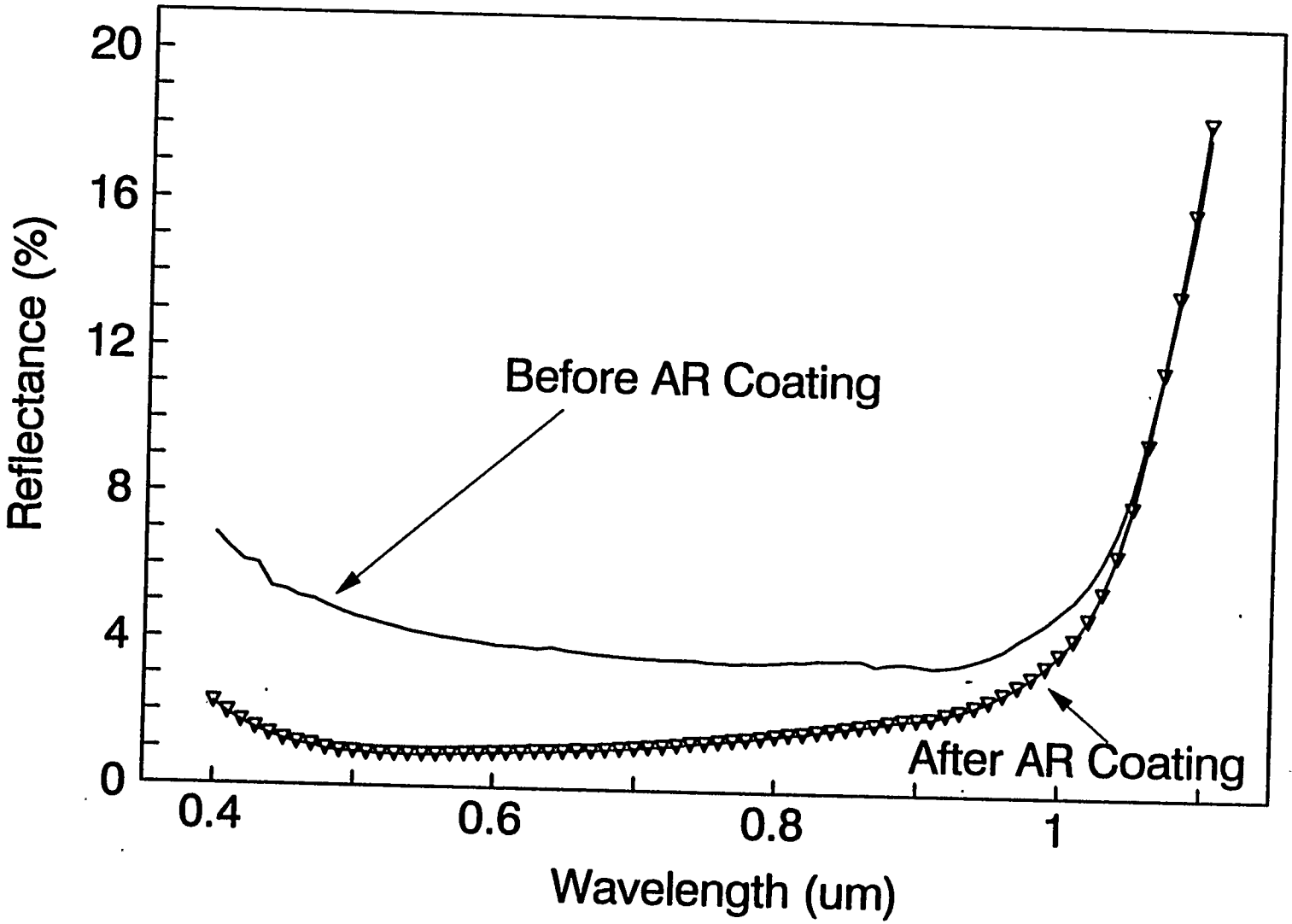


Figure 2.24. The reflectance of the best grooved multicrystalline silicon before and after AR coating.

2.11 Endnotes

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CHAPTER 3. HIGH-EFFICIENCY CELLS ON SINGLE-CRYSTAL SILICON

Chapter 2 described the research and development of high efficiency cells with multicrystalline silicon. This chapter discusses the progress on single crystal silicon. Figure 3.1 shows that four kinds of single-crystal cells are being fabricated in our labs. These cells include (a) simple n^+-p-p^+ baseline cell (SBLC) with phosphorus-diffused emitter and Al back surface field (BSF), (b) advanced baseline cell (ABLC) with deep phosphorus diffusion underneath the grid and point Al contacts on the back, (c) textured baseline cells (TBLC) with random pyramid texturing on front for light trapping and (d) IBLC cells with inverted pyramid texturing on front and localized diffusion and point contacts on the back. SBLC cells involve two masks while IBLC is a very complicated six-mask process.

Figure 3.2 shows a schematic diagram of the SBLC process, which starts with phosphorus diffusion on the front, followed by Al BSF. During the Al drive-in, a five-minute oxidation is performed to grow 100 Å thick passivating oxide on top of the emitter. The front grid pattern is formed by photolithography and a lift-off technique. The back contact is formed by evaporation of Ti/Ag, and the front grid contact is finished by 4-6 μm thick silver plating on top of evaporated thin Ti/Ag contact. Finally a double-layer ZnS/MgF_2 antireflection coating is thermally evaporated on the front-side.

Table 3.1 shows the SBLC cells with efficiencies in the range of 18.5-19.5% on 0.2 ohm-cm FZ silicon. Figure 3.3 shows the internal quantum efficiency of one of the best SBLC cell tested and verified at Sandia National Laboratories. This cell had an efficiency of 19.4% with excellent short wavelength response. However, the long wavelength response drops sharply, partly because of the use of 0.2 ohm-cm silicon with diffusion length of only 250 microns.

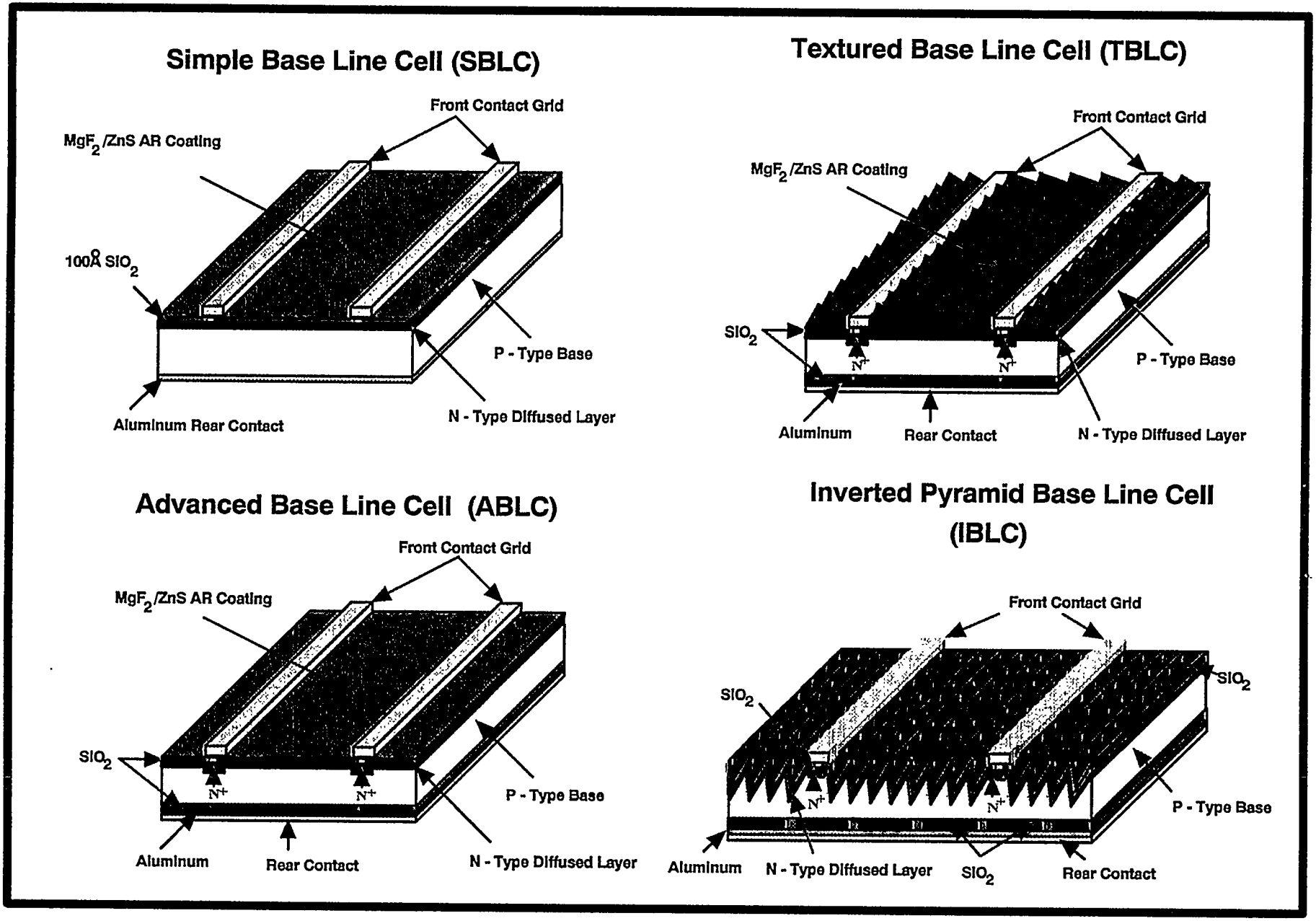

Figure 3.1. Four kinds if single-crystal cells: (a) simple n^+-p-p^+ baseline cells (SBLC) with phosphorus diffused emitter and Al back surface field (BSF), (b) advanced baseline cell (ABLC) with deep phosphorus diffusion underneath the grid and point Al contacts on the back, (c) textured baseline cells (TBLC) with random pyramid texturing on front for light trapping and (d) IBLC cells with inverted pyramid texturing on front and localized diffusion and point contacts on the back.

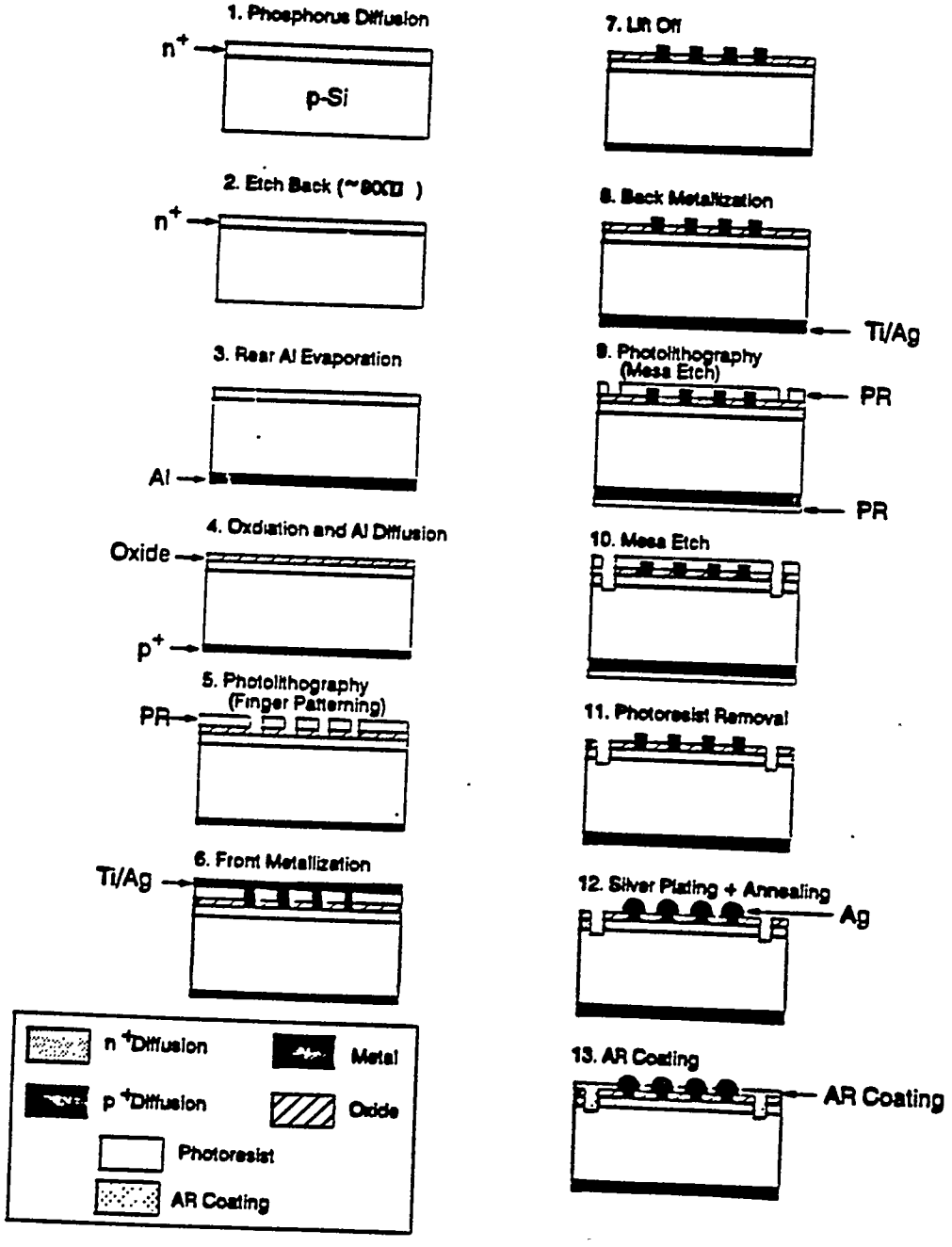

Figure 3.2. Process outline for simple base line solar cell (SBLC).

Table 3.2 shows cell data of a few advanced baseline cells with double phosphorus diffusion. Because of deep grid diffusions, the field diffusion sheet resistance was raised to 120 ohm-sq as opposed to 80 ohms-sq in the case of SBLC cells. This reduced the heavy doping effects, resulting in higher V_{oc}, on the order of 690 mV as opposed to 660mV for the SBLC cells. ABLC cell efficiencies of about 20% were achieved. Another advantage of the ABLC process is reflected in the IQE curves shown in Figure 3.4, which, due to reduced contact recombination and heavy doping effects, not only gave higher short wavelength response compared to the SBLC cells, but also resulted in better long wavelength response. This may be the result of a gettering-induced lifetime increase due to the intense phosphorus grid diffusion.

We have also fabricated textured TBLC and IBLC cells, in addition to the flat SBLC and ABLC cells. Figure 3.5 shows that the IBLC cell involves six masks. A second mask is used for Al or boron localized BSF. A third mask is used to perform deep phosphorus diffusion underneath the grid lines. A fourth mask is for field diffusion and cell isolation. After 100-Å- thick front thermal oxide passivation, a fifth mask is used to make small-area point contacts to localized rear diffusion. The sixth and final mask is used to define front grid lines. The IBLC cells may be ideal to test the capability of a fabrication lab, but because of their complexity and the many mask steps required to make them, they may not be able to meet the criteria for cost-effective solar cells. An IBLC run takes roughly three weeks in our lab and is also quite vulnerable to failures because of the six mask process, and for that reason not too much emphasis was placed on the IBLC runs this year. Instead, more effort was directed toward developing simplified, rapid and low-cost processes.

Table 3.1. SBLC Cells tested and verified by Sandia.

Cell ID	V_{oc} (mV)	J_{sc} (mA/cm2)	CFF	EFFY
RUN TGM (NEW 1X1)				
2	664.8	35.7	.817	19.4
3	664.8	35.7	.812	19.3
6	664.8	35.8	.814	19.4
7	664.1	35.6	.808	19.1
10	663.4	35.7	.788	18.6
11	664.8	35.5	.819	19.3
12	663.2	35.3	.814	19.1
14	663.7	35.2	.819	19.2
RUN JT3 (OLD 1X1)				
4	666.8	35.2	.797	18.7
14	664.9	35.2	.804	18.8
15	658.4	34.8	.797	18.3
16	663.0	35.3	.787	18.4
RUN TGM (2X2'S)				
1	658.6	34.3	.820	18.5
2	659.4	34.6	.819	18.7
3	658.8	34.4	.818	18.6
4	658.6	34.2	.817	18.4

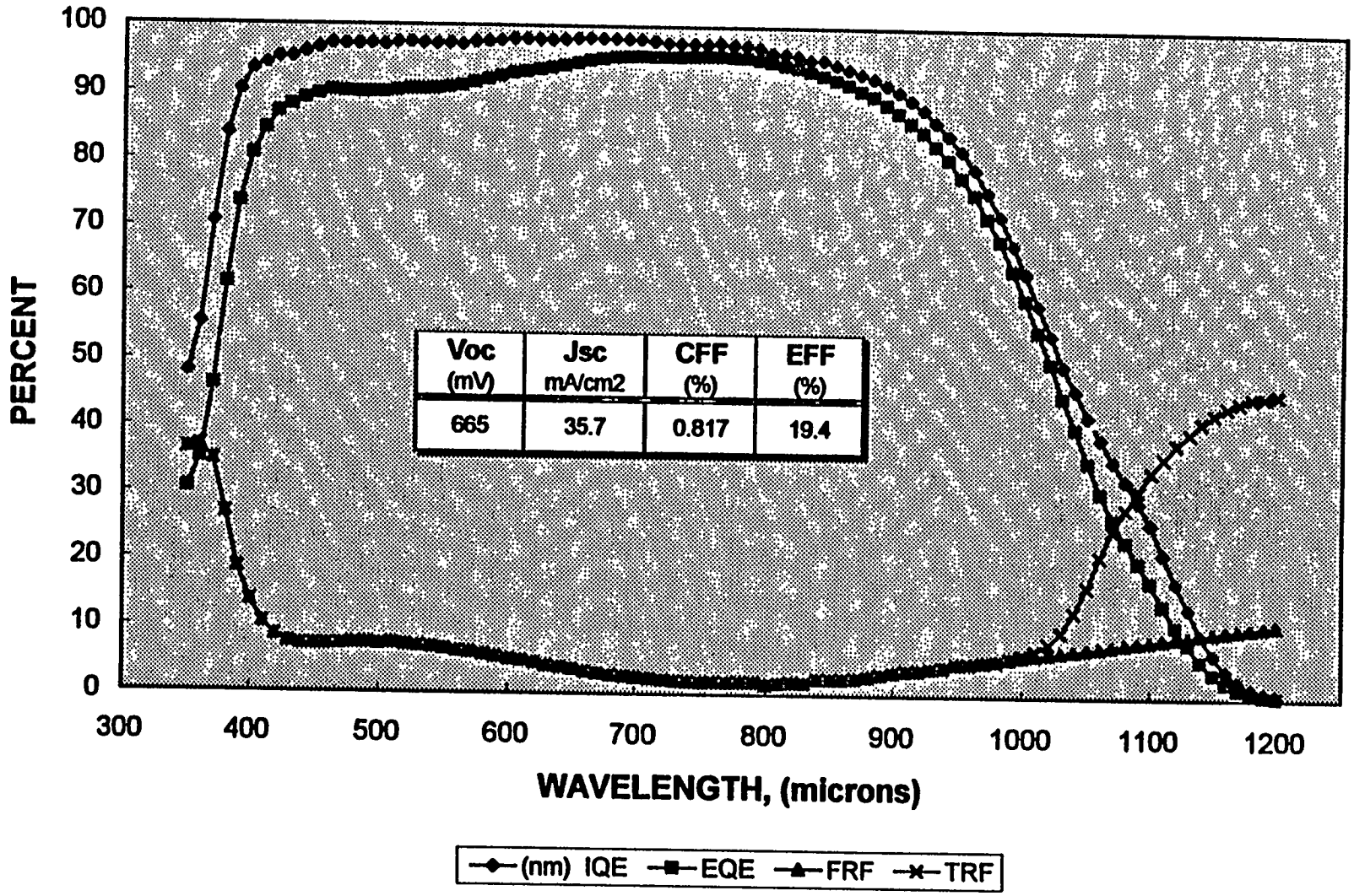

Figure 3.3. IQE and REF for SBLC cell.

Figure 3.6 shows the IQE response of a ~21% efficient IBLC cell made on a 0.2 ohm-cm FZ Si-. For comparison we have plotted the IQE response of the 23.5% efficient UNSW cell. Figure 3.6 shows that the short wavelength response of both the cells is quite comparable, but the long wavelength response of our cell is lower. This is largely because we used 0.2 ohm-cm silicon with bulk lifetime of 30 μs while UNSW used 2 ohm-cm silicon with a lifetime of 2 ms.

Table 3.2. Run SN2 2x2 ABLC Solar Cell Data

Cell	V_{oc} (mV)	J_{sc} (mA/cm^2)	CFF	EFFY
WAFER 1				
1-1	681.2	36.8	.811	20.3
1-2	677.8	37.0	.809	20.3
1-3	676.7	36.8	.809	20.2
1-4	675.7	36.7	.811	20.2
WAFER 2				
2-1	667.1	36.7	.806	19.8
2-2	666.5	36.7	.814	19.9
2-3	665.5	36.3	.794	19.2
2-4	666.4	36.2	.784	18.9

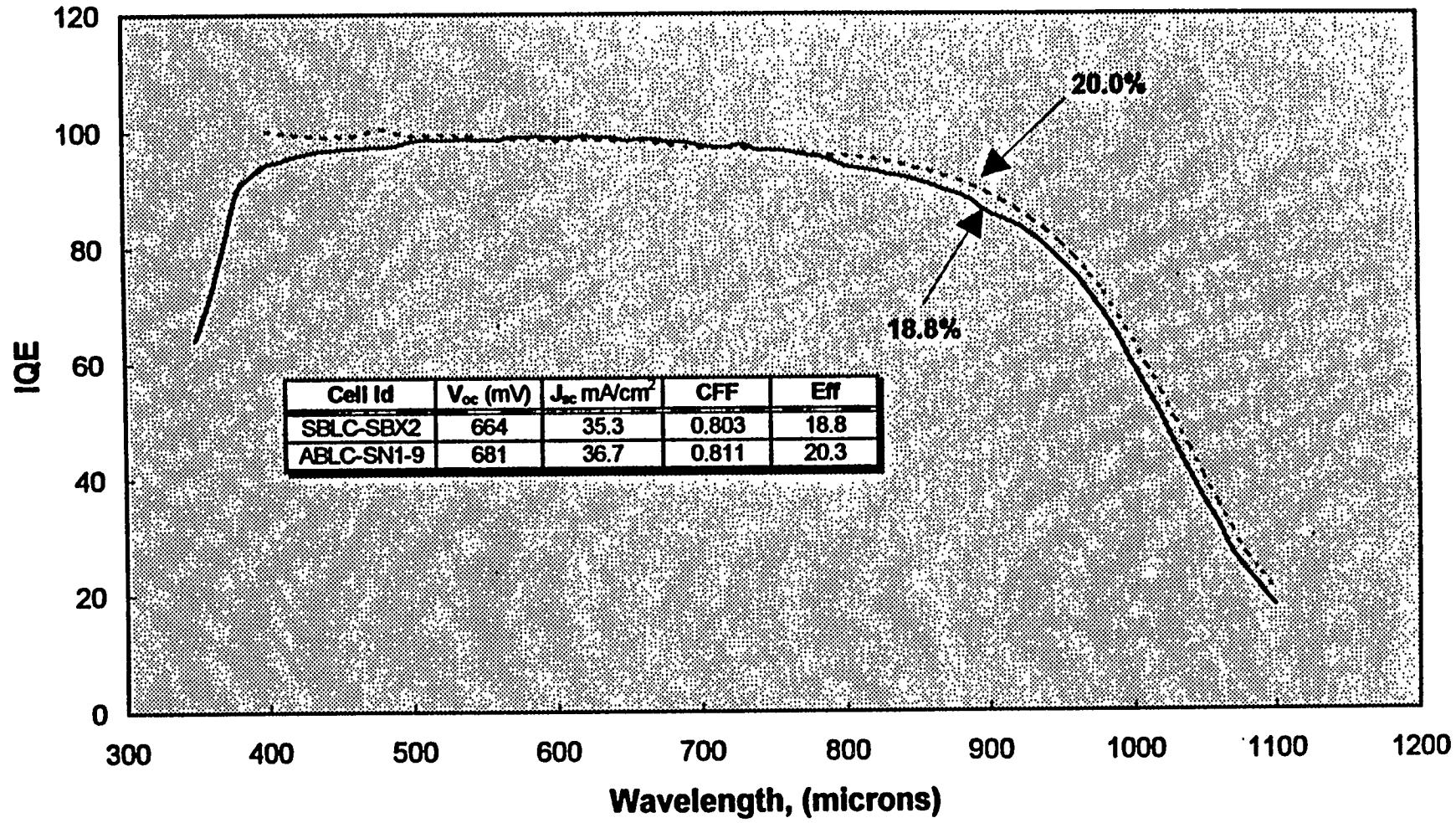

Figure 3.4. Optical response data.

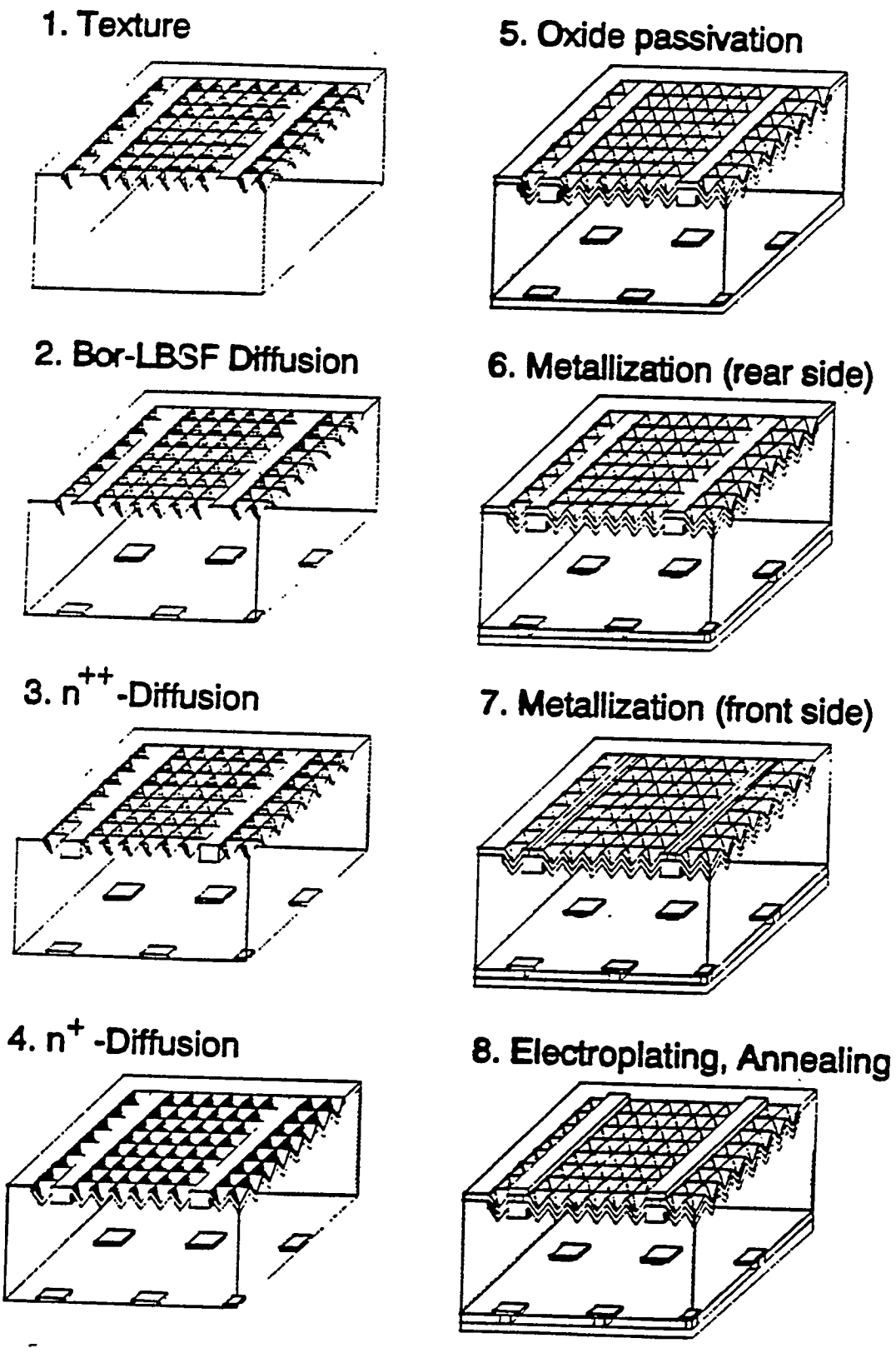

Figure 3.5. Advanced IVP silicon solar cell process.

Model calculations in Figure 3.7 show that it is possible to achieve 25% efficient IBLC cells. However, if surface recombination velocities are on the order of a few hundred, cm/S then 0.2 ohm-cm silicon needs to have a lifetime of 1 ms, which does not exist, or 2-10 ohm-cm silicon should have a lifetime of several ms, which is possible but hard to maintain during the prolonged cell processing. The lower part of the Figure 3.7 shows that in order to achieve $\geq$ 25% IBLC cell efficiency, using 2 ohm-cm with 2 ms lifetime, SRV values of less than 50 cm/s will be required. This not only requires point contacts, but very good front and back surface passivation.

In summary, in the area of single-silicon solar cells, we have fabricated 19% efficient SBLC cells, 20% efficient ABLC cells and ~21% efficient IBLC cells.

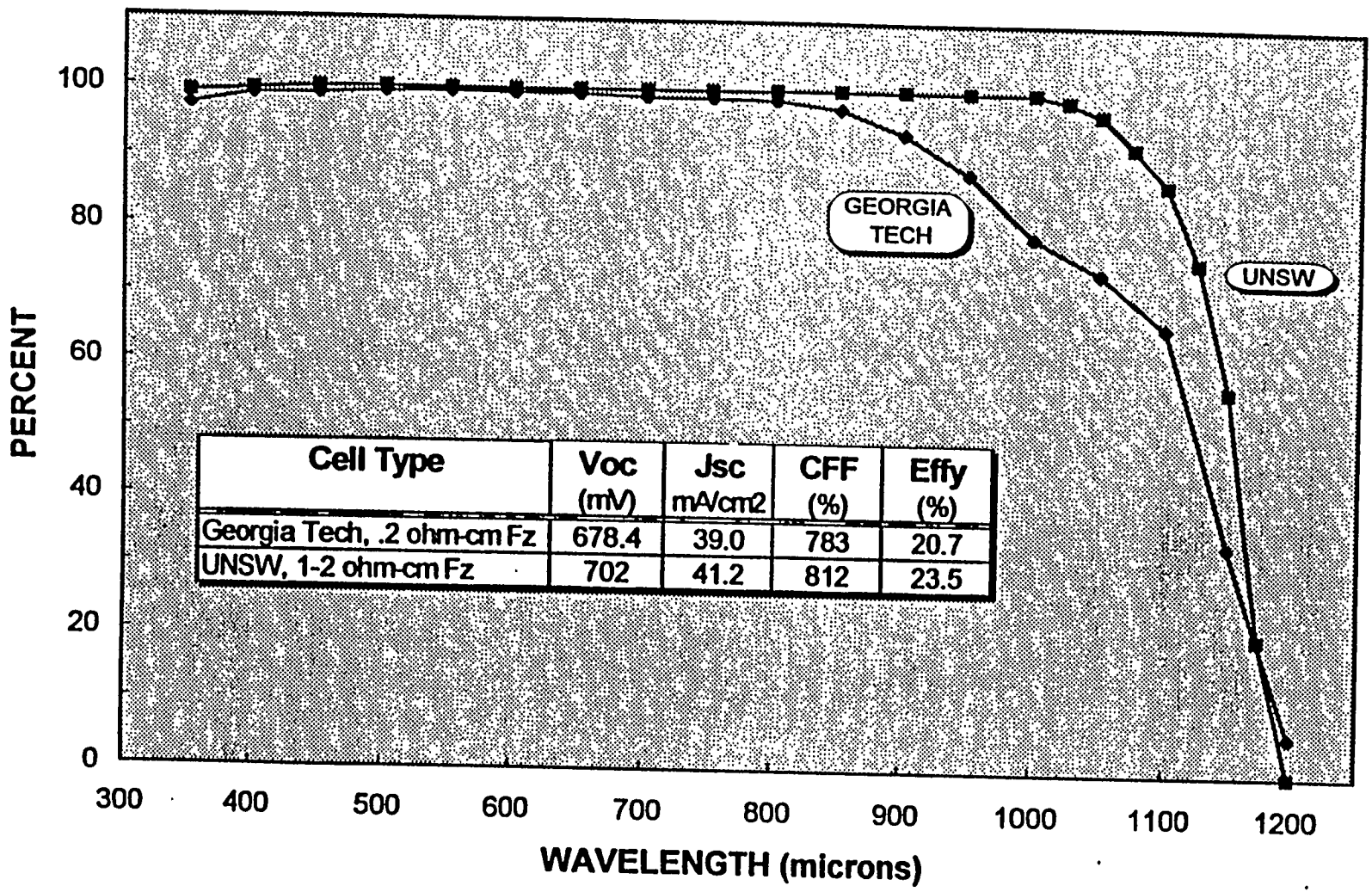

Figure 3.6. Internal quantum efficiency.

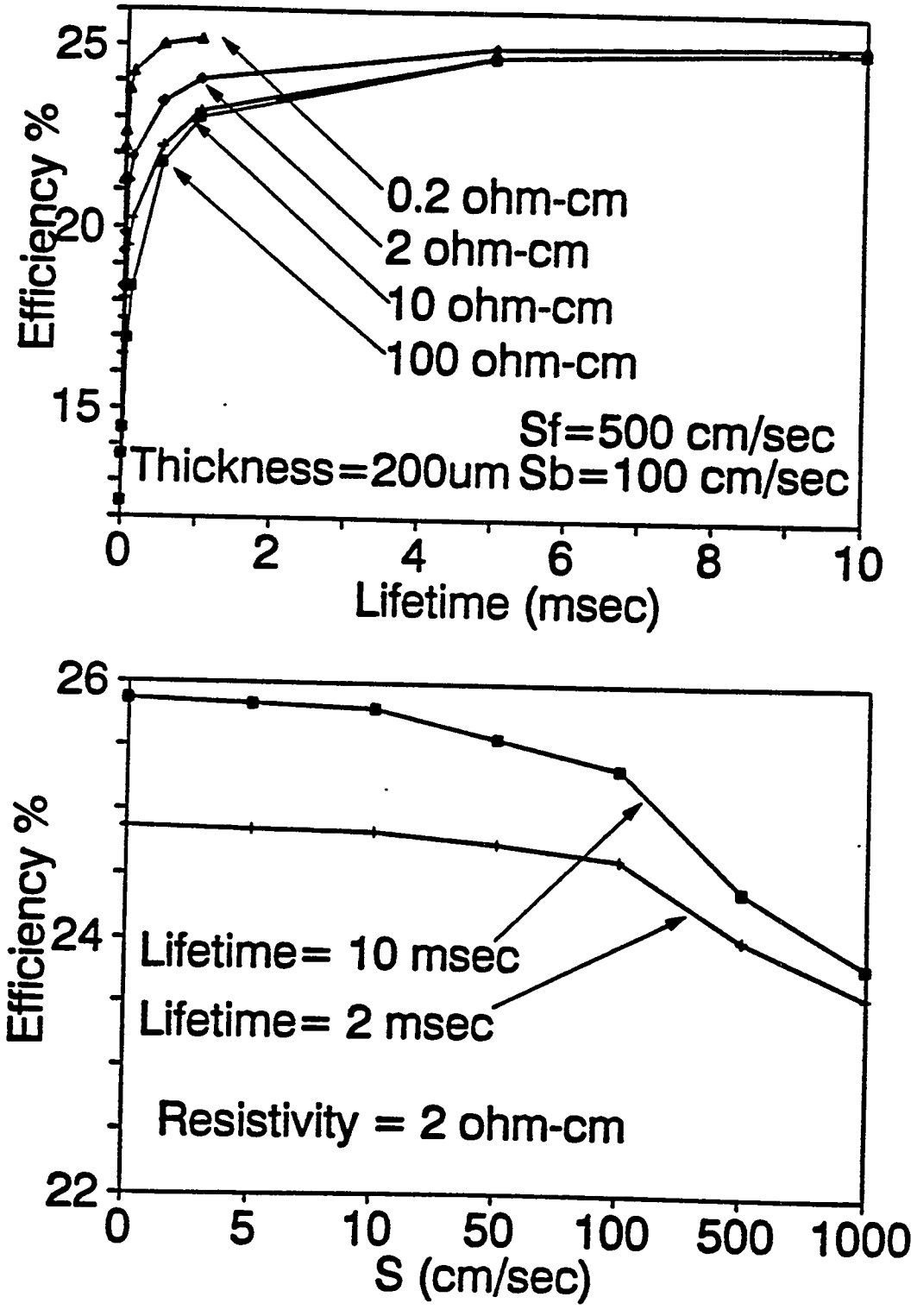

Figure 3.7. Approach toward 25% efficient inverted pyramid silicon solar cells.

CHAPTER 4. SURFACE/BULK DEFECT PASSIVATION BY PLASMA ENHANCED CHEMICAL VAPOR DEPOSITED

4.0 Modeling And Characterization of Interface State Parameters And Surface Recombination Velocity At Plasma Enhanced Chemical Vapor Deposited SiO_2-Si Interface.

4.0.1 Introduction

Low surface recombination velocity and high effective recombination lifetime both are critical for high-efficiency Si solar cells. Thin thermal oxides grown at high temperatures (850 - 1050°C) are generally used for surface passivation. [1] However, low-temperatures deposited oxide is more desirable because of the possibility of high-temperature induced degradation of bulk lifetime, increased flexibility in cell processing and reduced cell cost.

We have developed and reported a low-temperature process to passivate a Si surface by plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 at 250°C followed by forming gas anneal at 350°C in a tungsten halogen lamp furnace. This process gives low effective surface recombination velocity (S_{eff}) of less than 2 cm/sec at intrinsic FZ-Si/PECVD-SiO_2 interface. [2] It should be noted that this process is compatible with a double-layer anti-reflection coating process using PECVD SiO_2 and SiN. [3] Therefore PECVD oxide passivation is considered promising for improving the efficiency and cost effectiveness of Si solar cells.

The low S_{eff} of PECVD SiO_2 passivated Si surface is attributed to a combination of moderately low density of interface states at midgap (D_{it} = (1 - 10) x 10^{10} cm^{-2} eV^{-1}) and high positive oxide-fixed charge density [Q_{ox} = (1 - 10) x 10^{11} cm^{-2}]). [2] The higher Q_{ox} results in increased downward band bending (ψ_s) at the surface. The larger ψ_s lowers surface hole concentration for recombination and consequently reduces the

S_{eff}. Therefore even if the D_{it} is moderately high, it is possible to get low S_{eff} with higher Q_{ox}. A preliminary study shows that D_{it} and Q_{ox} increase with increasing PECVD oxide deposition rate. [4] However, Q_{ox} increases at a higher rate than D_{it}. These results suggest the possibility of optimizing the PECVD process to get low S_{eff} with high throughput. In order to optimize the PECVD passivation process for Si cells, a knowledge of the interface properties of PECVD SiO_2-Si interface and model calculation of S_{eff} as a function of D_{it}, Q_{ox} and other interfaced parameters are essential.

Numerous studies have been conducted on the properties of the thermal SiO_2-Si interface, along with realistic modeling of the recombination at the interface using experimentally obtained parameters. [5-8] The modelling studies on the thermal Si-SiO_2 interface have shown that besides the interface state density, the capture cross-section model for electrons and holes can significantly affect the calculated value of S_{eff}. However, the fundamental properties of PECVD SiO_2-Si interface states including the capture cross sections have not yet been investigated.

Recently, several authors reported on the capture cross sections for electron and holes at the thermal SiO_2-Si interface using small bias DLTS method. [8-10] Although this method gives energy dependence of capture cross sections for majority carriers, capture cross sections for minority carriers cannot be obtained. When temperature is varied in the DLTS measurements, the interface state charge density changes with temperature because of the shift in the Fermi level, which in turn causes significant flat band voltage shift in CV measurement especially when D_{it} is high. Therefore the bias setting for the DLTS measurement should be temperature dependent, which makes the measurement complicated. In this paper we have employed a simple method for measuring S_{eff} as a function of gate bias voltage in order to obtain the information on capture cross sections at PECVD SiO_2-Si interface states. [11] The principle of this measurement is described in Section 4.3.2.

In this work, we first performed capacitance voltage (CV) measurements on the metal oxide semiconductor (MOS) structure and photoconductive voltage decay (PCD) measurements as a function of

gate bias voltage to investigate the properties of PECVD SiO_2-Si interface states. Then we used a combination of these measurements and the model calculations to obtain the information about the defect parameters (D_{it}, σ_n, σ_p) at the interface. Finally, model calculations were extended to obtain the correlation between D_{it}, Q_{ox} and S_{eff}, utilizing the experimentally determined parameters at this interface.

4.0.2 Experimental

Boron-doped p-type (100) 5-inch diameter CZ-Si wafers with resistivity of about 5 Ω-cm was used in this study. Two samples (a quarter of the wafer) cut from the same wafer were used for PCD and MOS measurements. After cleaning the wafers, 1000 Å PECVD oxide was deposited at 250°C on the front surface for the MOS sample. Detailed PECVD deposition conditions have been reported elsewhere. [2] After evaporation of Al on both front and back surfaces, the MOS samples were annealed at 350°C in forming gas for 20 min in a tungsten halogen lamp furnace. The lamp annealing in forming gas with Al present was found to be extremely effective in passivating the PECVD SiO_2-Si interface. [4] The same procedure on the back surface gave good ohmic contact. After defining 1-mm-diameter MOS capacitors on the front, the D_{it} distribution in the band gap was determined by the combination of standard high frequency (HF) and quasi-static (QS) CV measurements. [5] The fixed oxide charge Q_{ox} was determined by the HF-CV measurement.

In order to measure gate bias dependence of S_{eff} PECVD SiO_2 was deposited on both sides of another sample. The same deposition conditions were used. After the forming gas anneal, ~ 1000 Å Indium tin oxide (ITO) was sputtered on both surfaces of S_{eff} measured samples to form transparent conducting gate electrodes for applying bias. The measurement system and the sample configuration are similar to that illustrated in Yablonavich, Swanson, and Eades. S_{eff} was measured by the PCD method as a function of gate bias voltage and injected carrier density. The details of the PCD measurements are described in Parag and Rohatgi. [12]

4.0.3 Theory and Modeling

4.0.3.1 Calculations of S_{eff} at the PECVD SiO_2-Si Interface

The effective surface recombination velocity (S_{eff}) defined at the edge of the surface depletion region can be calculated by standard Shockley-Read-Hall (SRH) theory. [13,14] For a continuum of non-interacting interface states, S_{eff} is obtained by the following integration over the band gap: [7,8 and 15]

$$S_{eff} = \frac{V_{th}(n_s p_s - n_i^2)}{\Delta n} \times$$

$$\left[\int_{E_V}^{E_C} \frac{D_{itA}(E)}{\frac{(n_s + n_1)}{\sigma_{pA}(E)} + \frac{(p_s + p_1)}{\sigma_{nA}(E)}} dE + \int_{E_V}^{E_C} \frac{D_{itD}(E)}{\frac{(n_s + n_1)}{\sigma_{pD}(E)} + \frac{(p_s + p_1)}{\sigma_{nD}(E)}} dE \right] \quad (1)$$

where

$$n_1 = n_i e^{\frac{E - E_i}{kT}}, \qquad p_1 = n_i e^{\frac{E_i - E}{kT}} \quad (2)$$

Here n_i is the intrinsic carrier concentration, E the interface trap energy level, E_i represents the intrinic Fermi level, E_c is the bottom of the conduction band, E_v is the top of the valence band, v_{th} is the carrier thermal velocity, k is the Boltzman constant, T is the absolute temperature, Δn is the injected carrier concentration, D_{it} is the interface state density, and σ_n , σ_p are the capture cross sections for electrons and holes, respectively. Subscripts A and D denote acceptor and donor type interface states, respectively.

The concentrations of electrons and holes at the interface can be written as

$$n_s = n_i e^{\beta(\psi_s - \phi_n)}, \qquad p_s = n_i e^{\beta(\phi_p - \psi_s)} \tag{3}$$

where $\beta = q/kT$, ψ_s is the surface band bending, ϕ_n , ϕ_p are the quasi-Fermi potential for electrons and holes, respectively.

From the above equations, it can be seen that S_{eff} is strongly dependent on the surface band bending ψ_s, which can be calculated from the overall charge neutrality condition for the system,

$$Q_{si} + Q_{it} + Q_{ox} + Q_g = 0 \tag{4}$$

Here, Q_{si} is the charge density induced in the silicon, Q_{it} is the interface state charge density, Q_{ox} is the oxide fixed charge density and Q_g is the charge density induced in the gate electrode. A numerical procedure for calculating ψ_s under the approximation of flat quasi Fermi-levels through the whole semiconductor region was proposed by Girisch et al. And was adopted by Aberle et al. to calculate the recombination velocity at the thermal SiO_2-Si interface. [8-15]

We started from the flat quasi-Fermi level approach to numerically solve the band bending problem to calculate S_{eff}. However, for the case of high recombination interface this approximation may not be valid. Therefore, we modified the flat quasi-Fermi level approach by using the different minority quasi-Fermi level ϕ_n in the depletion region at the interface compared to that in the bulk ϕ_{nB} (Figure 4.1).

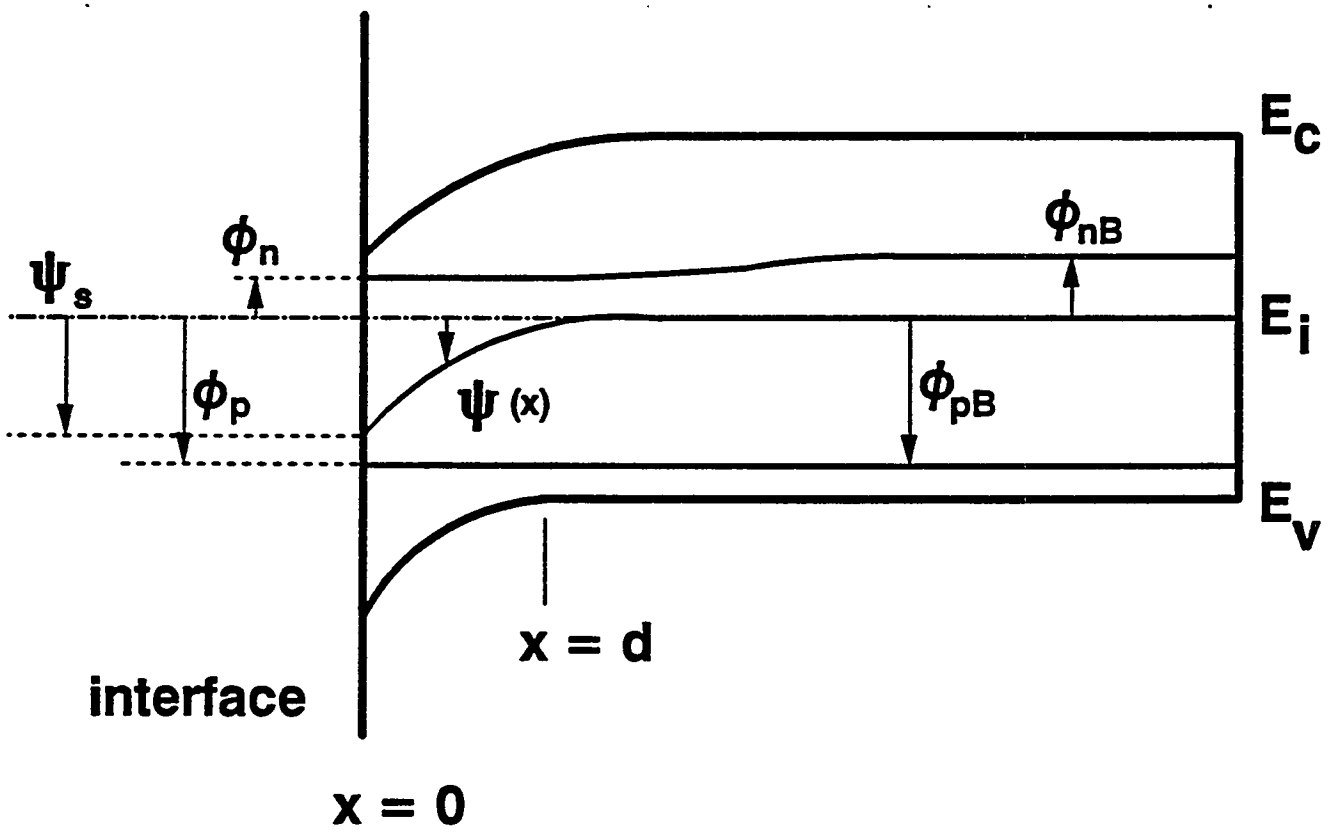

Figure 4-1. Energy band diagram at SiO_2-Si interface under non-equilibrium condition with definitions of electron energy and potentials.

These quantities can be calculated using the current continuity equations neglecting the recombination in the depletion region: [16]

$$J_n(x) = J_r(0) \tag{5}$$

$J_n(x)$ is the minority carrier current density in the depletion region which for p-type case is given by

$$J_n(x) = -q\mu_n n(x)\nabla\phi_n(x)\ , \tag{6}$$

and J_r is the interface recombination current density which is obtained from the flat quasi-Fermi level approach according to

$$J_r(0) = q\Delta n(d)S_{eff} \tag{7}$$

where μ_n is the minority electron mobility and d is the width of the depletion region. Assuming flat minority quasi-Fermi level in the depletion region, we calculated ϕ_n at the surface from equation (8) shown below and then used this value for more accurate calculation of ψ_s and S_{eff} (a detailed derivation of equation (8) is shown in the Appendix).

$$e^{-\beta\phi_{nB}} - e^{-\beta\phi_n} = \pm\frac{\Delta n S_{eff}}{D}\left[\frac{\epsilon_s}{2q\beta n_i^3}\right]^{\frac{1}{2}}\left[e^{-\beta\psi_s} - 1\right]\times$$
$$\left[\frac{\beta\psi_s(p_o - n_o)}{n_i} + e^{\beta[\phi_p - \psi_s]} - e^{\beta\phi_p} + e^{\beta[\psi_s - \phi_n]} - e^{-\beta\phi_n}\right]^{-\frac{1}{2}} \tag{8}$$

where the plus sign represents downward band bending the minus sign is for upward band bending, D_n is the minority carrier electron diffusion coefficient, ϵ_s is the dielectric constant of Si, n_o is the equilibrium electron concentration and p_o is the equilibrium hole concentration. In the derivation, $\phi_p = \phi_{pB}$ is assumed.

4.0.3.2 Effects of ψ_s and Interface State Parameters on S_{eff}

For a realistic calculation of S_{eff}, the interface state parameters (D_{it}, σ_n , σ_p) as well as Q_{ox} should be known. D_{it} can be obtained by the standard HF-QS CV analysis, but reliable values of σ_n , σ_p and the type of the interface states (acceptor or donor) are difficult to obtain as described earlier. However, if S_{eff} can be measured as a function of ψ_s , useful information can be obtained about the cross sections. By differentiating Eg. (1) with respect to ψ_s , the band bending $\psi_{s,max}$ at which S_{eff} is maximum can be obtained from $dS_{eff}/d\psi_s = 0$, which gives

$$\psi_{s,max} = \left(\frac{kT}{2q}\right) ln\left[\frac{\sigma_p(E)(p_o + \Delta n)}{\sigma_n(E)(n_o + \Delta n)}\right] \tag{9}$$

for either acceptor or donor type states. Under high-level injection condition Eg. (9) reduces to $\psi_{s,max} = 0.03 \log(\sigma_p/\sigma_n)$ in volts.

Figure 4.2 shows the results of the theoretical calculation of S_{eff} as a function of ψ_s based on the uniform D_{it} distribution model with two different cross-section models under a high-injection condition. The first model (case 1 in Figure 4.2) assumes that the electron capture cross section is 100 times larger than that of the holes, irrespective of the nature of D_{it}.

$$\sigma_{nA} = \sigma_{nD} = \sigma_n , \qquad \sigma_{pA} = \sigma_{pD} = \sigma_p \qquad and \qquad \sigma_n > \sigma_p \tag{10}$$

which was used in the recent model calculation. [8] The second model (case 2 in Figure 2) assumes that the capture cross section for the charged states (σ_c) is 100 times larger than the neutral ones (σ_N):

$$\sigma_{nD} = \sigma_{pA} = \sigma_C , \qquad \sigma_{nA} = \sigma_{pD} = \sigma_N \qquad and \qquad \sigma_C > \sigma_N \tag{11}$$

which is considered physically more realistic. [15] In Figure 4.2, cross sections are assumed to be independent of energy for both models, and $D_{itA} = D_{itD}$ is assumed. A model calculation showed that for case 1, there is one $S_{eff, max}$ at $\psi_{s, max} = -0.06$ V, but for the case 2 we get two $S_{eff, max}$ peaks at $\psi_{s, max} = -0.06$ and 0.06 V, corresponding to the contribution from the donor and the acceptor type states, respectively. Thus the calculations show that not only the information on the cross section ratios for electron and holes can be obtained from the measured $\psi_{s, max}$ values but the predominance of donor or acceptor type interface states can also be deduced.

4.0.4 Results and Discussion

Figure 4.3 shows high and low frequency CV measurements on a PECVD MOS sample. The voltage ramping rate was 0.1 V/s for both HF and QS-CV measurements. The standard analysis gave an oxide charge density of about 5×10^{11} cm^{-2} and a U shape distribution of $D_{it}(E)$ shown in Figure 4.4. [4-5] The experimental data, shown with the filled square, gave a good fit to an empirical function:

$$\begin{aligned} D_{it}(E) &= D_{itA}(E) + D_{itD}(E) \\ &= 6.5 \times 10^{15} \times |E - 0.57|^8 + D_{it} \qquad (cm^{-2}eV^{-1}) \end{aligned} \tag{12}$$

where D_{it} is the mid gap value of $D_{it}(E)$ and is equal to 1.17×10^{11} cm^{-2} eV^{-1} in this case. This function is indicated by the solid curve in Figure 4.4 and will be used for the later calculation.

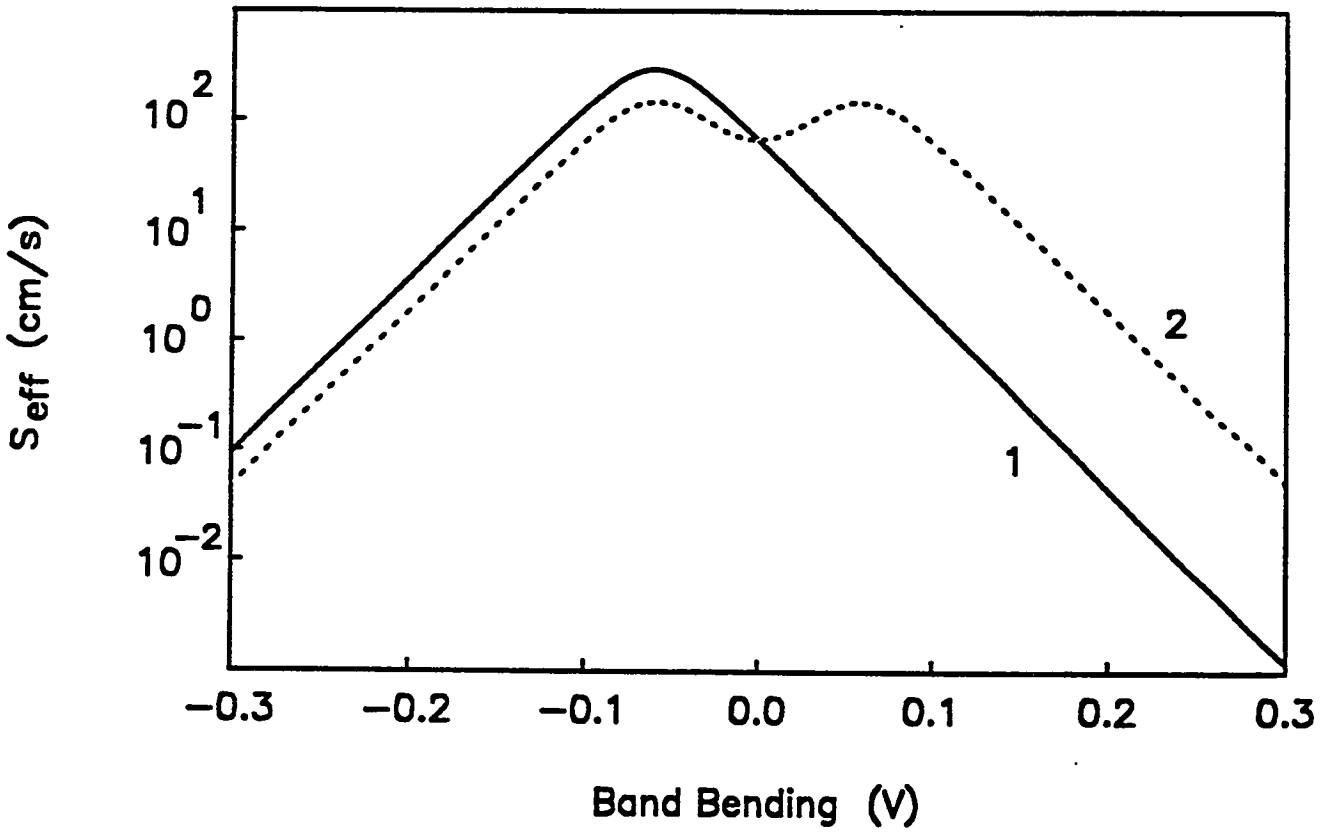

Figure 4.2. Calculated effective surface recombination velocity S_{eff} at SiO_2-Si interfaces as a function of the surface band bending based on the uniform distribution model of D_{it} in the energy gap. 1: $\sigma_n = 100\ \sigma_p = 10^{-14}$ cm^2. 2: $\sigma_e = 100\ \sigma_N = 10^{-14}$ cm^2. Other parameters for both curves: $p_o = 10^{-13}$cm^{-3}, $\Delta n = 5 \times 10^{14}$ cm^{-3}, $D_{it} = 10^{11}$ cm^{-2} eV^{-1}.

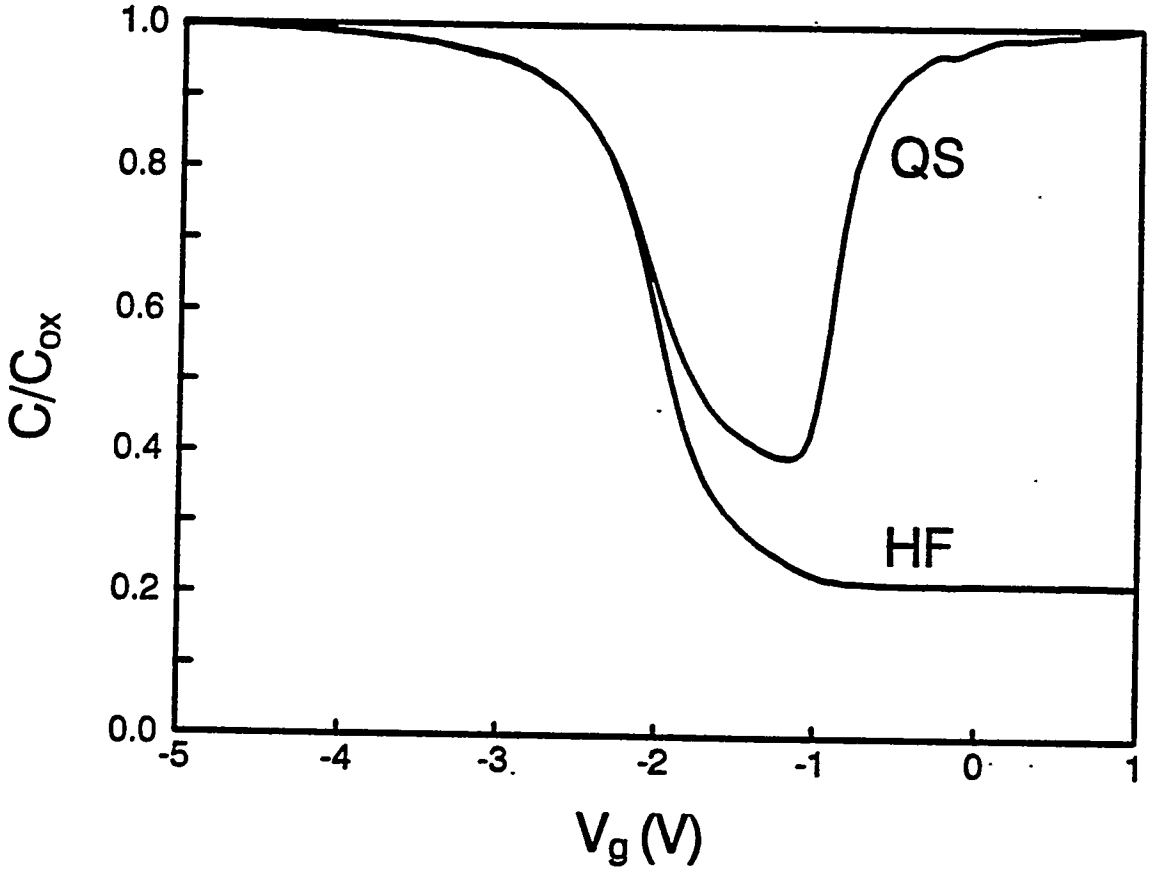

Figure 4.3. High frequency and quasi-static CV curves of the MOS structure for PECVD SiO_2-Si.

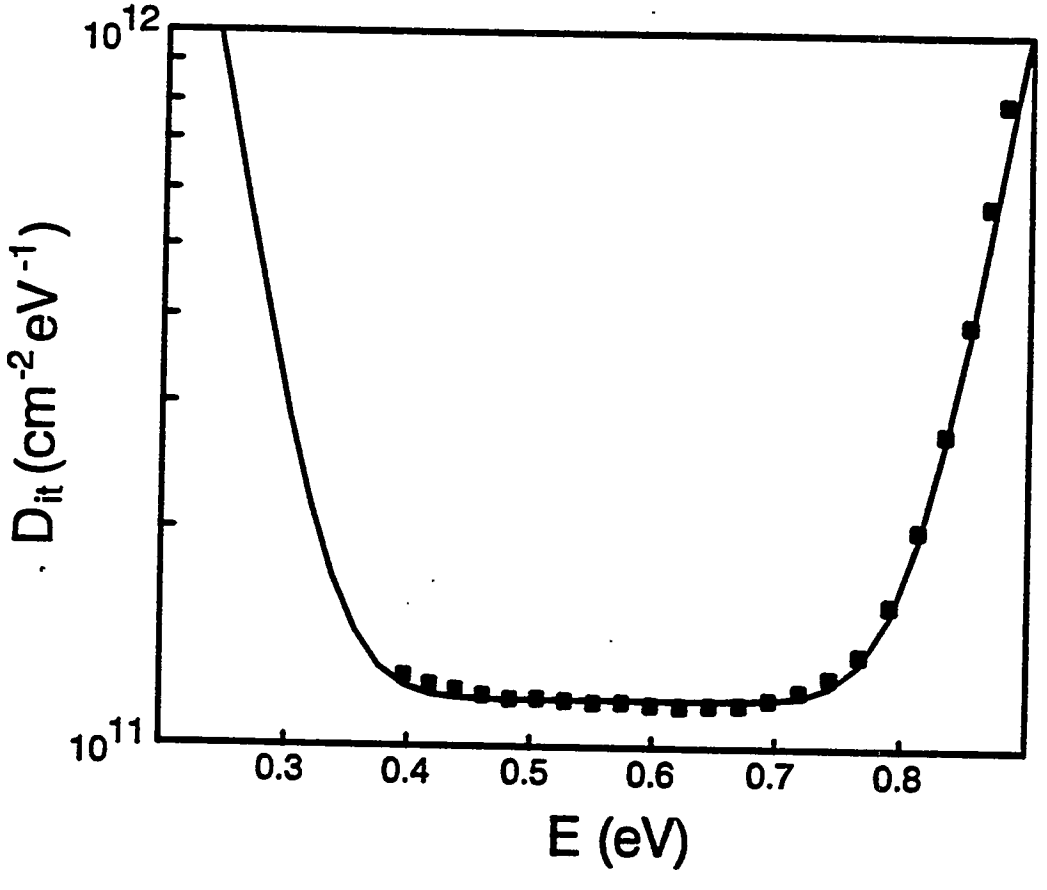

Figure 4.4. D_{it}(E) distribution in the energy gap obtained from the HF-QS CV curves in Figure 4.3 (■) and the assumed function of equation (12) (solid curve).

From the PCD measurements of the sample, we obtained the effective lifetime τ_{eff}. The relation between S_{eff}, τ_{eff} and the bulk lifetime τ_b is given by the following equations. [17]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + D_n \frac{\Delta^2}{W^2} \tag{13}$$

$$\Delta \tan(\frac{\Delta}{2}) = \frac{S_{eff} W}{D_n} \tag{14}$$

where W is the wafer thickness. From the measurements of the thickness dependence of τ_{eff} we obtained τ_b = 430 μsec at the injection level of $\Delta n = 10^{16}$ cm^{-3}. The measured τ_{eff} as a function of gate bias voltage V_g was converted to S_{eff} using the equations (13) and (14), and then S_{eff} was plotted against V_g in Figure 4.5. S_{eff} appears to have one maximum at about V_g = -5 V and decreases with increasing or decreasing V_g in accordance with the change of ψ_s.

Because it is difficult to obtain ψ_s from experiments under the illuminated condition, we tried to simulate the results in Figure 4.5 theoretically using the distribution of $D_{it}(E)$ in Figure 4.4. Adjustable parameters were the ratio of D_{itA}/D_{itD} and capture cross section. The work function difference between Si and ITO was neglected in accordance with a recent report, which suggests very little difference in work functions for these materials. [18] Notice that the peak position of S_{eff} can be adjusted by changing the ratio of σ_n and σ_p. The best theoretical fit to the S_{eff} data in Figure 4.5 was obtained by assuming $D_{itA} = D_{itD}$ and energy independent cross section values of

$$\sigma_{nD} = 4 \times 10^{-15}\ cm^2, \qquad \sigma_{pD} = 1 \times 10^{-17}\ cm^2,$$
$$\sigma_{nA} = 3 \times 10^{-17}\ cm^2, \qquad \sigma_{pA} = 3 \times 10^{-16}\ cm^2. \tag{15}$$

These results suggest that the capture cross sections are dependent on the charged state of the interface defects. Yablonovitch et al. reported two cross section ratios σ_n/σ_p for the interface states of thermally grown

SiO_2, which suggests a remarkable similarity between the interface properties of thermally grown and PECVD deposited SiO_2-Si interfaces. [11] As we mentioned in Section 4.3, the plot of S_{eff} as a function of ψ_s can provide more information about the interface states. Therefore, S_{eff} is re-plotted as a function of ψ_s in Figures 4.6a and 4.6b for the two different cross-section models, by obtaining ψ_s from V_g using equation (4). In Figure 4.6a, the theoretical curve using the first capture cross section model (equation (10) is shown with the dashed line. Although the first cross section model gives good fit at the dominant maximum of S_{eff}, the shoulder at about 0.03 V could not be fitted by this model. The better fit is obtained by the second model described by Eg. (15) as shown in Figure 4.6b. However, there still exists a discrepancy between the theoretical curve and data points at ψ_s larger than 0.08 V. This can be improved by using the energy-dependent cross-section model; however, the experimental error also increases with decreasing S_{eff}. Therefore, at this point, the capture cross section values in Eg. (15) are considered to be sufficiently accurate to perform further calculations.

Utilizing the cross-section model given in Eg. (15), the dependence of S_{eff} on Q_{ox} was calculated for several values of D_{it} for a boron-doped substrate with $N_A = 2 \times 10^{15}$ cm^{-3}. Figure 4.7 shows the assumed $D_{it}(E)$ distribution where mid-gap D_{it} was varied in the range of 10^{10} - 10^{12} cm^{-2}, (10^{10}, 5×10^{10}, 10^{11}, 5×10^{11} and 10^{12}), which is experimentally achievable for PECVD oxides. The calculated results are shown in figures 4.8a and 4.8b for an injected carrier density of $\Delta n = 10^{14}$ cm^{-3} (close to flat plate one-sun solar cell operating condition) and $\Delta n = 10^{16}$ cm^{-3} (concentrator cell operating condition), respectively.

From Figures 4.8a and 4.8b, we can estimate the required density of Q_{ox} to reduce S_{eff} for PECVD SiO_2-Si interface. Under a high-injection condition, see Figure 4.8b, we need a higher Q_{ox} to reduce S_{eff} compared to the low-injection case, seen in Figure 4.8a, because the high-injected carrier density neutralizes the charges at the interface and lowers the ψ_s. This requires higher Q_{ox} to obtain the same ψ_s. It is important to recognize that the band bending due to this mechanism will begin to decrease if the injection level becomes very high. We have limited experimental data that shows the S_{eff} value increases from 2 to 30 cm/s when the

injection level increases from $5x10^{14}$ to $1x10^{16}$ cm^{-3}. For high D_{it} values, the S_{eff} - Q_{ox} curves in Figures 4.8a and 4.8b show a hump or a rise in S_{eff} with increasing Q_{ox} before S_{eff} decreases monotonically. This is the result of the two kinds of cross sections, Eg. (15), where the acceptor type interface states contribute to the hump. Calculations in Figures 4.8a and 4.8b indicate that Q_{ox} should be more than 10 times the value of D_{it} at the mid gap in order to reduce S_{eff} below 10 cm/s. This Q_{ox} to D_{it} ratio is approximately 10 times higher than our previous calculation[2] based on uniform distribution of D_{it} in the band gap and the cross section model of Eg. (10). In the present model, increasing $D_{it}(E)$ toward the band edges (Figure 4.7) and the presence of acceptor type states contribute to the need for higher Q_{ox}.

Careful PECVD deposition of SiO_2 can produce 10 times larger Q_{ox} values than the D_{it} at the mid-gap values. Our recent results of a low $D_{it} = 1.1 \times 10^{10} cm^{-2}\ eV^{-1}$ with $Q_{ox} = 3.4 \times 10^{11}\ cm^{-2}$ for carefully prepared PECVD SiO_2-Si[4], proves the potential of PECVD SiO_2 passivation of Si surfaces and also suggests the importance of optimization of PECVD process. The situation becomes more difficult when D_{it} is greater than $10^{11}\ cm^{-2}\ eV^{-1}$. Further study on the properties on PECVD SiO_2-Si interface (especially grown at different conditions and with different substrate doping density) will be helpful and necessary for optimizing the PECVD SiO_2 passivation process for solar cells.

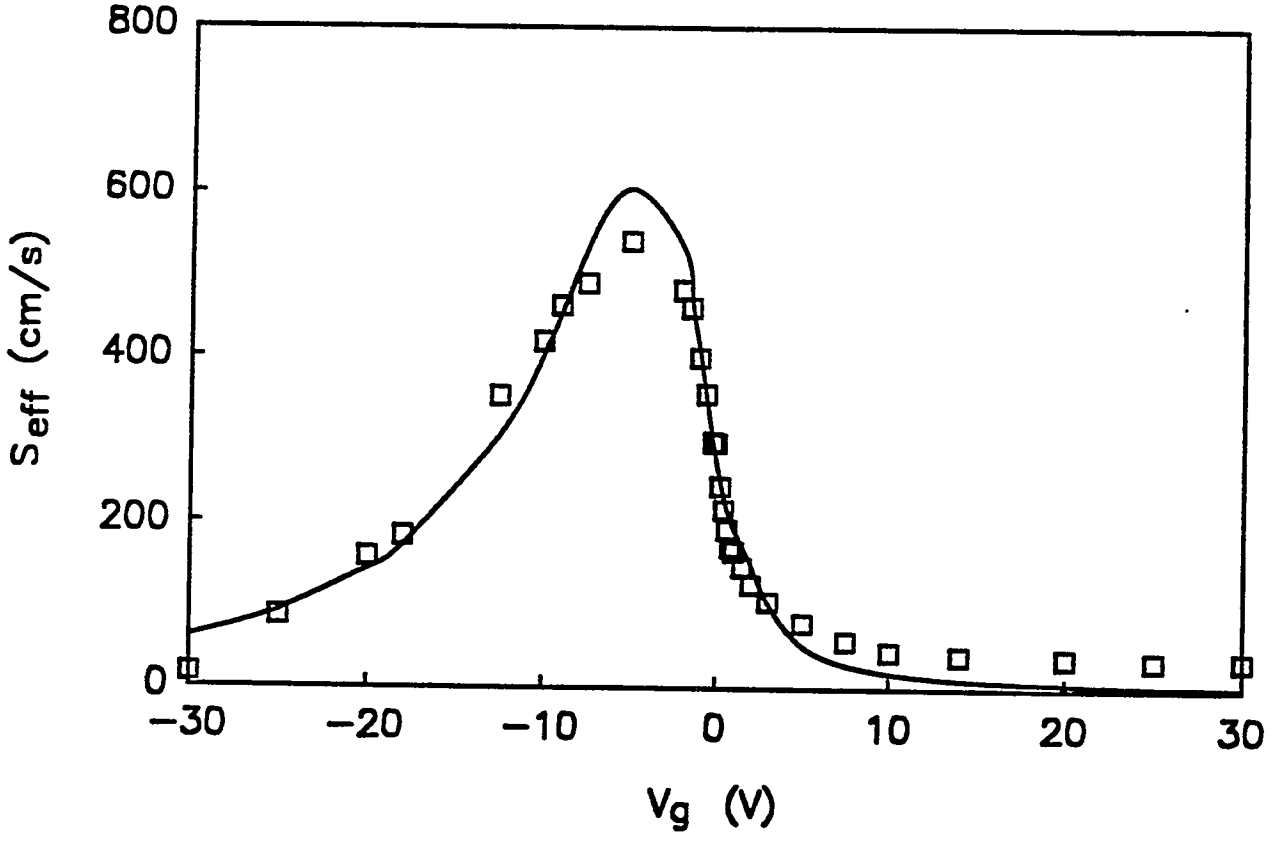

Figure 4.5. Gate voltage dependence of effective surface recombination velocity obtained by the PCD measurements (□) and theoretically fitted curve.

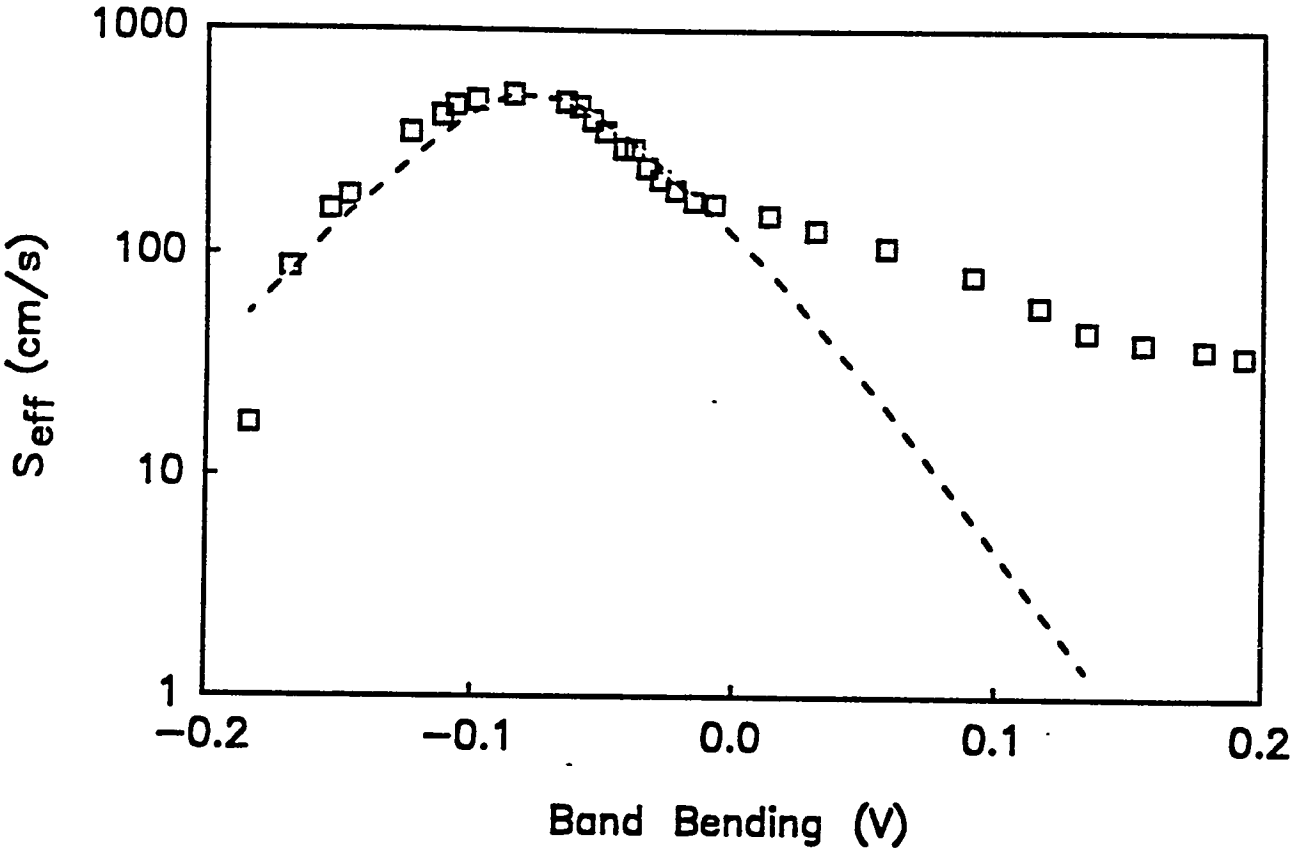

Figure 4.6a. S_{eff} as a function of surface band bending. Dashed curve: theoretically fitted curve based on the capture cross section model shown in equation (10).

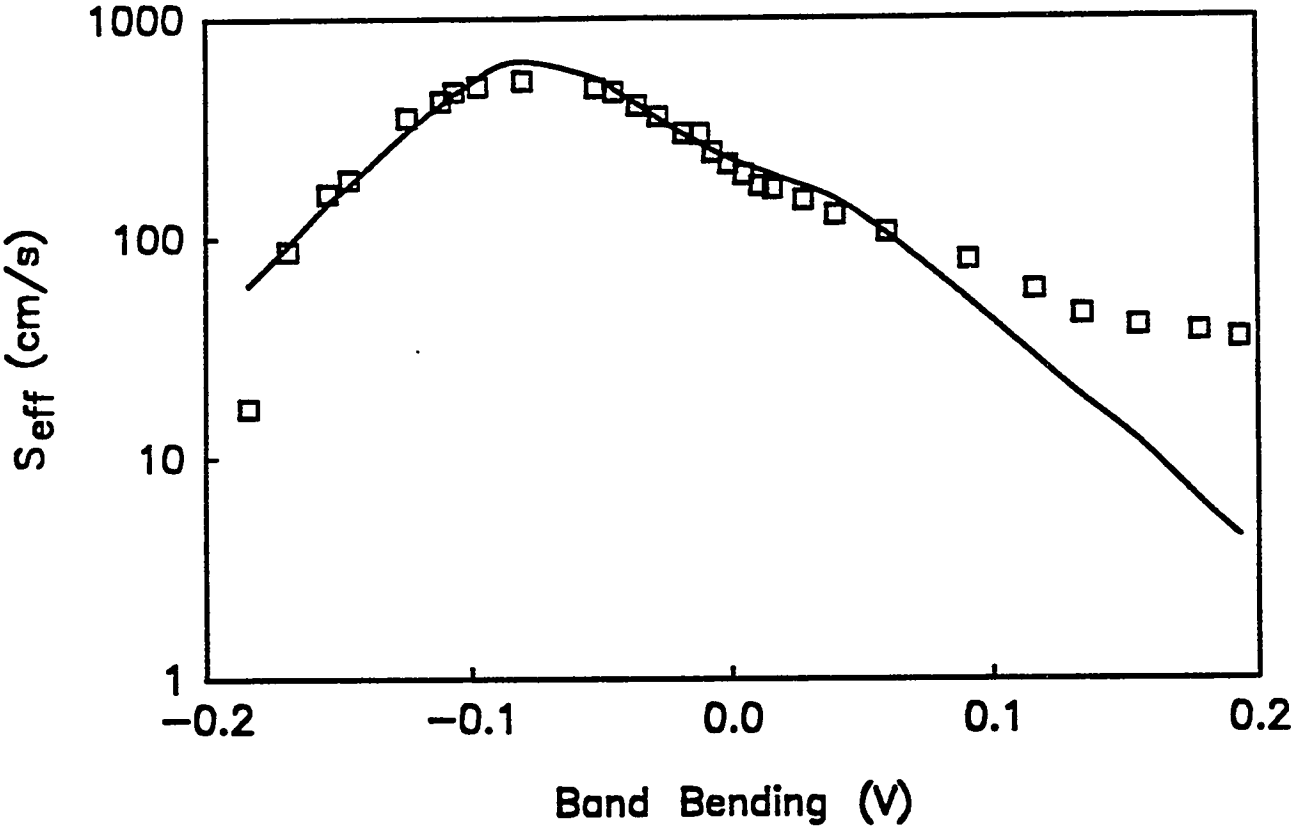

Figure 4.6b. Solid curve: theoretical curve based on the capture cross section model of equation (15). □: Experimental results plotted against the calculated band bending.

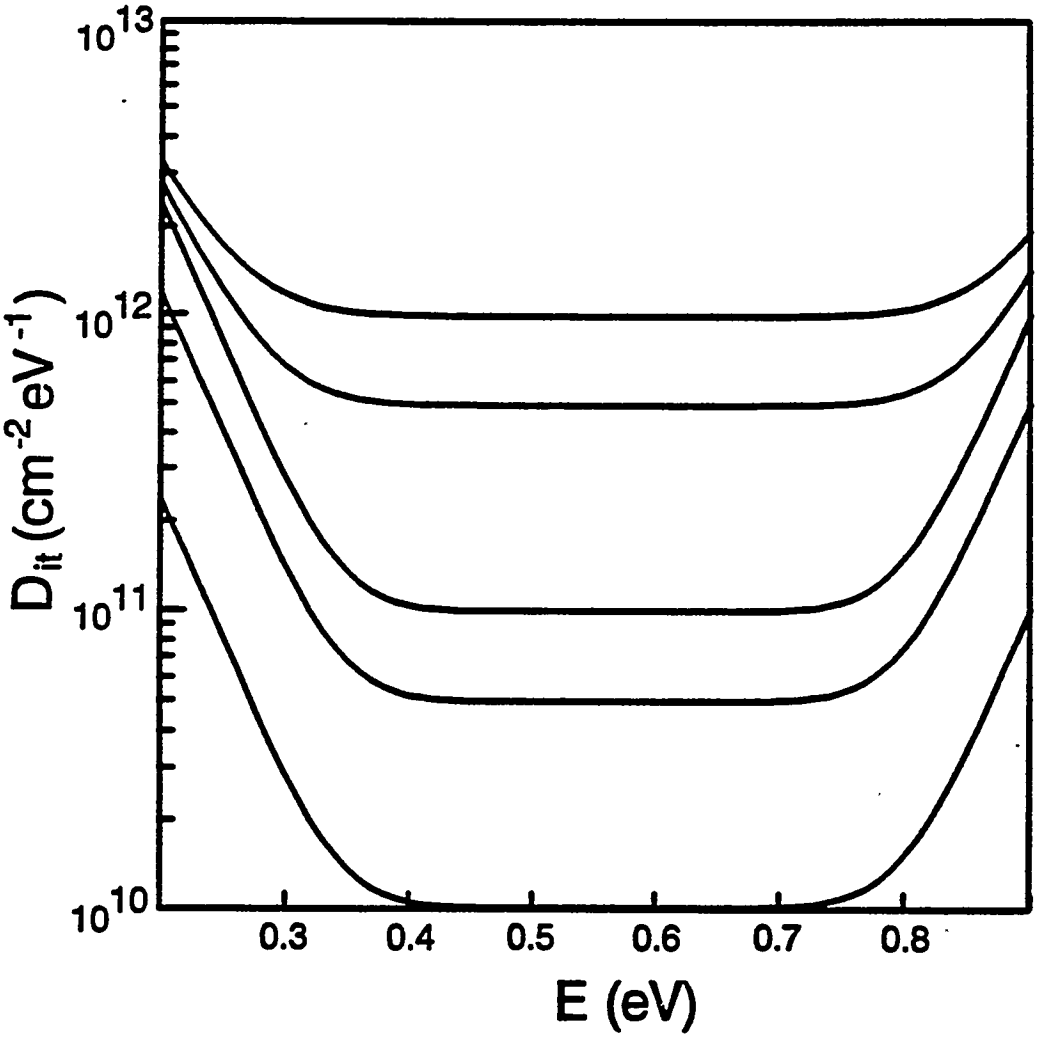

Figure 4.7. Assumed D^{it} (E) distributions in the energy gap used for the calculation.

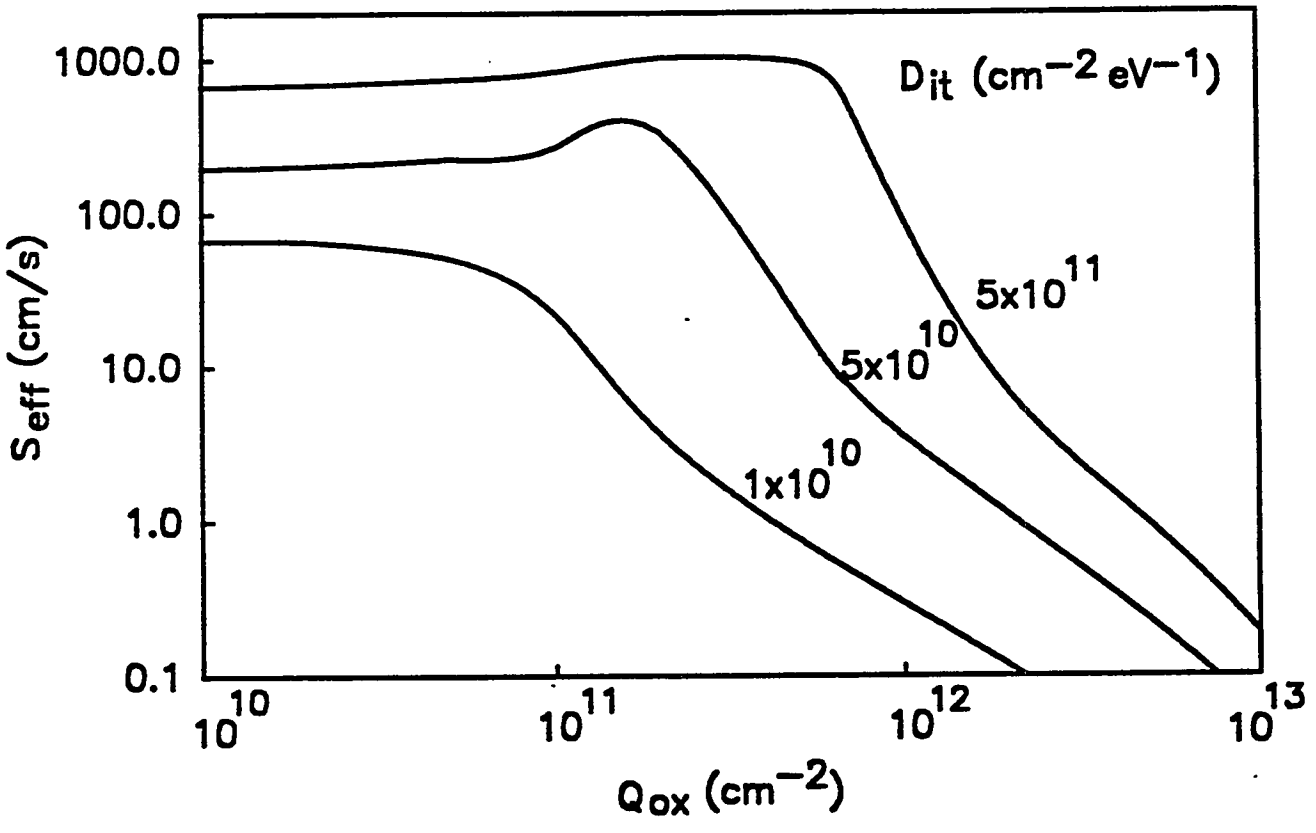

Figure 4.8a. Calculated S_{eff} as a function of positive fixed oxide charge density under the injection of $\Delta n = 10^{14}$ cm^3.

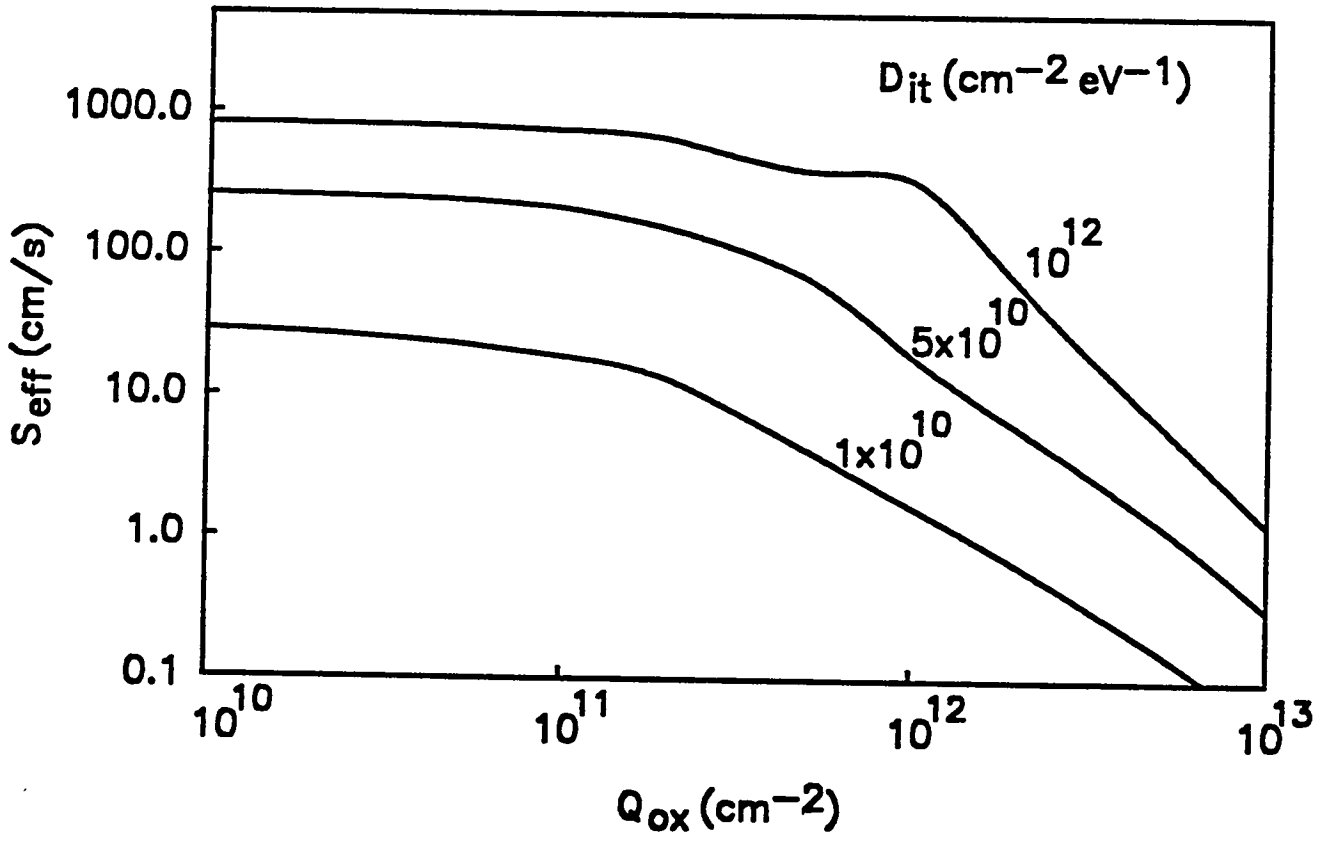

Figure 4.8b. Calculated S_{eff} as a function of positive fixed oxide charge density under the injection of $\Delta n = 10^{16}$ cm^{-3}.

4.0.5 Conclusion

The effective surface recombination velocity (S_{eff}) at the PECVD SiO_2-Si interface was measured by a PCD method in conjunction with the gate bias voltage via transparent ITO gates. A theoretical analysis based on the measured $D_{it}(E)$ distribution in the band gap was performed to obtain S_{eff} as a function of the surface band bending, from which the electron and hole capture cross sections for the PECVD Si_2-Si interface states were estimated to be $\sigma_{nD} = 4 \times 10^{15}$ cm^2, $\sigma_{pD} = 1 \times 10^{-17}$ cm^2, $\sigma_{nA} = 3 \times 10^{-17}$ cm^2 and $\sigma_{pA} = 3 \times 10^{-16}$ cm^2. Model calculations were extended further to investigate the relationship between S_{eff}, Q_{ox}, D_{it}, and injection level. It was found that Q_{ox} should be roughly 10 times larger than the mid gap D_{it} value to in order to reduce S_{eff} below 10 cm/s for 5 Ω-cm (100) p-type Si. These results prove the effectiveness of PECVD SiO_2 for passivation of Si surfaces and its application for devices like solar cells.

4.1 Surface And Bulk Defect Passivation In Multicrystalline-Si Materials By Plasma Enhanced Chemical Vapor Deposition Of SiO_2/SiN Coatings

4.1.1 Introduction

Previous studies have shown that the application of single-layer PECVD-SiN thin film can be helpful in improving efficiency of mc-Si solar cells. [19 to 24] It not only acts as an antireflection coating layer with a suitable refraction index of ~2.0, but can also improve the performance of photovoltaic devices. This is because the PECVD process ambient contains a large amount of atomic hydrogen, some of which can be incorporated in the PECVD film and the substrate. In addition, PECVD is a low-temperature process (about 300°C) with high throughput, good uniformity, better thickness control (<5%) and excellent reproducibility, compared to other CVD processes (LPCVD or APCVD) and physical evaporation. All these advantages make PECVD SiN film very attractive for silicon solar cells.

The beneficial effects of single-layer PECVD SiN on J_{sc}, V_{oc}, and cell efficiency (Eff) on mc-Si cells have been reported. [22 to 24] Recently, Kishore etal. have reported a 28% improvement in J_{sc}, and a 13 mV increase in V_{oc} due to single-layer PECVD SiN. [23] Even though it has been shown that PECVD SiN improves the Si solar cell performance, it is still not clear whether this improvement results from surface passivation, bulk defect passivation, or a combination of both. No attempt has been made in the past to decouple and quantify the surface and bulk passivation effects. Moreover, the defect passivation effect of the PECVD deposition on different promising photovoltaic mc-Si materials has not been investigated. Recently we showed that the deposition of thin PECVD SiO_2 on single-crystal silicon followed by a photo-assisted anneal results in very high effective minority carrier lifetime, very low surface recombination velocity, and very low interface state density. [25,26] We also showed that the deposition of PECVD SiN film on top of a thin PECVD SiO_2 not only improves

the degree of surface passivation but also the stability of the passivation. We have shown elsewhere that a combination of PECVD grown 600 Å SiN on Si with an refractive index of 2.3 and 950 Å SiO_2 on top of that SiN can act as a very efficient double-layer antireflection coating. [27] In our previous studies, single-crystal Si was used and no attempt was made to decouple bulk and surface passivation effects. [25 to 27] In this article, the surface and bulk passivation effects are quantified due to the double-layer PECVD coating on different multicrystalline Si materials, including EFG sheet silicon, Osaka regular cast (Osaka), Solarex, and Wacker cast multicrystalline silicon materials. The bulk defect passivation was monitored by minority carrier lifetime measured by a photo-conductivity decay (PCD) technique. Some solar cells were fabricated with PECVD coatings and the bulk and surface passivation effects on solar cells were quantified by a combination of quantum efficiency measurements and modeling.

4.1.2 Experimental

Low-temperature PECVD is used for the defect passivation of various multi-crsytalline Si materials. The process sequence involves PECVD deposition of 600 Å SiN on top of PECVD grown 100 Å SiO_2 on various substrates, followed in a photo-assisted anneal by a tungsten halogen lamp heated system in forming gas ambient. The PECVD SiN and SiO_2 films were prepared in a Plasma-Therm Inc reactor (series 700) operated at 13.6 MHz. SiH_4, NH_3, N_2 gases were used for SiN deposition, and SiH_4 and N_2O gases were involved in SiO_2 deposition. The saline concentration was 2%. The ratio of SiH_4/NH_3 was controlled to obtain SiN films with refractive index of 2.3. Substrate temperature was 250°C and the rf power was 20 W for SiO_2, and 275 C and 30 W for the SiN deposition, respectively. After the PECVD depositions, a photo-assisted anneal was performed at 350°C for 20 min, in forming gas ambient. Four kinds of wafers were studied, including EFG, Osaka cast (Osaka), Solarex, and Wafer cast Si, with a thickness of 390μm, 270μm, 305μm, 330μm,

respectively. The as-grown wafer cleaning process, prior to PECVD film deposition, is described in detail in Chen etal.25. Each sample was tested by PCD lifetime measurements before and after the passivation. The bulk and surface passivation effects were decoupled and quantified by PCD lifetime measurements in air and HF solution, and also by modeling and IQE measurements before and after the passivation on solar cells fabricated on cast silicon from Osaka Titanium Corporation.

4.1.3 Results and Discussion

4.1.3.1 Determination of bulk and surface passivation by PCD lifetime measurements

PCD measurement in air gives an effective lifetime by

$$\frac{1}{\tau_{eff}} = -\frac{1}{N}\frac{dN}{dt} \qquad (1)$$

where N is the injected carrier concentration and t is the decay time. The τ_{eff} includes both bulk and surface recombination of photogenerated carriers. [28] Table 4.1 shows the effective minority carrier lifetime (τ_{eff}) for the four kinds of as-grown samples determined by PCD measurements in the air. The uc and c terms in the brackets of Table 4.2 represent samples not coated and coated, respectively, with the PECVD SiO_2/SiN double layer coating. It is clear from the data that a substantial improvement in τ_{eff} was observed in all four materials after the PECVD depositions followed by photo-assisted anneal. The τ_{eff} improved by a factor of 2.5 to 9.5 due to the PECVD passivation, depending upon the material. It is important to recognize that τ_{eff} includes both surface and bulk passivation effects.

Table 4.1. The effective lifetime (Ms) measured before and after the PECVD coating

	EFG	Osaka	Solarex	Wacker
τ_{eff}(uc)	1.4	2.2	5.9	2.1
τ_{eff}(c)	4.3	21.0	23.1	5.6
τ_{eff}(c)/τ_{eff}(uc)	3.1	9.5	3.9	2.6

Table 4.2. The lifetime (Ms) in HF measured before and after the PECVD coating

	EFG	Osaka	Solarex	Wacker
τ_{HF}(uc)	3.6	22.3	41.4	4.1
τ_{HF}(c)	5.4	38.6	58.7	5.3
τ_{HF}(uc)/τ_{HF}(c)	1.5	1.7	1.4	1.3

In order to decouple the bulk and surface passivation effects, each sample was also measured in concentrated HF solution before and after the PECVD passivation. HF solution is known to provide a near-perfect surface passivation for silicon, via H-Si bond formation. [28] Therefore, the PCD lifetime measured in HF (τ_{HF}) reveals true bulk recombination, and the change in τ_{HF} before and after the PECVD passivation should represent bulk defect passivation. Table 4.2 shows the improvement in τ_{HF} due to the PECVD passivation of all four materials. It can be seen that these four materials show significant bulk defect passivation after the PECVD deposition of SiN/SiO_2. The τ_{HF} increases by 30% to 70% after the passivation depending upon the multicrystalline material. It should be noted that the passivation efficiency is material specific, but seems to be independent of the initial bulk lifetime value.

As indicated above, τ_{HF} can be used as a good measure of true bulk lifetime; therefore, τ_{eff} can be approximately expressed as: [28]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{2S}{L} = \frac{1}{\tau_{HF}} + \frac{1}{\tau_s} \qquad (2)$$

where L is wafer thickness, S is surface recombination velocity, and τ_s is the surface lifetime. Thus τ_s can now be determined by measuring τ_{eff} and τ_{HF}. The surface lifetime after the PECVD passivation, shown in Table 4.3 increases by a factor of 5.5 to 23, depending upon the material.

Table 4.3. The surface lifetime before and after the PECVD coating where (c) And (uc) stand for coated and uncoated, respectively.

	EFG	Osaka	Solarex	Wacker
τ_s(uc)	2.3	2.4	6.9	4.3
τ_s(c)	21.1	46.1	38.1	98.9
τ_s(c)/τ_s(uc)	9.2	18.8	5.5	22.9

By knowing the sample thickness and τ_s, the S value can be determined from Eq. (2). For example, Osaka cast with a thickness of 270 μm and the τ_s of 46.1 μs after the PECVD passivation, then S value was found to be 292 cm/sec. Using Eq (2), the relationship between τ_{eff}, τ_{HF}, and τ_s can be expressed as:

$$\frac{\tau_{eff}(c)}{\tau_{eff}(uc)} = \frac{\tau_s(c)\frac{\tau_{HF}(c)}{\tau_{HF}(uc)} + \tau_{HF}(c)\frac{\tau_s(c)}{\tau_s(uc)}}{\tau_{HF}(c) + \tau_s(c)} \qquad (3)$$

The first and second terms in the numerator on the right side of Eq.(3) are related to the improvements in τ_{HF} and τ_s, and represent the partial contribution to the improvement in τ_{eff} from bulk and surface passivation, respectively.

Thus, the above results show that the PECVD SiO_2/SiN coating provides significant bulk and surface defect passivation, but the degree of passivation is material specific. For example, Osaka cast silicon showed the highest degree of bulk passivation, and Wacker material showed maximum improvement in surface passivation. This is not surprising because these materials are made by different manufacturers and contain a large variation in bulk and surface defects. No attempt was made to correlate the degree of passivation with defect variation at the microscopic scale in the materials. Therefore, the exact passivation mechanism is not fully understood at this time. However, atomic hydrogen, generated during PECVD SiN deposition and the use of forming gas in photo-assisted anneal are expected to play a significant role in the defect passivation. This was supported by the large amount of hydrogen detected by FTIR measurements in the PECVD SiN film. [29]

4.1.3.2 PECVD-induced bulk and surface defect passivation in multicrystalline silicon solar cells

Simple n^+-p-p^+ solar cells were fabricated by phosphorus diffusion on the front and Al diffusion on the back of the cells. The internal quantum efficiency (IQE) measurements were performed to decouple bulk and surface passivation effects in the cells. The IQE of a solar cell is a strong function of surface recombination velocity(s) and bulk lifetime (τ). [30] The short wavelength response is primarily influenced by surface passivation, while the long wavelength response is primarily affected by bulk defect passivation. Therefore, the experimentally measured IQE of a solar cell before and after the PECVD passivation, in conjunction with IQE modeling, can provide useful information about the degree of both surface and bulk passivation. A one-dimensional

simulation program, PC1D, was used to calculate and fit the measured IQE as a function of wavelength with varying front surface recombination velocity(s) and bulk lifetime (τ). [31] The important input parameters for the n^+p-p^+ cell structure used in the PC1D simulation are listed in Table 4.4 Grain boundary and defect passivation effects are represented by effective bulk lifetime.

Table 4.4. The Input Parameters Used In PC1D Simulation Of Cell's IQE

Material	p-Si
Substrate resistivity	0.8 Ω-cm
Substrate thickness	300 μm
Emitter surface doping concentration	$1x10^{19}cm^{-3}$
Emitter junction depth	1μm
Emitter doping profile	external
Front surface recombination velocity	variable
Bulk lifetime	variable
Rear surface recombination velocity	10^6cm/s
Rear surface doping	p-type
Rear surface doping concentration	$5x10^{18}cm^{-3}$
Rear junction depth	1μm
Rear doping profile	Erfc
Rear surface reflection	70%
Auger coefficient for hole	$9.9x10^{-32}cm^6s^{-1}$
Auger coefficient for electron	$2.8x10^{-31}cm^6s^{-1}$
Temperature	25 °C

The calculated variation in IQE for s = 10^4 cm/s and τ in the range of 5 - 25 μs is shown in Figure 4.9a. Similarly variation in IQE for a fixed τ = 25 μs and s in the range of 10^3 - 10^6 cm/s is shown in Figure 4.9b. It is clear that, for this cell design with fixed back surface conditions, short wavelength IQE (λ < 800 nm) is a strong function of front surface recombination velocity, s, but s has no effect on the IQE in long wavelength region (λ > 850 nm), Figure 4.9b In contrast to the effect of s, bulk lifetime τ has strong influence on IQE in the long wavelength region λ > 800 nm, but has no effect on the short wavelength IQE (λ < 700 nm), Figure 4.9a . Thus, the change in IQE

can be modeled by selecting s and τ to fit short and long wavelength IQE, respectively. Thus the PECVD coating induced changes in s and τ can be estimated from modeling the measured IQE data.

Figure 4.10 shows the measured and calculated IQE data for the same cell before and after the PECVD coating. The s and τ values were adjusted in the PC1D simulation to obtain the best fit to the experimental data. Before the PECVD passivation, s = $2x10^5$ cm/s and τ = 10 μs gave a very good match between the measured and modelled IQE data. However, after the PECVD coating, s = $5x10^4$ cm/s and τ = 20 μs gave the best fit to the measured IQE data, Figure 4.10 It should be noted that in the wavelength range of 400 - 475 nm, the calculated IQE is higher than the measured IQE. We have shown elsewhere that the slight absorption in short wavelength is due to high index of PECVD SiN, which is not accounted for in the PC1D modeling. [27] The higher refractive index of SiN (2.3, instead of 2.0) is used for the better double layer antireflection coating. [27] The decrease in s from $2x10^5$ to $5x10^4$ cm/s and increase in τ from 10 to 20 μs indicate that the PECVD coating not only passivates the surface but also gives rise to significant bulk defect passivation. This is consistent with the passivation results on as-grown samples in the Tables 4.1, 4.2 and 4.3 It is interesting to note that the bulk and surface passivation effect of the PECVD remained noticeable in the cells even though cells have undergone phosphorus and Al gettering. This suggests that PECVD passivation is complementary to the getting treatment.

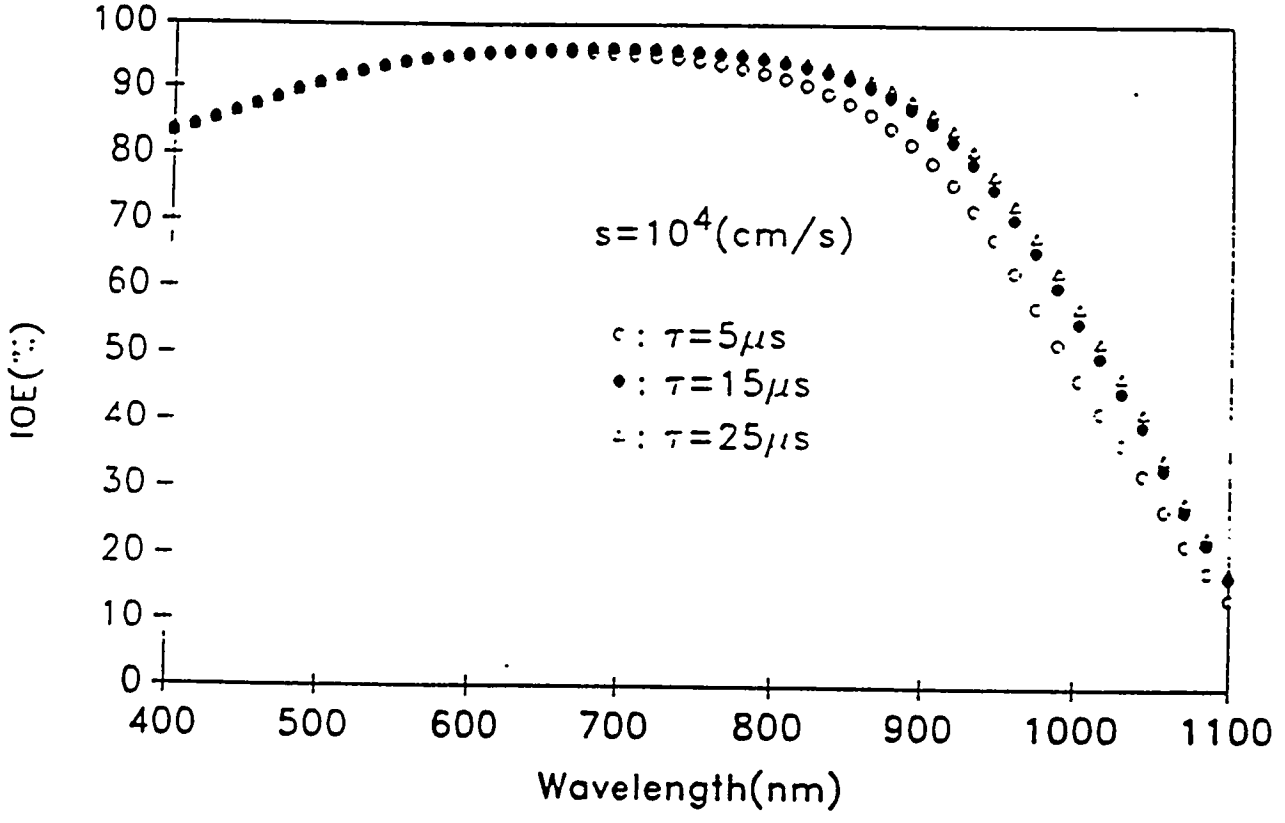

Figure 4.9a. The calculated IQE for n^+pp^+ solar cell with variation of substrate bulk lifetime τ and for a fixed front side surface recombination velocity S.

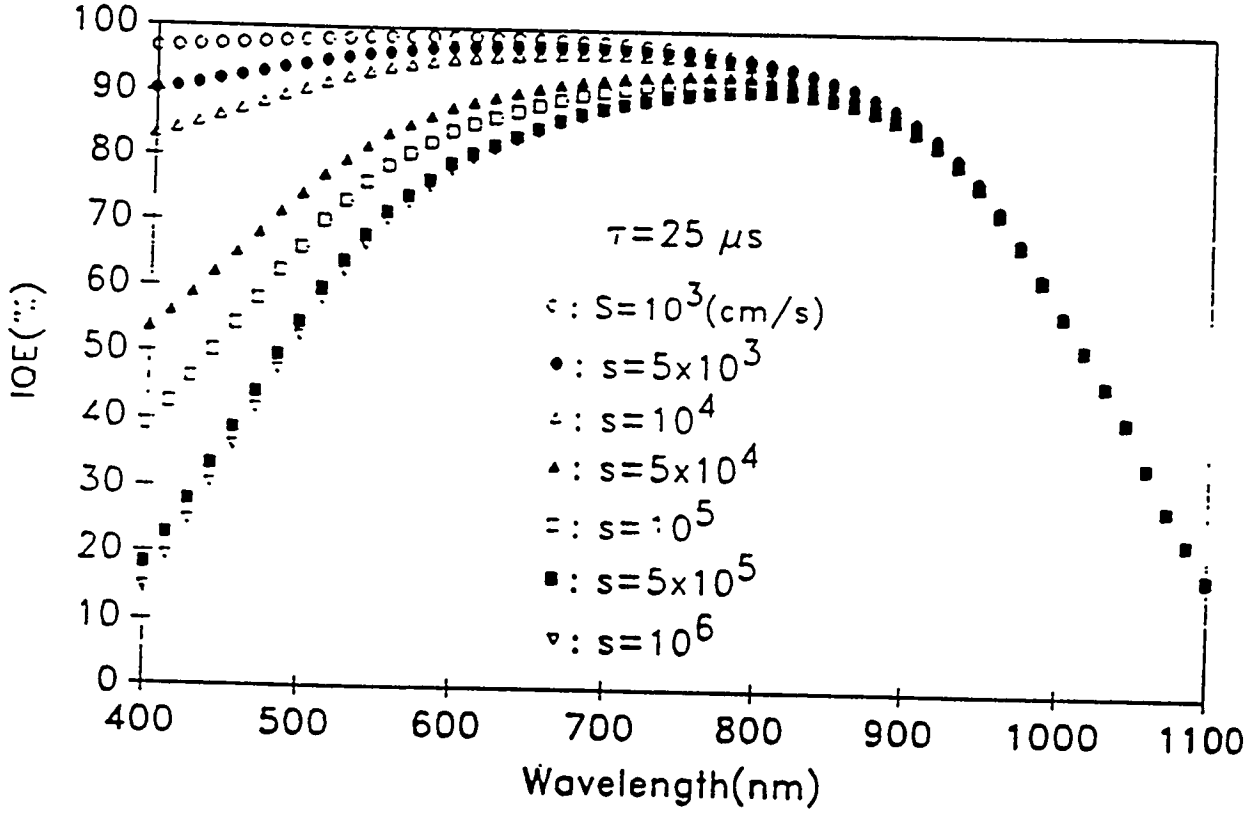

Figure 4.9b The calculated IQE variation with front surface recombination velocity S for a fixed bulk lifetime.

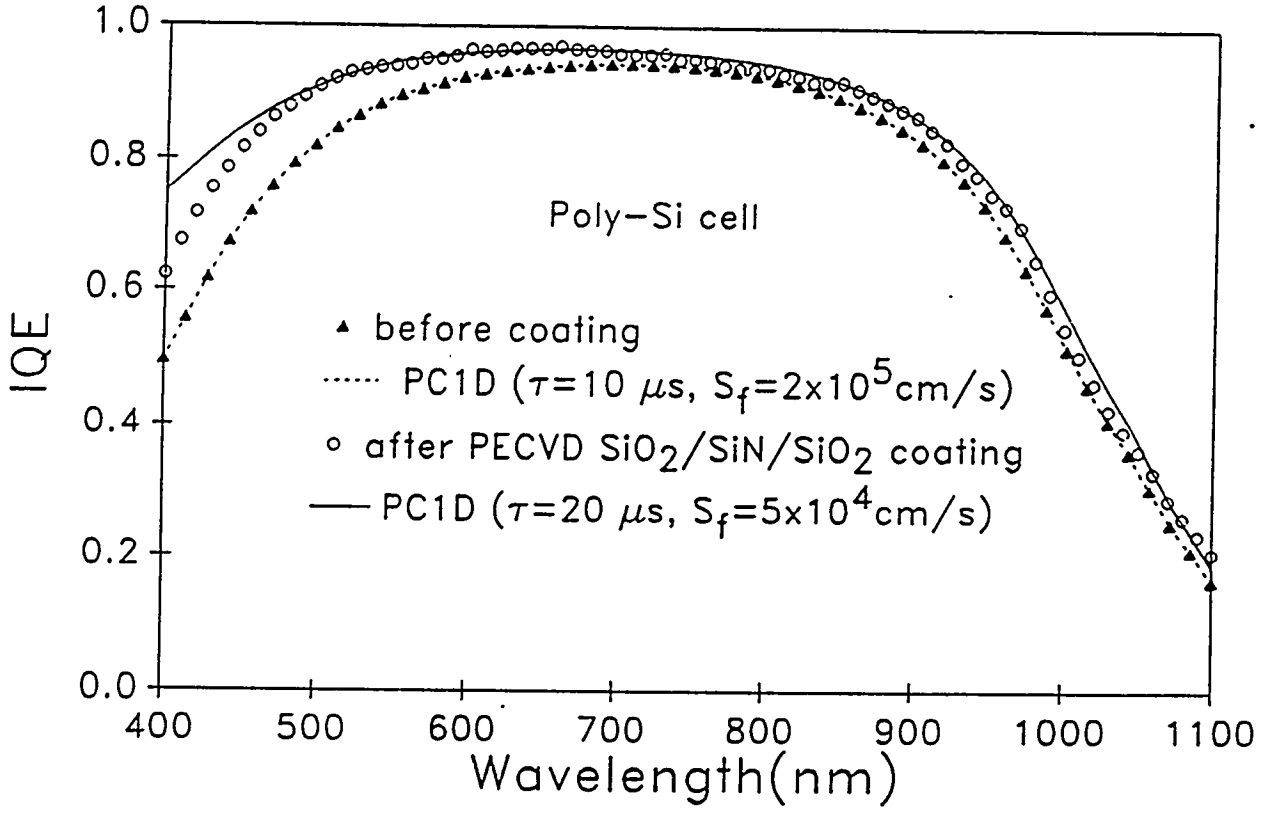

Figure 4.10 Comparison of measured and calculated IQE to asses change in S and τ_b due to PECVD coating.

4.1.4 Conclusions

A novel PECVD passivation technique has been used for bulk and surface passivation of multicrystalline Si materials. This technique consists of low-temperature (250°C) PECVD deposition of SiN(600 Å)/SiO(100 Å) double layer coating followed by photo-assisted anneal at 350°C in forming gas ambient. The surface and bulk defect passivation effects of the PECVD passivation were decoupled and quantified for the first time by the PCD lifetime measurements in air and HF solution, as well as by cell fabrication, followed by matching the measured and calculated IQE. It is shown that the PECVD coating is very effective for both surface and bulk defect passivation of promising photovoltaic mc-Si materials. However, the passivation efficiency is found to be material specific. In the as-grown materials, the bulk lifetime improved by 30% to 70% and the surface passivation improved by a factor of 5.5 to 23 due to the PECVD coating. Solar cells made on Osaka-cast multicrystalline Si showed a decrease in surface recombination velocity by a factor of 4 and increase in bulk lifetime by a factor of 2. This compares with an increase in bulk lifetime by a factor of 1.7 and τ_s by a factor of 18.8 for PECVD coated as-grown sample. The significant difference in the surface passivation of the cell and the as-grown wafer suggests that the PECVD is less effective in passivating the heavily diffused front surface of the cells compared to the lightly diffused as-grown wafer surface.

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CHAPTER 5. LOW-COST, HIGH-EFFICIENCY SILICON SOLAR CELLS BY RAPID THERMAL PROCESSING

5.1 Introduction

Low cost and high-efficiency is the key to large scale acceptability of photovoltaic systems. PV modules today cost about $4/Watt, which can produce electricity at a rate of about 25¢/kWhr. A factor of two in cost reduction is needed to make PV attractive for peak-power load applications and about a factor of 3 or 4 reduction would make it extremely competitive with conventional energy sources for base load utility applications. No PV material or technology has yet been able to achieve the cost and efficiency goals simultaneously because the efficient cells are too expensive and the cheaper cells are not efficient enough. Rapid thermal processing (RTP) is becoming established as a simplified and cost-effective fabrication technique which significantly reduces the cell process time, thermal budget, and wafer cleaning steps, without a significant loss in cell efficiency. In this study, RTP involves a rapid, simultaneous front and back diffusion for the formation of an emitter and back-surface-field. To minimize process steps and time, low temperature plasma enhanced chemical vapor deposition (PECVD) of SiN/SiO_2 dielectrics was used for efficient front surface passivation and antireflection (AR) [5-1]. Currently, the RTP process at Georgia Tech utilizes photolithography for patterning contacts; however, research is underway for defining industrially viable, screen-printed contacts on RTP emitters.

5.2 Comparison Between RTP and Conventional Furnace Processing (CFP)

The fundamental difference between RTP and conventional furnace processing (CFP) is the spectrum of electromagnetic energy used to heat the substrate. The radiation spectrum of a furnace consists mostly of photons in the infrared region that excite the ground state of the substrate's molecules to higher vibrational states, and dissociation occurs when sufficient energy is

concentrated in the bond to be broken. In contrast, RTP typically consists of tungsten-halogen lamps which radiate from the vacuum ultra violet to infrared regions. These higher energy photons emitted in an RTP system can induce transitions into quantized electronically excited states as well as higher vibrational modes. Since these dominating photophysical effects in RTP differ from thermal reactions of the furnace, RTP can provide lower temperature cell processing compared to furnace processing [5-2].

These physical differences allow various advantages in favor of RTP over CFP. Conventional cell processing generally involves separate long furnace diffusions and oxidations at high temperatures, which require extensive and careful wafer cleaning, prolonged cell processing, and use of more chemicals and gases. RTP generally involves short thermal cycles (on the order of seconds or minutes—instead of hours) which results in a reduced thermal budget (i.e. lower power consumption).

Perhaps the best advantage of RTP is the rapid, simultaneous diffusion of the emitter on the front and the BSF on the back. Figure 5-1 compares the single wafer process time for each step of the RTP and CFP performed at Georgia Tech. RTP can reduce the total cell fabrication time by about a factor of two. Note that nearly 6.5 hours (P diffusion + emitter etch back + wafer cleaning + Al diffusion/front-surface oxidation) of CFP is replaced by a quick, 40 min spin-on plus RTP simultaneous diffusion. As a result of the reduced exposure to high temperatures, RTP also requires fewer cleaning steps and therefore lesser use of chemicals (as shown in the shorter initial cleaning time required for RTP).

As stated earlier, at Georgia Tech, RTP was used in conjunction with PECVD to provide front surface passivation and AR properties; whereas, ZnS/MgF_2 coatings were evaporated on top of the 10 nm oxide grown during the Al diffusion step in the case of CFP. Integrating PECVD with RTP reduced the deposition time of a double-layer antireflection (DLAR) coating from 2 hours, as in the case of ZnS/MgF_2 coatings in CFP, to about 15 min for PECVD. PECVD also serves as an ideal alternative to oxides for front surface passivation since the simulatneous diffusion in RTP cannot incorporate oxidation of the front surface without additional steps.

It is important to note that out of the 8.75 hour RTP sequence that 5.75 hours are lost in the photolithographical techniques for contact formation (useful only in laboratory cells) which involve numerous steps including spin-on of photoresist, baking, exposing, developing, evaporation, metal lift-off, plating, and annealing. Substantial simplification can be achieved by screen printing the front and back contacts which takes only a few minutes. Figure 5-2 illustrates the potential of RTP with screen-printed contacts. By a reduction in cleaning time and metallization, cells can be fabricated in almost 1 hour. This process involves a simultaneous diffusion and contact firing/annealing in a single step. Many experiments will have to be performed in order to achieve such a "single-shot" process step, however, the diffusion and contact firing can be separated into two steps if unsuccessful. The key for this technology is to limit any diffusion of metal into silicon (which can short the cell) while the P dopants are diffusing to form the emitter. Use of appropriate high temperature Ag pastes doped with P dopants will help to limit the interface contact resistance. Integrating screen-printing with RTP and PECVD may achieve an industrially viable process for low-cost cell fabrication. The question, however, will be how much will be given up in terms of efficiency since screen-printing requires a very low emitter sheet resistance and the quality of the contacts are inferior compared to evaporated contacts.

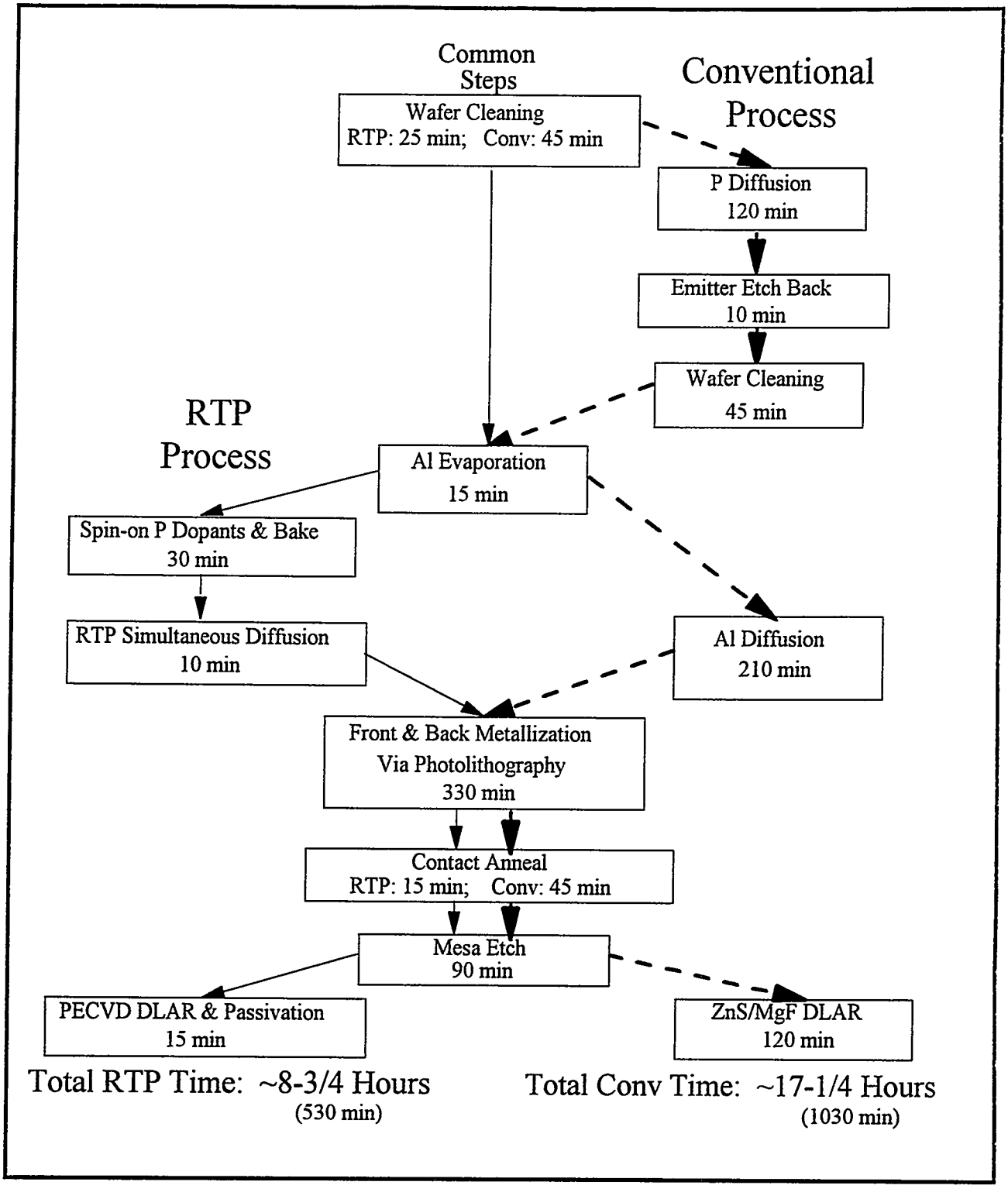


Figure 5-1. Single wafer fabrication time for RTP and conventional furnace processing.

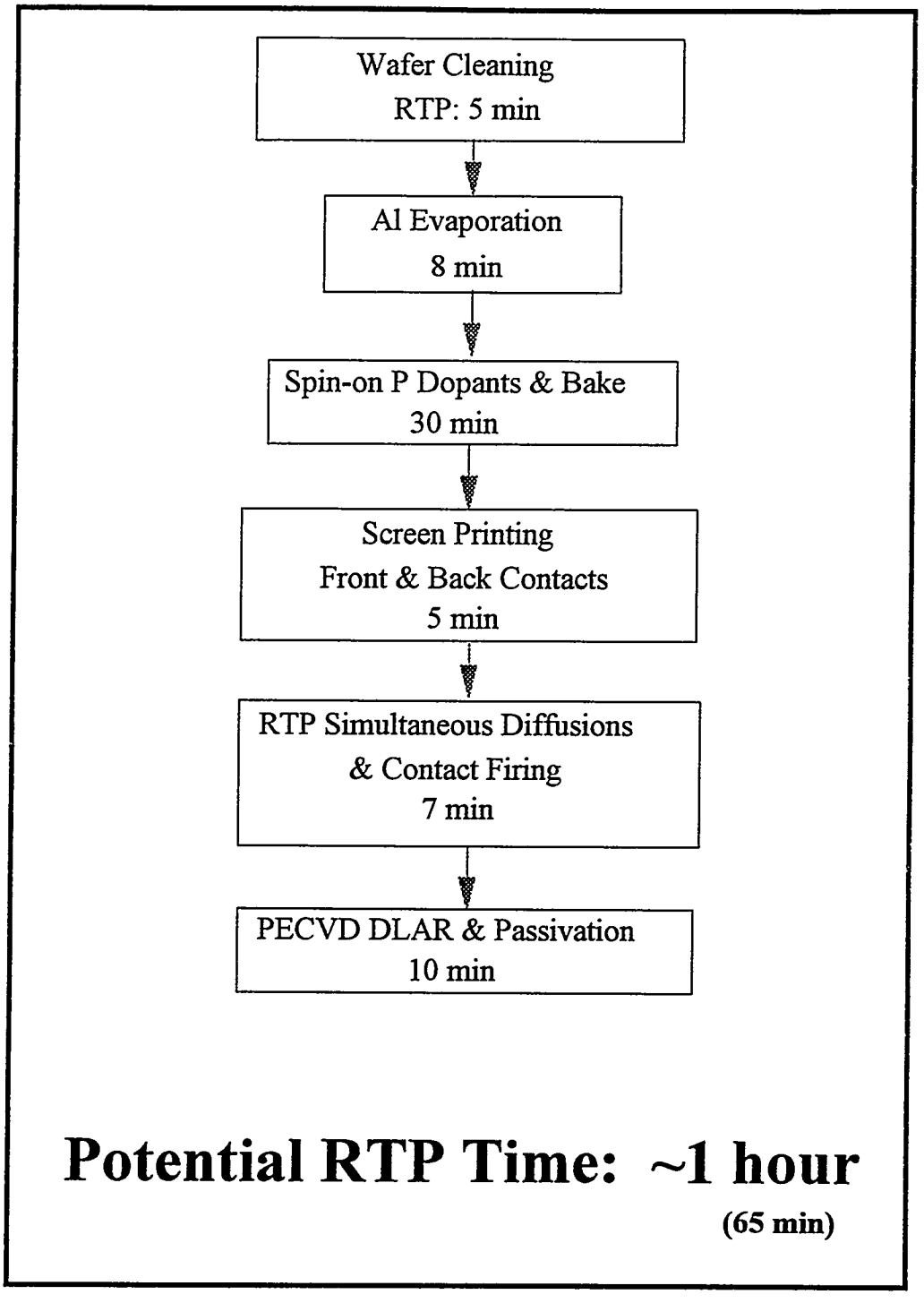


Figure 5-2. Potential single wafer fabrication time for RTP with screen printed contacts.

RTP systems can also be utilized as a multiprocessing tool. Processes such as diffusion, oxidation, annealing of contacts and films (such as antireflection coatings), and surface cleaning via ozone or UV exposure can be integrated into a single RTP system as *in-situ* processes. Multiprocessing is feasible in RTP systems because of the water-chilled "cold walls" which prevent impurities on the wall from contaminating the substrate or creating problems such as cross-contamination or auto-doping. All of these advantages tranlate into reduced cell processing cost. The goal is to incorporate these advantages of RTP into an optimized process sequence that allows cost reduction without sacrificing cell efficiency greatly. RTP technology has the potential of reducing the total **dollars/watt** for electricity production thus making PV competitive to other forms of energy conversion and more industrially relevant.

5.3 Progress of RTP/PECVD Silicon Solar Cells at Georgia Tech

Simple n^+-p-p^+ solar cells were fabricated on 0.2 Ω-cm, p-type, (100) float zone Si. Wafers were cleaned in 4:1 H_2SO_4:H_2O_2 for 5 min followed by 1 min 40:1 HNO_3:HF treatment, 20 sec dip in 10:1 H_2O:HF, 8 min boil in 1:1:5 HCl:H_2O_2:H_2O and a final 20 sec dip in 10:1 H_2O:HF. After DI water rinse and N_2 blow dry, about 150 nm thick phosphorosilica film was spun-on onto the front using a spin-on source with a phosphorous concentration of $1x10^{21}$ P-atoms/cm^3 . After a 120°C/30min. bake, 1 μm thick aluminum was evaporated onto the back of the wafer. A commercial RTP system with tungsten-halogen heating lamps below a graphite susceptor was used. Samples were placed on the susceptor, with the spin-on layer facing away from the lamps. (Note that this configuration does not directly illuminate the spin-on layer, however, there may be some reflected light from the top of the chamber heating the front. The system is currently being modified to allow direct optical heating of wafers.) After a number of experiments, an appropriate time and temperature profile was established for simultaneous P and Al diffusions with acceptable junctions depths, surface doping concentration, reverse saturation

currents (J_{oe}) and bulk lifetime for high efficiency cells. Figure 5-3 shows the programmed heating and cooling cycle which involves 20 sec. initial rapid heating at a rate of 43°C/sec to 880°C, followed by a 30 sec. hold at 880°C, a 3 min. slow cool at a rate of 0.33°C/sec to 820°C, and rapid cool of ~4.4 °C/sec until natural (uncontrolled) cooling takes over. After RTP, the phosphosilicate glass was stripped off in a dilute HF solution and the front metal grid was defined by evaporating 60 nm Ti and 5 μm Ag using lift-off photolithography. The back contact was formed by evaporation of 60 nm Ti and 2 μm of Al over the entire back followed by a 400°C/30 min contact-anneal in forming gas. Finally, a double layer antireflection coating, consisting of a 59 nm SiN layer with refractive index of 2.27 and 95 nm SiO_2 with a refractive index of 1.46, was deposited in a deposition time less than 9 min by PECVD at low temperatures (<300°C) for emitter surface passivation.

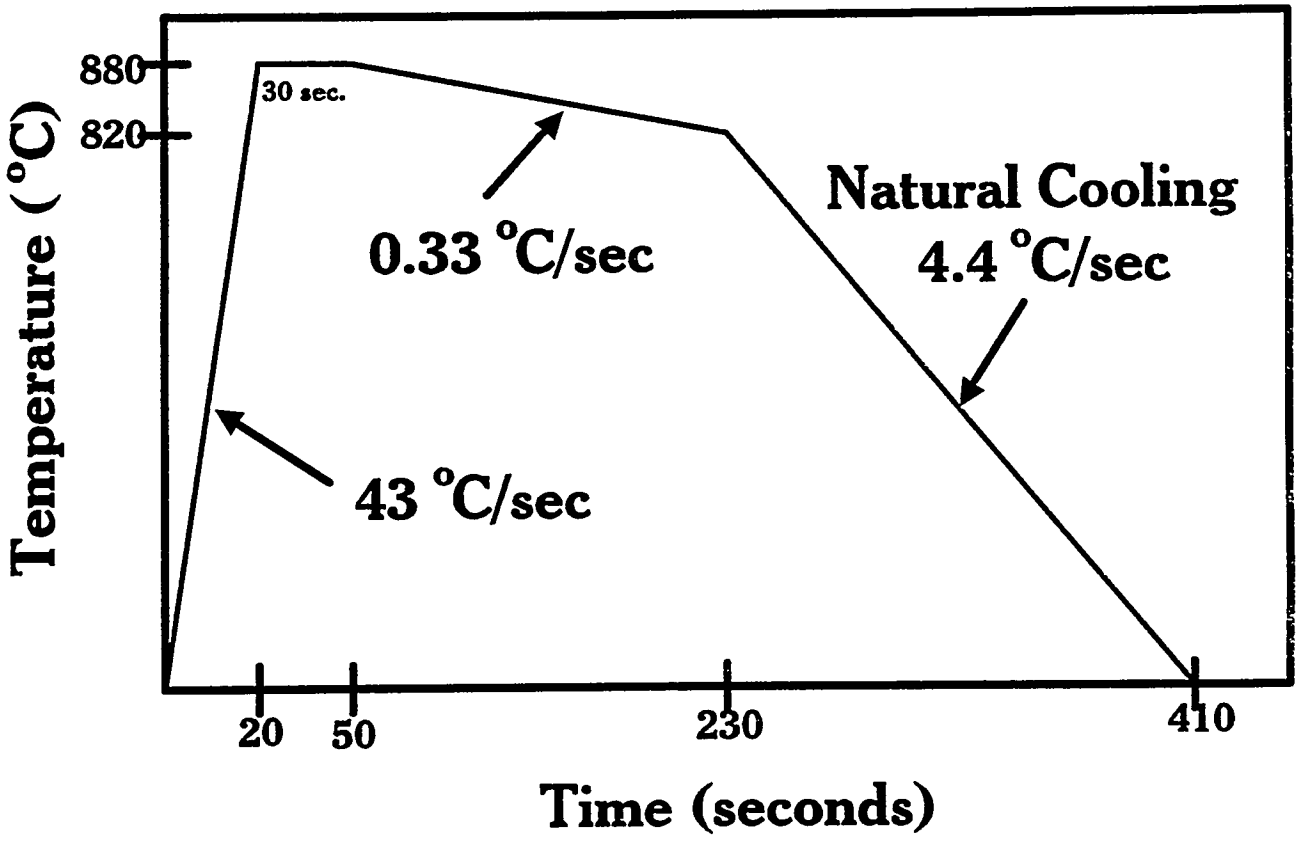
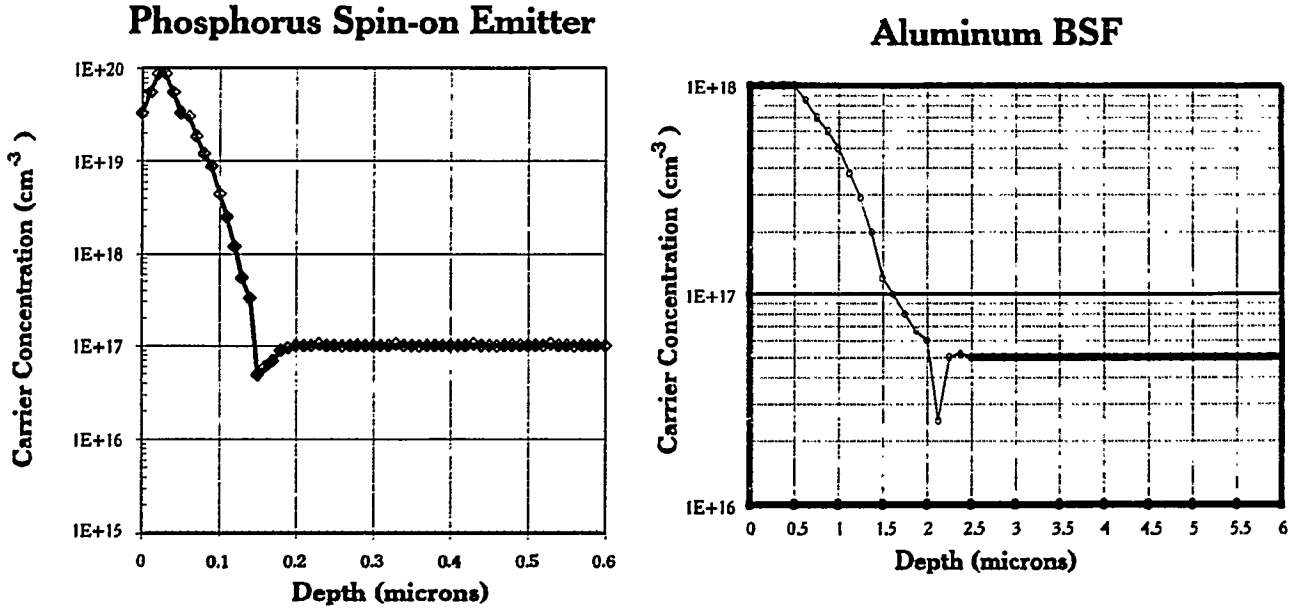


Figure 5-3. Programmed temperature cycle for RTP simultaneous diffusion and in-situ anneal.

A number of experiments were performed to select the RTP temperature cycle in figure 5-3. For example, the peak temperature of 880°C and holding for 30 sec determine the surface concentration, J_o, and sheet resistance; similarly, the slow cooling rate of 0.33°C/sec for 3 min allows the formation of an Al back-surface-field, performs Al gettering, prevents lifetime degradation due to rapid quenching from high temperatures, and creates appropriate junction depths and diffusion profiles for high efficiency cells. PECVD SiN/SiO_2 coatings provided good surface passivation, very efficient double layer AR properties, and passivation of grown-in or process-induced bulk defects in silicon. Thus, the combination of appropriate RTP sequence and PECVD coatings allows control of key material and device parameters necessary to fabricate high efficiency cells. Additionally, it reduces the thermal budget, relaxes the wafer cleaning requirements, reduces the use of chemicals and gases, and increases the throughput.

Figure 5-4 shows the front and back diffusion profiles obtained by the 7 min time/temperature cycle in figure 5-3. Phosphorus emitter profiles, measured by spreading resistance, had a surface concentration about $2x10^{20}$ cm^{-3} and a junction depth of 0.15 μm. This resulted in a sheet resistance of 80 Ω/□. The aluminum back surface field profile, determined by C-V measurements using an electrochemical etching profiler, had a surface concentration of 10^{18} cm^{-3} and a junction depth of 2 μm. These simultaneously diffused profiles are quite consistent with the requirements for high efficiency silicon cells and can be optimized further for even better results. Figure 5-5 shows the light I-V characteristics and the cell data, measured by Sandia National Laboratories (SNL). The record high 16.9 % efficiency RTP cell had a V_{oc} of 623 mV, J_{sc} of 33.6 mA, and a fill factor of 0.808. Figure 5-6 shows the measured reflectance and the internal quantum efficiency (IQE) of this cell. The IQE analysis calculated an average weighted reflectance of 5.1 % and a bulk diffusion length of 212 μm corresponding to a bulk lifetime of about 22 μs in the 0.2 Ω-cm base.



(a) (b)

Figure 5-4. (a) Front emitter and (b) back BSF carrier concentration profiles resulting from the RTP temperature cycle in figure 5-3.

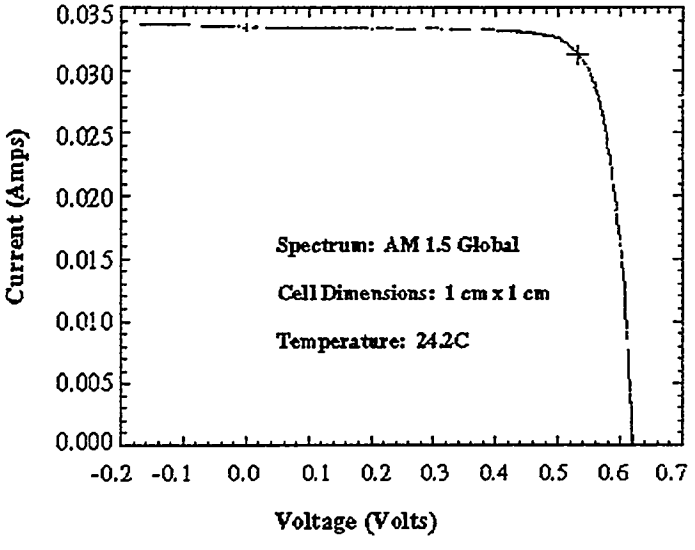
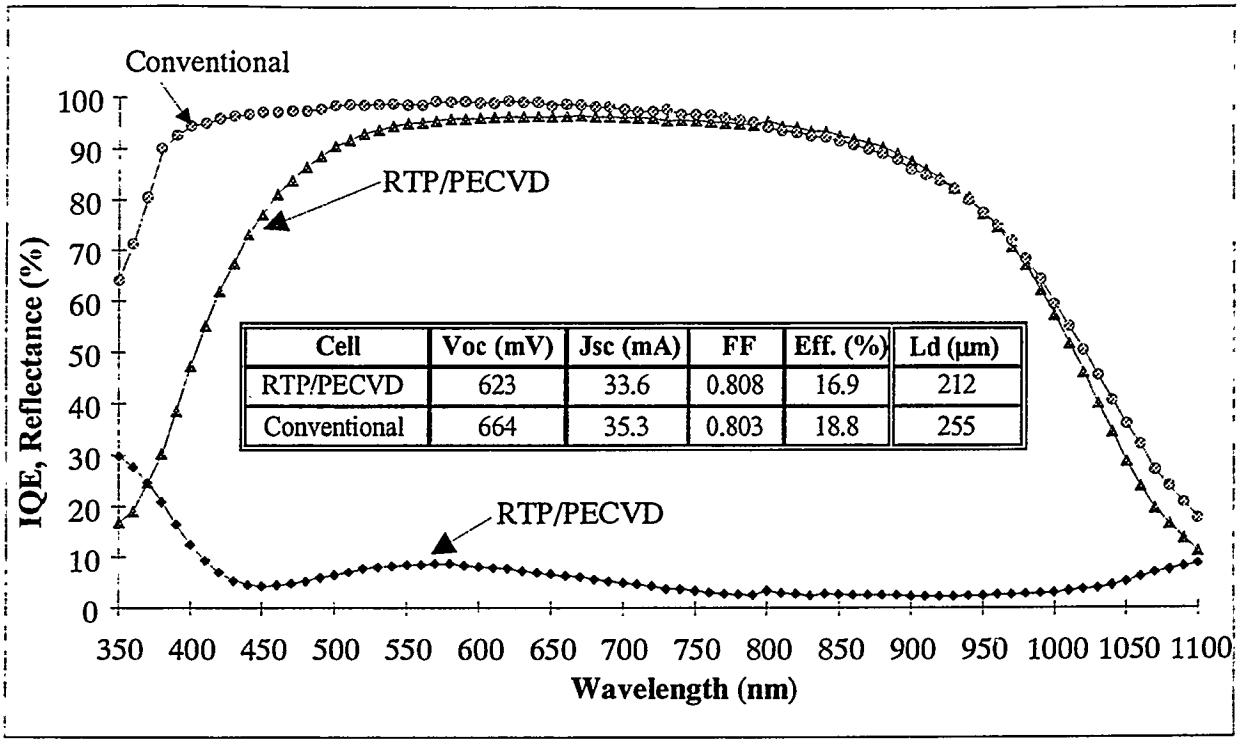


Figure 5-5. I-V curve for the 16.9% efficient RTP/PECVD solar cell on 0.2 Ω-cm FZ silicon. (Measured at Sandia National Laboratories.)



Cell	Voc (mV)	Jsc (mA)	FF	Eff. (%)	Ld (μm)
RTP/PECVD	623	33.6	0.808	16.9	212
Conventional	664	35.3	0.803	18.8	255

Figure 5-6. Comparison between the internal quantum efficiency of the 16.9 % RTP/PECVD cell and the 18.8% conventional cell. Measured at Sandia National Laboratories.

Figure 5-6 also shows a comparison of IQE and cell data of a conventional furnace diffused and RTP diffused cell on 0.2 Ω-cm FZ Si. The conventional cell fabrication involved 930 ^{o}C / 25 min phosphorus diffusion on the front, followed by an etch back to obtain a comparable emitter sheet resistance of 80 Ω/□, and 850 ^{o}C / 45 min Al diffusion on the back which includes a 10 min thermal oxide passivation on the front. The conventional cell gave an efficiency of 18.8% with a slightly better long wavelength response but considerably better short wavelength response indicating somewhat higher bulk lifetime (255 μm) and much lower front surface recombination velocity (FSRV or Sf). Emitter doping profile measurements for the conventional cell showed a much lower surface concentration of $2x10^{19}$ cm^{-3} and a junction depth of 0.6 μm. The order of magnitude higher surface concentration of the RTP emitter can increase Sf, Auger recombination, and bandgap narrowing to account for the poor short wavelength response. Absorption due to the SiN coating accounts for some of the reduced short wavelength response. Research is underway to

increase the short and long wavelength response of the RTP/PECVD cells by optimizing the J_o and bulk lifetime values to bridge the gap between the conventional and RTP cells. The RTP cell efficiencies in excess of 17% achieved in this study demonstrate the potential for low cost high efficiency RTP cells.

More recently, an even more efficient RTP cell has been fabricated at Georgia Tech. Figure 5-7 is the I-V curve for the new record high 17.1 % RTP/PECVD cell tested at SNL. This cell had a V_{oc} of 637 mV, a J_{sc} of 32.6 mA, and a FF of 0.819. Table 5-1 indicates that many RTP/PECVD cells above 16.5 % efficiency have been fabricated on FZ silicon at Georgia Tech. Also record high efficiencies have been attained on lower-cost PV materials such as 16.4 % on Siemens CZ, 14.9 % on dendritic web, and 14.8 % on multicrystalline silicon without any furnace processing. Figure 5-8 exhibits the good uniformity of these 1 cm x 1 cm cells on typical samples.

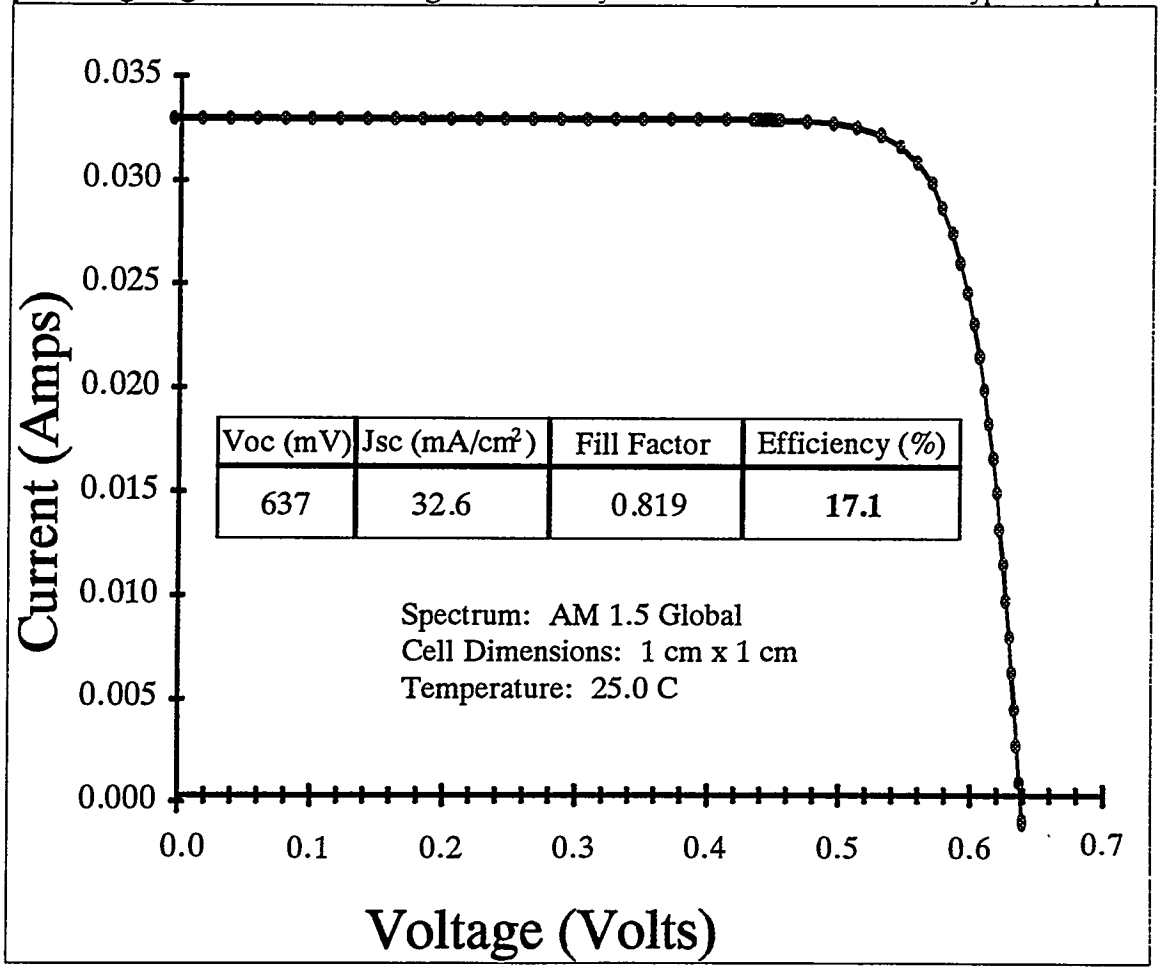


Figure 5-7. I-V curve for the record high 17.1% efficient RTP solar cell. Measured at SNL.

Table 5-1. High Efficiency RTP/PECVD Silicon Solar Cells Fabricated at Georgia Tech

Voc (mV)	Jsc (mA/cm^2)	FF	Eff (%)	Material
637	32.8	0.819	17.1	FZ
627	34.9	0.779	17.0	FZ
623	33.6	0.808	16.9	FZ
622	33.5	0.809	16.8	FZ
626	32.6	0.813	16.6	FZ
627	32.3	0.819	16.6	FZ
609	35.2	0.763	16.4	Cz
559	34.5	0.771	14.9	Dend. Web
594	33.0	0.756	14.8	mc-Si

All cells measured at Sandia National Laboratories

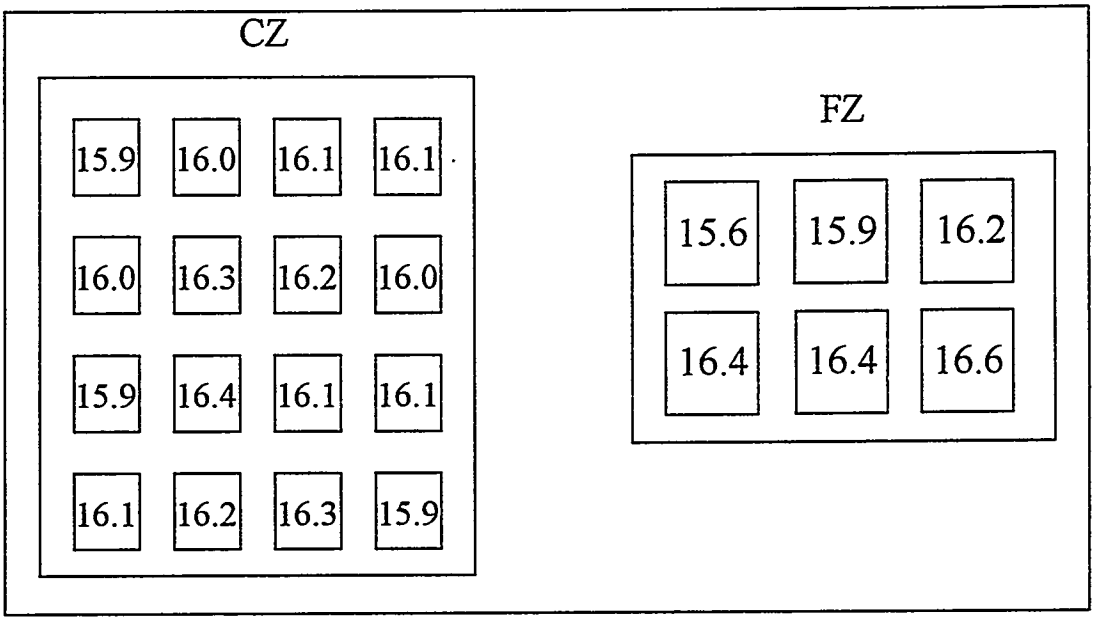


Figure 5-8. Uniformity of RTP/PECVD Solar Cells.

Figure 5-9 depicts the progress on RTP cells. Many investigators have used RTP in the past. However, because of the improved understanding of the thermal cycle and proper choice of cooling rates to limit lifetime degradation and J_0 (due to appropriate diffusion profiles), Georgia Tech has maintained the highest efficiencies on all silicon materials. In order to push these efficiencies even higher, it is necessary to properly optimize the cooling rates of the *in-situ* RTP anneal for greatest cell performance. In the next section, the effect of these cooling rates and their material specific nature revealed and quantified.

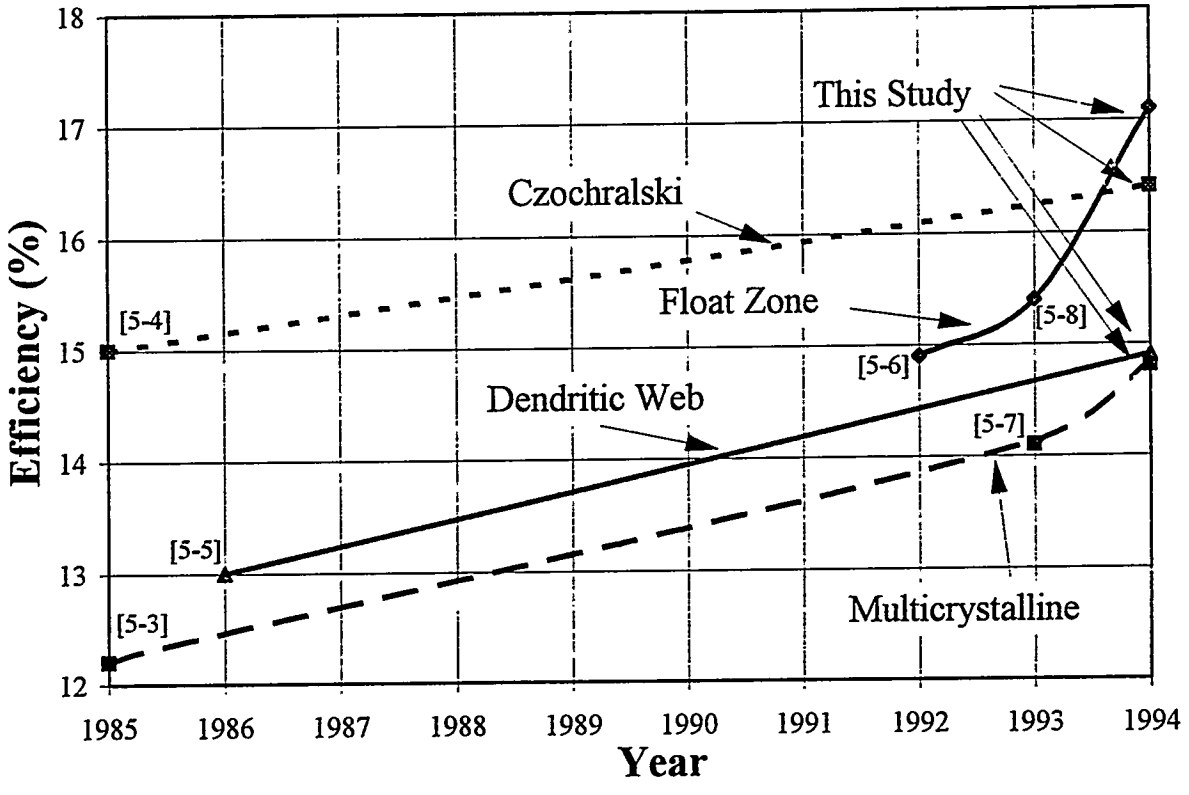


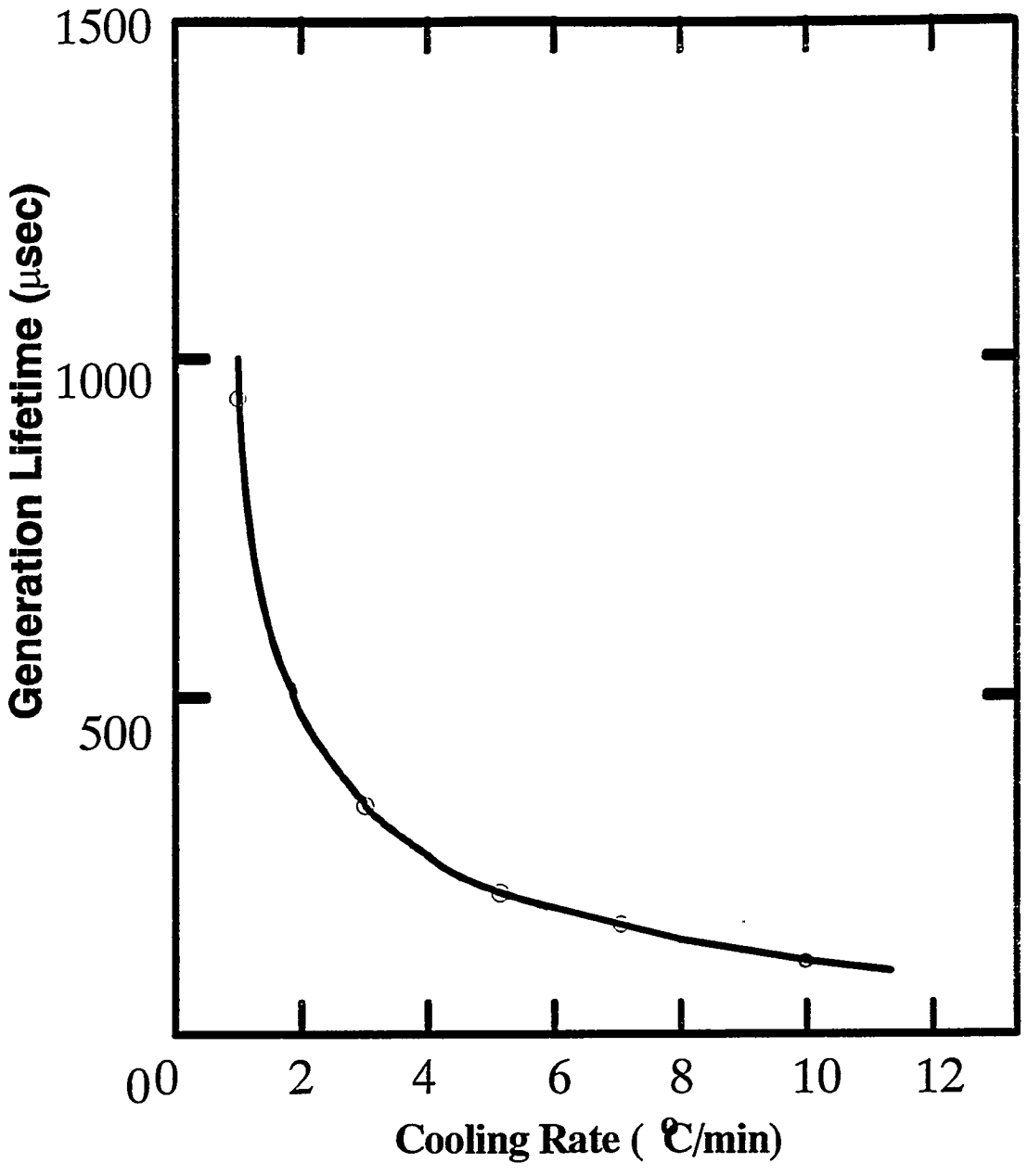
Figure 5-9. Progress of RTP-diffused silicon solar cells without any furnace treatment. (The number in brackets represents the reference.)

5.4 RTP Cooling Rate Effect on Silicon Solar Cells

5.4.1 Quenching Problems During RTP

Various investigators have attempted RTP techniques in the past for silicon solar cell fabrication with only moderate success [5-3 to 5-8]. This is because RTP is susceptible to generating electrically active quenched-in defects. The quenching induced lifetime degradation from a conventional process is well documented. Quenching can give rise to defects such as vacancies, interstitials, and point defect clusters. Dissolved impurities such as metallic contaminants are quenched into interstitial sites and can form deep levels that serve as effective recombination centers. Such defects become extremely detrimental when they are decorated with further impurities. During slow cooling these impurities may have sufficient time to migrate, precipitate, and become electrically inactive. In figure 5-10, Rohatgi et al. have shown that rapid cooling rates and high quench temperatures can significantly reduce the generation lifetime [5-9]. In this case, rapid cooling was capable of killing a material with 1 ms generation lifetime by an order of magnitude. Quenching from 900°C can severely degrade the lifetime—in this case by nearly two order of magnitude.

Researchers at Westinghouse noticed similar problems when they performed an RTP diffusion with a quench temp of 1100 °C and a cooling rate of 60 °C/sec [5-5]. Such a process would achieve only 13% efficient RTP cells on dendritic web silicon. But, when they went back into a conventional furnace to perform a high-temp anneal, they were capable of reviving the bulk lifetime and achieving cells up to 15.2 % efficiency. They found that the optimum temperatures for the post-RTP anneal was between 750°C-900°C. This post-RTP anneal, however, greatly mitigates the attractiveness of RTP since it would mean taking the wafer out of the RTP system, performing extra cleaning steps, and then going back to a long high-temp furnace step. Therefore, we have focused on performing an ***in-situ*** anneal during the RTP diffusion step. But, in order to properly optimize the annealing conditions, a better understanding of RTP cooling rates and how



Quench Temperature (°C)	Gen. Lifetime (μsec)
500	2012
600	2000
700	850
800	73
900	40

Figure 5-10. **Effect of quenching during a conventional furnace process on FZ silicon.**

they can affect cell performance is required. It is also important to recognize that the cooling rate effects may be material specific.

5.4.2 Optimization of the RTP Cooling Rate and *In-situ* Anneal

As indicated earlier, many preliminary experiments were performed to select the RTP temperature cycle in figure 5-3. However, this cycle has not been fully optimized. Of key importance is the *in-situ* anneal (between the temperatures of 880°C and 820°C) which may prevent lifetime degradation due to rapid quenching. Although a cooling rate of 0.33 °C/sec gave good preliminary results, the question of what is the optimum cooling rate has not been investigated—nor has the effect of cooling rate on different materials been assessed. To achieve higher bulk lifetimes (τ_b), we have begun in-depth characterization, modeling, and analysis to improve the understanding of RTP cooling rate effects on PV materials and devices. The lower quench temperature of 820°C was chosen because, on FZ silicon, no significant quenching problems were seen below 820°C for the 880°C peak temperature process.

Two major experiments involving four RTP cooling rates were performed. The cooling rate was varied only between the temperatures of 880°C and 820°C. In all cases, the cooling rate was maintained at a controlled rate 5°C/sec below 820°C until natural cooling takes over (at ~520°C). Figure 5-11 illustrates the four different cooling rates, namely:

0.1°C/sec which involves a 10 min *in-situ* anneal

0.33°C/sec which involves a 3 min *in-situ* anneal

1°C/sec which involves a 1 min *in-situ* anneal

~100°C/sec which involves no annealing (Quenched)

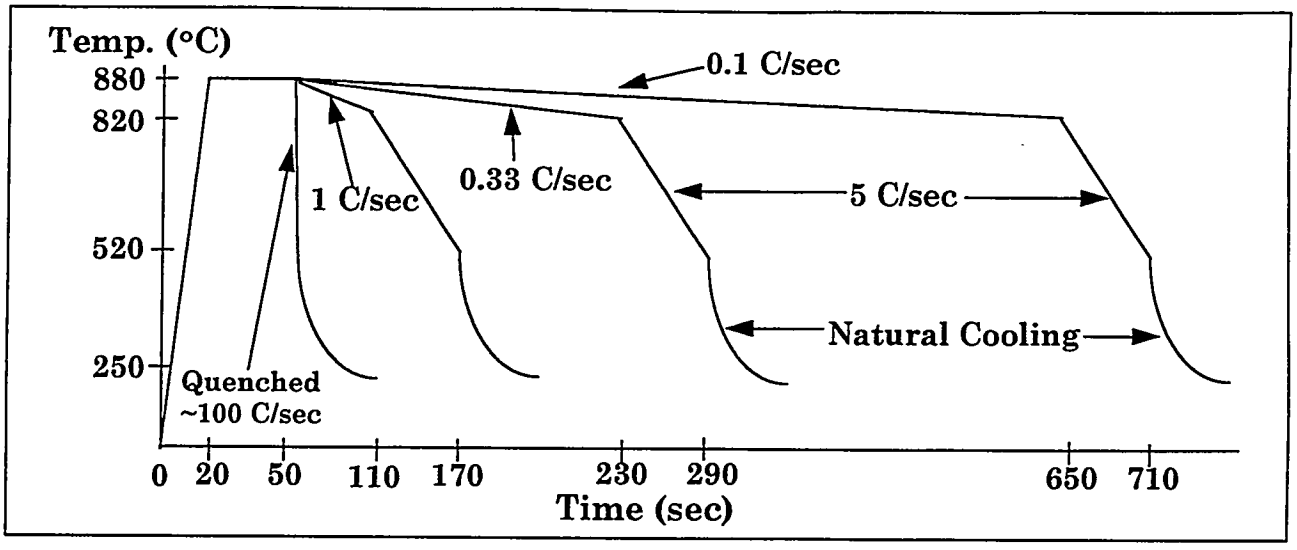


Figure 5-11. Temperature cycles of four different cooling rates between 880°C and 820°C for RTP cooling rate experiments.

The cooling rate of 0.33 °C/sec corresponds to the baseline RTP process in which the 16.9% cell was fabricated. The 1st experiment involved PCD measurements of bulk lifetime on high resistivity FZ samples for the different cooling rates. To determine the effects of cooling rate on cell performance, the second experiment involved PV materials such as low-resistivity FZ and dendritic web. Research on Cz and multicrystalline are underway and will be presented in following reports.

The results from the 1st experiment on high resistivity FZ material is shown in figure 5-12. In order to replicate cell processing, these samples were prepared with the identical cleaning and emitter formation steps involved in cell processing. Emitters were fabricated to manifest any phosphorus gettering that may occur in the cells during the RTP diffusion. Following the RTP temperature cycles where only the cooling rate was varied (figure 5-11), the emitters were etched off and the bulk lifetimes were measured with the samples immersed in HF (to passivate the surfaces).

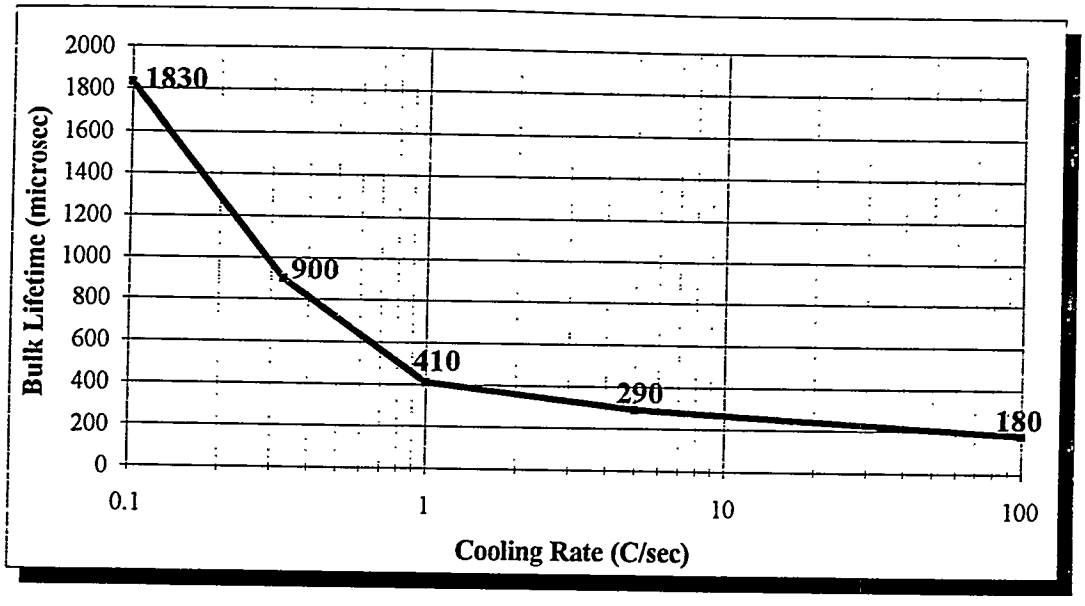
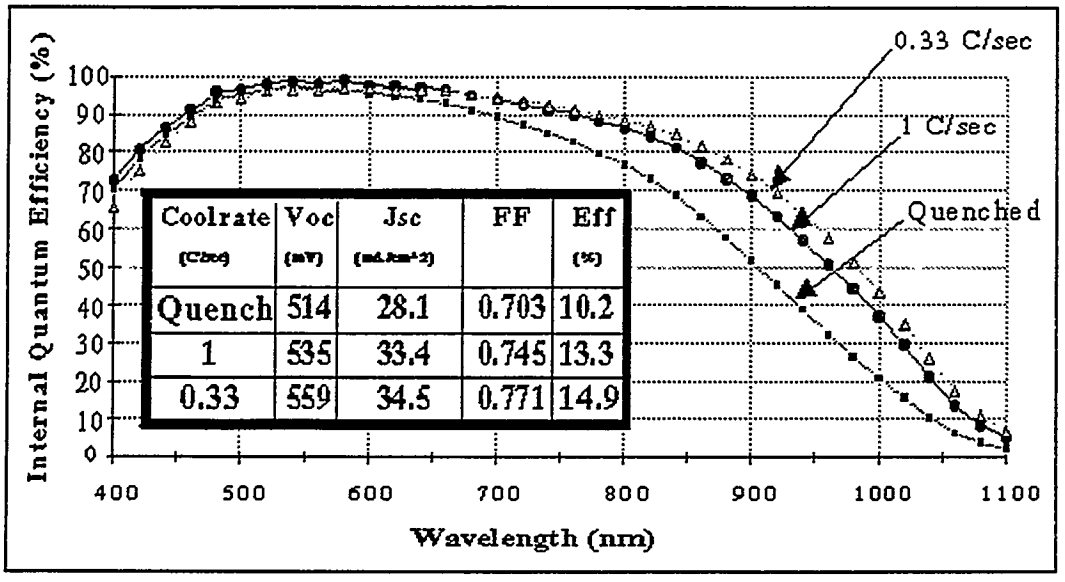


Figure 5-12. RTP cooling rate induced lifetime degradation of high resistivity FZ silicon.

For the first time, a similar trend in cooling rate induced lifetime degradation has been established for an RTP system. Figure 5-12 reveals that quenching from 880°C results in a poor τ_b of only 180 ms; however, by controlling the cooling rate to as slow as 0.1 °C/sec, very high lifetimes above 1.8 ms are achievable. Such high t_b values demonstrate that RTP systems are capable of achieving lifetimes compatible with high efficiency solar cells.

Next, the same cooling rates were applied to PV devices on materials such as dendritic web. Figure 5-13 shows that the web exhibits a strong dependence on the RTP cooling rate. Quenching of the web material resulted in only a 10.2% efficient RTP/PECVD cell; however, a dramatic improvement of 50% in efficiency occurs when web cells are slow-cooled at a rate of 0.33 °C/sec. 14.9% is the record high efficiency for RTP web cells without any furnace anneal. Figure 5-13 also depicts that there is substantial improvement in the long wavelength internal quantum efficiency (IQE) response which can be attributed to bulk diffusion length enhancement with the slower cooling rates. Extended IQE analysis confirmed this fact by depicting a bulk

diffusion length (in figure 5-14) as high as 194 μm which is over 4 times greater than that of the quenched case of only 45 μm.



Coolrate (C/sec)	Voc (mV)	Jsc (mA/cm^2)	FF	Eff (%)
Quench	514	28.1	0.703	10.2
1	535	33.4	0.745	13.3
0.33	559	34.5	0.771	14.9

Figure 5-13. Effect of RTP cooling rate on 11 Ω-cm dendritic web silicon solar cells.

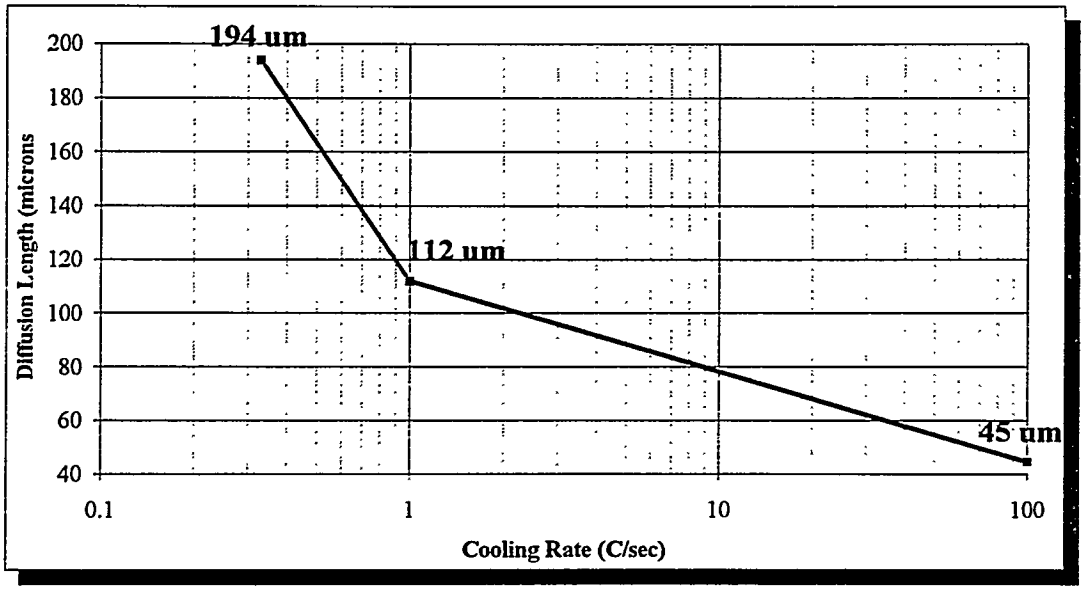


Figure 5-14. Diffusion length of the dendritic web cells as a function of RTP cooling rate.

In figure 5-15, Dark I-V analysis revealed that the reverse saturation current, Jo, drops by a factor of 5 for the slow cooled case relative to the quenched one. Since the bulk diffusion length enhancement is accompanied by an improvement in J_o, this suggests that J_{ob} is the dominating component of the total $J_o = J_{oe} + J_{ob}$, and that recombination in the base is the limiting mechanism for RTP cell efficiency on dendritic web silicon.

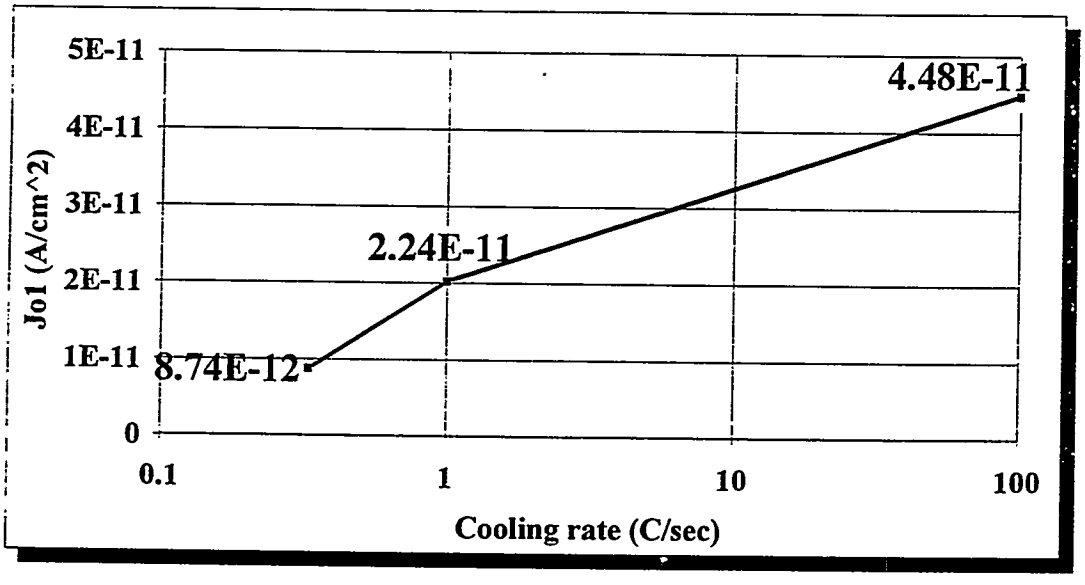
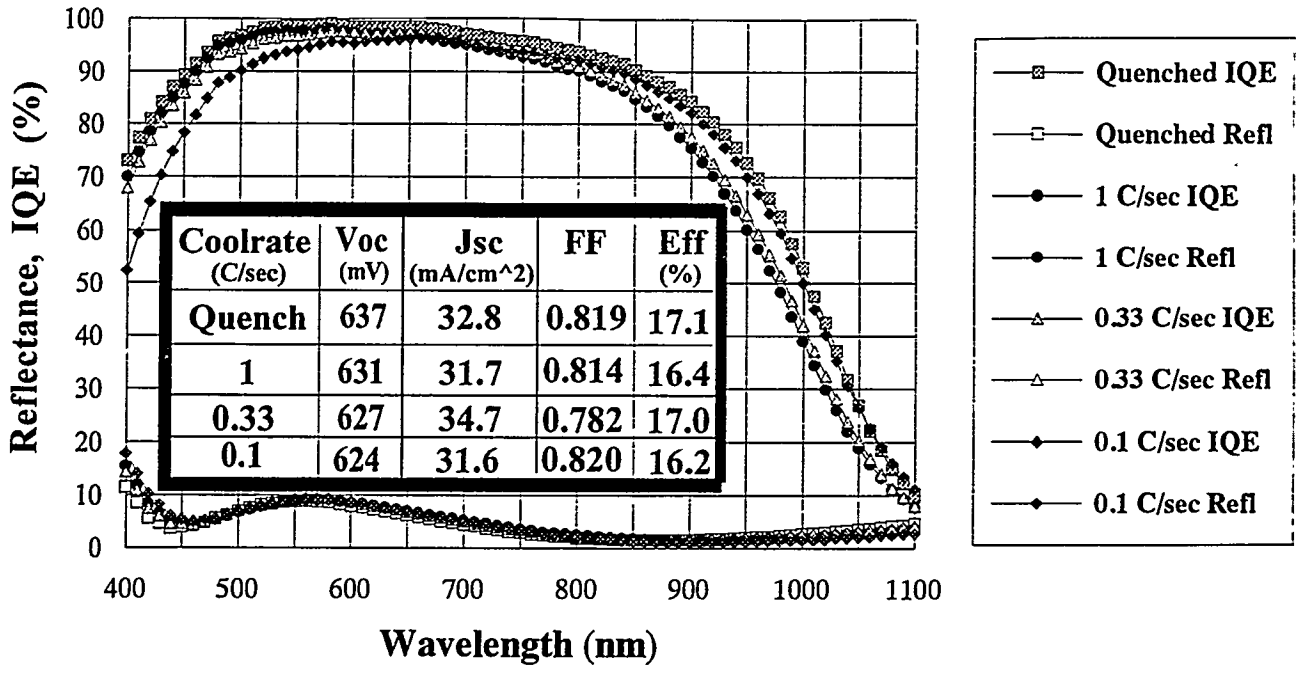


Figure 5-15. Total J_o as a function of RTP cooling rate for the dendritic web cells. (Measured at approximately 300 K.)

The performance of the FZ cells was nearly opposite (see figure 5-16). No significant trend in the long wavelength (i.e. τ_b) and efficiency was observed. In fact, the quenched cell in this case turned out to be the new record for RTP cells with 17.1% efficiency. As a result, the cooling rate effects on low-resistivity FZ is not completely understood , however, there was a clear trend in the short wavelength response.



Coolrate (C/sec)	Voc (mV)	Jsc (mA/cm^2)	FF	Eff (%)
Quench	637	32.8	0.819	17.1
1	631	31.7	0.814	16.4
0.33	627	34.7	0.782	17.0
0.1	624	31.6	0.820	16.2

Figure 5-16. Effect of RTP cooling rate on 0.2 Ω-cm FZ silicon solar cells.

Note that the quenched cell had the superior short wavelength response which decreased with the decrease in cooling rate. This phenomenon can be explained on the basis of emitter profiles. Recall that the cells with slower cooling rates encountered much longer *in-situ* annealing times—10 min in the case of 0.1 °C/sec. Since these anneals represent a substantial portion of the total thermal budget during RTP diffusion, these slow-cooled cells should have deeper emitters accounting for the observed lower short wavelength response due to greater heavy doping effects such as Auger recombination and band-gap narrowing. Unlike the web cells, it seems that these FZ cells are emitter influenced if not emitter dominated. The V_{oc} trend which decreases with cooling rate seems to support this idea.

As expected, Dark I-V analysis (figure 5-17) of the FZ cells did indeed reveal a trend completely opposite to that of the web cells. The J_o actually decreased by increasing the cooling rate. Quenching of FZ cells reduced the value of J_o by a factor of 1.5 relative to the slowest cooling rate of 0.1°C/sec. Since both the web and FZ cells had similar emitters, the J_{oe} for the web cells should be at most in the 10^{-13} A/cm^2 range (similar to the FZ cells in figure 5-17).

Figure 5-15 shows that the total J_o for the web cells is in the 10^{-11} A/cm^2 range. The remainder must therefore be J_{ob}, thus proving J_{ob} dominance for the web cells. In FZ, where recombination in the emitter (J_{oe}) accounts for most of the J_o, the slower cooling rates which involve longer *in-situ* annealing times INCREASE J_o. In dendritic web, where bulk recombination (J_{ob}) accounts for most of the total J_o, the slower cooling rates enhance the lifetime and DECREASE J_o.

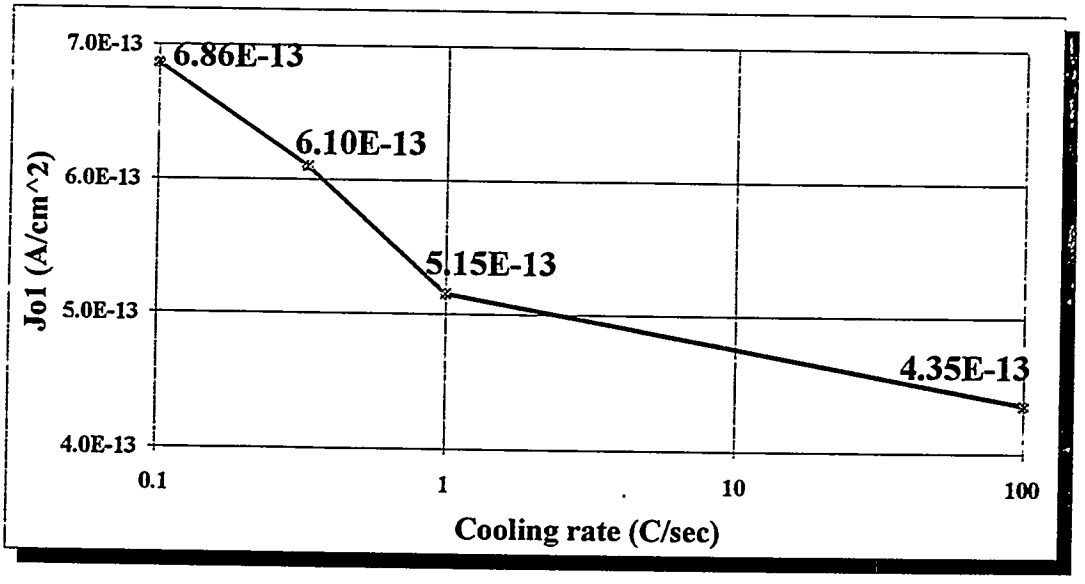


Figure 5-17. Total J_o as a function of RTP cooling rate for the FZ cells. (Measured at approximately 300 K.)

The observed difference in the performance between web and FZ cells imply that the RTP cooling rate effect is highly material and base-resistivity specific. For example, in contrast to DW, cells fabricated on FZ showed little or no improvement in τ_b. Unlike FZ, DW contains point defects and dislocations; consequently, vacancies, silicon self-interstitials, and possibly impurity atoms such as oxygen and/or iron may be quenched into electrically active sites upon rapid cool-down. Also, the high base doping of ~10^{17} cm^{-3} in the 0.2 Ω-cm FZ base masks the impact of

quenching due to two reasons. First, quenching may not influence the lifetime of heavily doped materials as much because of the low starting lifetime associated with dopant-related complexes. Secondly, these low-resistivity cells generally are more emitter (J_{oe}) controlled so that small changes in τ_b, which affect J_{ob}, do not alter the total J_o. In fact, the longer annealing times associated with the slower cooling rates hurt the short wavelength response of FZ cells due to excessive heavy doping effects in the emitter. Preliminary results of slow-cooling on 0.8 Ω-cm Cz and mc-Si exhibit the similar competition between τ_b enhancement and the undesirable increase in J_{oe}. Proper optimization of RTP cooling rates thus requires tuning both the τ_b and J_o for maximum efficiency. The next logical step for controlling the J_O is to etch-back the emitters to reduce the J_{oe} component without sacrificing bulk lifetime.

5.5 Characterization, Modeling, and Optimization of RTP Emitter Etch-Back

There are two ways to reduce the value of J_{oe}. First, doping concentrations can be decreased to reduce the recombination within the emitter. Second, techniques to improve the passivation conditions can be formulated to limit the front surface recombination. Etching-back the emitter is a convenient way to attenuate both the "dead layer" recombination within the emitter and the surface recombination due to a lower surface concentration. Although etching-back does not impair lifetime, it does increase the emitter sheet resistance and therefore the cell's series resistance. Figure 5-18 depicts the clear improvement in the short wavelength response resulting from emitter etch-back of two solar cells from 80 Ω/□ (lower curve) to 150 Ω/□ (two upper curves).

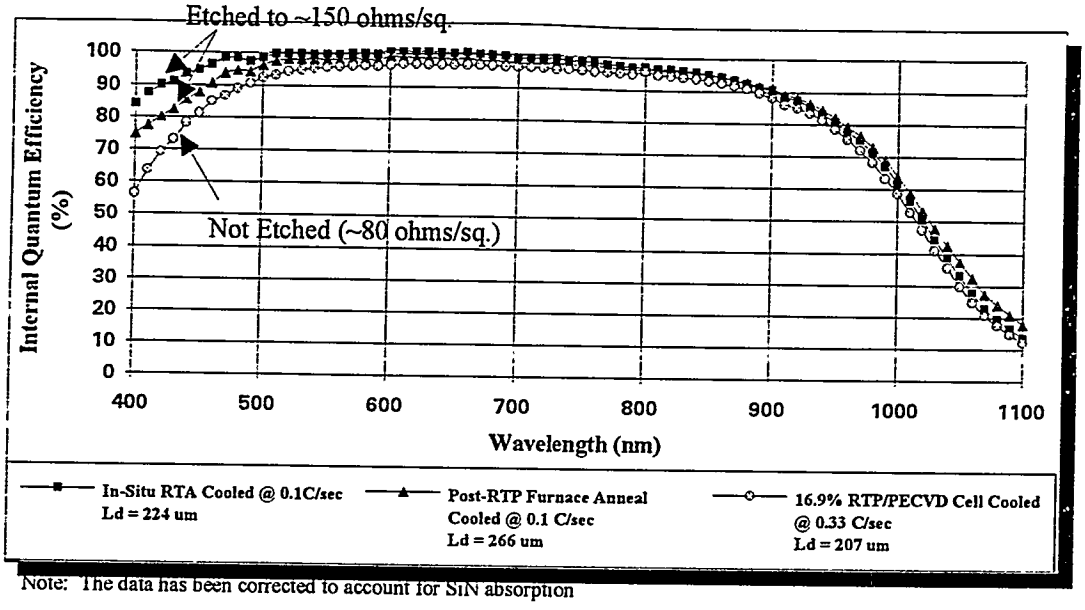
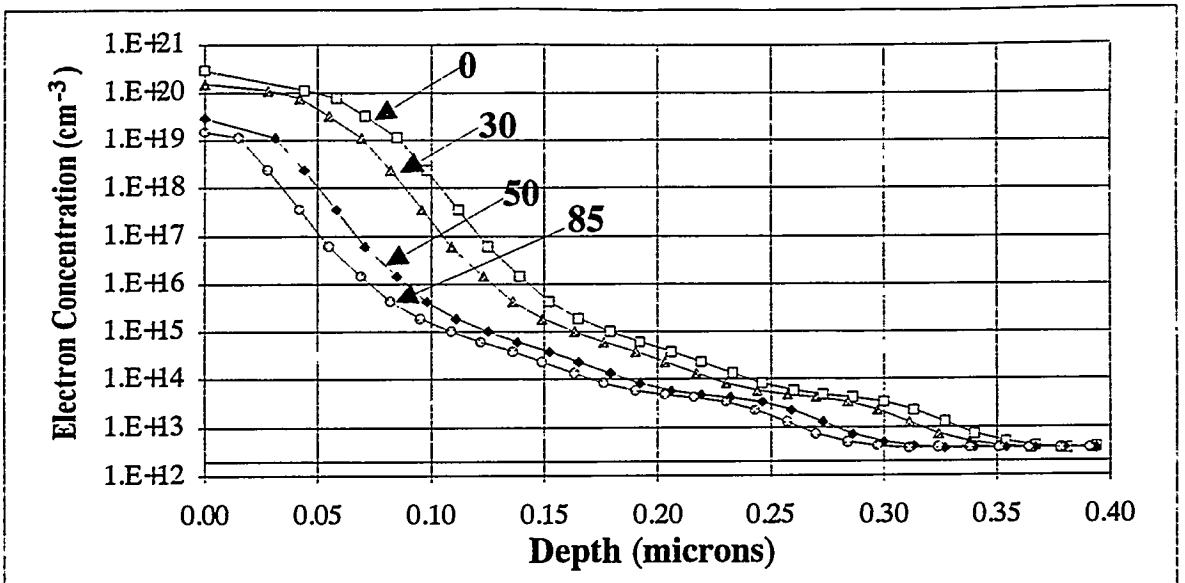


Figure 5-18. Improvement in short wavelength response due to emitter etch-back of slow-cooled cells.

In order to know how much etch-back is sufficient to optimize the RTP cell efficiency, extensive characterization and modeling is required. Proper optimization requires information about the etch-back induced change in emitter doping profiles and front surface recombination velocity (Sf).

To accomplish the first objective, spreading resistance profile measurements (figure 5-19) were obtained for four etched-back RTP emitters diffused according to the baseline RTP temperature cycle (involving a cooling rate of 0.33 ^{o}C/sec). The amount of etch-back was monitored by the etch times of 0 sec (i.e. no etch-back), 30 sec, 50 sec, and 85 sec in a solution of 1 HF : 100 H_2O : 1000 HNO_3. Both the surface concentration and junction depth decreases with etch time, but the sheet resistance goes up. The 0 sec etch time represents the baseline RTP process with very high surface concentrations of about $3x10^{20}$ cm^{-3}—resulting in detrimental heavy doping effects.



Etch Time (sec)	Surf Conc (cm^{-3})	Junc Depth (μm)	Sheet Rho (ohms/sq.)
0	3.0E+20	0.15	70
30	1.5E+20	0.13	140
50	3.0E+19	0.10	280
85	1.5E+19	0.07	1370

Etching Solution: 1 HF : 100 H_2O : 1000 HNO_3

Figure 5-19. Spreading resistance measurements of etched-back RTP emitters (diffused with the temperature cycle in figure 5-3).

Next, in order to quantify the effects of enhanced surface passivation due to the etch-back, the four etched-back RTP emitters were passivated with the typical PECVD passivation/AR coatings used for solar cells and J_{oe} measurements were performed by the PCD technique. Modeling in PC-1D allowed the computation of the Sf as a function of etch time for these RTP emitters.

The procedure for determining the Sf from measured values of J_{oe} is shown in figure 5-20. Basically, PC-1D is used to compute the cumulative recombination rate in the emitter and the split in quasi-Fermi levels at the depletion region edge on the emitter side. By iteration, the value for the

Sf can be calculated by using the formula which equates the dark forward biased current to the total current loss due to recombination in the emitter.

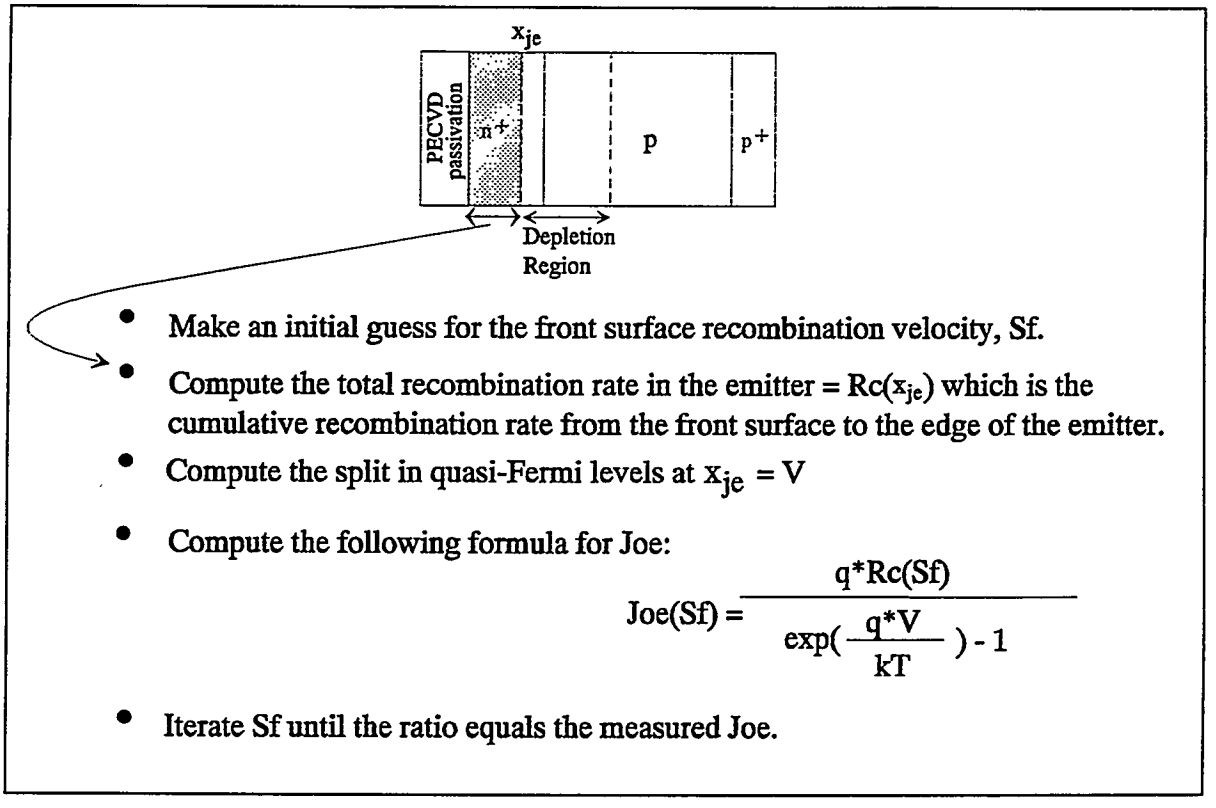


Figure 5-20. Determination of front surface recombination velocity (Sf) from measured J_{oe}..

The results of the analysis is shown in figure 5-21 which displays the measured value of J_{oe} and the computed values of Sf. Etching-back for 85 sec reduced the J_{oe} by a factor of 9—from $4.4x10^{-13}$ A/cm^2 to $4.9x10^{-14}$ A/cm^2. Without any etch-back, the Sf is very high (64,000 cm/sec); but 85 sec emitter etch-back reduces Sf by an order of magnitude (5700 cm/sec). Another important observation is that the J_{oe} of $4.4x10^{-13}$ A/cm^2 is a significant portion of the total J_o of the FZ cell shown as $6.1x10^{-13}$ A/cm^2 in figure 5-17. This fact proves the strong influence of the emitter on the total J_o in FZ cells.

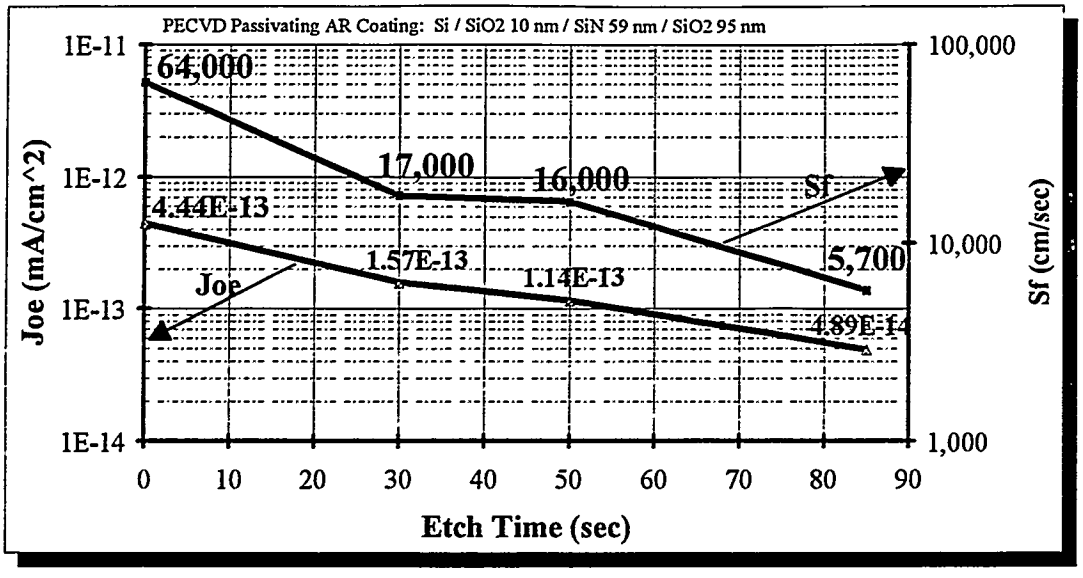


Figure 5-21. Measured J_{oe} and calculated Sf for etched-back RTP emitters with PECVD passivation. (J_{oe} was measured at Sandia National Laboratories.)

After quantifying the etched emitter profiles and front surface recombination velocities, cell performance can be predicted by PC-1D simulations. Table 5-2 presents the results of the model calculations. Note that PC-1D predicts that the cells efficiency will continue to go up (from 17.61% to 18.19%) with increasing amounts of etch time. However, it is important to note that increased amounts of etch-back increase the sheet resistance. In order to model this effect properly, it is necessary to correct the efficiencies computed by PC-1D to account for the increased series resistances due to various etch-backs. By running the *GridModel* program, to compute the series resistance for the four different emitters for a typical grid pattern used at Georgia Tech, the efficiencies were corrected. The "Eff w/ Grid" column indicates that there is a clear optimum that accounts for the competition between reduced emitter recombination and increased series resistance associated with emitter etch-back. According to this modeling, 30 sec etch-back (of RTP emitters diffused with the cycle in figure 5-3) is the optimum time which can improve RTP cell efficiencies from 17.16% to 17.53%. Optimizing the grid pattern for each particular emitter sheet resistance

makes up some of the difference for the longer etch times, however, 30 sec will still be the optimum time.

Table 5-2. Simulated Performance of RTP/PECVD Solar Cells with Etched-Back Emitters.

Etch Time (sec)	Sf (cm/sec)	Sheet Rho (Ω/□)	PC-1D w/o Front Grid			Grid w/ Rs Corrections		
			V_{oc} (mV)	J_{sc} (mA/cm^2)	Eff w/o Grid	Rs (Ω)	Eff w/ Grid	Eff w/ Optimized Grid
0	64,250	70	632.7	34.07	17.61	0.185	**17.16**	17.17
30	17,340	140	646.2	34.28	18.02	0.227	**17.53**	17.53
50	16,100	280	647.7	34.31	18.07	0.308	**17.49**	17.51
85	5,737	1370	653.5	34.33	18.19	0.935	**16.98**	17.41

5.6 Guidelines for Achieving Greater than 19% Efficient Low-Cost RTP/PECVD Cells

It has been established that a combination of in-depth characterization, modeling, and analysis is necessary to improve the efficiency of RTP cells intelligently. We are committed to pursuing this path. Through further PC-1D modeling, we have developed guidelines for achieving above 19% efficient RTP solar cells without any texturing or furnace processing. Figure 5-22 illustrates (in the first block) the existing ~17% RTP solar cell (fabricated on 0.2 Ω-cm with a τ_b of ~22 μs) which was matched by PC-1D. A 30 sec emitter etch-back has already been shown to offer ~0.4% improvement. Improving the lifetime to 55 μs will offer another quarter percent increase in efficiency. This can be done, not only by better optimization of cooling rates, but also by moving to a slightly higher resistivity of 0.5 Ω-cm. Back surface passivation which can reduce the back surface recombination velocity from 10^6 cm/sec to 10^3 cm/sec can push the efficiency well beyond 18%. This will require replacing the full metal back contact with either point or grid contacts. Further improvement in lifetime up to 220 μs which is justifiable on a 2 Ω-cm substrate will give an extra 0.5% enhancement. Lifetimes of 220 μs should be reasonable—if not conservative—since lifetimes approaching 2 ms have been reported for 500 Ω-cm (figure 5-12).

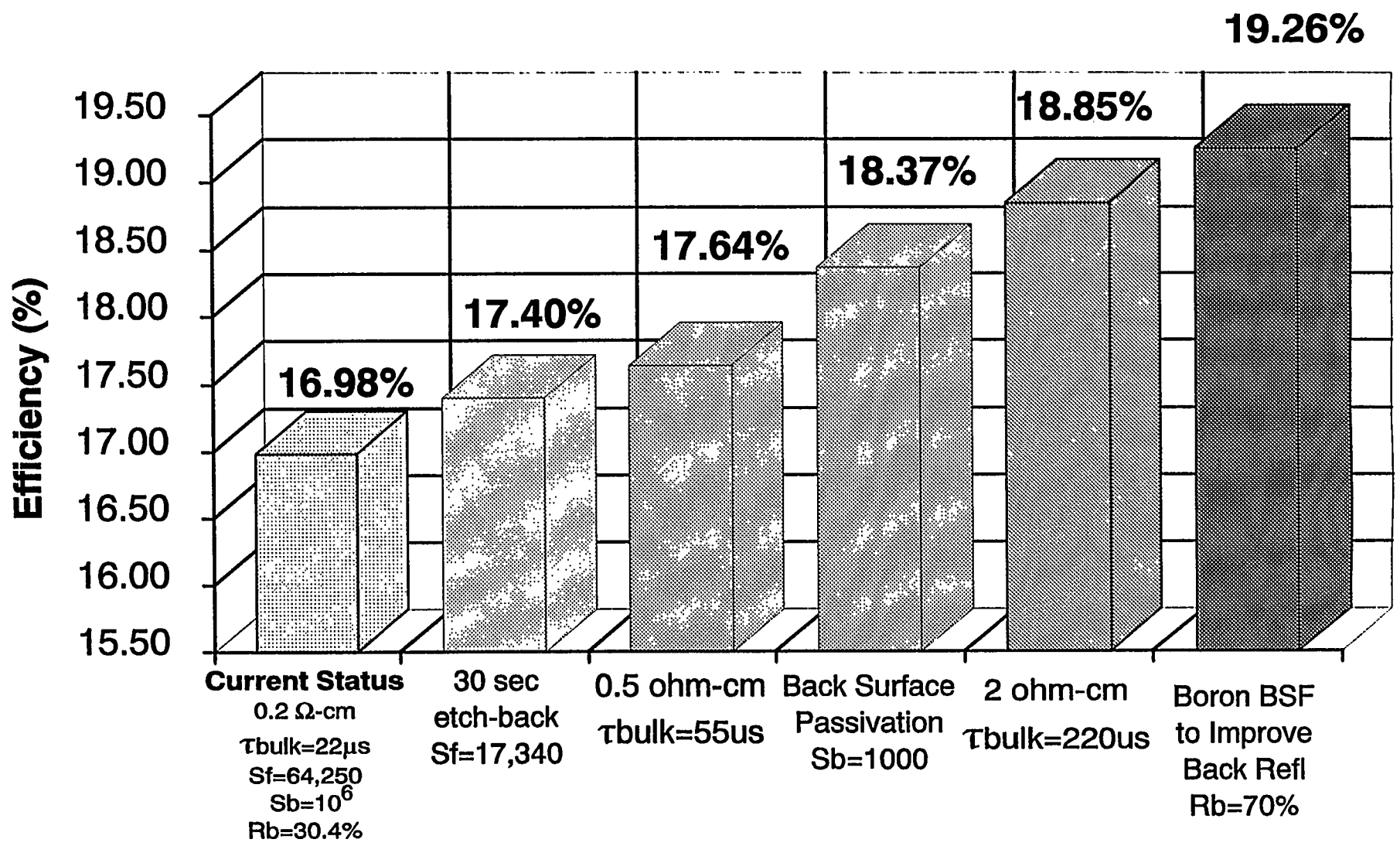


Figure 5-22. Guidelines for achieving greater than 19% efficient RTP/PECVD solar cells

5.7 Conclusion

RTP silicon solar cell efficiencies above 17% have been realized for the first time by simultaneous front and back diffusion using tungsten-halogen lamps and no high-temperature furnace annealing. Low temperature PECVD SiN/SiO_2 coating further speeds up the process and renders good surface passivation and excellent antireflection qualities. Incorporation of surface texturing, screen-printing, and the use of low-cost polycrystalline materials can make the RTP/PECVD technique even more attractive for low-cost high efficiency cells. The basic understanding of the effects of RTP cooling rate on different PV materials has been improved. Some control in bulk lifetime can be achieved by adjusting cooling rates while the control of J_o can be performed by emitter etch-back. As a result of the current understanding, Georgia Tech has achieved record high RTP cell efficiencies of 17.1% on FZ, 16.4% on Cz, 14.9% on dendritic web, and 14.8% on multicrystalline silicon. All of these record efficiencies were attained without any high-temperature furnace processing. And finally, through in-depth modeling and analysis, guidelines for achieving between 19% and 20% efficient RTP/PECVD silicon solar cells (without any texturing) have been presented to provide the future direction of research.

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