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Thermal Design and Characterization of Heterogeneously Integrated InGaP/GaAs HBTs

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***Abstract*—Flip-chip heterogeneously integrated Npn InGaP/GaAs heterojunction bipolar transistors (HBTs) with integrated thermal management on wide-bandgap AlN substrates followed by GaAs substrate removal are demonstrated. Without thermal management, substrate removal after integration significantly aggravates self-heating effects, causing poor I-V characteristics due to excessive device self-heating.**

An electro-thermal co-design scheme is demonstrated that involves simulation (design), thermal characterization, fabrication, and evaluation. Thermoreflectance thermal imaging, electrical temperature sensitive parameter based thermometry, and infrared thermography were utilized to assess the junction temperature rise in HBTs under diverse configurations. In order to reduce the thermal resistance of integrated devices, passive cooling schemes assisted by structural modification, i.e., positioning indium bump heat sinks between the devices and the carrier, were employed. By implementing thermal heat sinks in close proximity to the active region of flip-chip integrated HBTs, the junction to baseplate thermal resistance was reduced by over a factor of two, as revealed by junction temperature measurements and improvement of electrical performance.

The suggested heterogeneous integration method accounts for not only electrical but also thermal requirements providing insight into realization of advanced and robust III-V/Si heterogeneously integrated electronics.

***Index Terms*— III-V semiconductor materials, Heterojunction bipolar transistors, Infrared imaging, Integrated circuit technology, Temperature measurement, Thermal management of electronics, Thermoreflectance imaging**

I. Introduction

HETEROGENEOUS integration of III-V based heterojunction bipolar transistors (HBTs) with dissimilar technologies such as optoelectronic devices, MEMS, and CMOS electronics has the potential to allow improved functionality and enhanced capability. In particular, heterogeneous integration of III-V electronics that exhibit unmatched high frequency performance and high power gain with conventional high density Si CMOS circuits can provide performance enhancement for mixed signal and RF circuits [1].

Integration of III-V materials with silicon has been of interest for several decades, and has been pursued with varying degrees of success. However, no large-scale technology has become available. For the purposes of this effort, “device transfer” or “epitaxial transfer” approaches are promising. Device transfer is well-established and is commonly used for integration of optical and photonic devices with other circuitry. The most relevant examples use flip-chip assembly to place individual die onto a CMOS wafer [2]. Transfer of substrates with pre-grown epitaxy is less common, but offers more intimate integration, minimizing device parasitic capacitance and substrate losses [3].

In spite of the opportunities for enhanced capabilities and functionality, degraded thermal characteristics are typically a consequence of 3-D heterogeneous integration [4]. In order to preserve pre-integration electrical performance of individual devices, device thermal impedance must be considered during the early design phase of heterogeneously integrated modules. For example, GaAs- and InP-based HBTs offer superior high speed performance with higher drive voltage than silicon CMOS or bipolar devices. However, these devices are prone to suffer from self-heating effects, such as a decrease in DC current gain ($\beta=I_C/I_B$) with increase in V_{CE} for individual devices and current collapse for multi-finger devices [5]. The GaAs substrate is a relatively poor thermal conductor and the internal III-V ternary compound materials of the HBT structure possess thermal conductivities an order of magnitude lower than that for GaAs [6]. These factors lead to aggravated thermal issues that may not only degrade the device performance but also impact the device reliability. Therefore, thermal management is a key factor for realization of high performance GaAs or InP HBT heterogeneous integration.

In this work, we explore thermal management challenges and potential solutions for a GaAs-based HBT technology that is heterogeneously integrated via flip chip bonding onto an insulating, high thermal conductivity, AlN flip-chip carrier.

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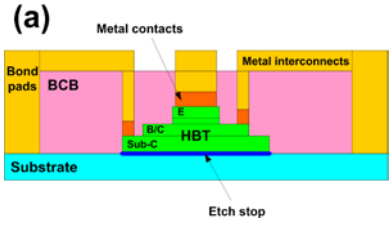
This "device transfer" process includes an additional step of GaAs substrate removal to improve size, weight, and power (SWAP). In order to reduce the thermal resistance of flip-chipped devices, a passive cooling scheme was adopted. Detailed thermal simulations were conducted for design purposes. To validate the model and assess the effectiveness of the thermal solutions, simulation results were compared with temperatures measured from thermoreflectance thermal imaging, electrical-temperature sensitive parameter (TSP) thermometry, and infrared (IR) thermography.

II. Fabrication of Heterogeneously Integrated HBT

Epitaxial layers of the InGaP/GaAs Npn HBT devices were grown via molecular beam epitaxy (MBE). The required n^+ GaAs subcollector, n^- GaAs collector, p^+ GaAs base, and N InGaP emitter layers were deposited in succession on an undoped semi-insulating GaAs substrate. The emitter InGaP composition was chosen to achieve a lattice match with the GaAs substrate. The base is carbon doped p^+ GaAs. A highly doped/graded InGaAs contact layer was grown over the emitter to form a low resistance ohmic contact. The InGaP emitter layer was also built to act as a passivating ledge over the extrinsic base region in order to reduce surface recombination. The emitter area was 10 µm x 50 µm. The structure was completed by appropriate etching of layers and the deposition of metal contacts. Spin-on benzo-cyclobutene (BCB) was used to achieve inter-level dielectric planarization. More details of the standard emitter up configuration HBTs and their fabrication process can be found in [5] and [7].

The integration approach, shown in Fig. 1, takes an individual emitter up HBT die fabricated using the standard HBT process (Fig. 1 (a)), flip-chip bonds it onto an AlN carrier, fills any voids with an underfill epoxy, and then removes the GaAs substrate (Fig. 1 (b)). The only changes to the standard HBT process are the addition of an etch stop layer underneath the device during epitaxial growth, an additional Si_3N_4 insulating layer with openings over the contact pads to reduce lateral metal (indium) diffusion along the traces, an under-bump metallization, and a metal bonding (indium) bump on top of the pads. The carrier substrate has the same interconnect metal, insulator, and bump layers as the final HBT layers, with the bump pattern matching that of the HBT die.



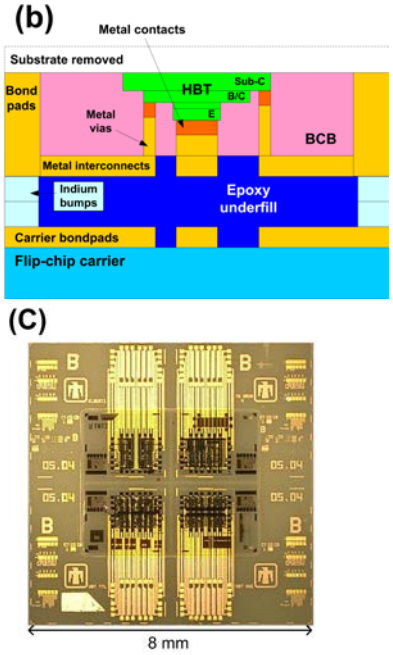


Fig. 1. Cross-sectional schematic of the integration approach to attach the GaAs HBT die to the carrier and remove the substrate. (a) Topside processed HBT with an etchstop underneath the device, insulating layer with openings (both not shown), and bonding metals (not to scale). (b) HBT device flip-chipped onto the AlN carrier with mating bumps (indium bump under emitter bond pad is not shown), underfill in the voids between the device and carrier, and substrate removed (not to scale). (c) Optical micrography of HBTs transferred onto an AlN carrier with the substrate removed.

While substrate removal after integration reduces the overall die height and eliminates substrate parasitics, this process significantly aggravates self-heating directly impacting the device's electrical performance (Fig. 2). In order to reduce the thermal resistance of integrated devices, indium bump heat sinks were positioned between the devices and the carrier. Various designs were tested as shown in Fig. 3. Locating heat sinks next to the device on interconnects is attractive in terms of ease of fabrication and device yield. The effectiveness of heat sinks positioned over the HBT emitter metal with various sizes was also investigated. The emitter heat sinks are expected to show better thermal performance since the heat generated under the emitter can be more directly dissipated through the heat sinks.

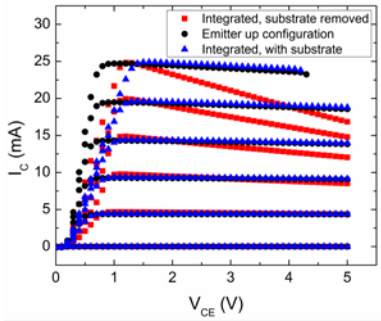


Fig. 2. I-V characteristics of devices before and after integration. For all cases I_B was ramped from 0 µA to 125 µA with 25 µA increments and T_{base}=25 ºC. The "emitter up configuration" corresponds to the device configuration illustrated in Fig. 1 (a). Devices flip-chip bonded onto the AlN carrier with the GaAs substrate still attached show electrical performance comparable with the normal emitter up configuration. After substrate removal, the device collector

current substantially decreases with increasing V_{CE}, exhibiting a large negative differential resistance due to excessive self-heating.

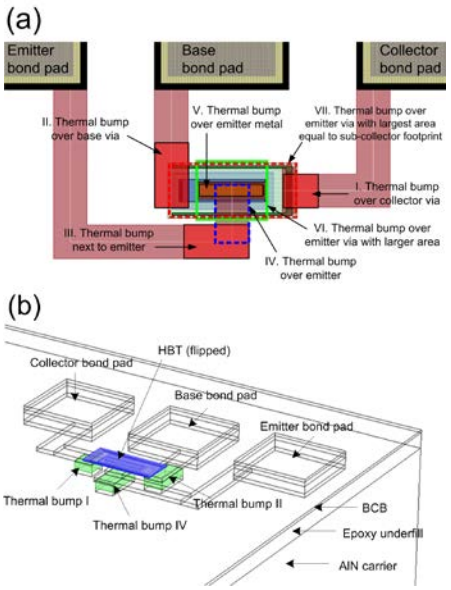


Fig. 3. (a) Heat sink designs for flip-chip integrated devices with having their substrates removed. (b) Selected 3-D representation.

III. Thermal Modeling

A steady state 3-D thermal model was developed using COMSOL Multiphysics to understand the thermal heat sink design trades for heterogeneously integrated devices. Material thermal conductivities were chosen from values reported in literature that account for temperature dependence and alloying effects (Table. I). Usage of the selected modeling parameters was validated by comparing simulation results with temperatures measured from experimental techniques detailed in the next section. Heat generation (ranging from 0.05 to 0.25 W) was assumed to occur uniformly within a cuboidal volume with a footprint equal to the emitter area (10 µm x 50 µm), vertically extending from the base-emitter junction down to the collector/subcollector interface. Emitter current crowding at the periphery of the emitter stripe caused by the finite base resistance was neglected for the purpose of model simplification and thus the heat source was assumed to be uniform across the emitter width. For the standard emitter up devices, the base temperature under the substrate was assumed to be 50 °C to match the experimental parameters used for thermal characterization. For flip-chip integrated devices, the same isothermal temperature boundary condition was applied to the carrier base plane. For all other surfaces exposed to room temperature (22 ºC) air, a natural convection boundary condition (h=5 W/m^2K) was applied. Model geometry was based on the actual device mask layout with minimal simplifying assumptions since the metal traces and through-via structures play a crucial role in transporting heat, especially for flip-chip integrated devices. The via and interface layer details are not represented in the cross-section figures including Fig. 1.

TABLE I

THERMAL CONDUCTIVITIES

Material	Value (W/mK)	Location	Reference
GaAs	$55x(T/300)^{-1.25}$	HBT active layers	[8, 9]
SiN	4.5	Passivation	[10]
BCB	0.309	Inter-level dielectric planarization	[11]
Au	317	Interconnects	[12]
AlN	$285x(T/300)^{-1.533}$	Device carrier	[13]
Epoxy	0.23	Underfill material	[14]
In	81.6	Thermal bumps	
InGaAs, InGaP	5	HBT active layers	[6]

IV. Experimental Thermometry Techniques

Device temperature measurements were conducted through the use of thermoreflectance thermal imaging, electrical-TSP thermometry, and IR thermography. These tests were performed to confirm the validity of the thermal model utilized to devise thermal solutions for the integrated device modules. Improvements in thermal management were also assessed through standard DC characterization.

A. Thermoreflectance Thermal Imaging

Thermoreflectance thermal imaging detects the change in a material's surface reflectance with temperature rise. Since the thermoreflectance coefficient [15] is very small for most materials, a lock-in technique is employed to enhance the signal-to-noise ratio to achieve good temperature images.

A Microsanj NT210B was utilized to assess the temperature rise of HBTs under diverse configurations. The HBTs were operated with periodic, 10% duty-cycle square voltage pulses (V_{CE}=1-7 V) at a lock-in signal frequency of 1 kHz while I_B was kept at a constant value (200 µA). This biasing scheme was chosen to ensure that the device temperatures would reach their steady-state values equivalent to those achieved with DC biasing. For all cases, ON-state measurement (application of a 100 ns LED pulse) was conducted 99.9 µs after initiating square V_{CE} pulses. A 20x objective was used to collect images. The diffraction limited spatial resolution was less than 1 µm for all measurements. The detector resolution was 0.45 µm/pixel using a 1624x1236 pixel CCD camera.

Interrogating 470 nm, 530 nm (these two wavelengths show high sensitivity to gold [16]), and white pulsed light emitting diode (LED) illumination were used to measure the temperature rise in the emitter up configured HBTs by targeting the electro-plated gold electrodes and interconnects. The thermoreflectance coefficients for each wavelength were determined to be $9.5x10^{-5}$ K^{-1} (470 nm), $-2.1x10^{-4}$ K^{-1} (530 nm), and $-1.1x10^{-4}$ K^{-1} (white). For flip-chip integrated devices, the backside of the sub-collector (GaAs) was measured with a 455 nm pulsed LED where the thermoreflectance coefficient had a value of $3.45x10^{-4}$ K^{-1}. The calibration (to obtain thermoreflectance coefficients) and measurement procedures

were similar to those described in [17].

The exposed gold metal surfaces for the emitter up configuration provide an adequate signal, have a well-defined calibration procedure, and are in close proximity spatially to the emitter area (having the peak temperature). Therefore this method is expected to provide adequate accuracy to validate the developed thermal model.

B. Electrical-temperature sensitive parameter (TSP) based junction temperature estimation

Electrical-temperature sensitive parameter (TSP) thermometry [18] is a noninvasive and fast technique requiring only simple experimental equipment. In addition, measurement is not limited by the device layout for fully packaged devices. However, care must be taken in choosing the correct simplifying assumptions applicable to the examined transistor depending upon its type, material system, and operating conditions. The electrical-TSP method adopted in this work [18] correlates the change in current gain (β) with the device junction temperature rise and was reported in [19] to provide reliable and accurate means to quantify junction temperatures in GaAs based HBTs. This electrical-TSP method relies on the negative differential resistance (NDR) in the HBT output characteristics originating from self-heating effects and requires only standard DC I_C-V_{CE} measurements taken with a fixed I_B at different base temperatures. The uniqueness of this method is that it can account for the dependence of the thermal resistance (R_{TH}) on the dissipated power (P_D) at a certain base plate temperature (T_{base}). Key assumptions in the technique neglect: i) the Early effect (base width modulation), ii) quasi-saturation, and iii) avalanche-multiplication. The first and second assumptions generally hold for GaAs HBTs. The third assumption applies if the HBT is characterized under operation in the linear region (forward active mode) with V_{CE} sufficiently lower than the breakdown voltage. The extracted temperatures from the electrical-TSP methods represent an average temperature over the active region (base-emitter junction) of the device.

Devices were biased in a common-emitter configuration and were tested under the forward-active mode of operation. The reference baseplate temperature was chosen to be T_{base}=50 °C. V_{CE} was swept from 0 to ~7 V and I_C was measured while I_B was kept at 200 μA for both standard emitter up and flip-chip integrated devices. When extracting the junction temperature rise from the electrical characteristics, data within the saturation region were excluded and the upper limit for V_{CE} was chosen low enough to preclude breakdown (more than 7 times less than the designed BV_{CEO}) or thermally induced permanent degradation. The HBT DC characterization was performed with an Agilent 4155C semiconductor parameter analyzer at base temperatures of T_B=40-60 °C with 10 °C increments.

The experimental procedure for this method is much simpler than those for the other two optical thermometry techniques. Also, it is the only technique that can probe the temperature rise in the active region of flip-chip integrated HBTs with the substrate still in place.

C. Infrared Thermal Imaging

Infrared (IR) micro-thermography is a widely used tool to image temperature distributions of electronic devices. This is a passive optical technique utilizing naturally emitted IR radiation from a surface. IR thermography was conducted using a Quantum Focus Instruments InfraScope II IR microscope, equipped with a 1024x1024 element InSb detector. Case studies were performed with and without emissivity enhancing pretreatment (“black” coating) of the device surfaces. 12x magnification was chosen, which offered a sampling resolution of 1.03 μm/pixel and diffraction limited spatial resolution of 2.9 μm. Pixel-by-pixel emissivity correction was performed with the devices uniformly heated to 50 °C. Measuring a total emittance, the method is most sensitive for materials possessing high emissivity (i.e., not metals). Since most materials are at least semi-transparent to infrared radiation, the sampled volume can be comparatively large. Thus, the deduced temperature is a volumetric average that may include not only the heated junction but also “cold” regions beneath it.

V. Results and Discussion

Fig. 2 shows the impact of self-heating on the I-V characteristics of flip-chip integrated devices (substrate removed) fabricated with no thermal considerations. As V_{CE} increases for a constant applied I_B, the power dissipation in the HBT increases, elevating the junction temperature above the ambient temperature. As the gain decreases at higher temperatures, the collector current, I_C decreases gradually with V_{CE}, exhibiting a negative differential resistance (NDR). At high powers, this NDR is observed in both standard emitter up configured devices as well as integrated HBTs with intact substrates. Flip-chip bonded HBTs still including the substrate demonstrated electrical characteristics similar to the standard emitter up devices. However, for integrated devices with substrates removed, the self-heating effect is much more pronounced and manifests at lower power conditions.

In GaAs Npn HBTs, the holes injected from the base into the emitter experience a larger energy barrier than the electrons injected from the emitter into the base. The ratio of the desirable electron injection to the undesirable hole injection is proportional to a factor $\exp(\Delta E_a/kT)$, where ΔE_a is the effective energy barrier difference for the electrons and the holes [20]. At temperatures higher than room temperature, this effective energy barrier difference at the base-emitter heterojunction decreases. The increasing amount of undesirable carrier hole injection contributes to the lower β in HBTs operating at high temperatures. Even though the GaAs substrate is not a great heat conductor (approximately 55 W/mK at room temperature) the surface area is very large compared to the device size. After flip-chip integration this substrate plays an effective role in laterally spreading heat away from the HBT. With the device substrate removed, the heat generated in the HBT is only transported laterally through the thin metal interconnects, vertically through BCB/epoxy underfill (both materials have thermal conductivities that are two orders of magnitude lower

than GaAs), and via natural convection in ambient air. All three paths are extremely inefficient in terms of heat transport and lead to the excessive device self-heating. Degraded device performance from the thermal limitation is shown in Fig. 2. The situation is expected to be even worse for integrated multi (emitter) finger GaAs HBT devices due to the potential for current collapse phenomena [20].

In order to mitigate the undesired consequences from excessive self-heating, indium thermal bumps were inserted between the flip-chipped HBTs and the AlN test carrier to facilitate vertical heat transport towards the carrier which has high thermal conductivity (285 W/mK at room temperature). The thermal bump (heat sink) designs under study are shown in Fig. 3. The design goal for the suggested integration scheme (flip-chip integration followed by substrate removal) was to optimize thermal bump placement and minimize its size so that an integrated device (with substrate removed) would experience a junction temperature rise similar to, or lower than, that for a standard emitter up style HBT at an identical power condition. For this purpose, a detailed 3-D thermal model was built. In order to validate its junction temperature predictions, simulation results were compared with experimentally determined temperatures for emitter up and integrated devices without any thermal bump insertion.

A. Basis for Confidence in the Thermal Model

Comparing the simulation results with temperatures acquired from thermoreflectance thermal imaging, Fig. 4 shows that the modeling accuracy is high enough to be utilized for heat sink design of integrated device modules. Temperatures measured via thermoreflectance show excellent agreement with the modeling results as this method is in general good for quantifying the temperature of metals (beneficial for the emitter up configuration) and offers a much higher spatial resolution than IR microscopy. For the flip-chipped/substrate removed configuration, 455 nm wavelength shows high sensitivity, (i.e., a large thermoreflectance coefficient is acquired in the calibration process which is a crucial factor in order to obtain accurate results) to GaAs (exposed surface of sub-collector) that ensures confidence in the measurement results. For emitter up configured HBTs, modeling shows the temperature difference between the emitter metal surface (measured by thermoreflectance) and the base-emitter junction (probed via electrical-TSP method and modeling) is less than 1 °C. The temperature difference between the backside of the sub-collector and base-emitter junction for integrated devices with no substrate was less than 7 °C in the model.

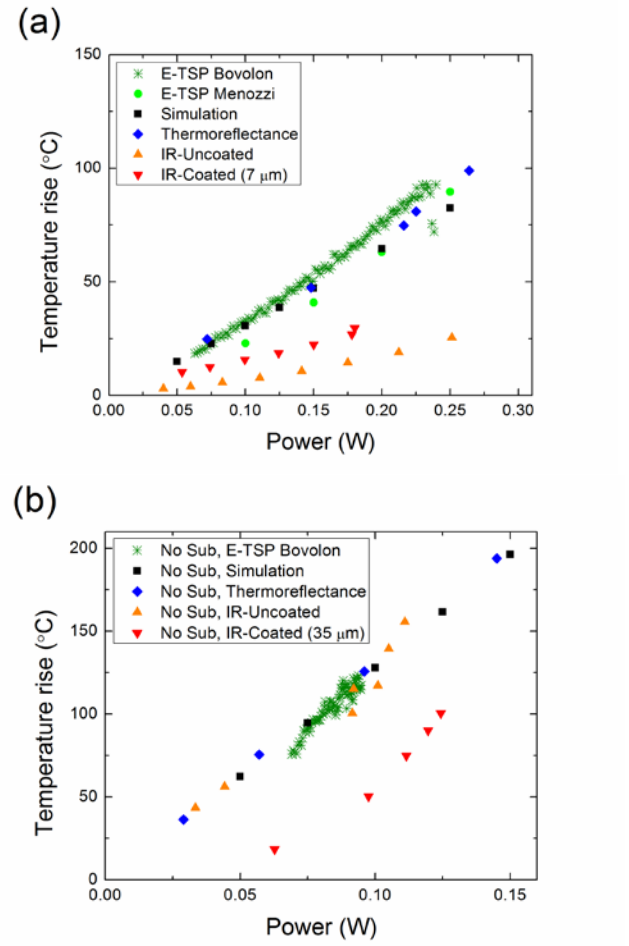


Fig. 4. Simulation results (average temperature at the base-emitter junction) compared with electrically determined junction temperatures for two configurations – (a) standard emitter up, and (b) flip-chip integrated with substrate removed.

Experimental results in Fig. 4 suggest that care must be taken when choosing a method for device thermometry. Electrical-TSP methods offer flexibility, reasonable accuracy, and simplicity in experiments as well as data processing. However, results from the electrical methods show larger uncertainty compared to temperatures acquired from optical methods unless experiments are properly setup and/or controlled. Exemplary abnormal data points are shown in Fig. 4 (a) around 0.24 W for the electrical method [18] utilized (marked as E-TSP Bovolon). Such errors may come from diverse sources including the metal trace resistance (on the AlN carrier) and improper contact between the device bond pads and the probe tips. To ensure the accuracy of the results from the electrical-TSP method adopted [18], another electrical method ([21], marked as E-TSP Menozzi in Fig. 4(a)) was used to extract junction temperature rise. These two methods account for the dependence of thermal resistance (R_{th}) on both the baseplate temperature (T_{base}) and the dissipated power (P_D), whereas most other electrical-TSP methods do not [19]. They were also reported in [19] to give accurate results for GaAs based HBT devices. The two methods show reasonable agreement with each other and also give results close to those

from thermoreflectance measurements. For integrated devices with substrates still attached, the two electrical-TSP methods [18], [21] show reasonable agreement with temperatures from modeling. Using the optical methods for this configuration is difficult as the GaAs substrate hinders optical access close to the device emitter region. Based on these observations, the electrical-TSP method by Bovolon [18] was mainly adopted in this study for simultaneous assessment of the temperature rise and electrical performance change in flip-chip integrated HBTs (substrates removed) with thermal management solutions incorporated.

In contrast, IR thermography fails to accurately measure the device junction temperature for emitter up devices largely due to the low emissivity of the emitter metal (gold). Metals, for instance, exhibit extremely low emissivities. Calibration of this parameter is therefore highly uncertain and, in our experience, most often results in an over prediction of emissivity relative to expected values. Over prediction in the calibration of emissivity, in turn, results in under-predictions of the resulting temperature (Figs. 4 (a) and 5 (a)). To overcome this difficulty, a 7 µm thick carbon particle based coating was applied to the surface of the device slightly improving correlation with the other methods. However, for this thickness, the coating was semi-transparent to mid-wavelength infrared (MWIR) radiation and thus difficulties arising from the metal persisted. Additionally, it was found that carbon particle based coatings could interrupt the device operation because of their non-negligible electrical conductivity.

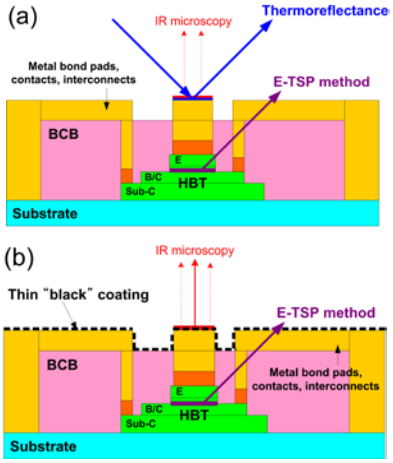


Fig. 5. (a) For the standard emitter up configuration (not to scale), IR microscopy fails in estimating the device temperature while the electrical-TSP method and thermoreflectance give accurate results. (b) A relatively thin (7 µm) high emissivity material coating is applied to a standard emitter up HBT (not to scale). IR thermal microscopy still measures lower device temperatures compared to those from the electrical-TSP method as the coating is not thick enough to prevent depth averaging of IR radiation coming from the emitter metal.

Fig. 4 (b) compares simulation results with those measured from experiments for integrated devices (substrate removed). Again, temperatures obtained from the electrical-TSP method represent the base-emitter junction temperature while thermoreflectance gives temperatures at the exposed surface of the HBT sub-collector (GaAs). In this device configuration, temperatures measured using IR thermography correlate with the other techniques and the model as shown in Fig. 4(b).

The correlation in this device geometry, as opposed to that of the emitter up configuration, is a consequence of the following factors. In the flip-chip geometry, IR thermography probes the backside region of the GaAs subcollector. The probed volume in this geometry is similar to that of both the electrical and thermoreflectance measurements as shown in Fig. 6(a). For example, IR thermography probes the temperature distribution through the thickness of the semiconductor layers down to the emitter metal since this is the region in which emitted IR light is capable of reaching the detector. IR emission from the colder bottom layers (epoxy, AlN carrier, etc.) is blocked and reflected by the 5 µm thick emitter metal as shown in Fig. 6 (a) thereby mitigating depth averaging. IR signals largely originate from the doped base region and the emitter/emitter metal (electro-plated gold) interface. Being similar in probed volumes, the resulting temperatures between the techniques thus correlate.

Finally, we note that the oft-used method of applying a high emissivity coating applied to the surface of a device for IR-thermography can also be a source of error. As shown in Fig. 4 (b), applying a thick layer (35 µm) of a carbon based coating to ensure opacity to MWIR radiation (measured emissivity was 0.98 at 50 °C), negatively impacted the accuracy of the measured temperatures. This is the result of large through-thickness temperature gradient that forms across this layer owing to its low thermal conductivity (<1 W/mK) as shown in Fig. 7. Such approaches must therefore be employed with caution.

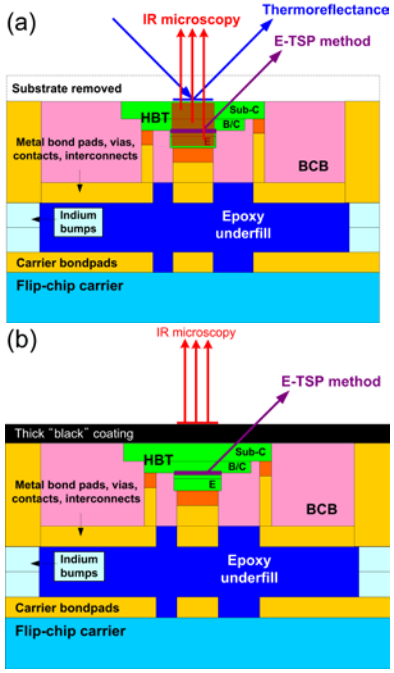


Fig. 6. (a) For a device under the flip-chip integrated and substrate removed configuration (not to scale), all three thermometry methods give results that agree well with each other. In particular, for this case the IR microscope collects MWIR radiation from only the HBT bulk which leads to reasonable results. (b) Thick (35 µm) high emissivity material coating applied to an integrated HBT (not to scale). IR thermal microscopy significantly underestimates device temperatures compared to those from the electrical-TSP method and thermoreflectance.

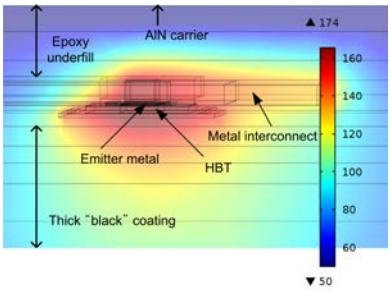


Fig. 7. Simulation indicates a large temperature drop occurs across the 35 µm thick high emissivity coating film. This leads to considerable misinterpretation of the device temperature rise. Errors were observed to be as large as >70 °C as shown in Fig. 4 (b).

B. Evaluation of Heterogeneous Integration Thermal Management and Mitigation Approaches

From design studies using the developed thermal model, it was found that placing an indium thermal bump with a footprint identical to the sub-collector area (45 µm x 100 µm) directly over the emitter metal (with electrical isolation achieved by depositing a 100 nm Si_3N_4 in between the metal structures) would guarantee that the final integrated device would experience a junction temperature rise comparable to that for a standard emitter up device at same power conditions (Figs. 3 and 8). Alternatively, locating thermal heat sinks on the metal interconnects is advantageous in terms of ease of processing, but leads to reduced heat removal from the transistor.

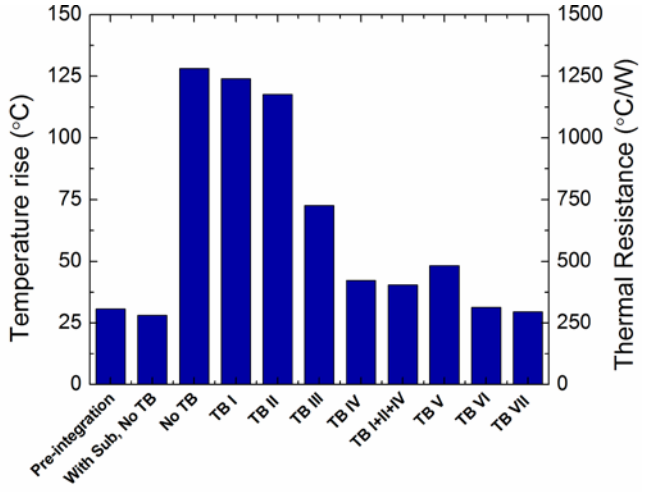


Fig. 8. Junction temperature rise and junction to baseplate thermal resistance for various device configurations predicted by modeling at a power dissipation level of 0.1 W. The goal is to achieve a temperature rise similar to that for a standard emitter up case (Pre-integration). Flip-chip integration without removing the substrate (With Sub, No TB) does not cause self-heating issues. The third through the last columns are configurations with the substrate removed. Thermal bump notations follow those defined in Fig. 3. Placing thermal bumps on interconnects (TB I-III) does not effectively remove the heat from the device. Larger thermal heat sinks located over the emitter metal (TB IV-VII) show better performance. The thermal bump area of designs V, VI, and VII were 10 µm x 50 µm, 45 µm x 50 µm, and 45 µm x 100 µm, respectively.

Among the various structural modifications studied, two representative cases, i) heat sinks on the emitter and base metal interconnects (TB II+III following notations defined in Fig. 3) and ii) direct heat sink over the emitter metal with an area identical to that for the sub-collector (TB VII as indicated in Fig. 3 and 8), are discussed here. By implementing a better structural layout, the junction temperatures of transistors were significantly reduced leading to electrical performance improvement. For the targeted operating condition (P_{diss}=0.1 W), the integrated devices with a large heat sink over the emitter show a measured reduction in their average device-to-baseplate thermal resistances (510 °C/W) by over a factor of two relative to designs without thermal structures (1240 °C/W). However, the devices still show a thermal resistance larger than the ideal value predicted from simulation (290 °C/W). Without indium heat sinks, the thermal energy is dissipated from the device junction region solely through the emitter, base, and collector metal interconnects. The cross sectional area of these interconnects is only 5 µm x 125 µm, resulting in large thermal resistance. The underfill material (epoxy) is unable to assist heat transport away from the junction region due to its low thermal conductivity (0.23 W/mK). Adding a heat sink directly under the emitter metal provides an effective mechanism for heat dissipation towards the AlN carrier and therefore significantly lowers the junction to baseplate thermal resistance. These results are illustrated in Fig. 9. Further increasing the heat sink area over the emitter metal (larger than the sub-collector footprint) did not significantly reduce the device junction temperature as predicted from simulation. It is likely that the thermal contact among the emitter metal, Si_3N_4 passivation and the indium heat sink were not intact as intended. Despite this, the effectiveness of the heat sink was sufficient to prevent thermally driven reliability problems [5] at the targeted operating condition (P_{diss}=0.1 W). However, improving process parameters, for example by reflowing the heat sink metal (indium) before bonding to reduce the thermal boundary resistance at the heat sink bonding interfaces, is necessary to further increase the heat sink effectiveness and meet predictions from simulation. Other thermal solutions have been considered including replacing the epoxy underfill with a material with higher thermal conductivity [22] and using a gold via or heat shunt from the emitter to the substrate instead of the indium bumps. These approaches have promise for improved effectiveness.

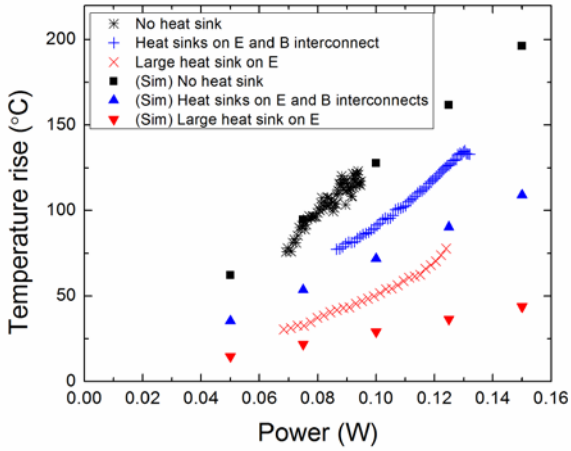


Fig. 9. Simulation results compared with temperatures measured from electrical-TSP method for three different substrate-removed devices with different heatsink configurations. Only the electrical method's results are displayed here as it also directly reflects change in electrical performance of the

device. Locating thermal bumps next to the device (on interconnects) is not as effective as placing a large thermal bump over the emitter metal which significantly reduces the device's thermal resistance. Due to processing limitations, actual fabricated devices do not completely meet expectations from simulation.

VI. Conclusion

An approach for heterogeneous integration of GaAs-based HBT devices onto wide-bandgap AlN carriers that implements an electro-thermal co-design scheme was demonstrated as an early step towards realization of heterogeneous integration of III-V and dissimilar technologies. Improved form factor is accomplished by flip-chip mounting of the III-V devices onto an AlN carrier with indium bumps, followed by removing the compound semiconductor substrate. Processing methods for flip-chip integration and substrate removal of III-V compound semiconductor integrated circuits onto insulating or wide-bandgap substrate materials have been developed. Electrical performance of the integrated HBTs comparable to standard HBTs with emitter up configuration on the native substrate was achieved through proper thermal management for nominal operating conditions. By implementing close proximity heat sinks to the active region of flip-chip integrated HBTs, the junction-to-baseplate thermal resistance was reduced by more than a factor of two.

The results presented in this study demonstrate the practicality of the flip-chip integration scheme. Suggested modeling and thermal characterization methods give insight into devising thermal solutions essential for realization of advanced and robust heterogeneously integrated III-V/CMOS electronics. The proposed integration scheme can be extended to InP-based HBTs, and allows future extension to co-integration of HBTs with silicon circuitry and optoelectronic devices.

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