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Reduced Complexity RHBD Logic Cells for 32-nm SOI ASICs

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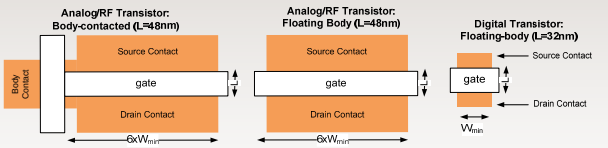
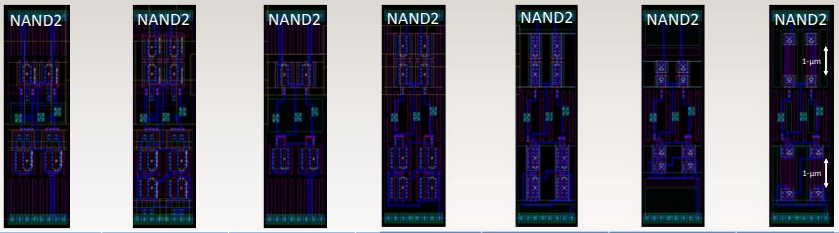
Abstract

Reduced complexity 32-nm silicon-on-insulator (SOI) logic cell libraries and test chips have been developed for evaluation in harsh radiation environments. SOI-specific radiation hardened by design (RHBD) methods, including body contacts and stacked transistors, were leveraged for improved radiation hardness. The number of cells and their complexity was intentionally limited to lower development costs and simplify portability to other SOI technology nodes.

Body Contacted and Floating Body Transistors

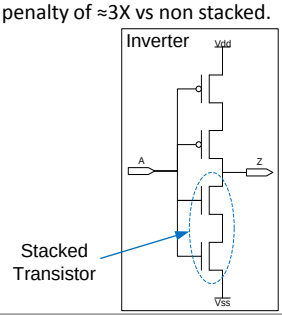




	Seven 32-nm Test Chips	ABNS	ABST	AFNS	AFST	DFST	DFSS	DFSX
Logic Cell	Digital Transistors					✓	✓	✓
	Analog/RF Transistors	✓	✓	✓	✓			
	Body Contacted Transistors	✓	✓					
	Floating Body Transistors			✓	✓	✓	✓	✓
	Stacked Transistors		✓		✓	✓	✓	✓
	Large Width Transistors (≈6xW_{min})	✓	✓	✓	✓	✓		
	Narrow Width Transistors (≈W_{min})						✓	✓
	1-µm Sensitive Node Spacing							✓
	Clock Speed (typical PVT conditions)	1936 MHz	690 MHz	2598 MHz	936 MHz	1026 MHz	931 MHz	845 MHz
IO Pad	Floating Body Transistors			✓	✓	✓	✓	✓
	Body Contacted Transistors	✓	✓					

Stacked Transistors

Used to mitigate particle strikes on any single transistor. Speed penalty of ≈3X vs non stacked.



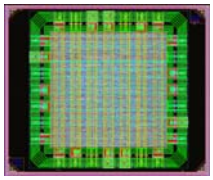
Reduced Complexity Cells

Number and complexity were minimized to lower cost and streamline portability.

Cell Name	Description
BUF	Medium-drive buffer for data signals.
CLKBUF	High-drive buffer for clock signals.
NAND2	Two-input NAND gate.
DFFR	Positive edge-triggered D flip-flop with asynchronous active-low reset.
TIE0/TIE1	Tie off to Vss/Vdd.
FILL	Empty cell to meet density rules.
ANTENNA	Cell to fix antenna violations.

Test Chip Layout

All seven test chips used the same 1.2x1.0-mm^2 auto-place-and-route layout to implement a Logic BIST function. Separate test chips were required for each RHBD library to isolate leakage current degradation and photocurrent generation in radiation environments.



Summary

- 32-nm test chips are currently in fab at IBM Trusted Foundry, and will undergo evaluation in relevant radiation environments.
- Enables direct comparison of body contacted transistors versus floating body transistors.
- Enables direct comparison of analog/RF transistors versus digital transistors.
- Enables direct comparison of stacked designs versus non-stacked designs.

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