SAND2015-0328C

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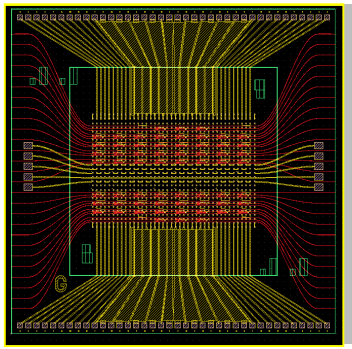
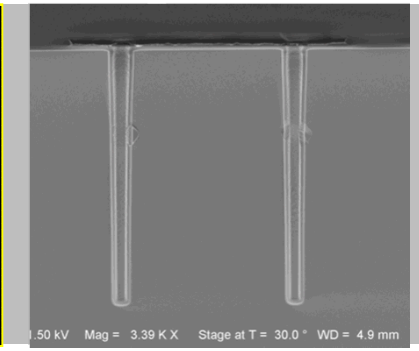
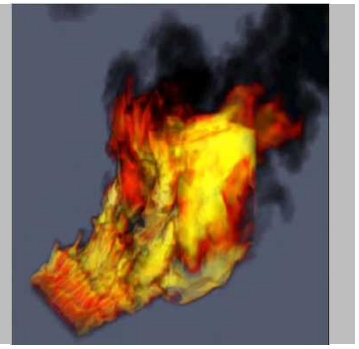
AbPro

Define an Abstract Protocol

Enable most any supporting component to interact with other components, and facilitate new and increasing future capabilities







U.S. DEPARTMENT OF ENERGY
NNSA National Nuclear Security Administration

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The State of Interconnections?

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- DDR-4 is the last full DDR-n standard
- HBM and HMC are going in different directions
  - For good reasons, but also need to come together
- Multi-level memory is coming
- Big benefit to get NAND (and other NV technology) as a 'first-level' memory: Fully addressable as memory using the same read and write commands as upgraded DRAM
- Need a standard in which there is a structure that allows new chip versions and new features to be done, but that keeps/allows compatibility between the old and the new, including support of many of the current protocols

Why AbPro?

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- Increased flexibility in system architecture
- Enable scalability, lower power, and higher performance—
  at the same time
- Reduced interaction complexity and reduced data motion
- Increased memory capabilities
  - New memory operations for increased performance, reduced power
  - Different types of memory (DRAM, NV, …) w/ common commands
- Design to support (encapsulate) some current protocols
- Support multiple data widths and rates, while enabling components to always communicate
- Enable common resilience capabilities, while supporting extensions as desired

Some Proposed Major Features

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- Intended to be fully open
- Packetized
  - Fixed high-level framing, but ‘sub-frames’ as needed to support other and extended protocols
- Variable length
  - But fixed flit size for compatibility for all versions
- Full Duplex
  - Any component can originate a request
- Configuration agreement between components at startup
  - Startup at slowest defined rate and smallest link width.
  - Then switch to faster & wider if supported on both sides
  - Also can agree on use of an encapsulated protocol

Possible Physical Features

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- Three link widths
  - 4, 8, 16 wide
- Three or four link rates
  - 1, 4, 8, 16 Gbits/sec ??
- Support both single-ended and differential transmission
  - Bandwidth growth will need differential lanes
- Spare lanes?
  - Would propose instead that links degrade width, if not minimum

Possible New Capabilities

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- Atomic and general Move functions in the memory system, ultimately supporting general computation in memory
- Chip-to-chip operations so can do things like indirect references, memory data base, search operations (and ?) without direct CPU interaction at low levels
- Better exception and error interaction with lower overhead
- Easier to use and lower overhead mechanisms for communication and synchronization
- Interaction with functions (like GPUs) that are the same whether the function is in the same chip or in an external chip
- New functions in new chips without upsetting the protocol or breaking then-existing components

Possible New Capabilities

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- Encapsulation to support multiple different protocols but running under AbPro
  - Interact at startup to choose a ‘sub’ protocol
  - Packets then contain needed data to support the chosen protocol
  - Command fields in AbPro allow for ‘foreign’ values
    - Not interpreted in AbPro; passed on as data

Moving Forward

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All the following is subject to change, but seems to be a reasonable way to proceed

- Form an interest group and a have a web site to enable discussion and interaction
- Define an initial proposal.
  The interest group is kept informed and provides input
- Do simulation and FPGA experiments to explore the design space and then verify the proposal (to the extent possible), while showing the benefits of abstraction and the proposal
- Run the proposal past the interest group
- Define physical interfaces that implement the protocol and *sell the results*

Development and Timeline?

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- Interest group signup starts now
- Website: **devabpro.sandia.gov**
- Have a version 0.9 ready in 6 to 9 months
  - What help can we get to do protocol simulation and/or logic experiments using FPGAs?
- Taking into account interest group feedback, AbProSpec 1.0

- Start definition of physical implementation(s)?

Sign Up

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- devabpro.sandia.gov accepting general signups and has a whitepaper on the need, benefits, etc.
- The site will have multiple discussion areas
- drresni@sandia.gov for questions or suggestions as things get started

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Input and Questions?

drresni@sandia.gov