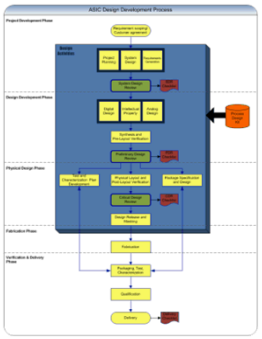
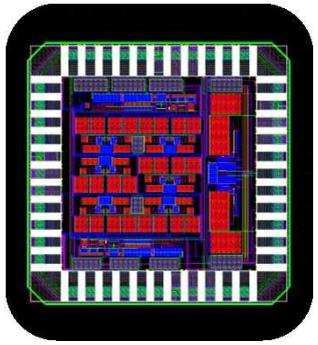
SAND2015-0305PE

Exceptional service in the national interest

Sandia National Laboratories





An Overview of the Sandia Labs Ultra-Fast X-ray Imager (UXI) Program

Liam Claus

1753 ASICs and SoC Products

U.S. DEPARTMENT OF ENERGY

National Nuclear Security Administration

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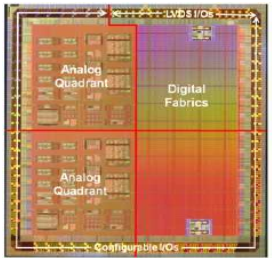
Agenda

Sandia National Laboratories

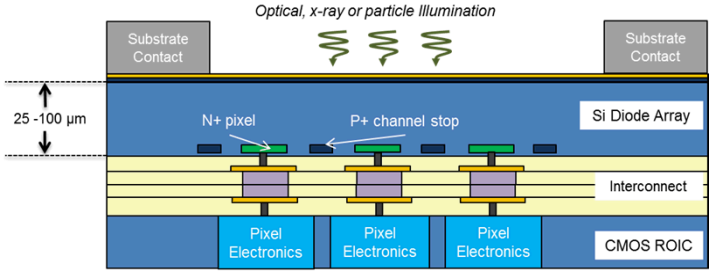
- Imager Overview
- UXI ROIC Discussion
- UXI Future
- Photodiode overview
- Hybridization overview
- Packaging overview
- ROIC Tradespace
- Roadmap

Imager Lexicon

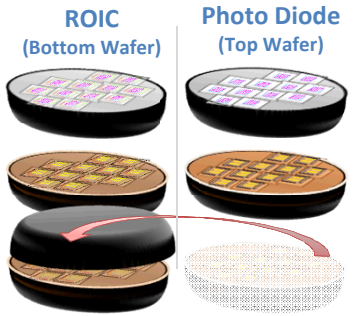
- Application Specific Integrated Circuit (ASIC)
  - Generic IC, often contains many millions of transistors
- Read Out Integrated Circuit (ROIC)
  - Camera circuitry ASIC, no photodetector
- Photodiode Array
  - Array of n x m photodiode elements
- Focal Plane Array (FPA)
  - Occasionally the photodetector array but often used to describe a complete camera
- Pixel/Unit Pixel
  - Unit cell of pixel transistor elements
- Hybridization
  - Process of “gluing” ROIC to the photodetector
- Hybrid Pixel Array Detector (HPAD)
  - Complete camera - hybridized ROIC & photodetector



ASIC



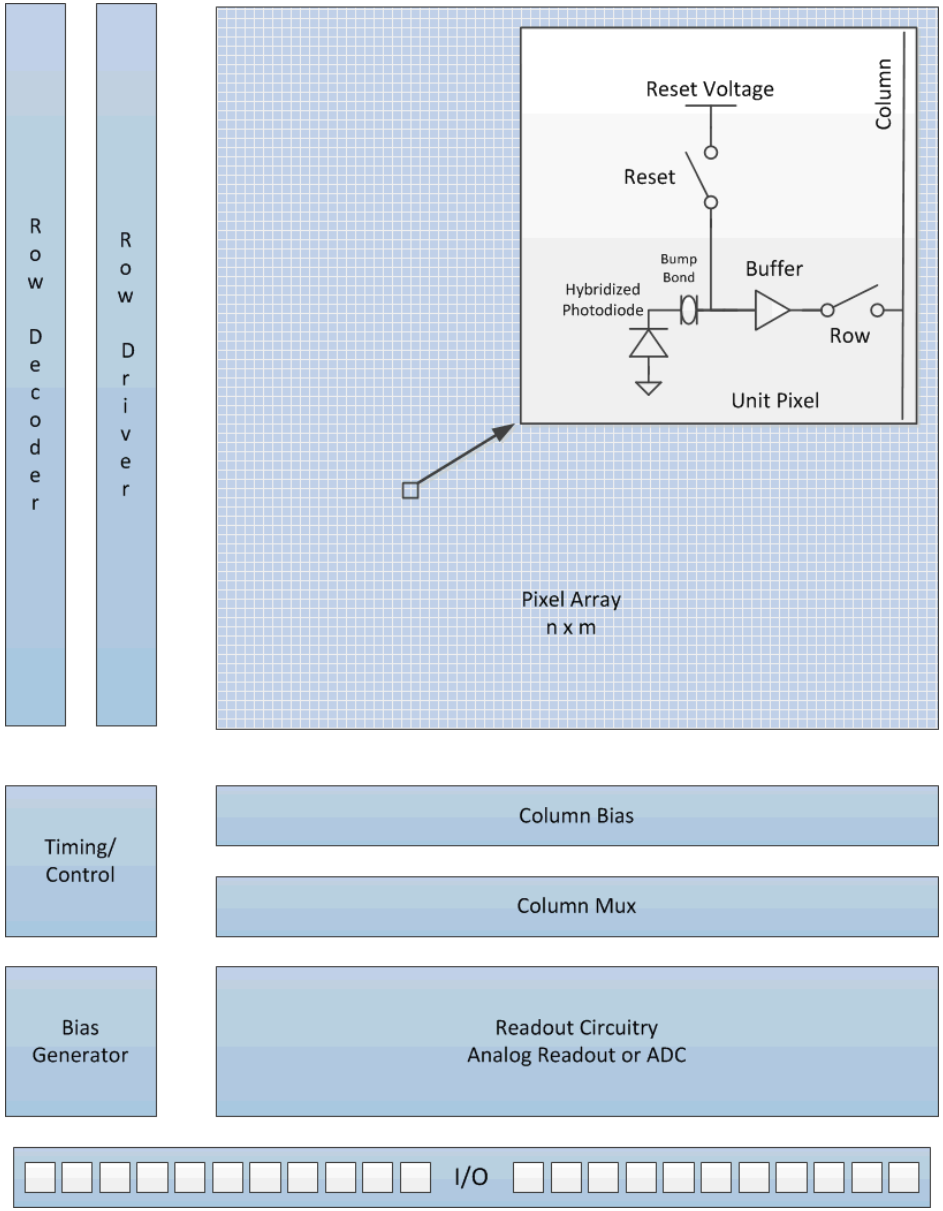
Hybrid FPA Cross Section



Wafer To Wafer Hybridization

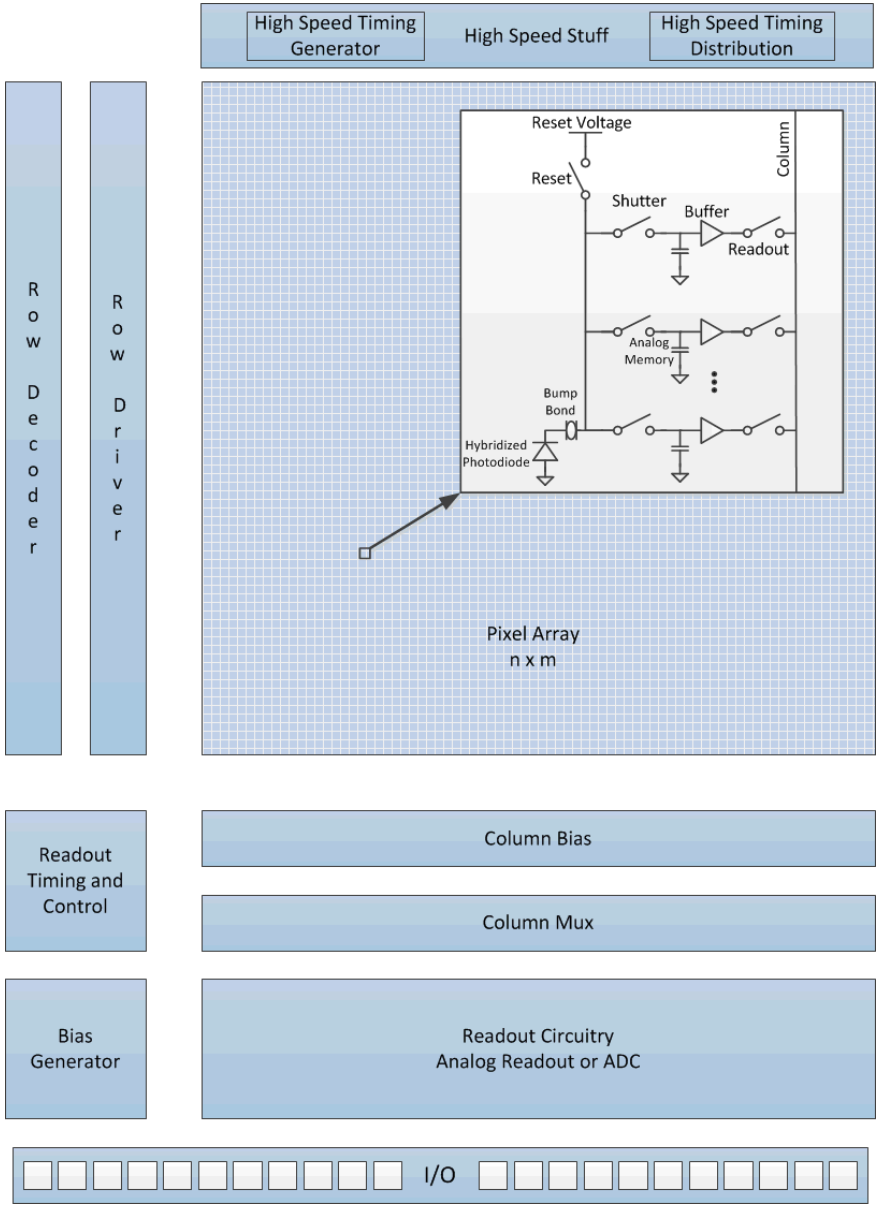
CMOS Camera Block Diagram

- Photodiode acts as photon to electron transducer
  - Diode can be monolithically incorporated into the pixel for either Front Side Illumination (FSI) or Back Side Illumination (BSI)
  - Diode can also be separate and hybridized to the ROIC (hCMOS)
- Pixel circuitry converts charge (Q) to a voltage or current
- Support circuitry facilitates decode and readout of the pixel array
  - Possible to incorporate on-chip A/D conversion and therefore high speed readout



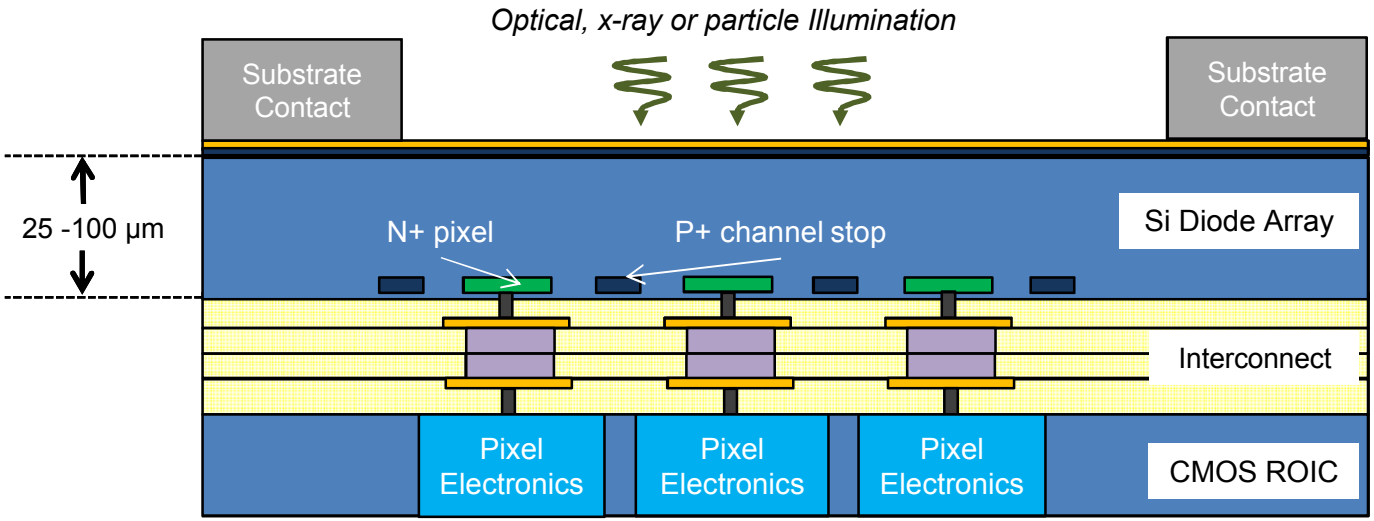
Framing Camera Block Diagram

- A framing camera adds in-pixel storage for multiple frames of data
  - Effectively we multiplex multiple pixels into one
- Electronic shutter implemented with a transistor switch
- In-pixel storage and on-chip timing allows for high speed operation
- We generate high speed timing signals on chip
- Somehow we distribute the high speed timing signals to the pixels



CMOS Hybrid Image Sensor Cross-Section

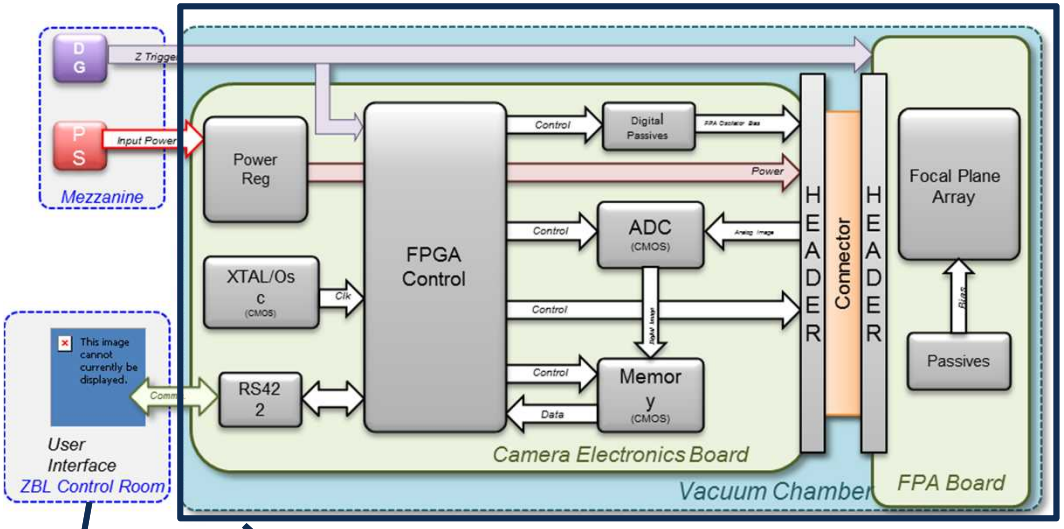
- A hybrid camera allows for independent design and optimization of the photodiodes and the ROIC
- Photodiodes can be optimized for sensitivity to relevant spectrum or particles of interest (visible light, x-rays, electrons, protons, or neutron)
- ROIC stores the charge from each photodiode on in-pixel capacitors during selected integration time for each frame
- Each pixel of photodiode array is directly connected to CMOS ROIC pixel input through wafer-to-wafer bonding electrical interconnect



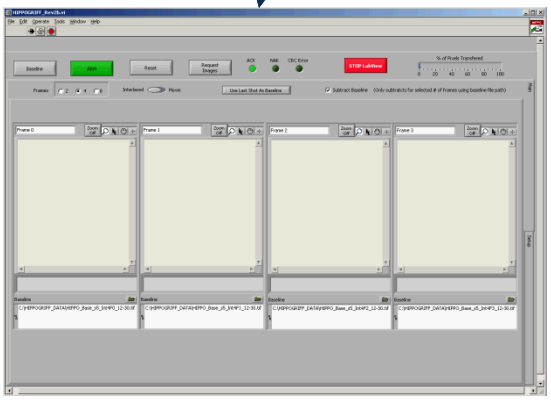
CMOS Hybrid Imager

What Makes up a Complete Camera?

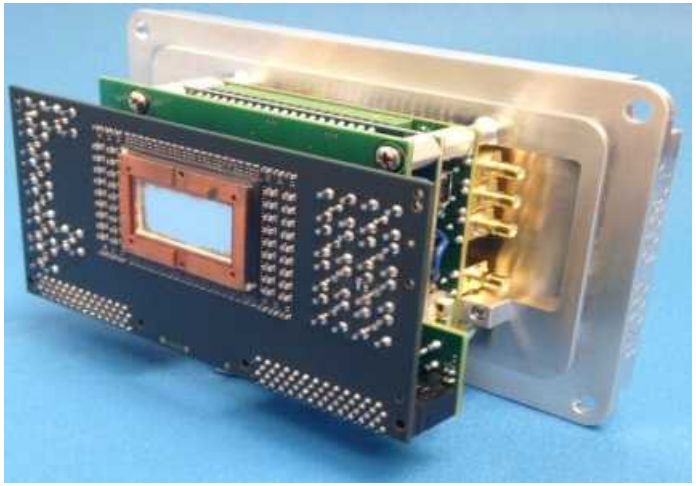
- ROIC
- Photodetector
- Hybridization
- Packaging
- System
- Software



Camera System Block Diagram



Camera System Software

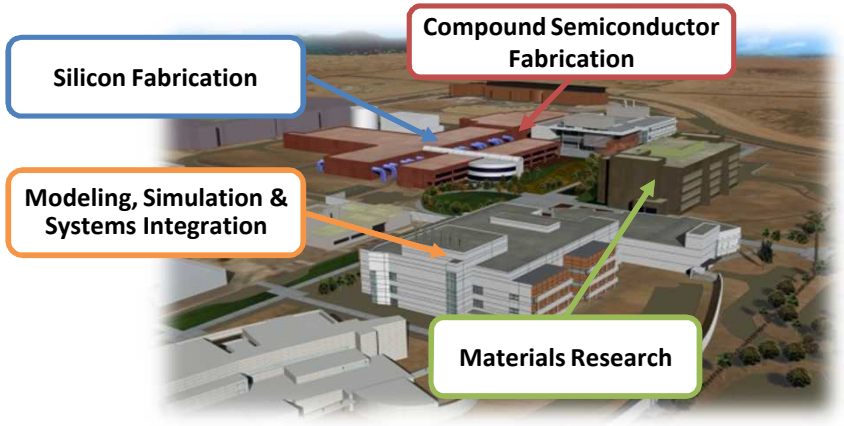


Camera System Hardware

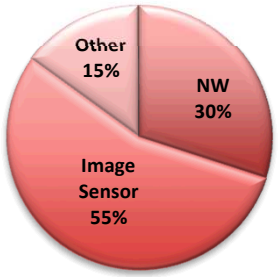
Mixed Signal ASIC/SoC

Sandia Imaging System R&D

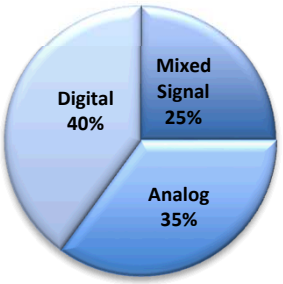
- MESA Complex
  - NNSA Investment
  - Microsystems Development/Integration
  - Radiation Hardened Microelectronics
  - Low Volume Applications
  - Production & R&D



- Core Competency In Image Sensor Design
  - Staff Expertise with Years of IC Design Experience
  - Industry Standard Full Mixed-Signal IC Design Flow



FY15 Work Breakdown



IC Design Expertise

- Imaging System Capabilities (Sandia 1600/1700 Partnership)
  - Read Out Integrated Circuit (ROIC) design and fabrication
  - Photodetector design and fabrication
  - Hybridization & 3D Development
  - Focal Plane Array (FPA) packaging
  - Camera system hardware/software design

UXI Imager Design Goals

Sandia National Laboratories

- High spatial resolution (25µm or better)
- High speed (1ns or better)
- Many frames (10 or more frames)
- High sensitivity to visible light and single keV X-rays (~100% fill-factor)
- Large dynamic range (1000:1 or better)
- Large format sensor (multi-cm scale)
- High timing precision (50 ps or better)
- Low trigger insertion delay (few 10's ns)
- Compact, rugged, and easy to integrate into diagnostic systems and experiments
- Radiation tolerant (can operate on High Energy Density Physics facilities)

Evolution of UXI Camera ROIC Designs

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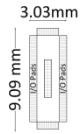
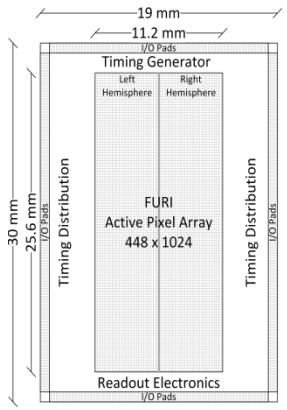
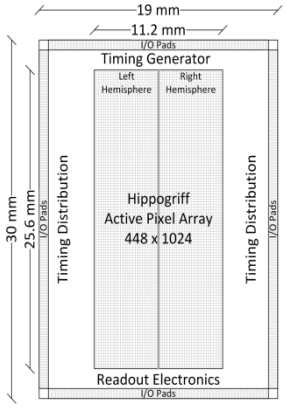
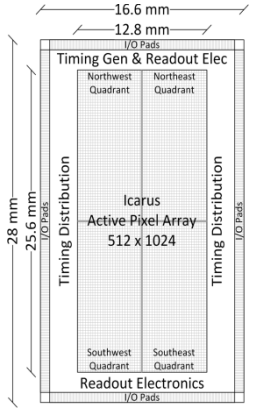
	Griffin	Furi	Hippogriff	Icarus	Acca
Year	FY13	FY14	FY15	FY16	FY17
Min. Gate Time	1.5 ns				1 ns
Pixels	15 x 128	448 x 1024		512 x 1024	512 x 512
Frames	4	2	2 4 or 8 Interlaced	4	8
Sensor Types	500-900 nm, 0.7-6 keV			400-900 nm, 0.3-9 keV 4 keV electrons	350-900 nm, 0.2-9 keV 2 keV electrons
Tiling Option	No				Yes
CMOS Process	350 nm				130 nm
Status	Completed		In Characterization	In Electrical Test	In Design

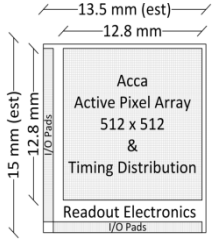


GRIFFIN
Active Pixel
Array
15 x 128





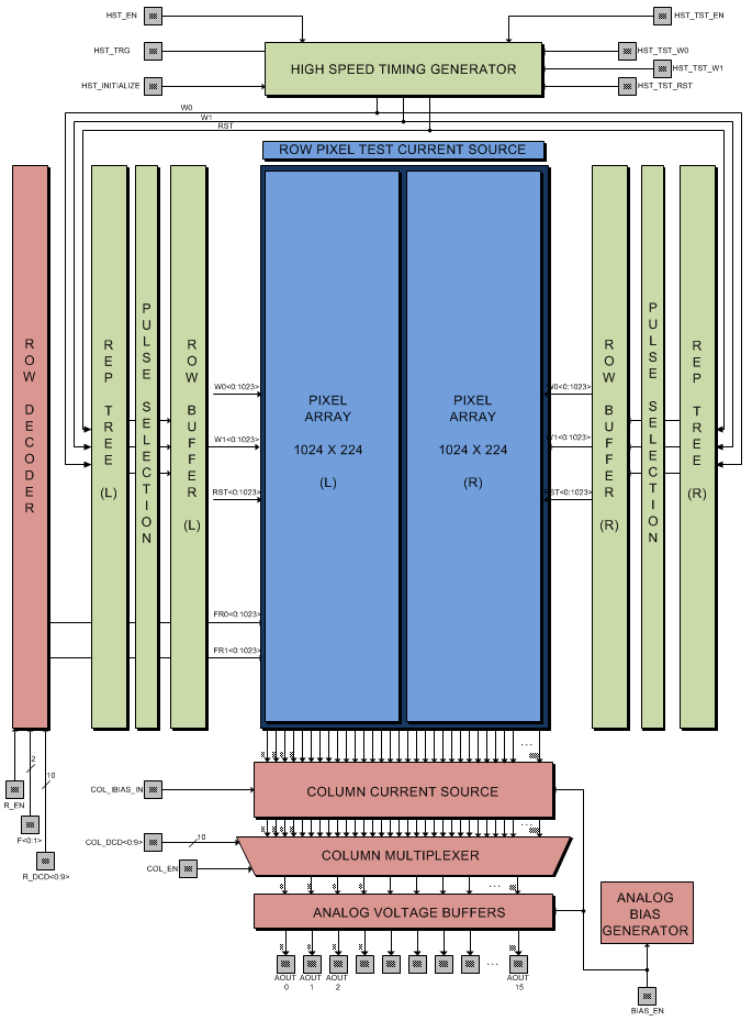




Mixed Signal ASIC/SoC

Hippogriff Architecture

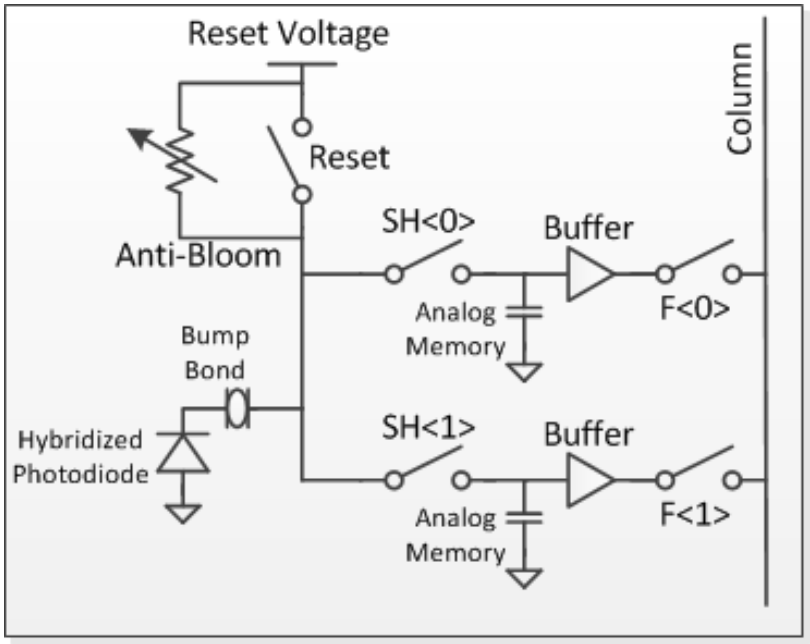
- Primary Design Blocks/Functions
  - High Speed Timing (Generation/Distribution)
    - Create and distribute the high speed pixel write and reset signals (electronic shutter)
    - Pulse selection block is where interlacing functionality is implemented
  - Pixel Array
    - Interfaces to the hybridized photo diode array, stores 2 frames of image data in-situ, and buffers the pixel data for column readout
  - Image Data Readout
    - These blocks provide random access read capability of the image data stored in each pixel frame



Block Diagram

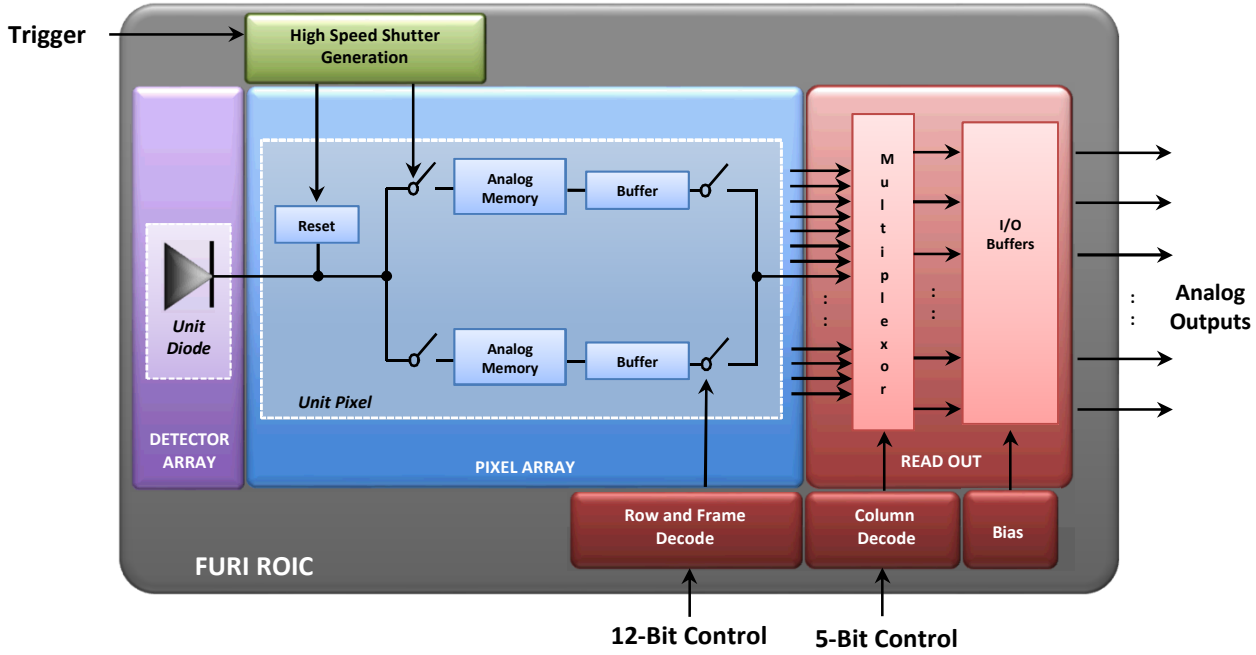
Hippogriff Pixel

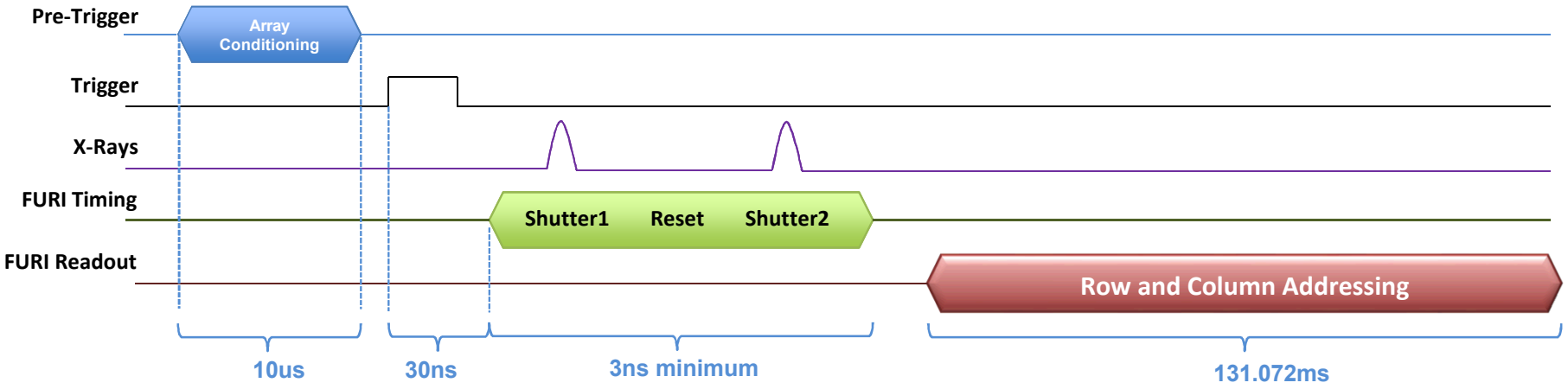
- Analog memory is a capacitor
  - Can be Metal-Insulator-Metal (MIM) or Metal-Oxide Semiconductor (MOS) depending on technology selected and design requirements
- Buffer is a Source-Follower single transistor amplifier with a gain of ~0.9
- SH<n> switches are the high speed electronic shutters
- Reset switch prepares the pixel for another high speed frame capture
- F<n> switches are slow speed readout multiplexers
- Anti-Bloom is a transistor configured to shunt current at high signal levels
  - This provides protection to the pixel transistors and protects previously stored frames of data



Pixel Block Diagram

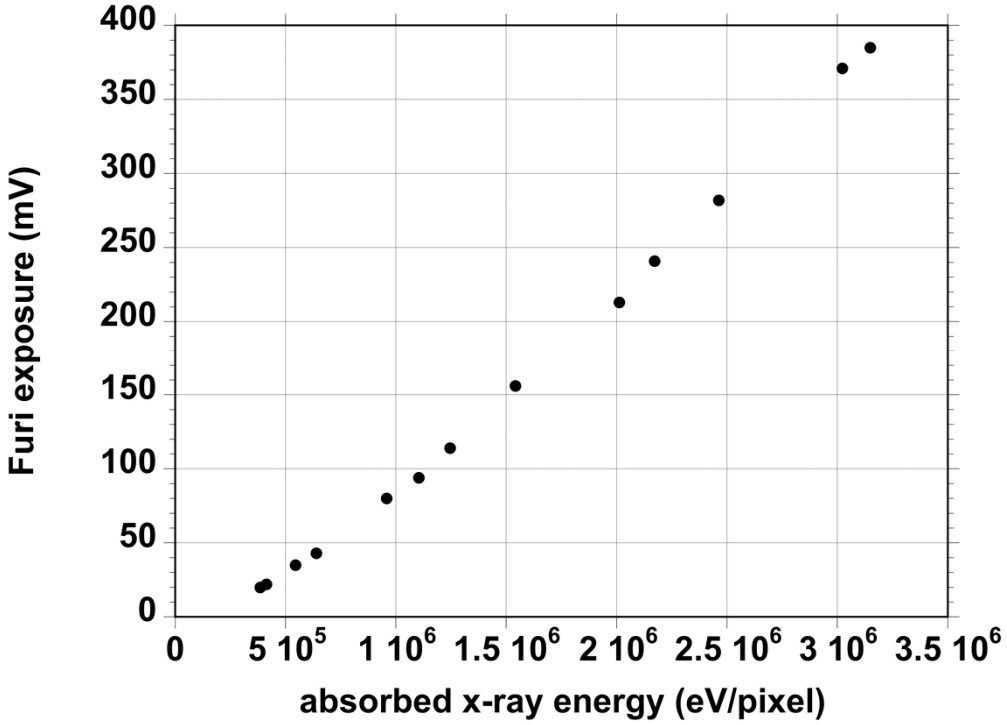
Hippogriff Functional Timing Example



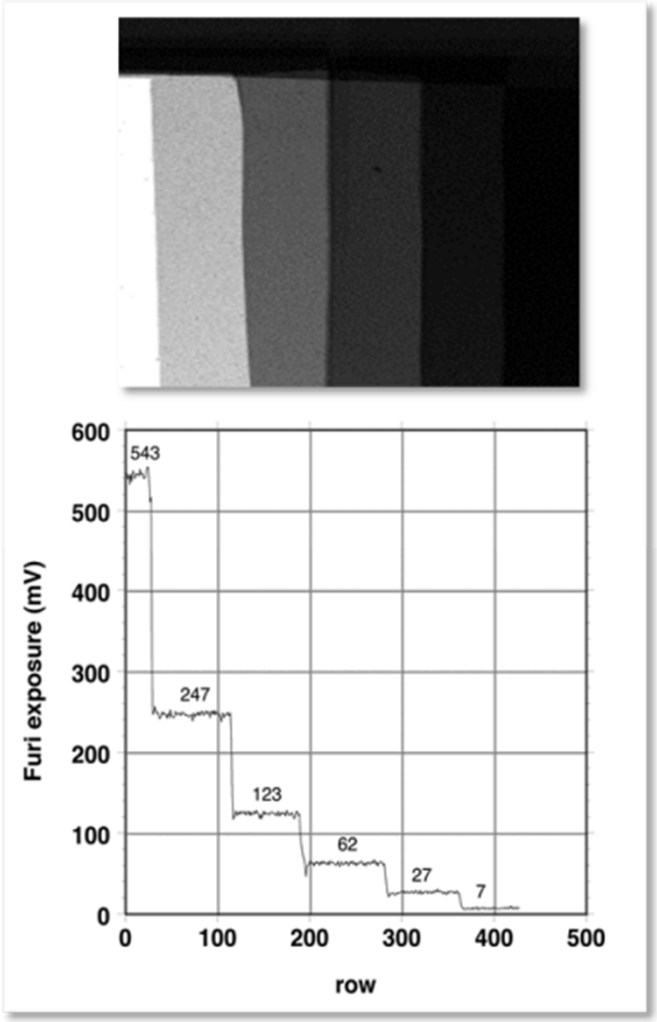


Program Accomplishments-X-ray

- X-ray data taken of static targets to date
  - Data taken with 4.7 keV X-rays
  - All static, non-moving images to date



Low Range X-Ray Linearity Sweep



X-Ray Intensity Step Wedge Test Pattern

Mixed Signal ASIC/SoC

Shutter Response Test

- X-ray pulse FWHM = 2.5ns, frame gate time = 4ns, 10ns frame separation
- X-ray pulse is convolved with 4ns gate time for comparison with measurements

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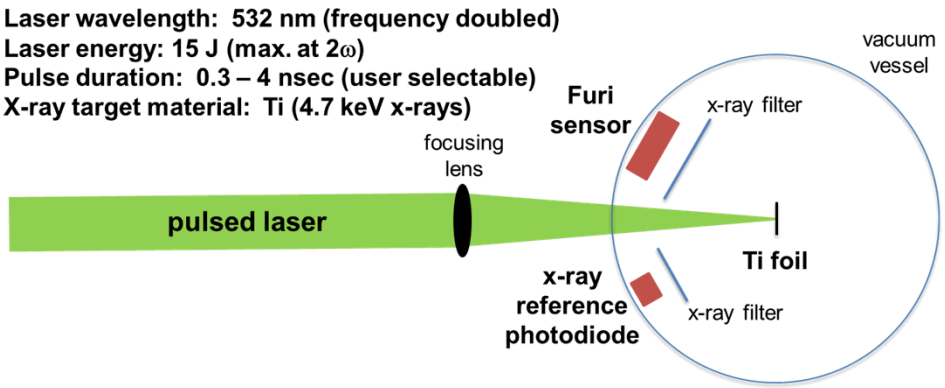
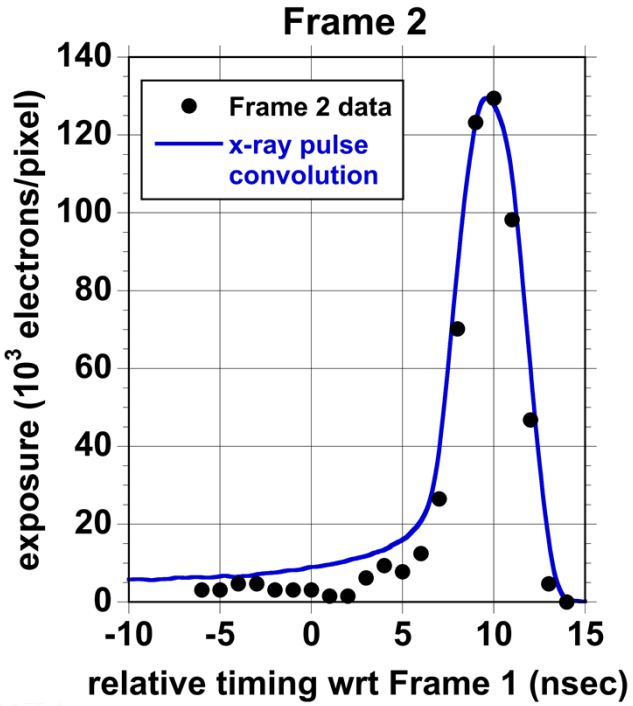
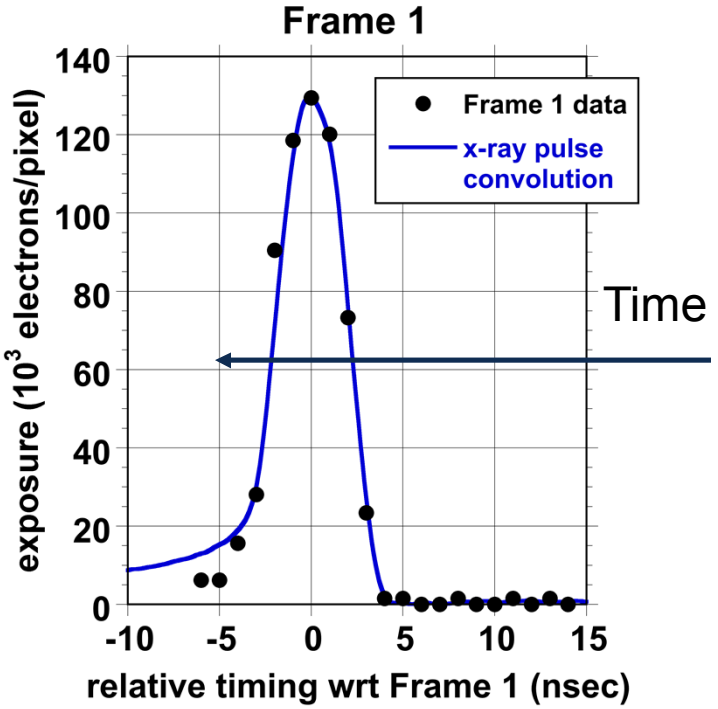
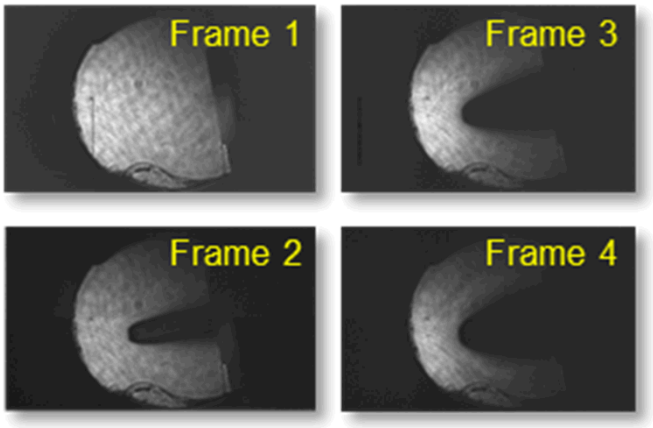


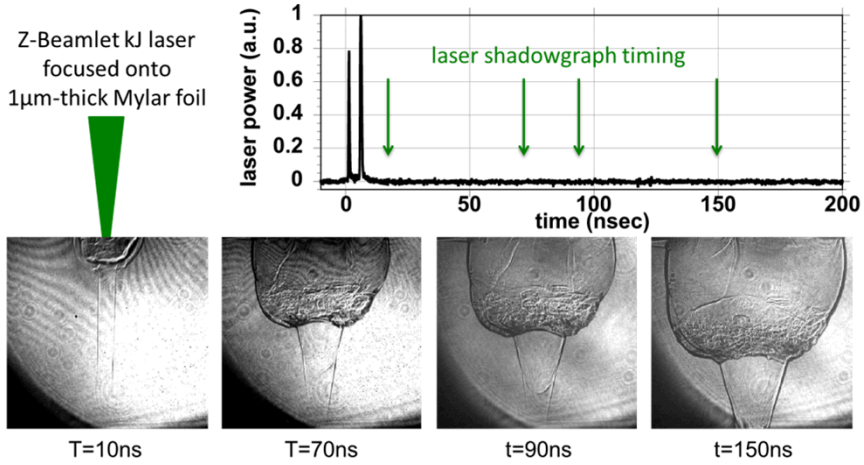




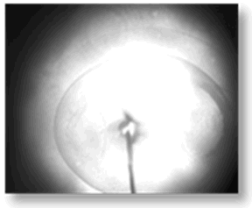
UXI Program Results-Continued



4ns "Gas Cell" Shadowgraphs



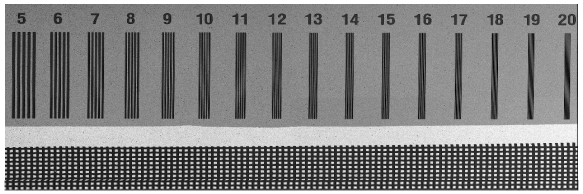
VS.

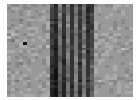


10ns "Blast Wave" Visible Images

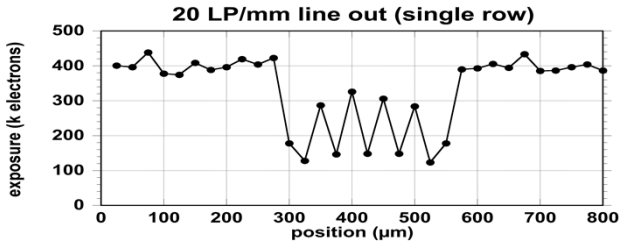
Commercial Double Exposed CCD

5 LP/mm
64 x 64
pixels





20 LP/mm
32 x 32
pixels

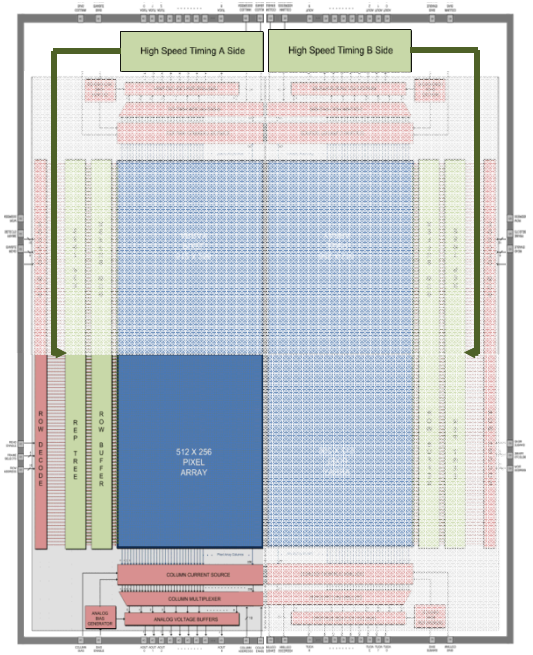


2ns Line Pair and Calibration Mesh X-Ray Test Patterns

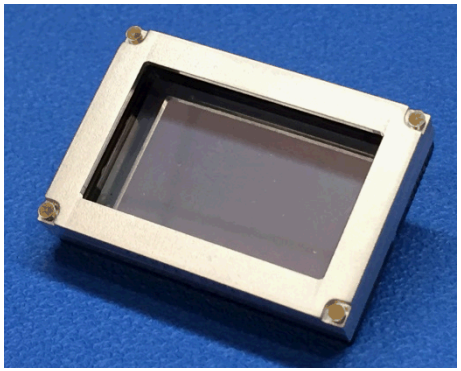
Mixed Signal
ASIC/SoC

UXI Program Near Term Future-ICARUS

- 4 frames
- Increased to 512 columns (1024x512 pixels)
- Incorporated as much learning as possible into this pixel
  - Improved well capacity
  - Improved readout linearity
  - Reduced shutter switch non-idealities
  - Improved anti-bloom protection/performance
- Added significant High Speed Timing (HST) generation, configurability, and tuning
- Implemented improvements in HST distribution
  - Can now tune out any hemispheric timing error in the array
  - Can “interlace” hemispherically
    - Left vs. right hemisphere timing is independently configurable
- Still using our validated IP as much as possible
- CMOS7 running into a transistor density/metal routing limitations
- Waiting on electrical testing as we speak



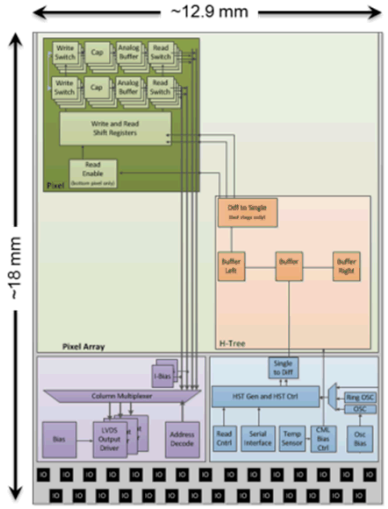
ICARUS Architecture



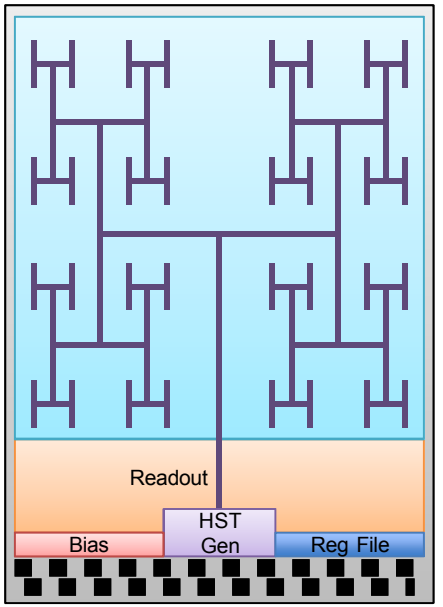
ICARUS Small Outline Package

UXI ROIC Ongoing Design Efforts-ACCA

- Porting to IBM130 nm technology to leverage improved transistor density
- 8 frames/pixel at 25 um pitch
- 512 x 512 pixel array
- 2 side abutable
- In-pixel digital timing generation enabled due to higher transistor density
  - Should yield improved pixel and timing performance
- Improved timing distribution methodology enabled by additional metal layers and Cu interconnect
- Improvements in process performance in some areas can bring a degradation in others
  - Poor leakage in IBM vs. CMOS7
  - Readout speed requirement is significantly more challenging to compensate for poor leakage
    - Results in far less dead time (~1.5ms vs. 130ms) than previous ROICs
    - Tradeoff is burning more power
    - Circuit complexity/design risk is significantly increased
- Taping out ~Q3 FY15



ACCA Block Diagram



ACCA Floorplan

Mixed Signal ASIC/SoC

UXI Program History-Summary

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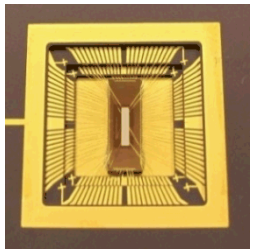
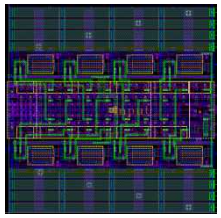


GRIFFIN FPA

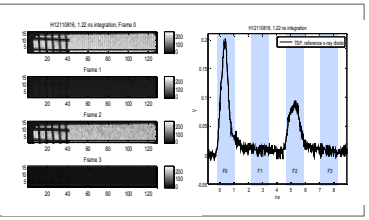
FURI FPA

HIPPOGRIFF FPA

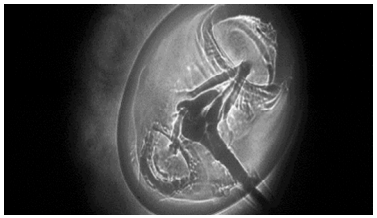
ICARUS FPA



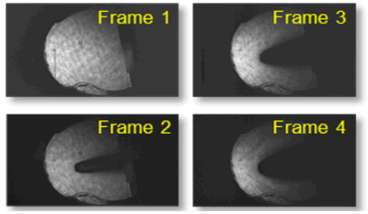
ACCA Layout



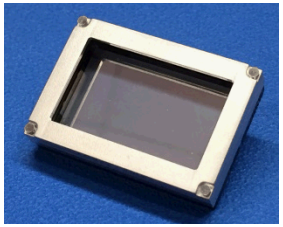
GRIFFIN Double 1ns X-Ray Pulse Exposure



FURI Visible Blast Wave Experiment



HIPPOGRIFF 4 frame visible image

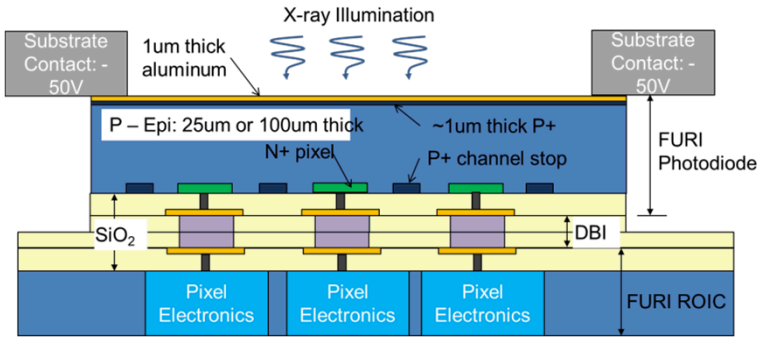


In Design

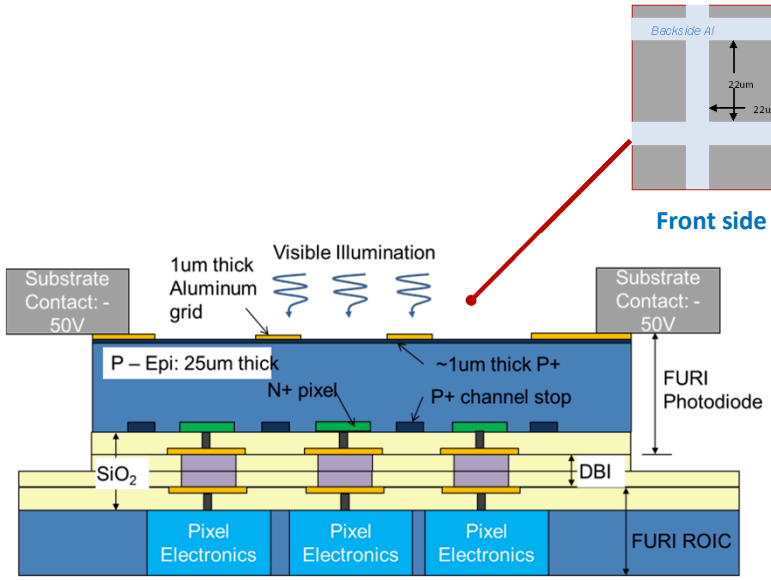
GRIFFIN	FURI	HIPPOGRIFF	ICARUS	ACCA
4 frames	2 frames	2-8 (interlace)	4	8
15x128 pixels	1024x448 pixels	1024x448	1024x512	512x512
1.5 million e- full well	1.5 million e- full well	1.5 million e- full well	500k e- full well	500k e- full well
Legacy	Currently Fielded	Currently Fielded	In Electrical Test	In Design

Photodiode Development

Required Spectral Responsivity	Technology	Comments	Status
6KeV X-ray	Common Anode 25um thickness silicon photodiodes	Baseline 25um thick silicon	Fielded for X-ray and visible photons
9KeV X-ray	Common Anode 100um thickness silicon photodiodes	Increase thickness to increase absorption	Fabricated and tested. Awaiting hybridization and fielding.
4 kev electron, 2 keV electron 0.3 keV – 6 keV X-Ray	Common Cathode 25um thickness silicon photodiodes	Surface properties are critical to electron and soft X-Ray response – thin passivation or delta doping	In fabrication. Awaiting test, hybridization, and fielding.
13KeV – 40KeV X-Ray	3D Silicon and High-Z photodiodes	Increase absorption	In conceptual design stage



X-Ray Photodiode

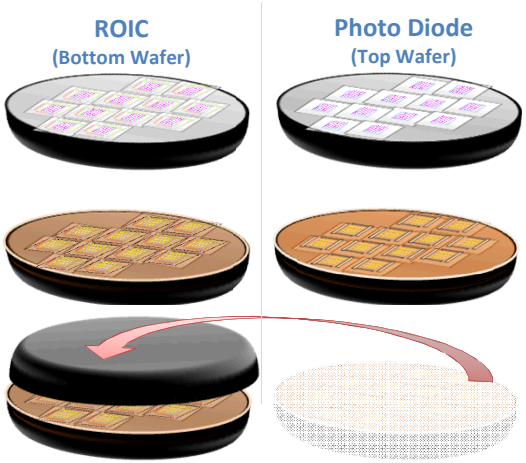


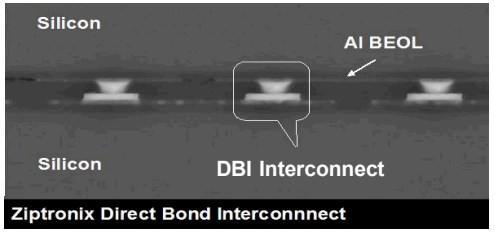
Visible Photodiode

Mixed Signal ASIC/SoC

Hybridization Technology

- Direct Bond Interface (DBI) Technology
  - Developed and commercialized by Ziptronix Corporation
  - Sandia began working with Ziptronix in 2007 to develop Silicon to Silicon hybridization capability with specific program requirements
  - UXI program developed a process specifically to hybridize silicon photodiode wafers to Readout Integrated Circuit (ROIC) wafers via wafer to wafer bonding
  - Sandia is currently working on licensing the process and standing it up in the MESA foundry in order to support future imagers





Packaging and Tiling Overview

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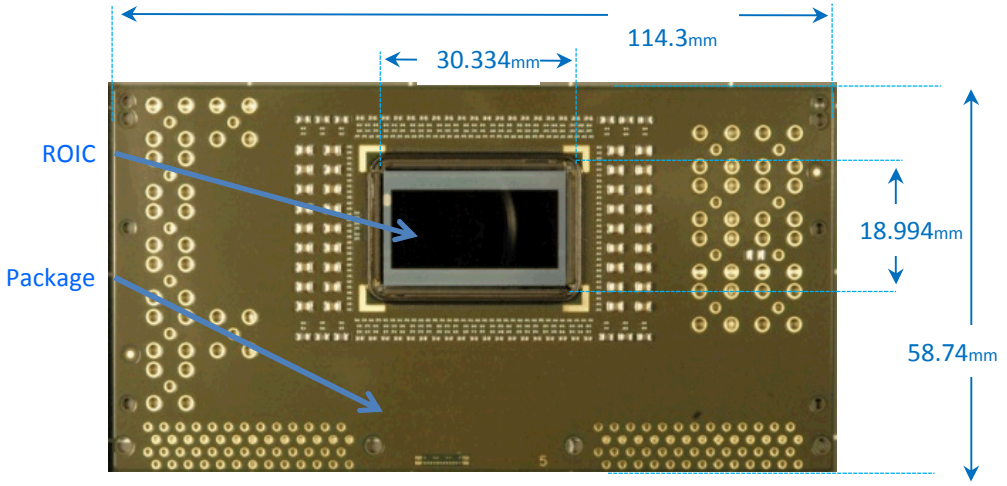
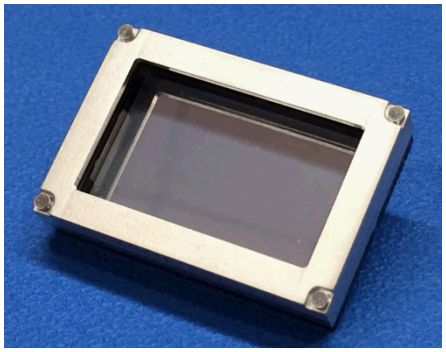
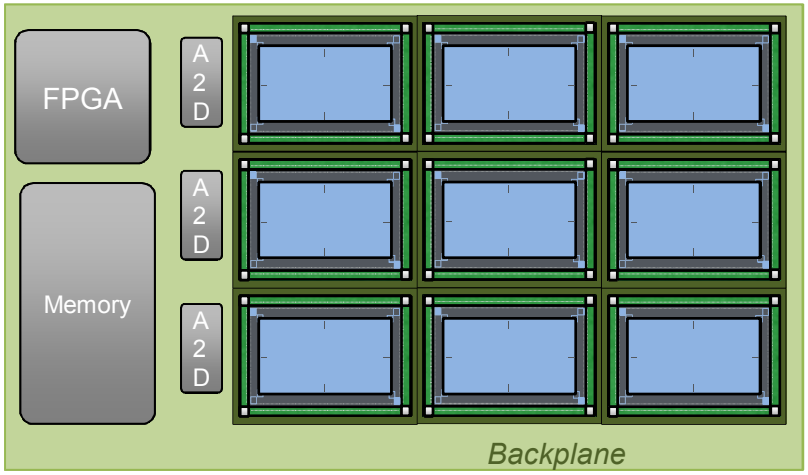


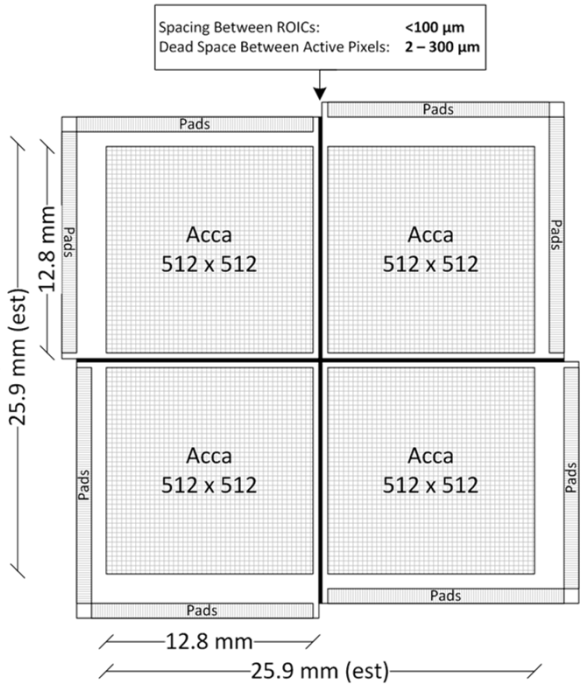
FURI Package-Fabricated



ICARUS SOP Package-Fabricated



ICARUS Tiling Concept
(~3mm between sensors)



2 side Abutable ACCA Tiling Concept

Mixed Signal ASIC/SoC

Tradespace

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- Things to contemplate when undertaking a custom multi-frame imager design
  - Technology Process
    - Process feature set
    - Transistor density
    - Cost
  - Total Detector Area
    - Tiling
    - 3-D integration
    - Stitching
  - Spatial Resolution
    - Transistor/capacitor density vs. pixel complexity
  - Number of Frames
    - Capacitive density vs. spatial resolution
  - Full Well Capacity/Noise Floor
    - Capacitive density
  - Readout Speed/Process Leakage
    - Burns power vs. loosing information
  - High Speed Timing Generation/Distribution
    - H-tree = dead pixels vs. Replication tree = timing skew
  - Simulation time vs. accuracy and confidence in the design
    - Might never tape out

Roadmap For Camera Development

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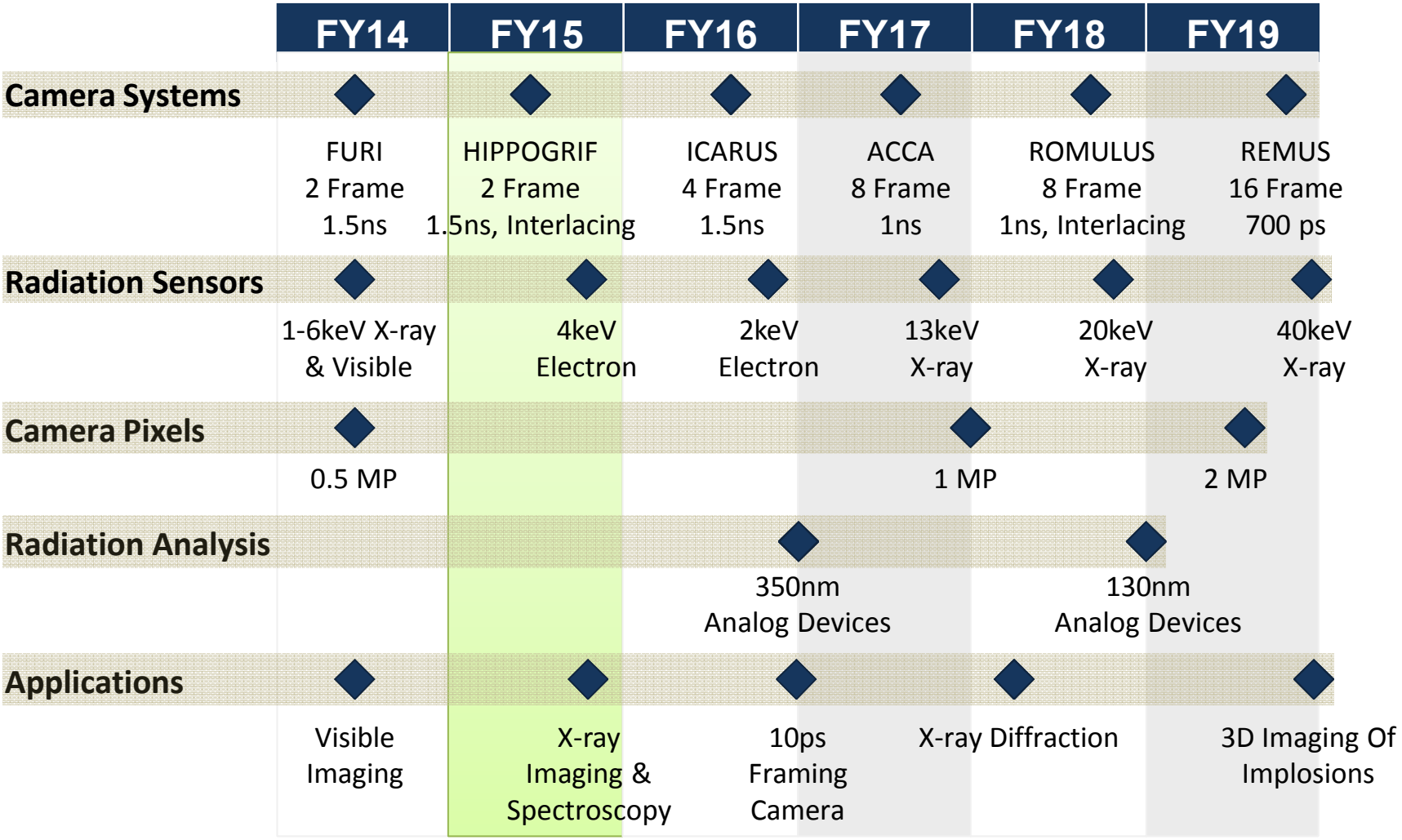

Mixed Signal
ASIC/SoC

UXI Team

- **ROIC Development** - Team Of 10 Staff Members
  - Design, fabrication, hybridization, and testing of existing/next generation ROICs and FPAs
- **Detector Development** - Team Of 7 Staff Members
  - Design, fabrication, hybridization, and testing of existing/next generation ROICs and FPAs
- **Packaging and System Integration** - Team Of 5 Staff Members
  - Design, fabrication, testing of custom ASIC packages
  - Integration of UXI FPAs into custom packages
  - Design, testing, and integration of custom camera hardware and software into 1600 facilities
- **Hybridization & 3D Development** - Team Of 8 Staff Members and 6 Technologists
  - Licensing and integration of the Ziptronix DBI process at Sandia
  - Development of a custom Through Silicon Via (TSV)process for FPA packaging

Conclusion

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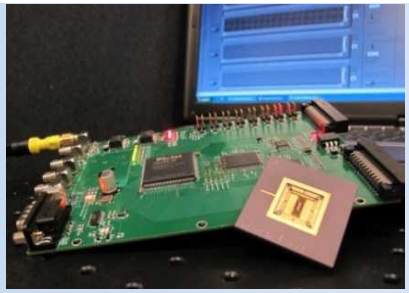
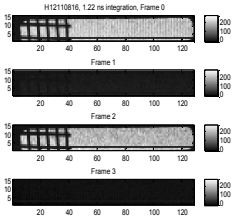
GRIFFIN
1.5ns, 4 Frames
15x128 pixels
350nm Sandia Process

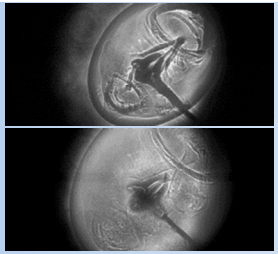




Calibration Mesh X-ray 1.5ns Images

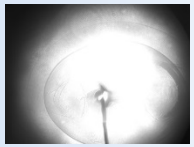
FY13

FURI
1.5ns, 2 Frames
448x1024 pixels
350nm Sandia Process



10ns "Blast Wave" Visible Images

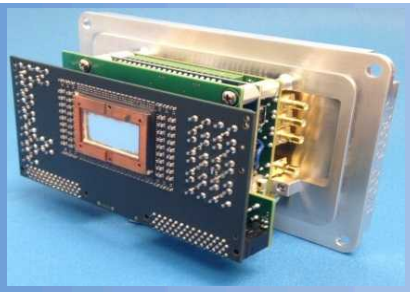
VS.

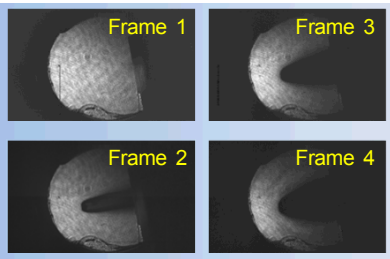


Commercial Double Exposed CCD

FY14

HIPPOGRIFF (FURI II)
1.5ns, 2-4 Frames (Interlacing)
448x1024 pixels
350nm Sandia Process



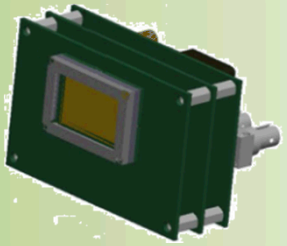


4ns "Gas Cell" Shadowgraphs

FY15

ICARUS
1.5ns, 4 Frames
512x1024 pixels
350nm Sandia Process

ACCA
1ns, 8 Frames
512x512 pixels
130nm IBM Process



FY16-17

Mixed Signal ASIC/SoC

Questions?

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