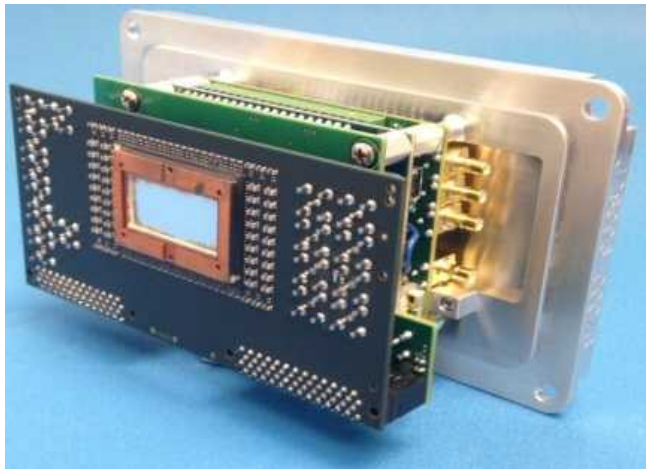
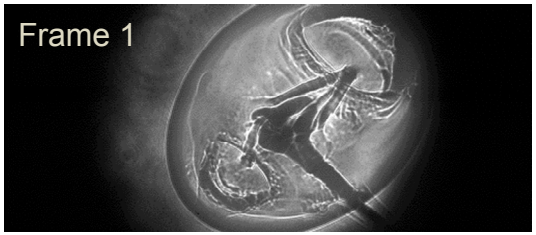
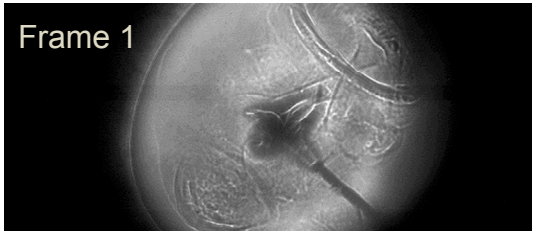
Exceptional service in the national interest

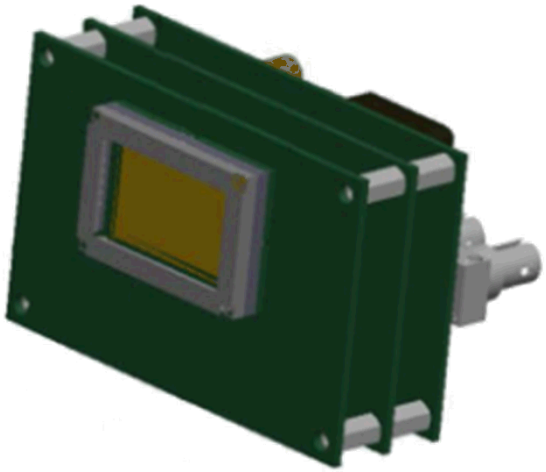
SAND2015-0030PE

Sandia National Laboratories









The Ultrafast X-Ray Imager (UXI) Program

January 14, 2015

Michael Holmes

Manager, Mixed Signal ASIC/SoC Products

Phone: 505-284-9673

Fax: 505-844-8480

Email: mlholme@sandia.gov

http://www.sandia.gov/mstc/

U.S. DEPARTMENT OF ENERGY | NNSA National Nuclear Security Administration

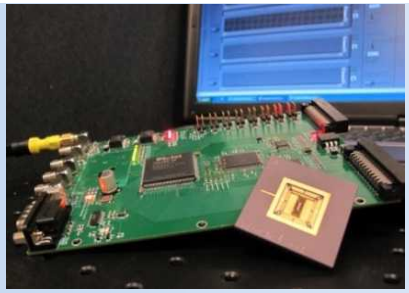
Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND No. ####-#####

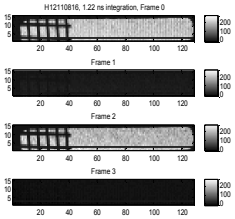
Camera System Development At Sandia

Sandia National Laboratories

GRIFFIN

1.5ns, 4 Frames
15x128 pixels
350nm Sandia Process



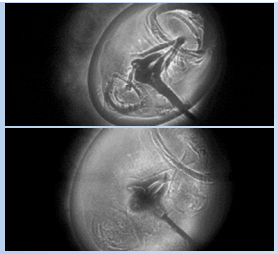


Calibration Mesh X-ray 1.5 Images

FY13

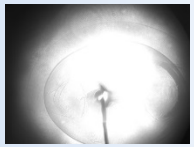
FURI

1.5ns, 2 Frames
448x1024 pixels
350nm Sandia Process



10ns "Blast Wave" Visible Images

VS.

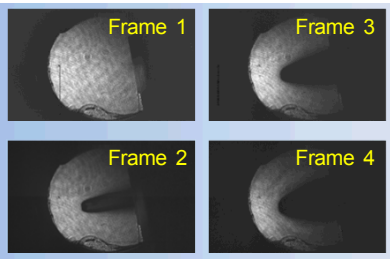


Commercial Double Exposed CCD

FY14

HIPPOGRIFF (FURI II)

1.5ns, 2-4 Frames (Interlacing)
448x1024 pixels
350nm Sandia Process



4ns "Gas Cell" Shadowgraphs

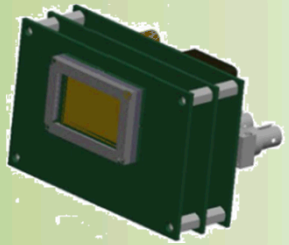
FY15

ICARUS

1.5ns, 4 Frames
512x1024 pixels
350nm Sandia Process

ACCA

1ns, 8 Frames
512x512 pixels
130nm IBM Process



FY16-17

Mixed Signal ASIC/SoC

Hybrid CMOS Camera System Motivation

Sandia National Laboratories

Currently On NIF, Z, OMEGA ➡ Image Plate & Film

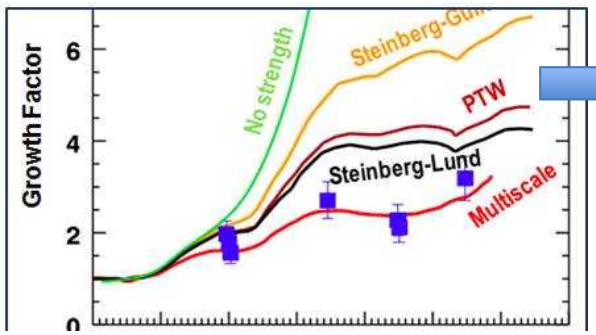


Image Plate Disadvantages

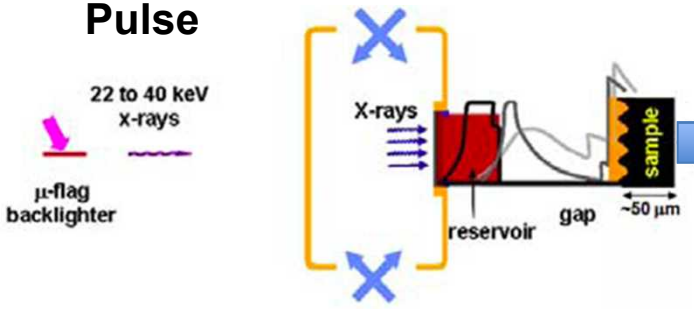
Five Shots Required To Do A Time Scan

- Uses IP: Measurement @Single Time
- Expensive To Process
- Requires Many Shots
- Issue of Non-Reproducibility

Image Plate Replacement

Future On All Facilities ➡ Hybrid CMOS (hCMOS) Imager

Picket Fence Pulse



hCMOS Imager
4-8
1ns Gates

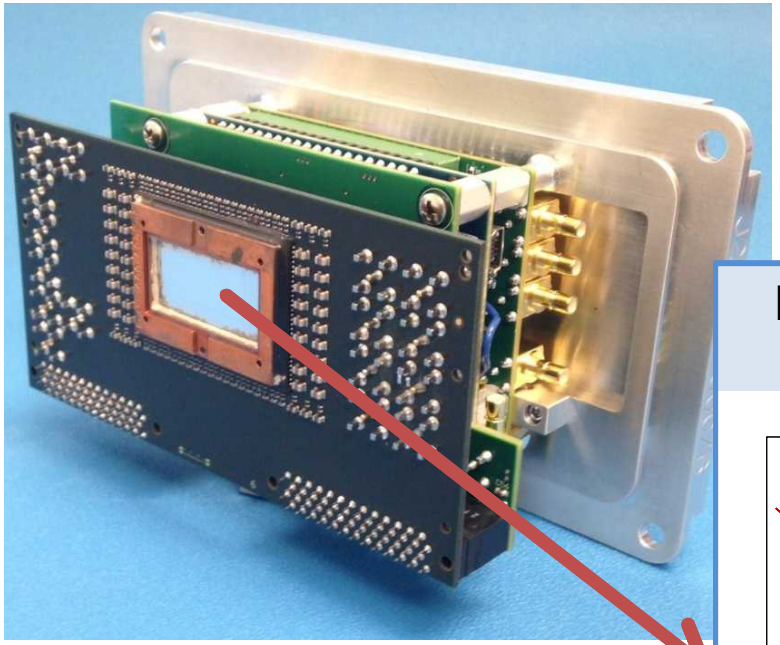
hCMOS Capabilities

- >256x256, Buttable
- 4-8, 1ns Frames
- Several Pixel Sizes/DILATION Tube
- 3D X-Ray Diode

A hCMOS Image Sensor Can (with caveats) Eliminate The Need For Four Shots Making Measurements At User Defined Times Within One Shot

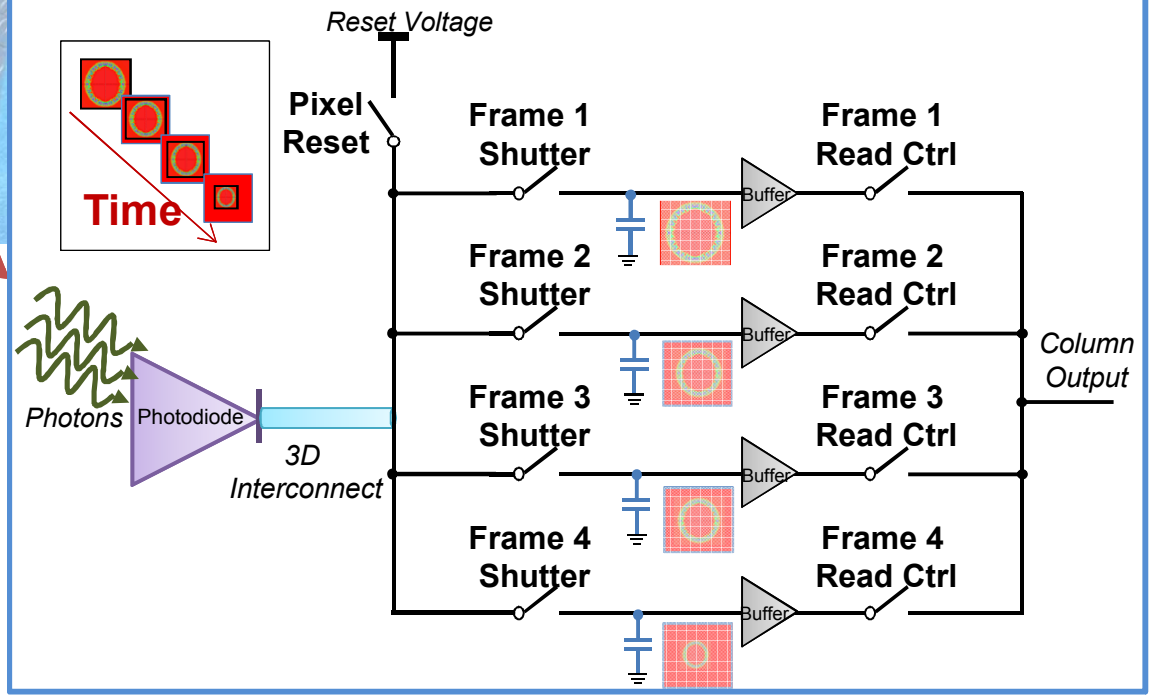
Applying The Wonders of Microlithography From MESA to Detectors For HED Science

Sandia National Laboratories



Four Images Per Pixel On One Shot!

Each Of The 458,752 (448 x 1024) Pixels Has This Four Sample, Hold & Read-Out Circuit



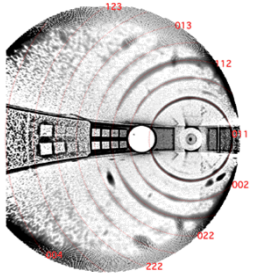
Mixed Signal ASIC/SoC

Fast-Gated Multi-Frame CMOS Sensors Will Transform Capability Across All HED Programs

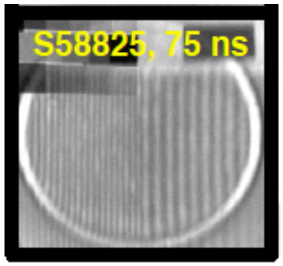
Sandia National Laboratories

High Pressure Materials

Diffraction

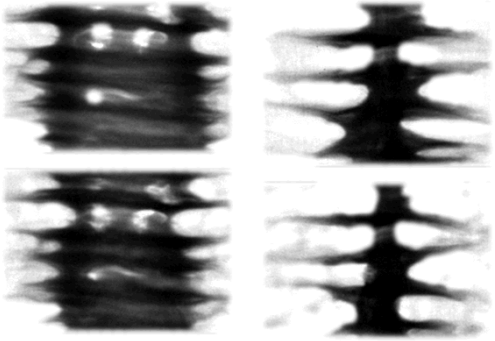


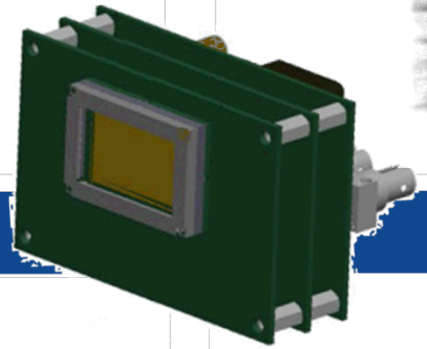
Strength



Complex Hydrodynamics

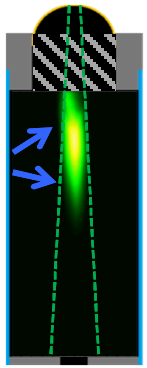
Radiography



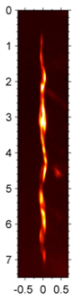


Ignition Applications

Laser Preheat



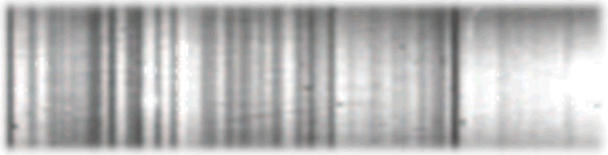
Stagnation



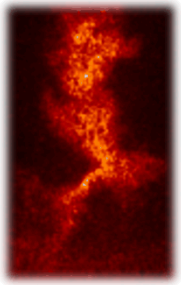
Spectroscopic Mix

Opacity, & Effects

Absolute Gated Spectra



High-Z K-α Imaging



Roadmap For Camera Development

Sandia National Laboratories

	FY14	FY15	FY16	FY17	FY18	FY19
Camera Systems	FURI 2 Frame 1.5ns	HIPPOGRIF 2 Frame 1.5ns, Interlacing	ICARUS 4 Frame 1.5ns	ACCA 8 Frame 1ns	ROMULUS 8 Frame 1ns, Interlacing	REMUS 16 Frame 700 ps
Radiation Sensors	1-6keV X-ray & Visible	4keV Electron	2keV Electron	13keV X-ray	20keV X-ray	40keV X-ray
Camera Pixels	0.5 MP			1 MP		2 MP
Radiation Analysis			350nm Analog Devices		130nm Analog Devices	
Applications	Visible Imaging	X-ray Imaging & Spectroscopy	10ps Framing Camera	X-ray Diffraction		3D Imaging Of Implosions

Mixed Signal ASIC/SoC

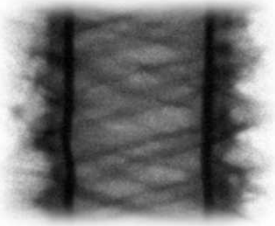
Multiple Sensors To Meet Diverse Mission Needs

Sandia National Laboratories

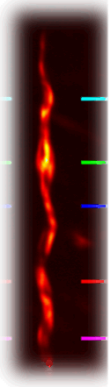
FY14	FY15	FY16	FY17	FY18	FY19

1-6keV X-ray & Visible | **4keV Electron** | **2keV Electron** | **13keV X-ray** | **20keV X-ray** | **40keV X-ray**

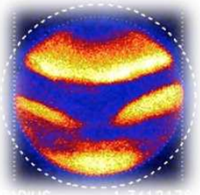
6 keV Radiography



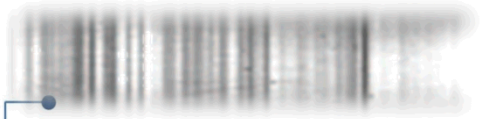
Stagnation Imaging



LEH Imaging

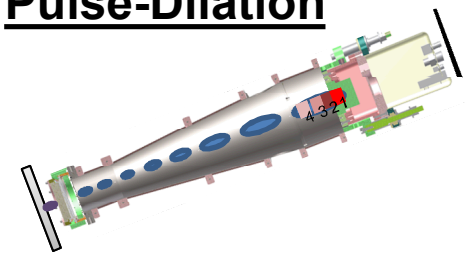


0.7-6 keV Spectroscopy

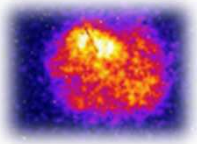


Mixed Signal ASIC/SoC

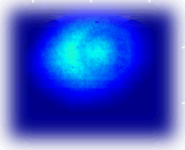
Pulse-Dilation



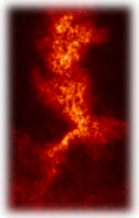
Hot-Spot Imaging



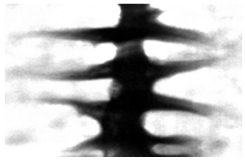
Capsule Radiography



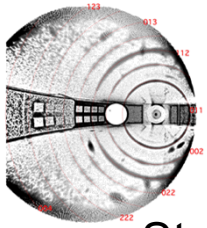
Kr He-α Imaging & Spectra



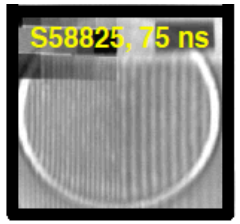
8-10 keV Radiography



Diffraction



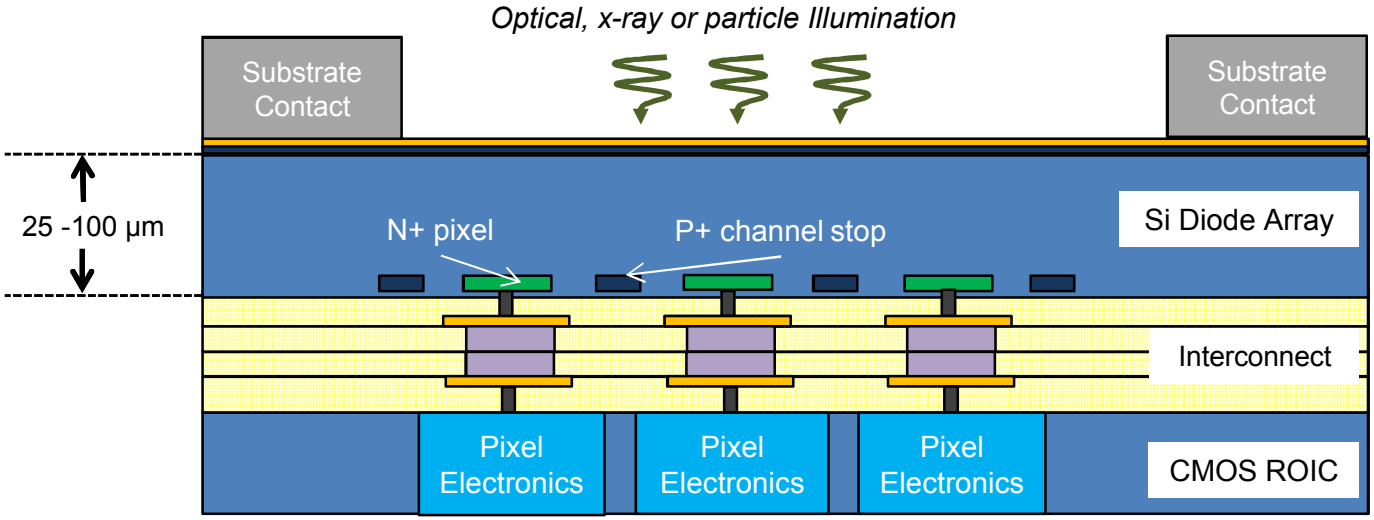
Strength



High-Z K-α Imaging/Spectra

CMOS Hybrid Image Sensor

- Photodiodes can be optimized for sensitivity to relevant spectrum or particles of interest (visible light, x-rays, electrons, protons, or neutron).
- ROIC stores charge from each photodiode on in-pixel capacitors during selected integration time for each frame.
- Each pixel of photodiode array is directly connected to CMOS ROIC through wafer-to-wafer bonding (Ziptronix 3D oxide-to-oxide bond process).



CMOS Hybrid Imager

A Hybrid Detector Enables Independent Optimization of The Photodiode Array & The Electronics

Mixed Signal ASIC/SoC

Sandia National Laboratories

UXI IMAGE SYSTEMS

- Goals
- Project Roadmap
- ROIC Overview
- Detector
- 3D Integration
- Accomplishments

UXI Imager Design Goals

Sandia National Laboratories

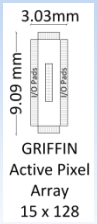
- High spatial resolution (25µm or better)
- High speed (1ns or better)
- Many frames (10 or more frames)
- High sensitivity to visible light, x-rays, or particles (100% fill factor and sensitive to single keV x-ray photons)
- Large dynamic range (1000 or better)
- Large format sensor (multi-cm scale size)
- High timing precision (50 ps or better)
- Low trigger insertion delay (few 10's ns)
- Compact, rugged, and easy to integrate into diagnostic systems and experiments
- Radiation tolerant (can operate on large Inertial Confinement Fusion facilities)

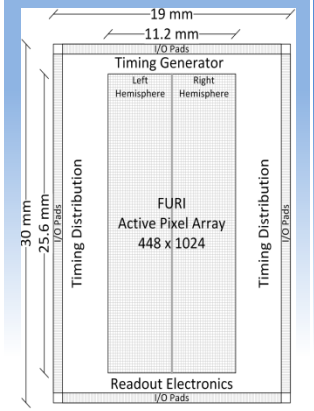
Mixed Signal ASIC/SoC

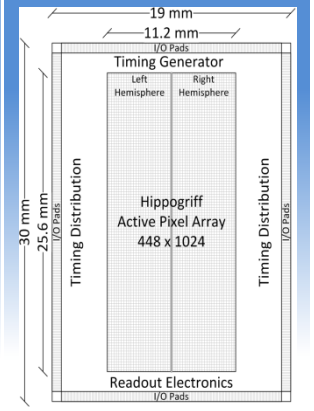
Evolution of UXI Camera Designs

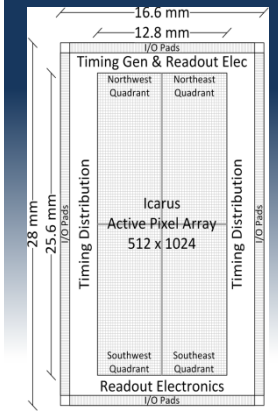
Sandia National Laboratories

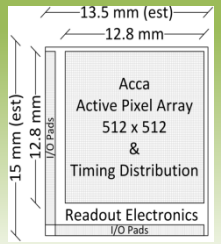
	Griffin	Furi	Hippogriff	Icarus	Acca
Year	FY13	FY14	FY15	FY16	FY17
Min. Gate Time					
Pixels					
Frames					
Sensor Types					
Tiling Option					
CMOS Process					
Status					







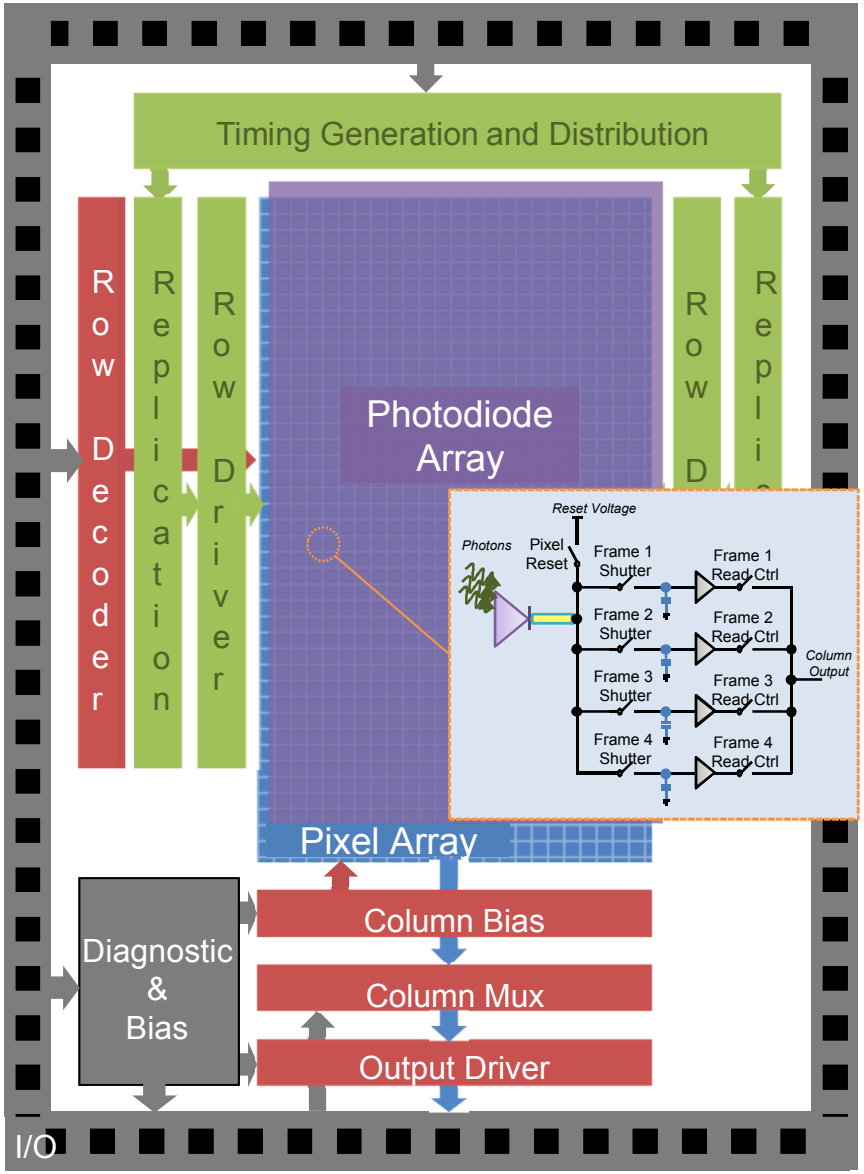




Mixed Signal ASIC/SoC

UXI ROIC Architecture

- **Pixel Array**
  - 2-4 Frame In Pixel Storage
  - Global Shutter
- **Timing**
  - High Speed Shutter & Pixel Control
  - Adjustable Shutter Timing 1-19ns
  - Adjustable Delay Between Shutters
- **Readout**
  - Random Access to pixels
  - Multiple Parallel Channels Of Image Data
- **Photodiode**
  - 0.7-6keV X-RAYS & 500-900nm Visible Light
- **I/O and Support**
  - Timing Signal Diagnostics



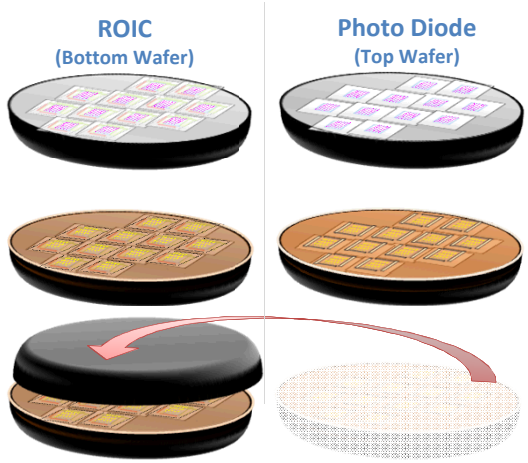
Mixed Signal ASIC/SoC

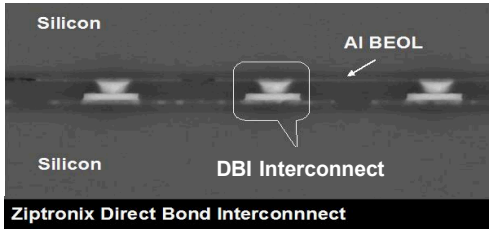
Hybridization Technology

	FY14	FY15	FY16	FY17	FY18	FY19
Camera Systems	◆	◆	◆	◆	◆	◆
	FURI 2 Frame 1.5ns	HIPPOGRIF 2 Frame 1.5ns, Interlacing	ICARUS 4 Frame 1.5ns	ACCA 8 Frame 1ns	ROMULUS 8 Frame 1ns, Interlacing	REMUS 16 Frame 700 ps

In House Bonding

- Direct Bond Interface (DBI) Technology
  - Developed and commercialized by Ziptronix Corporation.
  - Sandia began working with Ziptronix in 2007 to develop Silicon to Silicon hybridization capability with specific program requirements.
  - UXI program developed a process specifically to hybridize silicon photodiode wafers to Readout Integrated Circuit (ROIC) wafers (wafer to wafer bonding).
  - Sandia is currently working on licensing the process and standing it up in the MESA foundry in order to support future imagers.





Sandia Is Licensing The DBI Process To Increase Efficiency, Reduce Costs, & Buy Down Risk.

Sandia National Laboratories

UXI PROGRAM

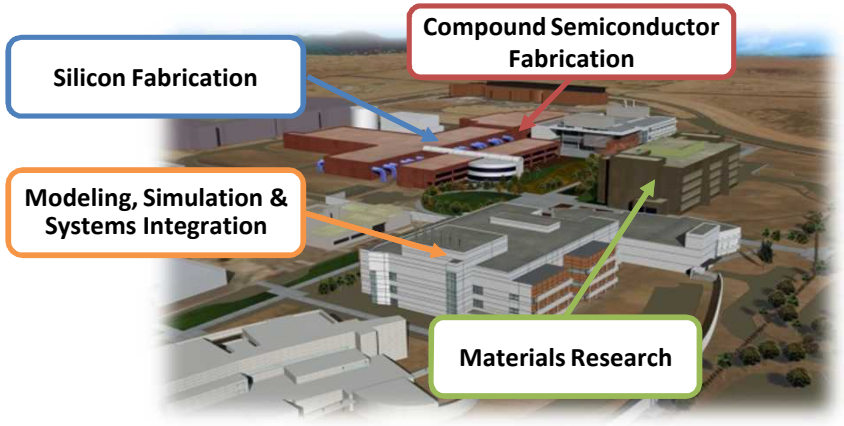
- Sandia Imaging System R&D
- Project Plan and Efforts
- Budget
- Risks and Challenges
- Summary

Mixed Signal ASIC/SoC

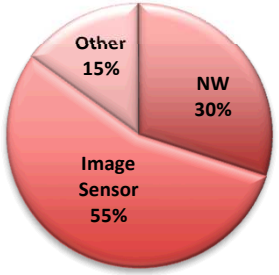
Sandia Imaging System R&D

Sandia National Laboratories

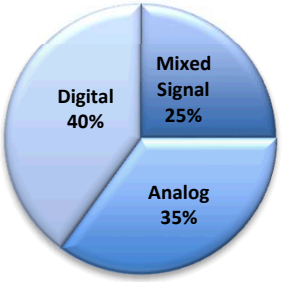
- MESA Complex
  - NNSA Investment
  - Microsystems Development/Integration
  - Radiation Hardened Microelectronics
  - Low Volume Applications
  - Production & R&D



- Core Competency In Image Sensor Design
  - Staff Expertise with Years of IC Design Experience
  - Industry Standard Full Mixed-Signal IC Design Flow



FY15 Work Breakdown



IC Design Expertise

- Imaging System Capabilities (Sandia 1600/1700 Partnership)
  - Read Out Integrated Circuit (ROIC) design and fabrication
  - Photodetector design and fabrication
  - Hybridization & 3D Development
  - Focal Plane Array (FPA) packaging
  - Camera system hardware/software design

Camera System Development Timeline

Sandia National Laboratories

Design (6-9 months)	*3-4 months*	Mixed Signal Design	• Circuitry is captured in a schematic and verified • The captured schematic is then translated into technology layers (layout) • Resistances and capacitances are extracted from the layout and incorporated into the schematic verification
	2-3 months	Physical Design	
	1-2 months	Parasitic Verification	
Fabrication (8-12 months)	*3-4 months*	Process Fabrication	• The design is fabricated in the selected technology • Die are then tested on fabricated wafers • ROIC wafers are bonded to detector wafers • Bonded wafers are tested again to identify damaged die due to hybridization • FPA die are singulated and packaged • FPA packages are assembled into camera system electronics
	1-3 months	Wafer Testing	
	2-3 months	Hybridization	
	1 month	Wafer Testing	
	1 month	Packaging	
Testing (2-3 months)	*1-1.5 months*	Bench Testing	• Packaged FPA are tested on a bench set-up and timing and DC array readout tests are performed • Packaged FPAs are incorporated into Z test chambers for at-speed and end use testing
	1-1.5 months	System Testing	

Mixed Signal ASIC/SoC

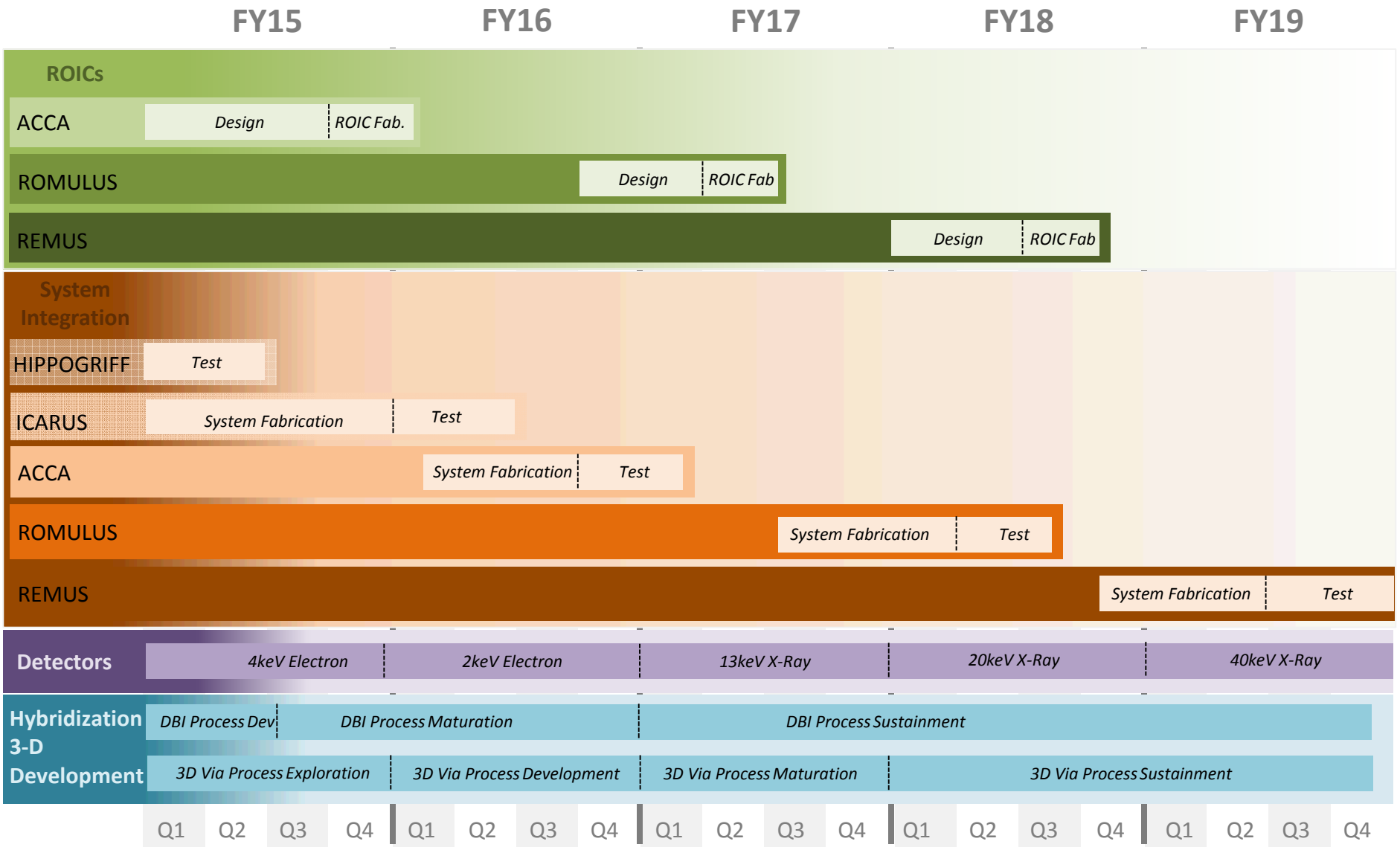
Program Efforts

Sandia National Laboratories

- **ROIC Development** - Team Of 10 Staff Members
  - Design, fabrication, hybridization, and testing of existing/next generation ROICs and FPAs
- **Detector Development** - Team Of 7 Staff Members
  - Design, fabrication, hybridization, and testing of existing/next generation ROICs and FPAs
- **Packaging and System Integration** - Team Of 5 Staff Members
  - Design, fabrication, testing of custom ASIC packages
  - Integration of UXI FPAs into custom packages
  - Design, testing, and integration of custom camera hardware and software into 1600 facilities
- **Hybridization & 3D Development** - Team Of 8 Staff Members and 6 Technologists
  - Licensing and integration of the Ziptronix DBI process at Sandia
  - Development of a custom Through Silicon Via (TSV)process for FPA packaging

Projected Five Year Plan

Sandia National Laboratories



Budget Projections

Sandia National Laboratories

Fiscal Year	Projected Funding Needs	Primary Efforts	Notes
FY15	$4,390K	• IBM Fabrication, ICARUS wafer testing • 4keV diode development • ICARUS system dev, ACCA package dev. • Hybridization licensing and process dev.	Current Budget: $2,100K **$2,290K Shortfall**
FY16	$4,470K	• 2 MPW Fabrication, ACCA wafer testing • 2keV diode development • ICARUS system char., ACCA system dev. • Hybridization maturation, 3D via dev.	
FY17	$4,720K	• IBM Fabrication, ACCA II wafer testing • 2keV diode development • ACCA system char., ACCA II package dev. • Hybridization maintenance, 3D via maturation	
FY18	$4,625K	• IBM Fabrication, ICARUS wafer testing • 20keV diode development • ACCA II system char, 16 frame package dev. • Hybridization maintenance, 3D via maintenance	
FY19	$4,025K	• IBM Fabrication, ICARUS wafer testing • 40keV diode development • ICARUS system dev, ACCA package dev. • Hybridization licensing and process dev.	

Mixed Signal ASIC/SoC

Program Risks and Challenges

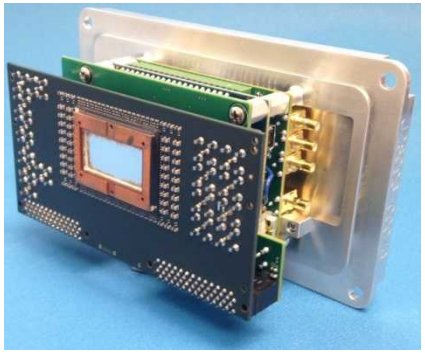
Sandia National Laboratories

- **ROIC Development**
  - Uncharacterized radiation response IBM 130nm bulk silicon design
    - Mitigation: Testing other product circuits and test circuits in the target environment
  - Power consumption causing heating of die
    - Mitigation: Lower duty cycle operation
  - Status of IBM foundry (recently acquired by Global Foundries)
- **Detector Development**
  - Using III-V material or novel silicon architectures/processes to create bondable high energy photodetector arrays
- **Packaging and System Integration**
  - Developing a comprehensive model that accurately represents all the pieces of the system
    - Mitigation: Piece-wise modeling of system components
  - Using the camera system in configurations outside of it's nominal use conditions
    - Mitigation: Communication and collaboration with users
- **Hybridization and 3D Development**
  - The availability of a cost effective and reliable wafer to wafer bonding technology
    - Mitigation: Bringing DBI bonding into Sandia foundry
  - Bonding Sandia 6" detector wafer to IBM 8" ROIC wafer
    - Mitigation: Indium bonding

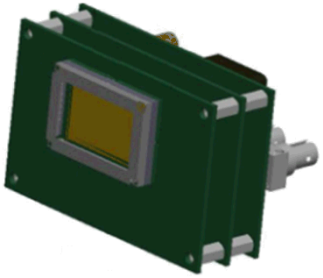
Conclusions

Sandia National Laboratories

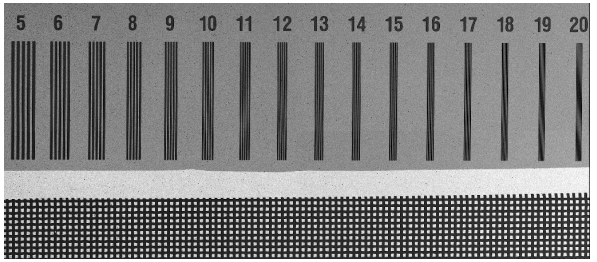
- The UXI program has immediate and near term camera systems that offer transformational imaging capability for HED experiments
  - FURI …… 2-frame, 448x1024 camera
  - HIPPOGRIFF …… 2, 4, 8 frame, 448x1024 camera
  - ICARUS …… 4 frame, 512x1024, Fabrication In Progress



- A path exists for the development of 8 and 16 frame cameras
  - Design done in IBM 130nm technology
  - In-house hybridization is being developed
  - In-house custom FPA packaging and system development
  - At speed testing in Z-facility test chambers



- ROICs are being developed as sensor agnostic
  - Parallel development of 2-4keV electron and 13-40keV X-ray pixelated detectors



Mixed Signal ASIC/SoC