Microsystems
Science, Technology & Components

SAND2014-19384PE

Characterization of Switching Filament Formation in TaOx Memristive Memory Films

Electronic Materials Conference

Santa Barbara, CA

June 26, 2014

Matthew Marinella, Stephen Howell, Seth Decker, David Hughart, Andrew Lohn, Patrick Mickel, Roger Apodaca, Ed Bielejec, Mike Brumbach, Thomas Beechem, Steve Wolfley, Jim Stevens, and Geoff Brennecka

Sandia National Laboratories

*matthew.marinella@sandia.gov

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Sandia National Laboratories

Emerging Memory

	Embedded NVM Replacement[1]	NAND Flash Replacement (e.g. SSD)[2]	S-Type Storage Class Memory[3]	M-Type Storage Class Memory[3]	Stand-Alone DRAM (DIMM) Replacement[4]	CMOS Integrated DRAM/Storage/Main Memory[5]
Time to Implementation	**Now**	**5 years**	**5 years**	**5-10 years**	**5-10 years**	**> 10 years**
Quantitative Requirements						
Min Bit Level Endurance	10^{3}-10^{6}	10^{3}	10^{6}	10^{9}	10^{16}	10^{16}
Min Bit Level Retention	10 y	6-12 months	10 y	5 days	64 ms	10 y
Max System Level Read/Write Latency	100 µs	100 µs	5 µs	200 ns	100 ns	10 ns
Max System Level Write Energy	10^{4} pJ	100 pJ	25 pJ	100 pJ	100 pJ	1 pJ
Max Feature Size	180 nm	12 nm	20 nm	20 nm	20 nm	10 nm
Min 2D Layer Density	10^{9} bit/cm	10^{11} bit/cm	10^{10} bit/cm	10^{10} bit/cm	10^{9} bit/cm	10^{11} bit/cm
Max Cost	30 $/GB[6]	2 $/GB	4 $/GB	10 $/GB	10 $/GB	10 $/GB
Qualatative Requirements						
Performance	Low	Low	Moderate	High	High	High
Reliability	High	Low/Moderate	Moderate	Moderate	Moderate	High
CMOS Compatibility	Required	Useful/Not Req	Useful/Not Req	Useful/Not Req	Useful/Not Req	Required
BEOL Process	Required	Not Required	Not Required	Not Required	Not Required	Required
Layering Capability	Not Required	Required	Required	Useful/Not Req	Required	Required

1: Based on common embedded microcontrollers with flash based program/data memory

2: Based on modern NAND flash characteristics, considering a stand-alone module.

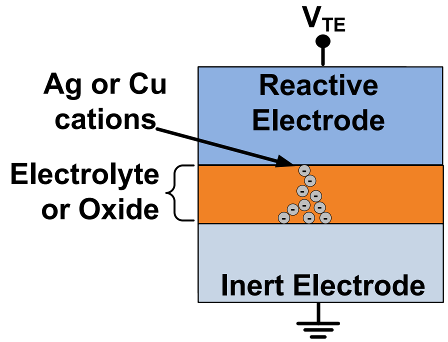
3: Based on SCM info from 2013 ITRS ERD Tables

4: Based on modern DRAM characteristics.

5: High performance logic CMOS integration based on estimated requirements for data-center level processor (e.g. a "nanostore" [6]). This could also be thought of as a "univeral memory" which does not require tradeoffs in performance or reliability.

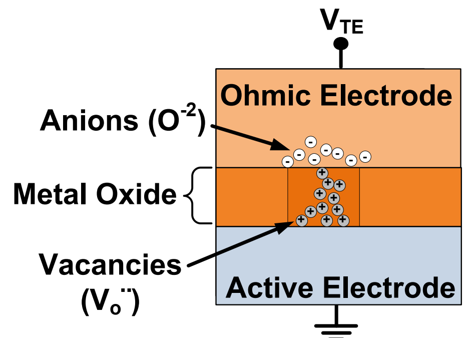
6: Based on the cost of a standalone external microcontroller memory; information on the cost per bit of flash integrated in a microcontroller is not available.

Electrochemical Metallization Bridge



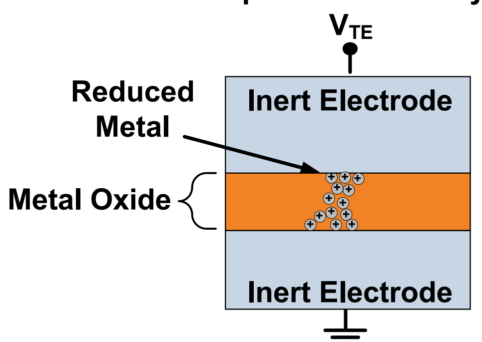
- Switching: Electrochemical formation and dissolution of Ag or Cu filament
- Cation motion (Ag or Cu)
- Chalcogenide or oxide insulating layer
- Switching depends on E-field direction
- R/W current independent of device area

Metal Oxide: Bipolar Filamentary



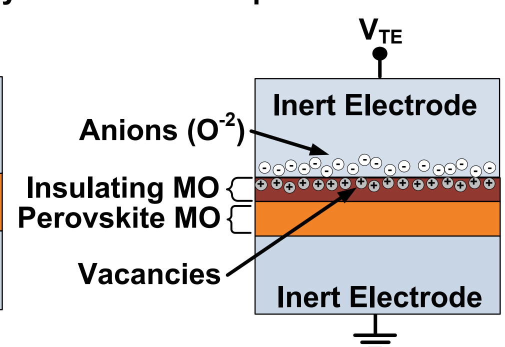
- Switching: Valence change and migration of oxygen vacancies
- Anion motion (O^{2-})
- HfO_x, TaO_x most common insulators
- Switching depends on E-field direction
- R/W current independent of device area

Metal Oxide: Unipolar Filamentary



- Switching: Thermochemical change in oxide valence state
- Anion motion (O^{2-})
- Symmetric structure
- NiO_x most common material
- Switching independent of E-field direction
- R/W current independent of device area

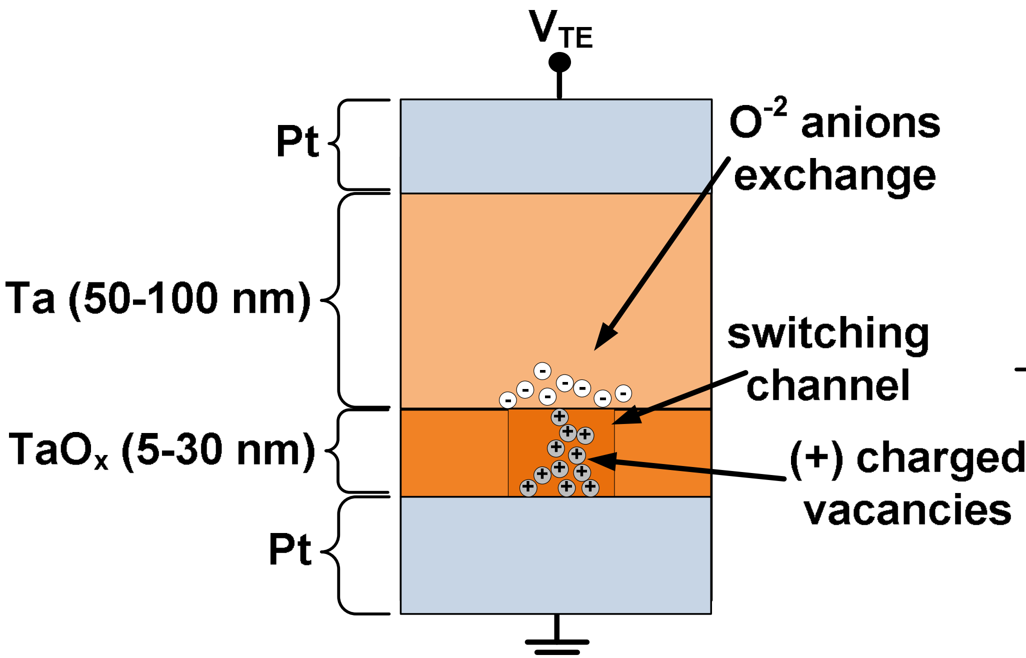
Metal Oxide: Bipolar Non-Filamentary

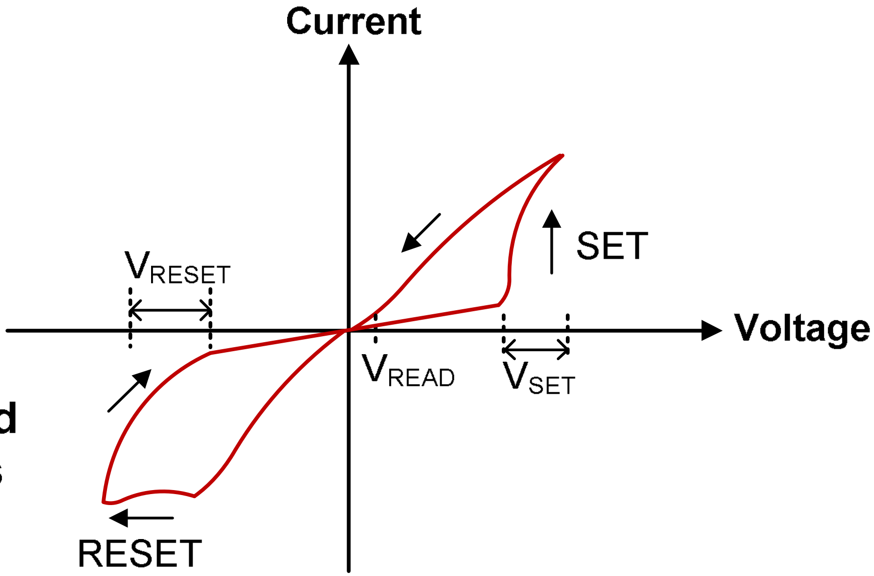


- Switching: Oxygen exchange causes Schottky barrier height change at interface
- Anion motion (O^{2-})
- Perovskite and insulating metal oxide
- Switching depends on E-field direction
- R/W currents depend on device area

Valence Change ReRAM

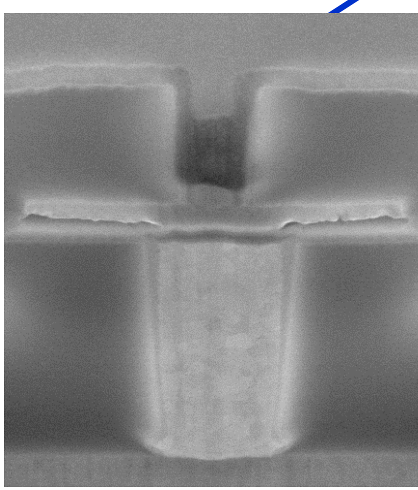
- "Hysteresis loop" is simple method to visualize operation
  - (real operation through positive and negative pulses)
- Resistance Change Effect (polarities depend on device):
  - Positive voltage/electric field: low R – O^{-2} anions leave oxide
  - Negative voltage/electric field: high R – O^{-2} anions return
- Common switching materials: TaO_x, HfO_x, TiO_2, ZnO

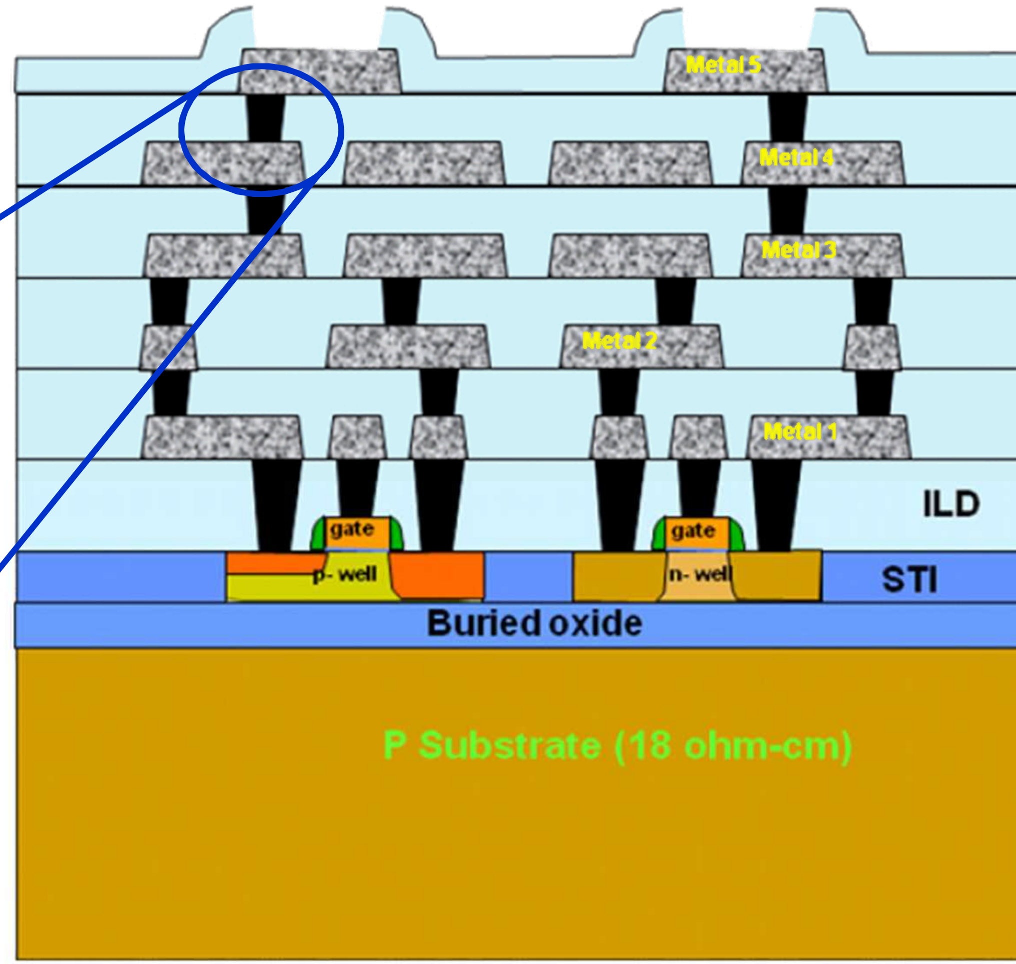




Memristors + CMOS

- Sandia CMOS7 Process
  - 3.3V, 350 nm, MOSFETs
  - SOI substrate
- Baseline for memristor integration





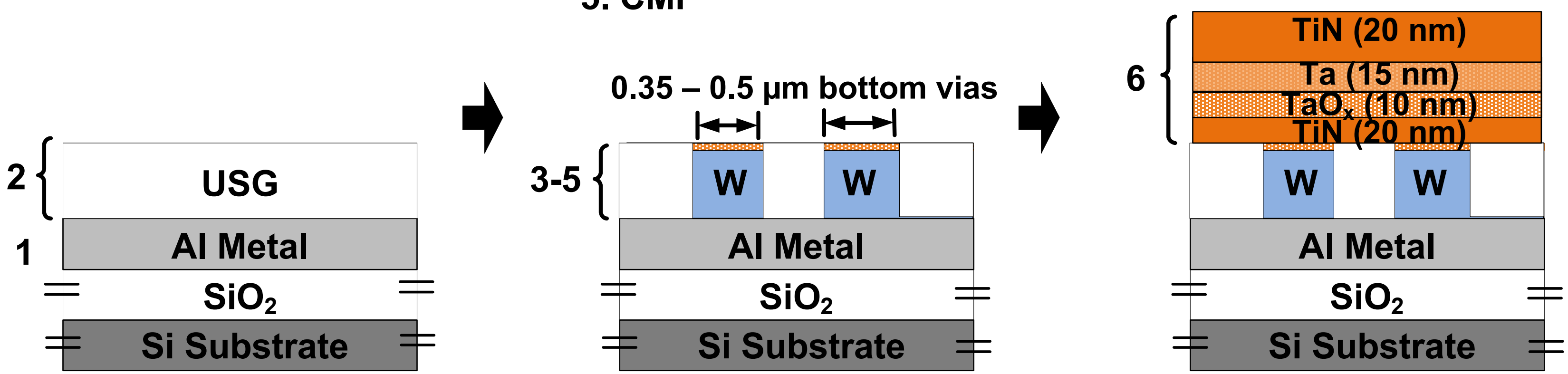
Microsystems
Science, Technology & Components

Process Flow

1. Deposit Bottom Metal (Al)
2. Deposit USG

3. Etch via holes in USG
4. Deposit W and TiN layers
5. CMP

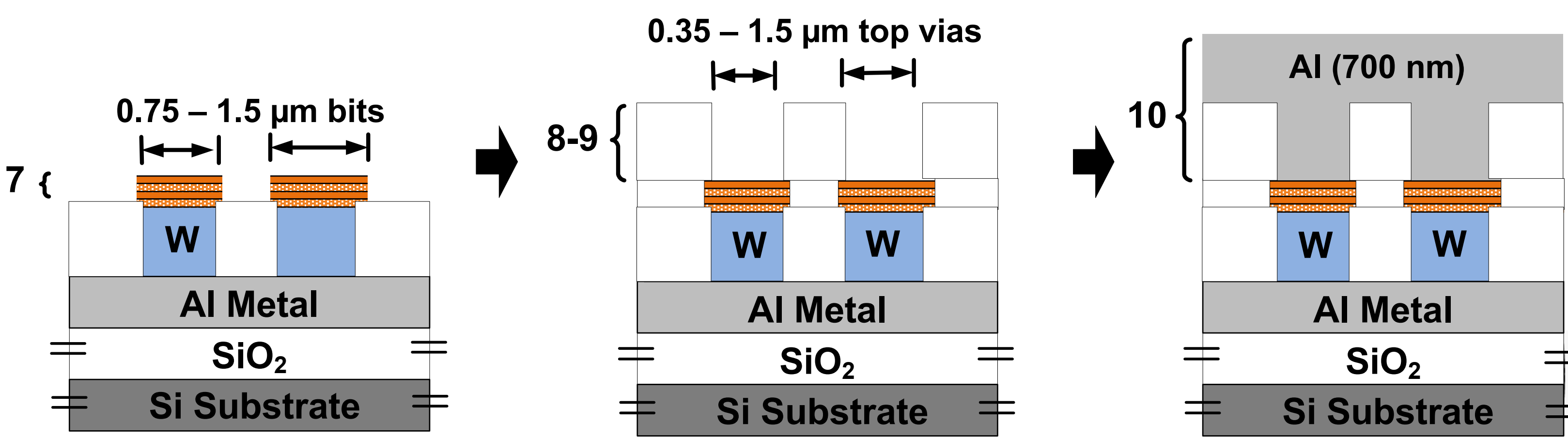
6. Deposit bit stack
(layers enlarged for clarity)



7. Etch bits

8. Deposit top USG
9. Etch top via holes in USG

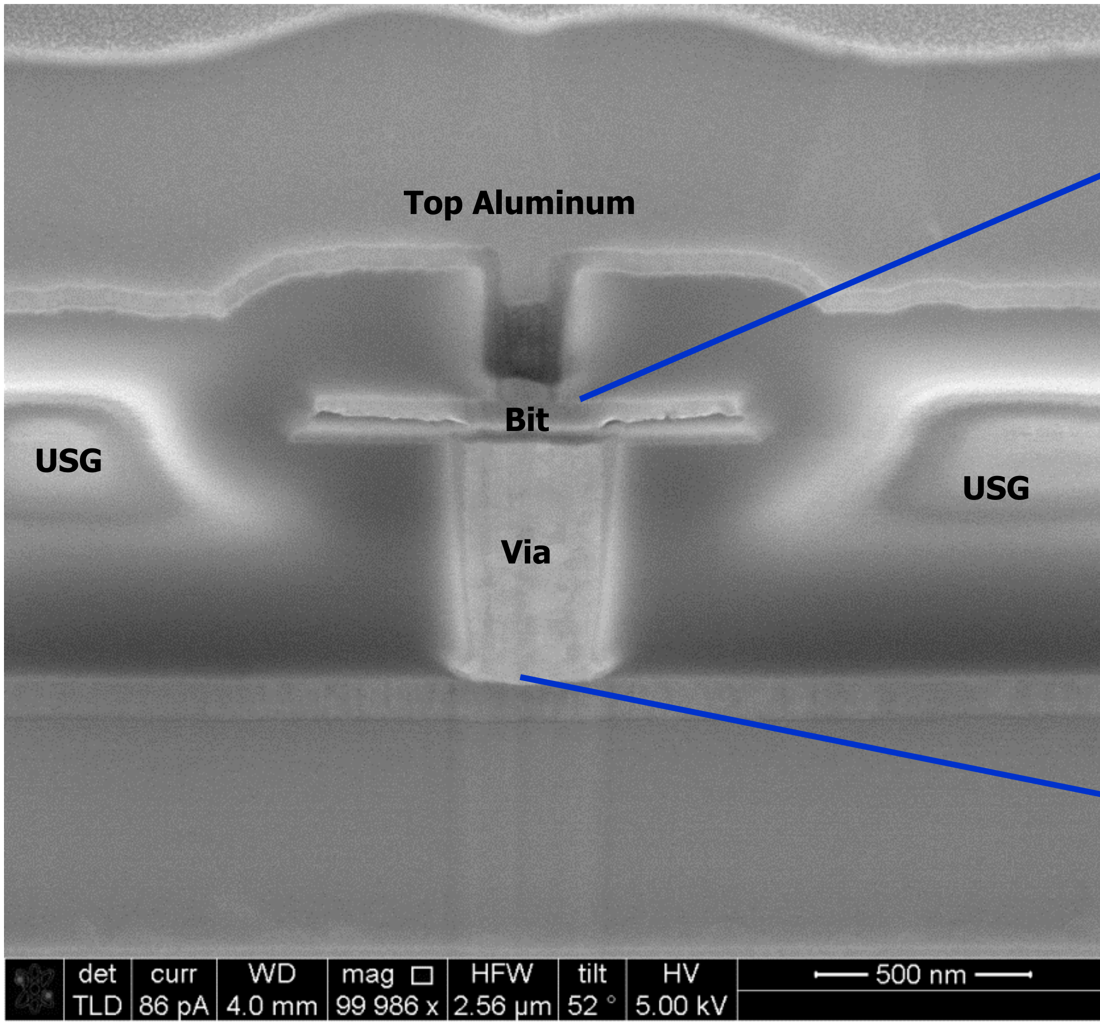
10. Deposit top Al



Sandia National Laboratories

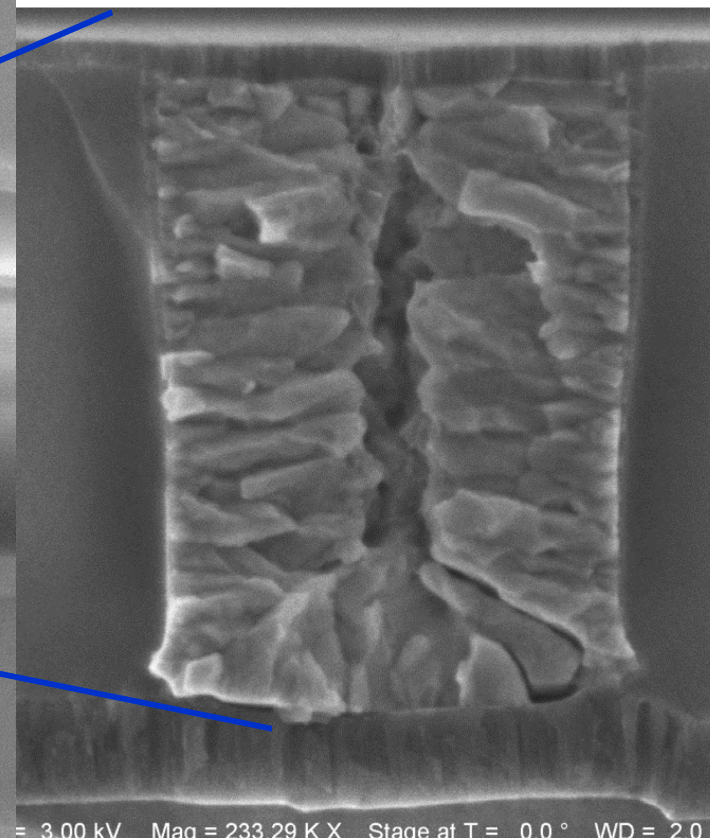
Microsystems
Science, Technology & Components

Final Structure



Important to have extremely flat surface under bit

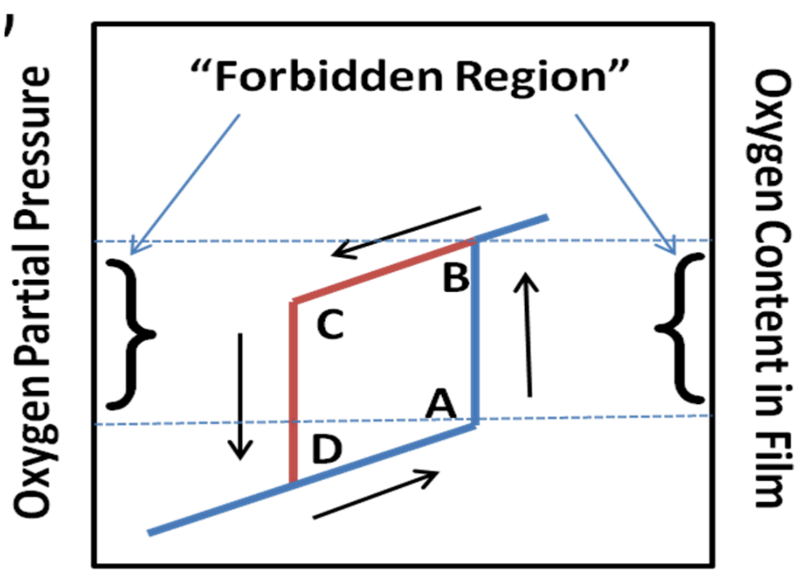
Polished TiN Surface



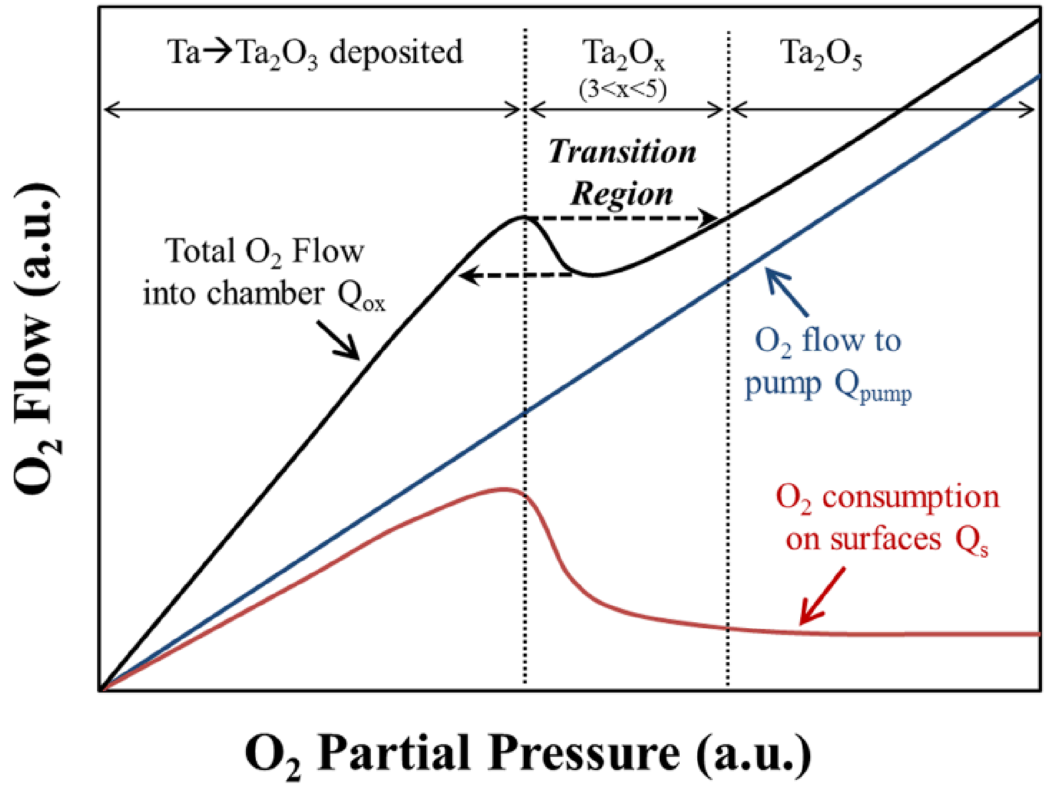
Sandia National Laboratories

Switching Film Development: Getting the Stoichiometry Just Right (TaO_2)

- Forbidden oxygen flow-pressure region occurs due to target poisoning
- This is the region we need to be in to get ideal ReRAM stoichiometry

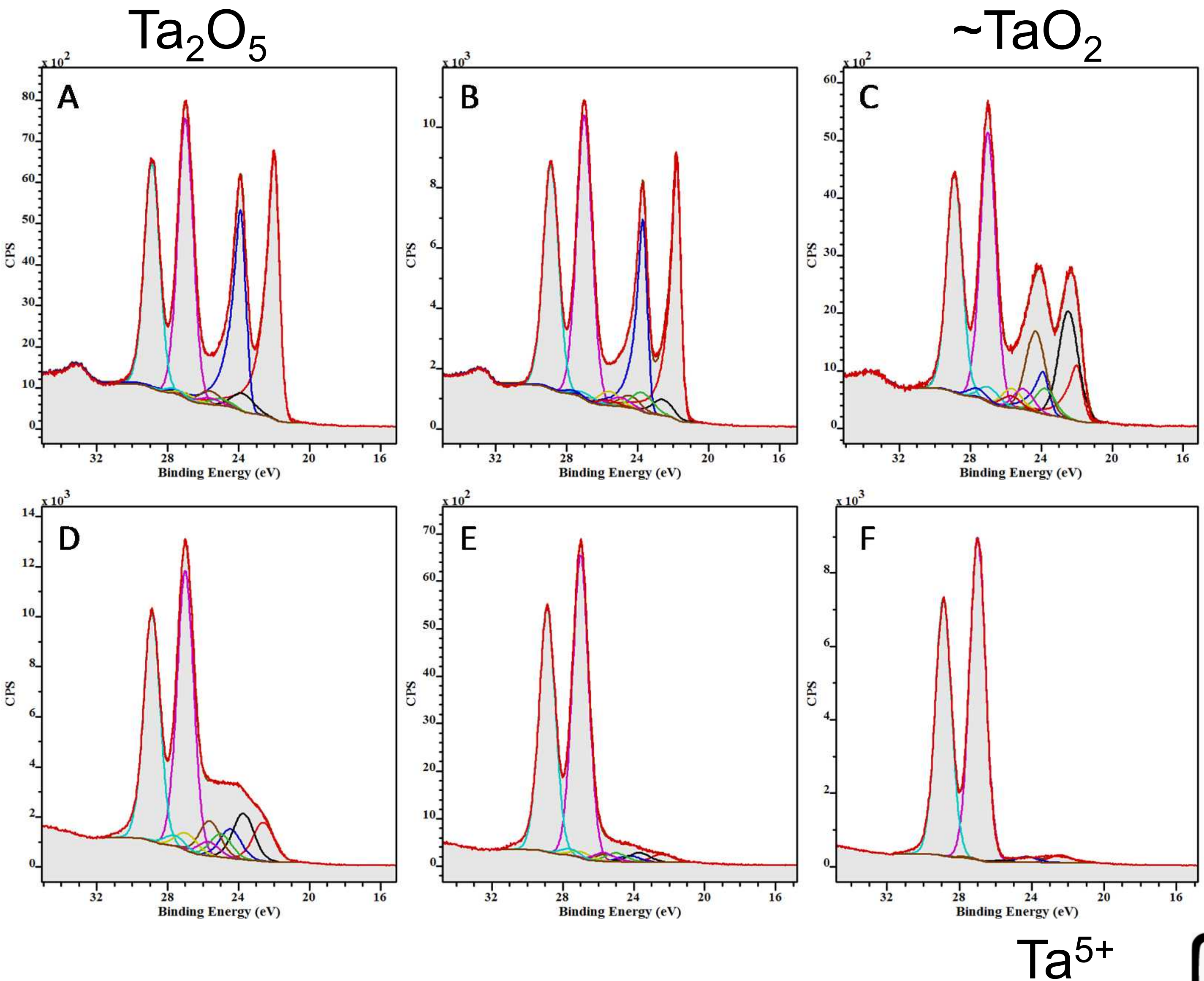


A.J. Lohn et al APL 103, 063502 (2013)

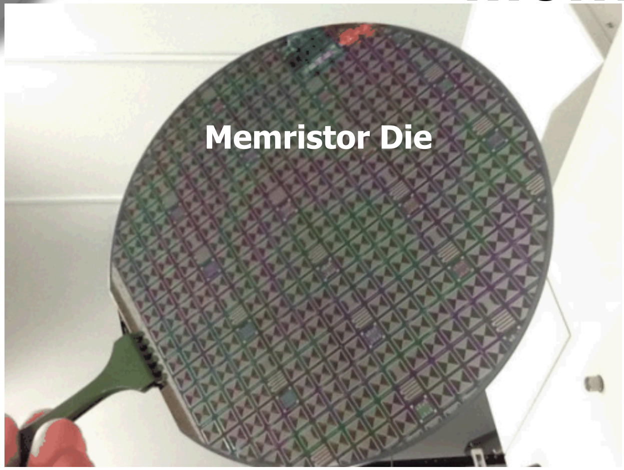


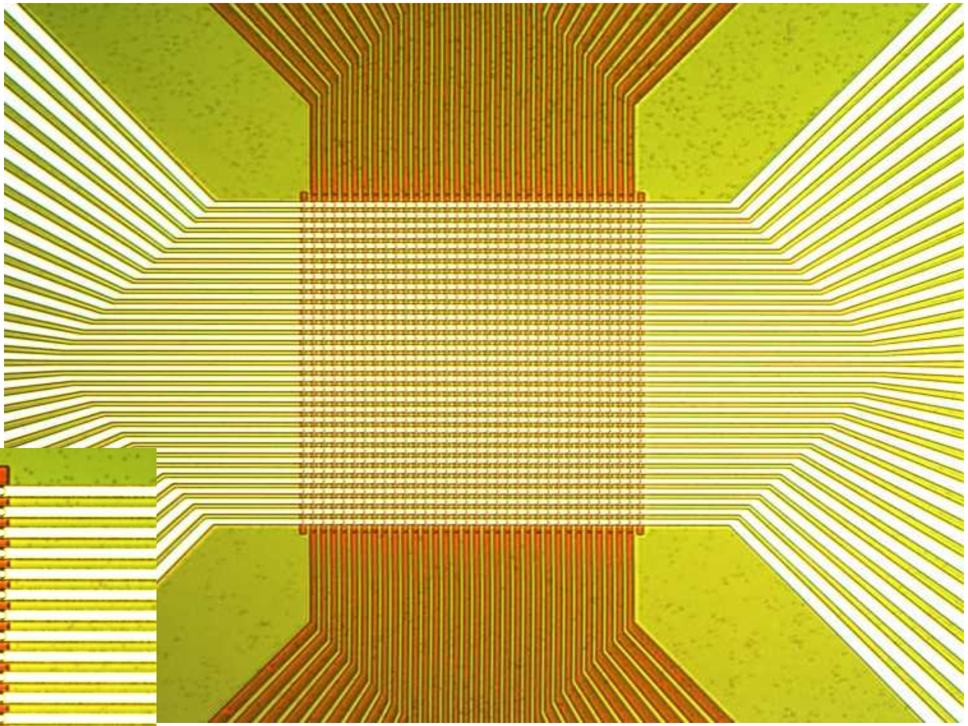
J.E. Stevens et al, J. Vac Sci. Tech., 32 021501 (2013)

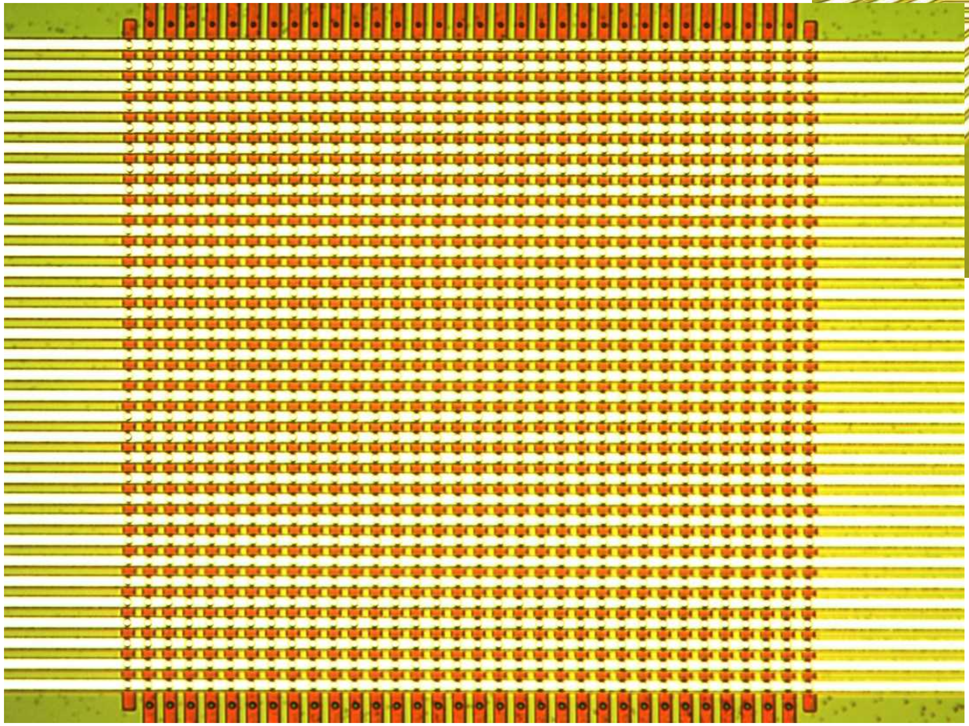
XPS analysis of O Deficient Films



Memristor Crossbar Die



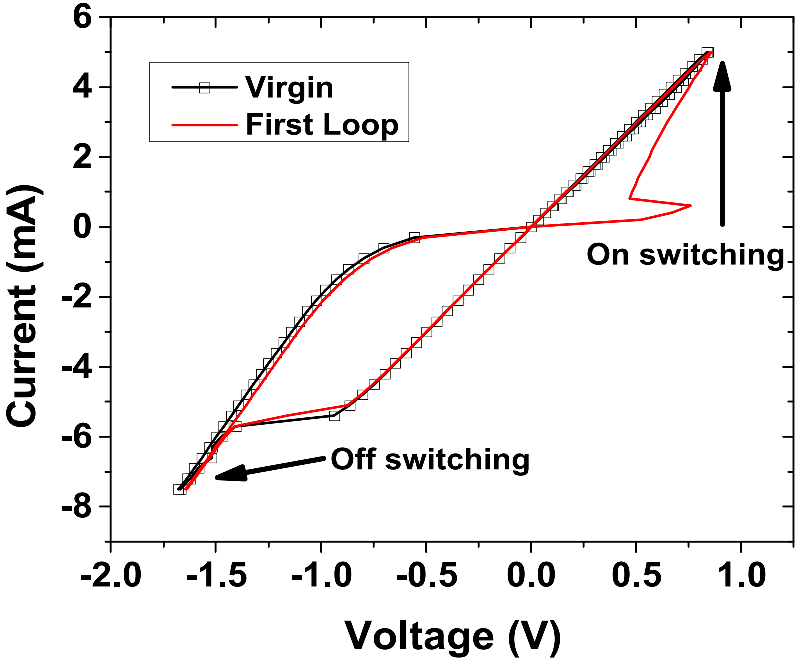




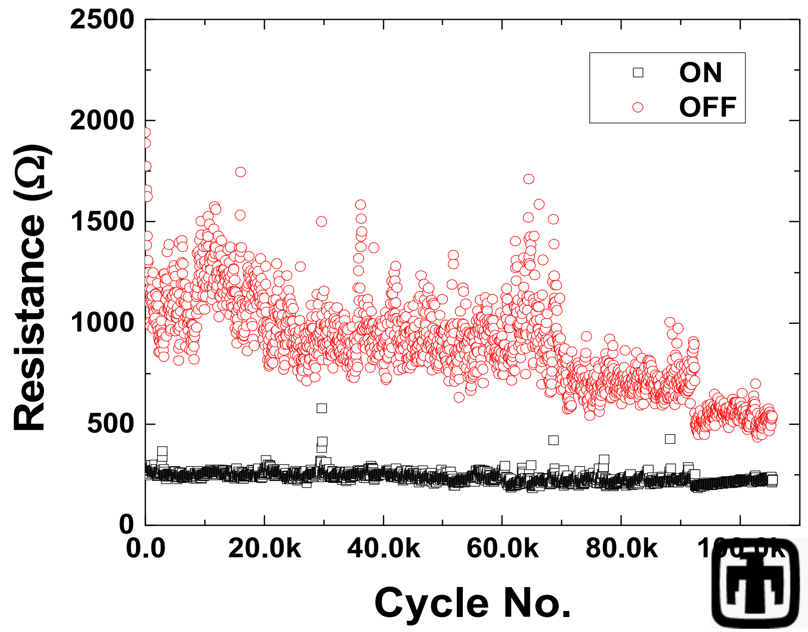
Basic Device Performance

- Typical devices form at very low currents
- Appear "forming free" in current sweep mode

DC I-V



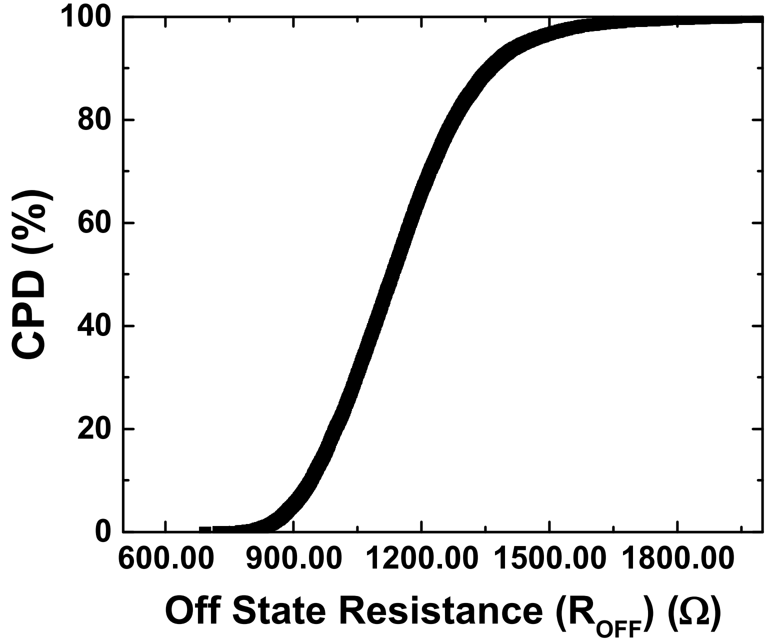
Endurance



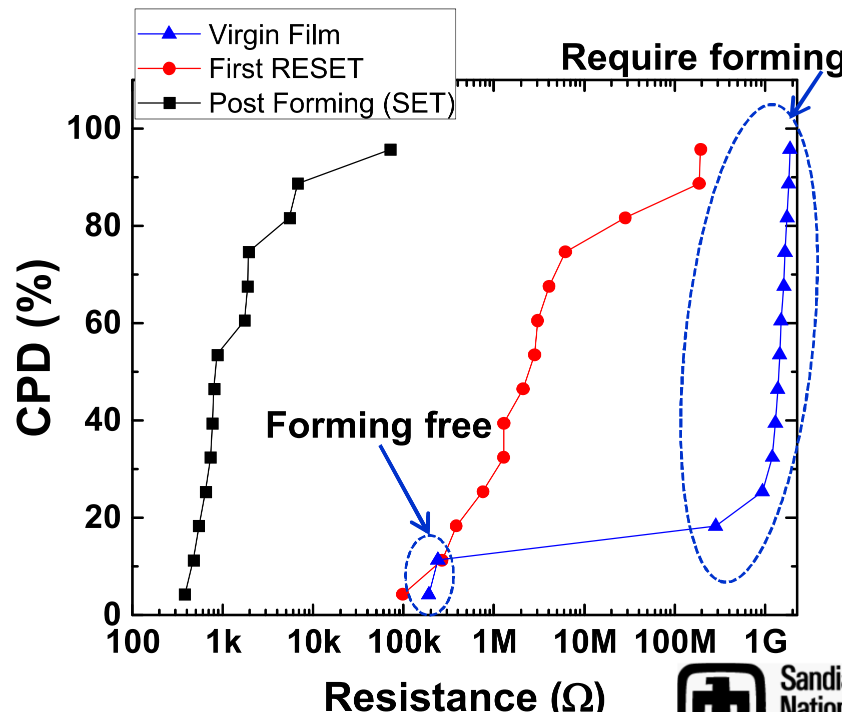
Nonuniform Device Characteristics

- Characteristics vary widely between devices and within a single device
- Some devices are "forming free" and some require forming

Single Device Cycling
(off state)

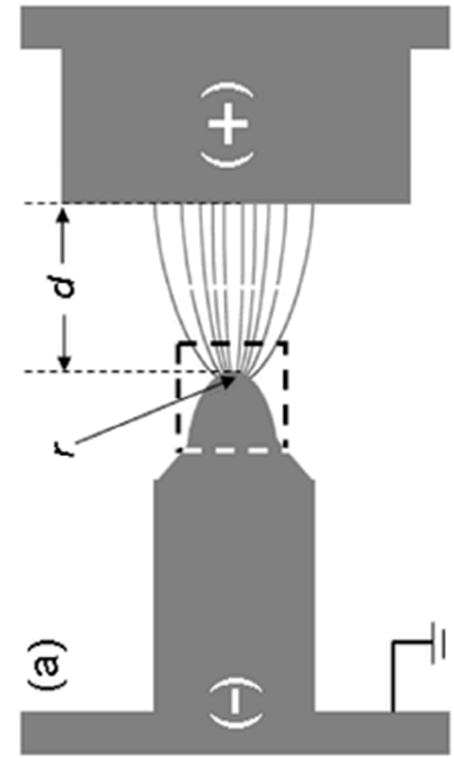


14 Devices



Key Questions

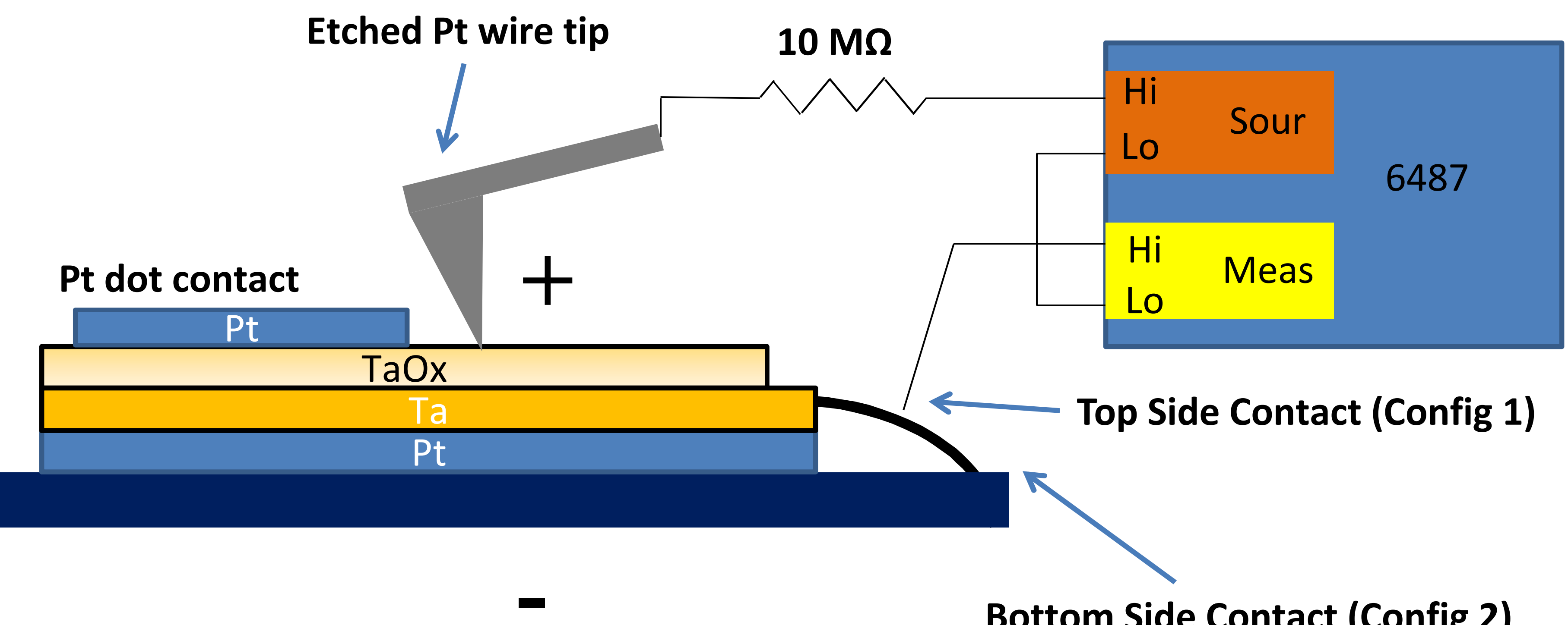
- Why are some devices "born on" some are "born off"?
- Where does the filament form?
  - Local geometric features/defects?
  - Field enhancement around a defect?
  - Local areas with high oxygen defect concentrations?
- How common are these features?
  - 1 per um^2?
  - Is this related to the filament
- How do film properties effect this?
  - I.e. stoichiometry



Fang et al, J. Mater. Chem. 18, 509, 2008.

Conducting Atomic Force Microscopy

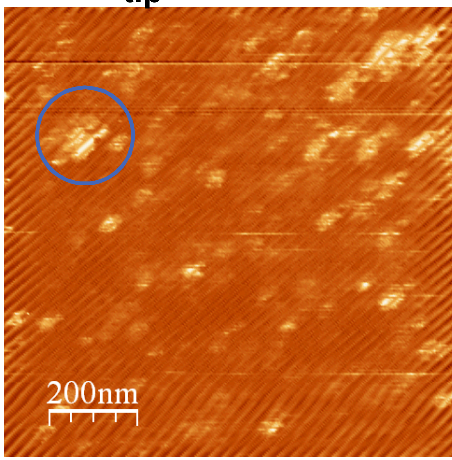
- AFM tip with capability to apply electrical bias
- Measure current-voltage with ~10nm resolution
- 10 MΩ series resistor to avoid over-current
- Tip voltage positive wrt sample to avoid oxidation



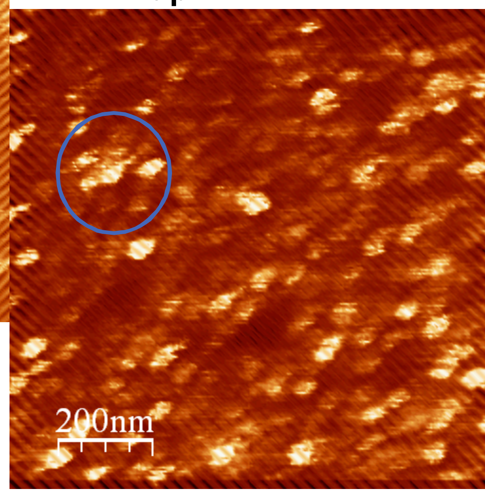
Microsystems
Science, Technology & Components

Hot Spot Formation

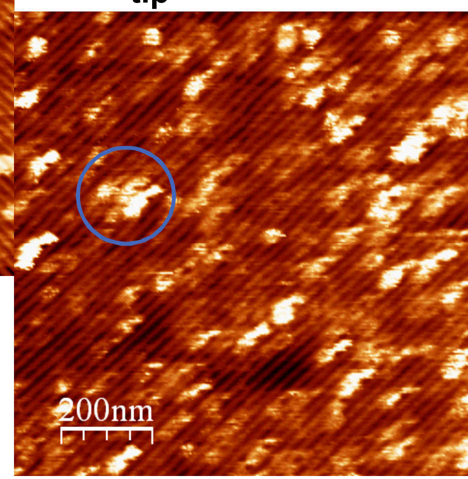
V_{tip}=2.4 V



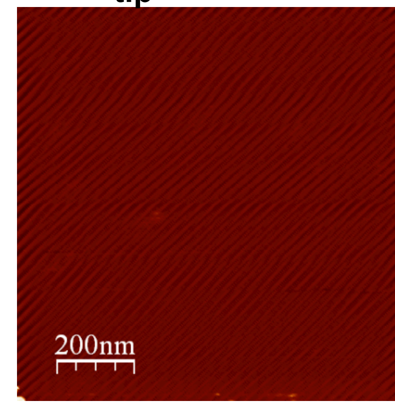
V_{tip}=2.6 V



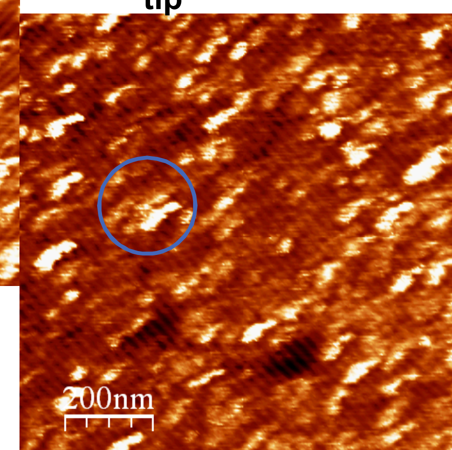
V_{tip}=2.8 V



V_{tip}=2.0 V



V_{tip}=3.0 V

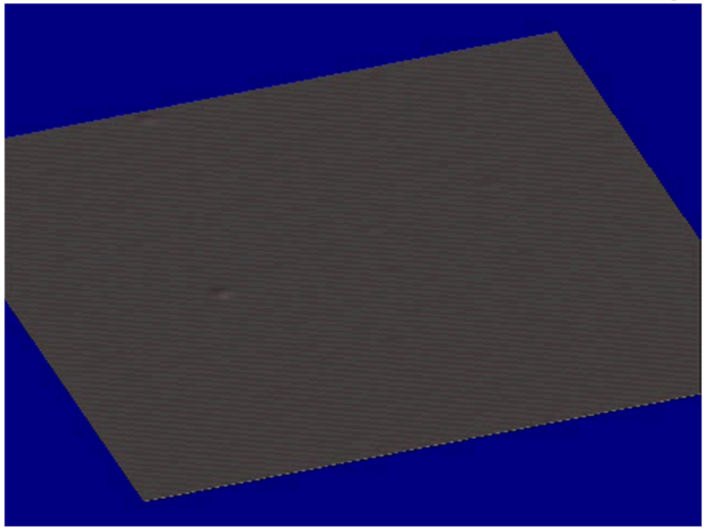


National Laboratories

Hot Spot Evolution

C-AFM Current Map Movie (2D)

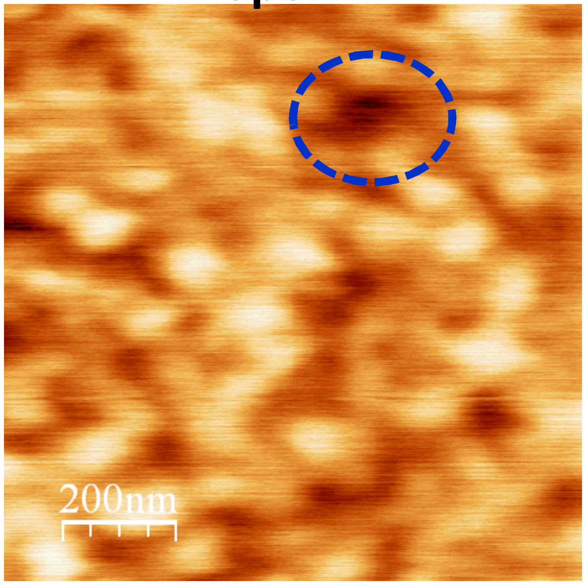
C-AFM Current Map Movie (3D)



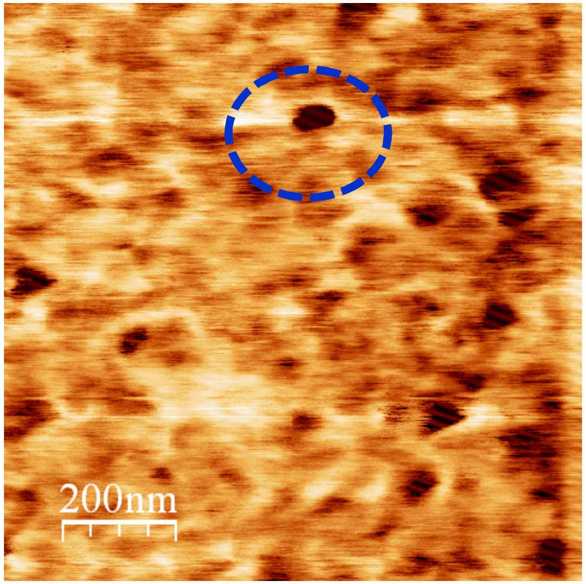
Topography versus Conductivity

- Prominent hot spot appears to depend on geometry
- Other hot spots do not necessarily correlate with geometric defect

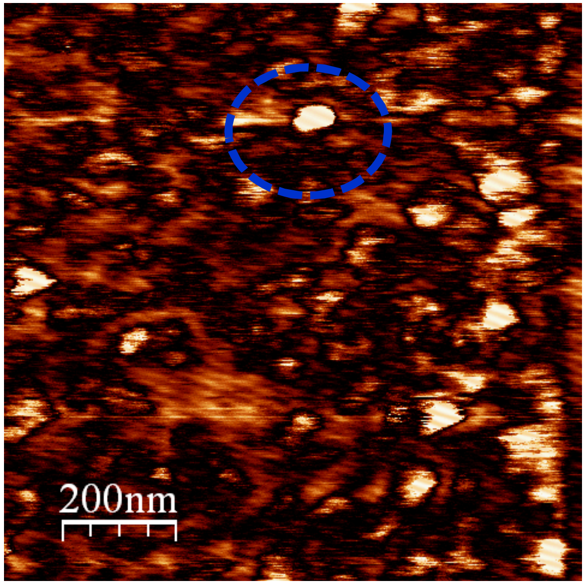
Topo



Current



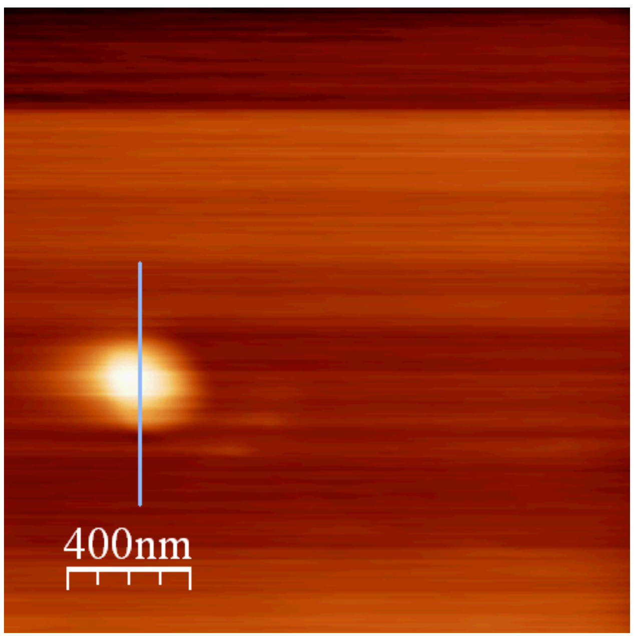
Merged (And)



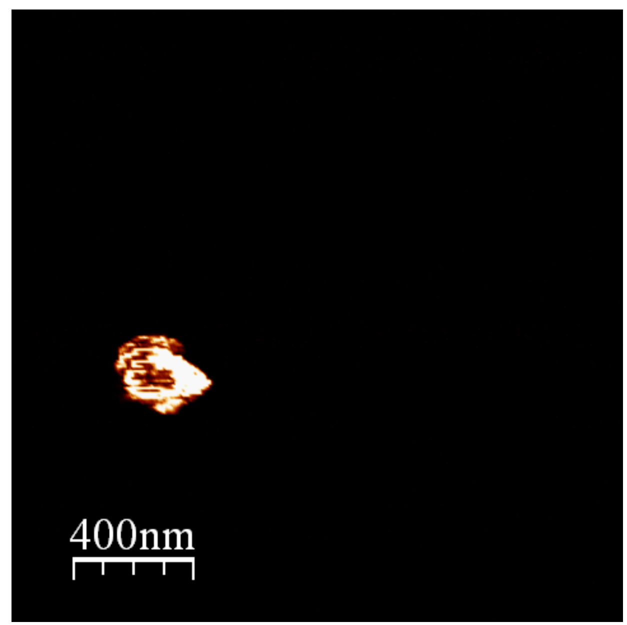
Hard Breakdown

- Permanent change in surface morphology when resistor removed
- 30 nm peak bump (blue line)
- Avoid this regime for film study (can destroy tip)

Topographic Image



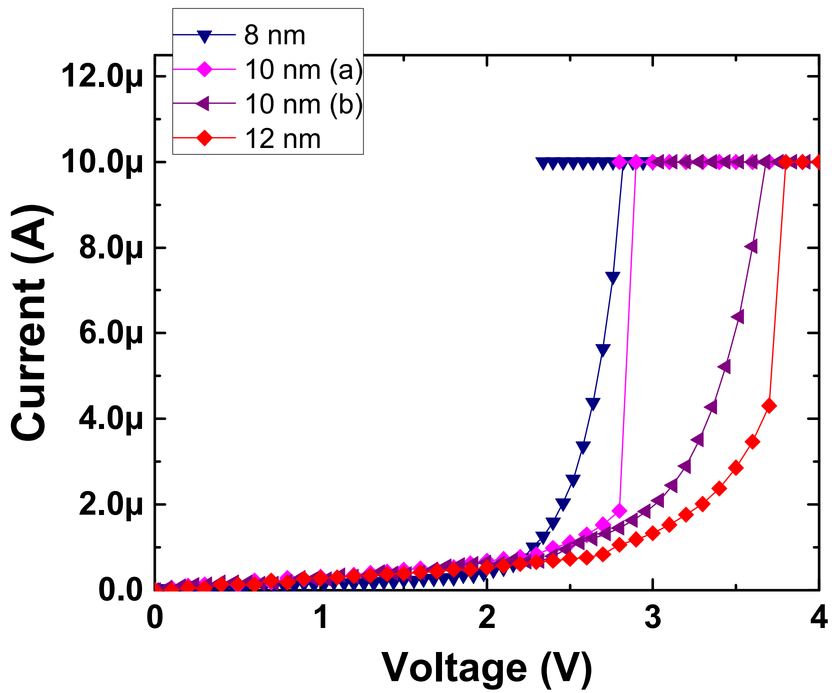
Current Image



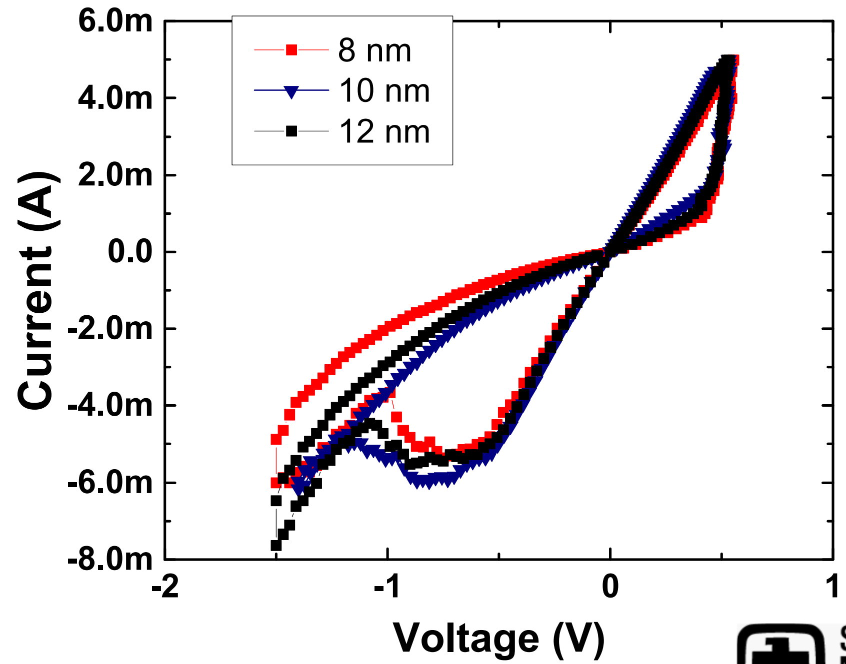
Forming Process

- Roughly depends on film thickness (still varies)
- Macroscopic (wafer scale) and nanoscopic variations in thickness

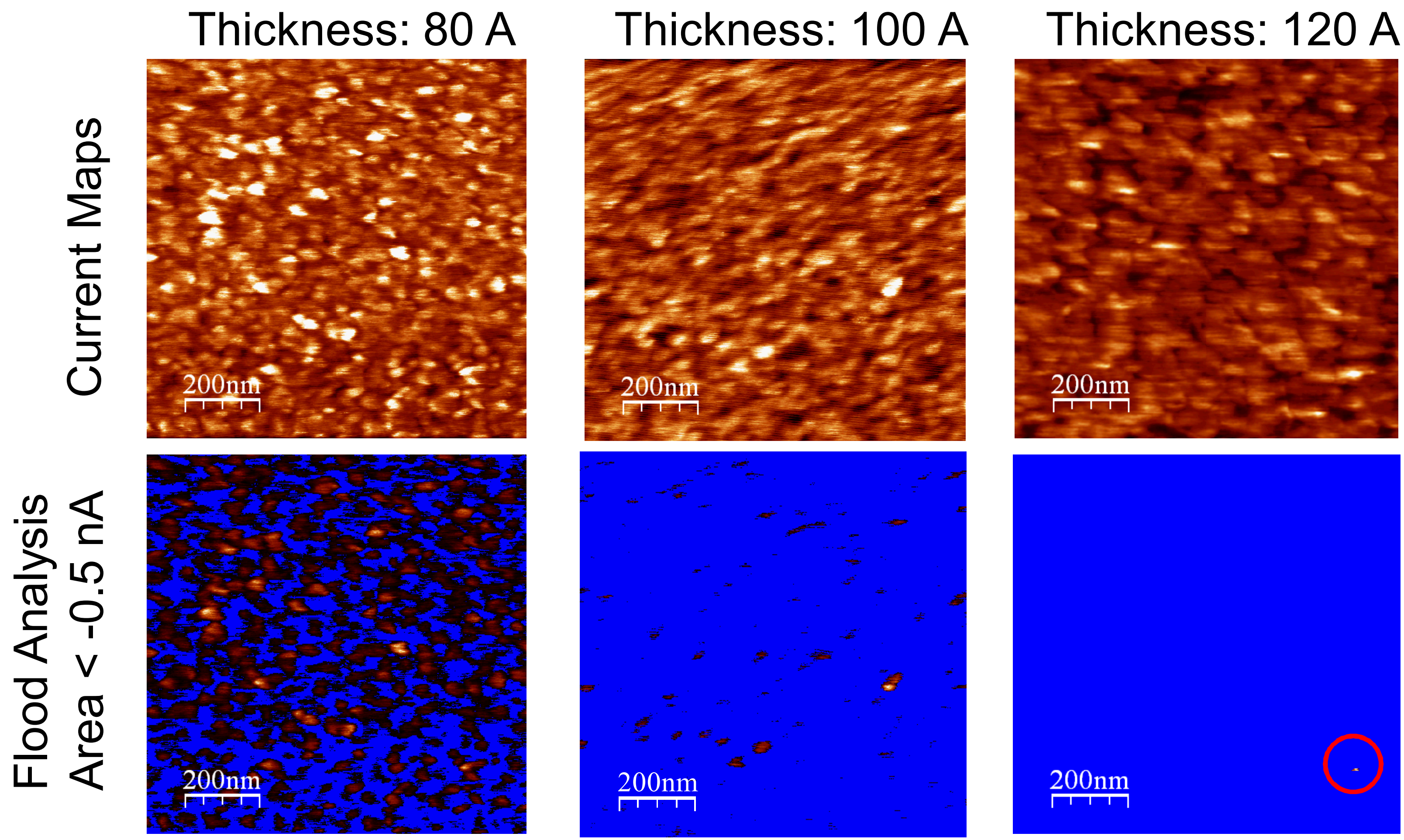
Forming



Switching



Hot Spot Density vs Thickness



Sample Voltage: -3.5 V
Same tip used for all imaging

Microsystems Science, Technology & Components

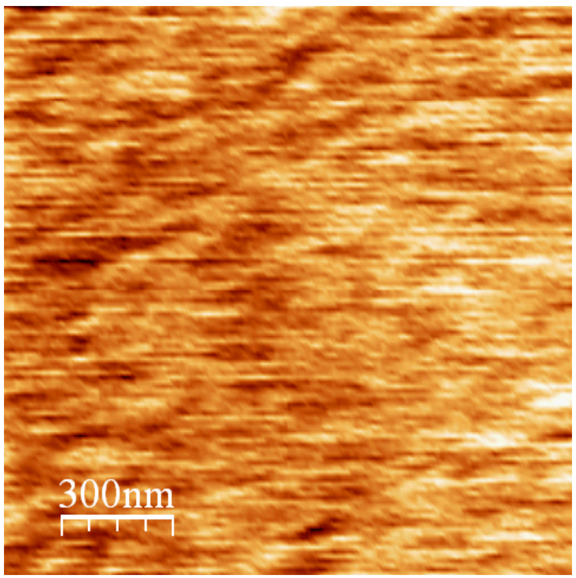
Sandia National Laboratories

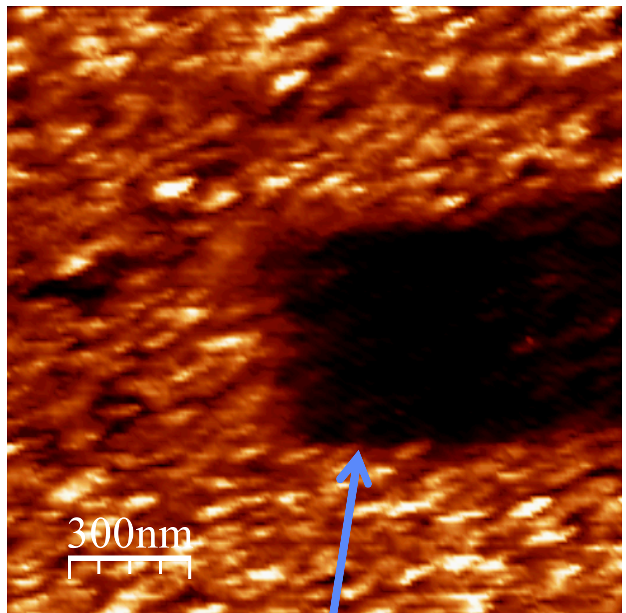
CAFM Comparison of TaOx Thickness

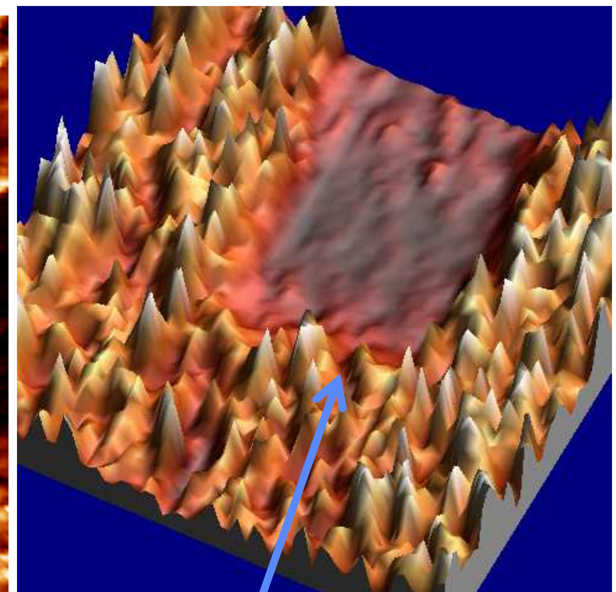
	% Image area < -0.5 nA			
TaOx Thickness (A)	Spot-1	Spot-2	Spot-3	Spot-4
120	0%	0.01%	0.00%	0.37%
100	0.52%	0.41%	1.92%	0.44%
80	49.77%	64.99%	62.26%	86.92%

Charging Effects

- **Charge buildup creates electric field which opposes current**



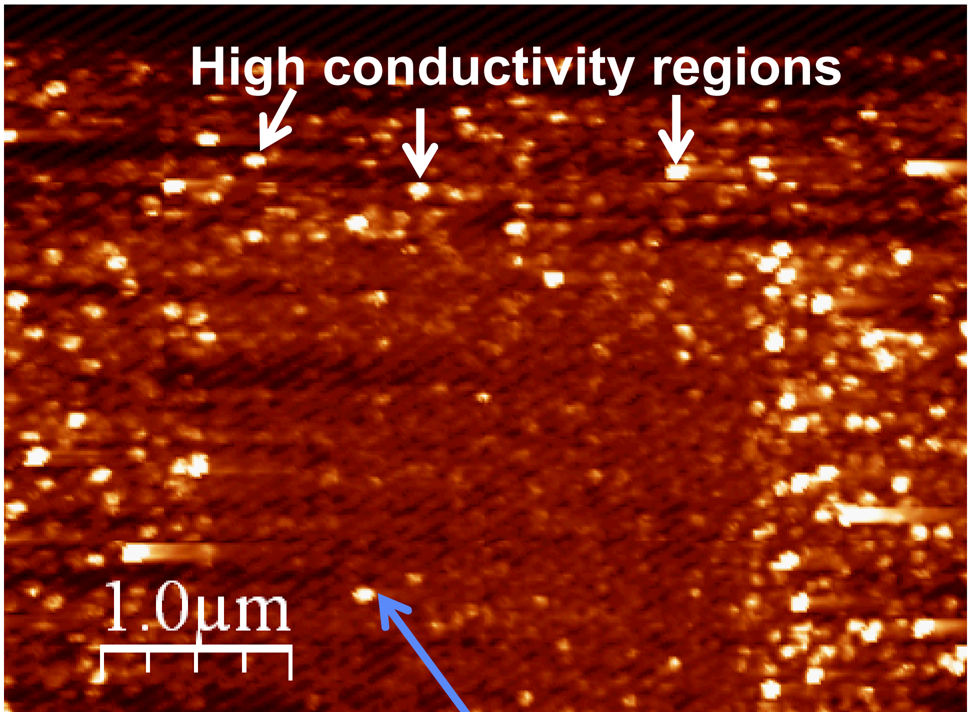


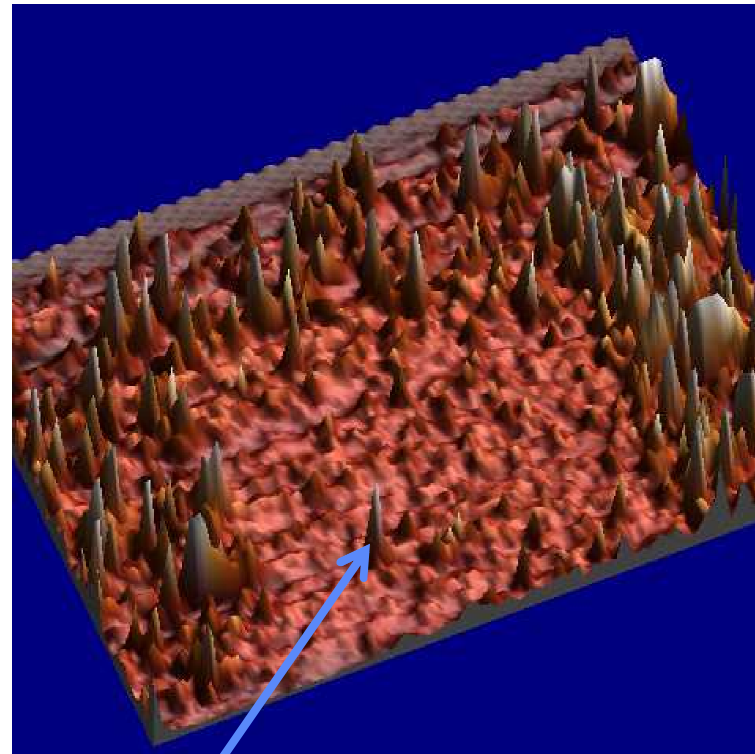


Morphology does not change

Conductivity declines after continued charging

Charging Effects

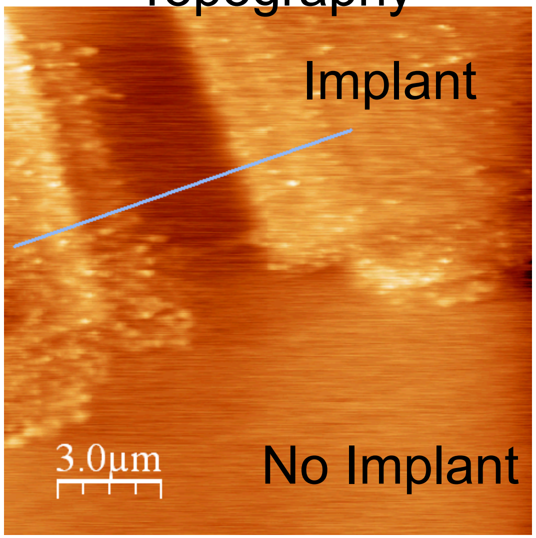




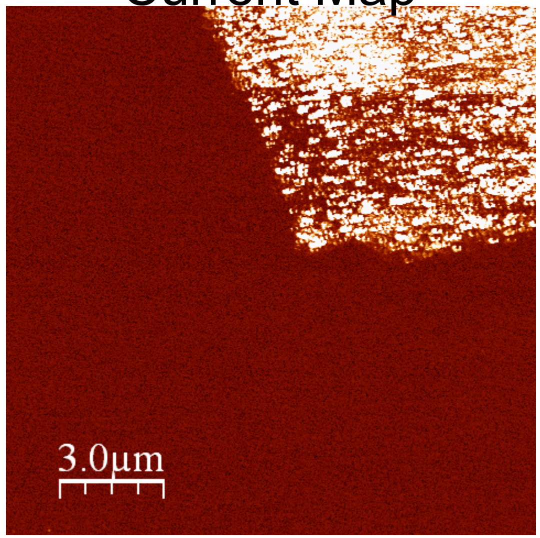
Single remaining hot spot

C-AFM Studies of Implanted TaOx/Pt Films

Topography

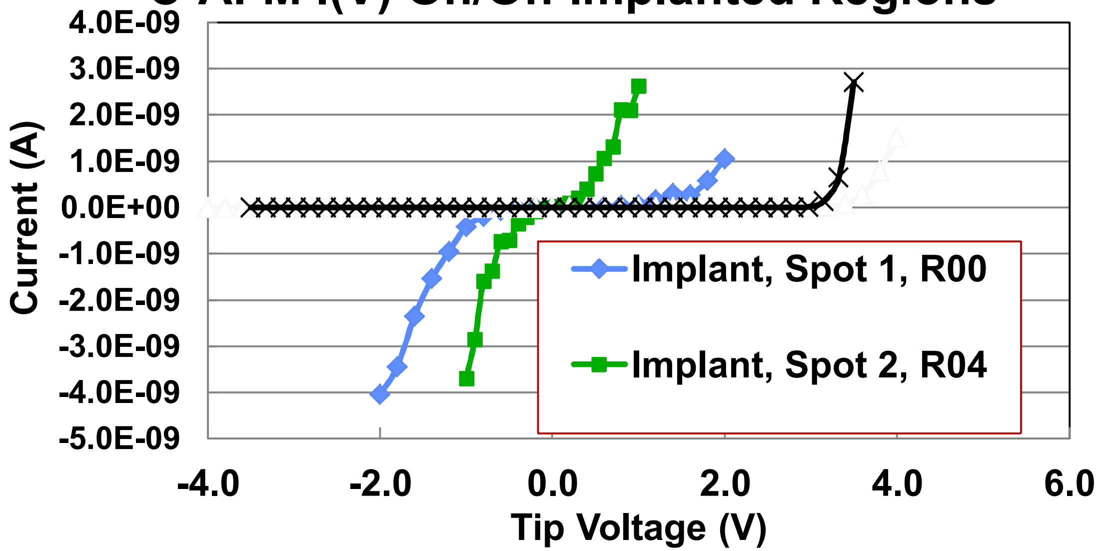


Current Map

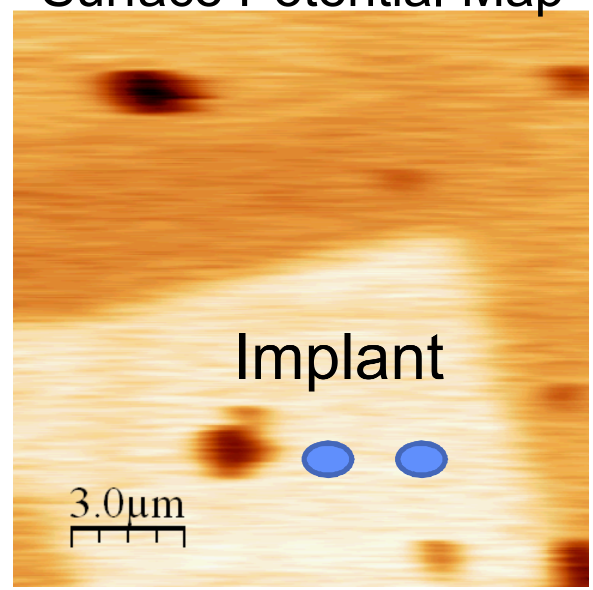


- **C-AFM of TaOx after implant:**
  - **Implant 200 keV Si**
  - **Changes in morphology**
  - **Increase in film conductance in implant region**

C-AFM I(V) On/Off Implanted Regions



Surface Potential Map



- Implanted region clearly visible in EFM image

Future Work

- Analyze hot spot density as a function of stoichiometry
- Compare hot spots to electrical contact formed filament
- Analyze time dependent charging as a function of thickness and stoichiometry
- Study conductivity through film over full stack with W via
- Optimize thickness to control hot spot densities in a film
- Created controlled vacancy concentrations with ion beam and correlate to conductivity
- Use CAFM to switch film (in vacuum)

Summary

- A CMOS compatible, forming free TaOx ReRAM process has been developed
- Devices show significant variability in electrical switching and forming behavior
- Conducting AFM is a useful tool to study the local variations in electrical conductivity
- Localized high-conductivity "hot spots" form under increasing tip bias
  - Appear to form at geometric defects
  - Density strongly dependent on thickness
  - May account for "forming free" behavior
  - Thickness variations of ~2 nm significantly affect the density of hot spots in a region

Microsystems
Science, Technology & Components

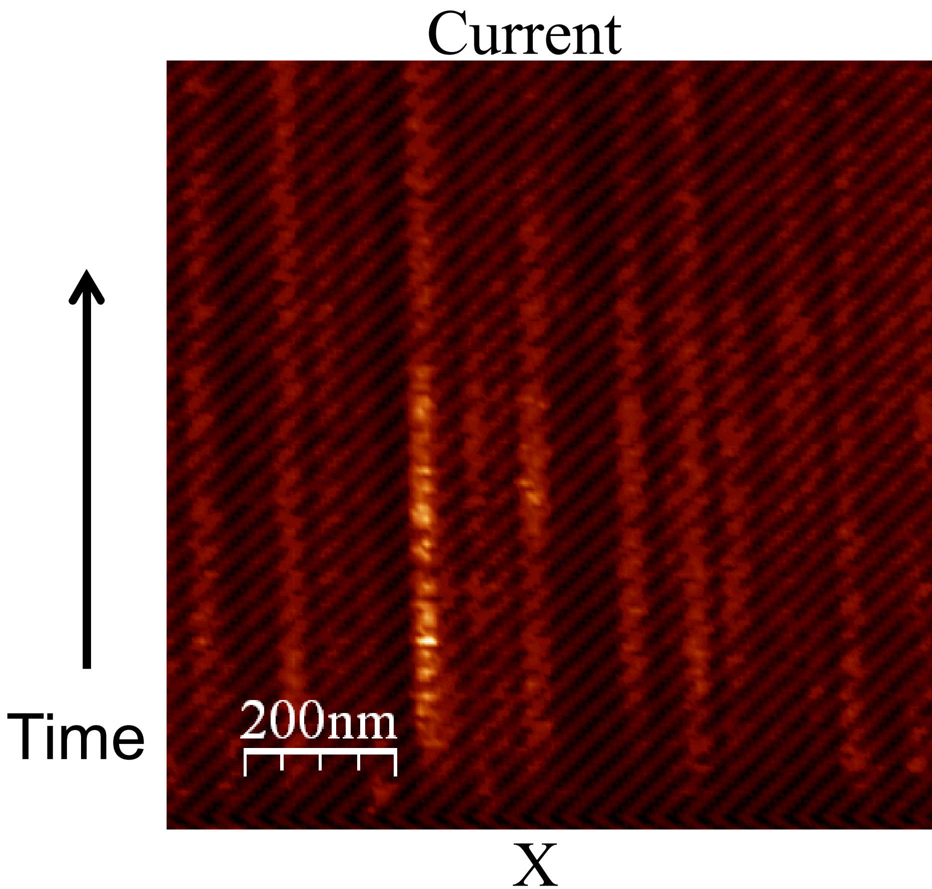
Acknowledgements

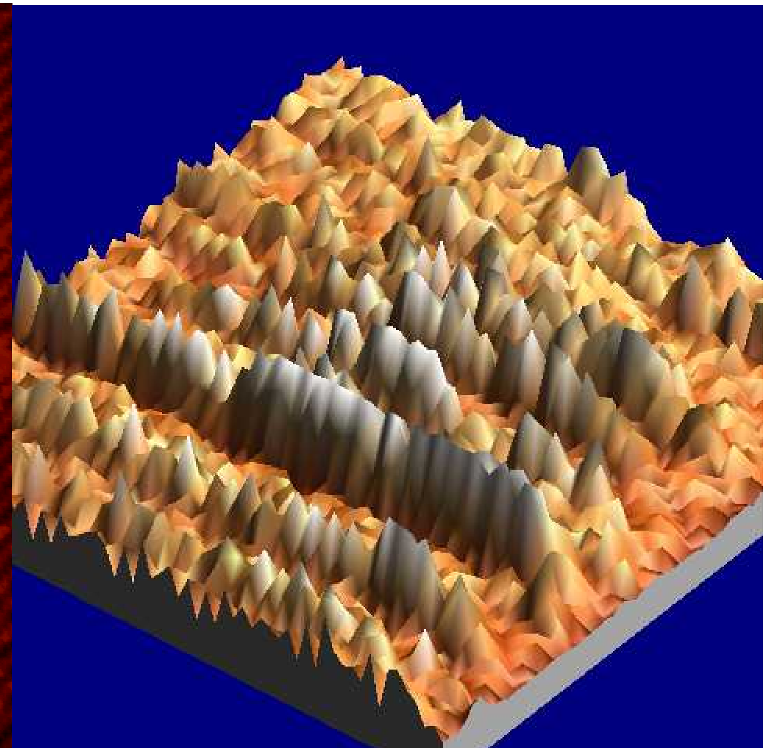
- Grateful to our collaborators at HP Labs, esp. Jianhua Yang, Yoocharn Jeon, John Paul Strachan, Si-Ty Lam, Brent Buchanan, Dick Henze, and Stan Williams
- Work partially funded by Sandia National Laboratories Laboratory Directed Research and Development program

Laboratory Directed Research & Development

Sandia National Laboratories

Hot Spot Evolution





FFT

Postdoctoral Position (Nano-Enabled Microelectronincs:646337)

The listed positing:
http://www.sandia.gov/careers/students_postdocs/postdocs.html

Desired:

- An experimental background in scanning probe microscopy.
  - **Tapping mode, scanning thermal microscopy, Conductive-AFM, near-field radiative heat transfer, Casimir force measurements, etc.**
- An experimental background in Graphene and Carbon Nanotube research.
- Ability to work well in a dynamic, large, and multi-disciplinary research team environment.
- A willingness to learn new experimental techniques.
- Extensive experience in the design, fabrication, assembly, and/or characterization of micro/nano-scale systems.
- Experience in industrial, government, or other laboratory environments outside the academic community.