High Performance ZVT with Bus Clamping Modulation Technique for Single Phase Full Bridge Inverters

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***Abstract*—This paper proposes a topology based on bus clamping modulation and zero-voltage-transition (ZVT) technique to realize zero-voltage-switching (ZVS) for all the main switches of the full bridge inverters, and inherent ZVS and/or ZCS for the auxiliary switches. The advantages of the strategy include significant reduction in the turn-on loss of the ZVT auxiliary switches which typically account for a major part of the total loss in other ZVT circuits, and reduction in the voltage ratings of auxiliary switches. The modulation scheme and the commutation stages are analyzed in detail. Finally, a 1kW, 500 kHz switching frequency inverter of the proposed topology using SiC MOSFETs has been built to validate the theoretical analysis. The ZVT with bus clamping modulation technique of fixed timing and adaptive timing schemes are implemented in DSP TMS320F28335 resulting in full ZVS for the main switches in the full bridge inverter. The proposed scheme can save up to 33 % of the switching loss compared with no ZVT case.**

Keywords—ZVT, bus clamping, full bridge, switching loss saving

I. INTRODUCTION

The single phase full bridge inverter is widely used for power conversion in numerous applications [1]. High power density has become a very important metric in many of these applications in recent years. Increasing the switching frequency to significantly higher levels can lead to high power density, but it is at the expense of correspondingly higher switching losses and therefore lower efficiency. Accordingly, soft-switching full-bridge inverters have been pursued [2-5]. The application of soft-switching techniques to inverters can not only realize reduced switching loss, miniaturization, and lightweight, but also reduce the electromagnetic interference (EMI) and switching noise.

Among these soft-switching techniques, the zero voltage transition (ZVT) technique is particularly advantageous, especially when the active switches are implemented with majority carrier devices such as power MOSFETs [6]. While there are different approaches to achieving ZVT, a commonly used method involves an auxiliary active circuit to divert the current from the main circuit to discharge the switch parasitic capacitance, allowing its turn on under null voltage [7]. Many ZVT inverters have been proposed. Among them, the representative circuits are triangular or stellate resonant snubber inverters, coupled inductor inverters, transformer-assisted inverters, and resonant ac-link inverters [8-15].

However, one major concern in these ZVT converters is the turn-on loss of the auxiliary switch which can be a dominant part of the total loss in the auxiliary circuit especially in high switching frequency applications [16-17]. Also the voltage ratings of the auxiliary switches are usually comparable to the voltage ratings of the main switches which increases the volume and cost of the auxiliary circuit. In addition, these topologies need either two bulk capacitors or complex coupled inductors, or transformers with corresponding magnetic flux reset circuits [18]. And for the full bridge inverters using unipolar PWM, two separate auxiliary circuits - one for each leg of the inverter, are needed.

Though the mechanism by which soft switching is achieved is similar for the various ZVT converters, the exact configuration in terms of where the auxiliary circuit is connected to the main circuit, how the driving voltage for the auxiliary circuit is obtained and the switching strategy for the auxiliary circuit have a major impact on the performance of overall converter system.

This paper proposes a ZVT circuit implementation that significantly decreases the voltage stress and the switching loss in the auxiliary switches. A synchronous buck converter operating under inherent ZVS is used to obtain the driving voltage for the auxiliary circuit. In addition, bus clamping modulation is employed in this work to avoid the need for two separate bi-directional auxiliary circuits. In bus clamping modulation, also known as hybrid PWM modulation, two of the four switches are driven by high switching frequency PWM signals for high quality sinusoidal output and the other two are commutated at the low, fundamental frequency [19-24]. Bus clamping modulation technique will be used in combination with the proposed ZVT circuit to achieve reduced voltage rating of auxiliary switches. This paper designs the modulation scheme for the realization of ZVT of main switches, while achieving low turn-on voltage and low switching loss of the auxiliary switches.

II. PROPOSED TOPOLOGY AND ANALYSIS OF OPERATION

Fig.1 shows the proposed topology employing the bus clamping modulation with low-loss ZVT technique for single phase full bridge inverters. The buck stage in the front provides a controllable, stable and relatively low voltage (designed to be around 20% of the input voltage in the experiment) for the auxiliary ZVT circuit. The buck stage needs to process only the power needed to realize ZVT for the main full bridge switches, and hence, its rating and the losses are quite small. Also the average value of the buck stage inductor current (i_b) is very low (almost 0), and the inductor is purposely chosen to be small enough to allow a relatively large ripple. The ripple current has the correct positive or negative direction at each switching interval, and hence, leads to natural ZVS for both the switches in the buck stage.

The two auxiliary switches S_1 and S_2 realize ZVT for Q_1 and Q_2 respectively. The voltage rating of the two auxiliary switches S_1 and S_2 are equal to the buck output voltage (V_b) which is small compared with previous ZVT topologies as discussed in [6] and [8] which is $V_{dc}/2$ and V_{dc} respectively. The turn-on loss of the auxiliary switches S_1 and S_2 which is a major part of the ZVT circuit can be decreased significantly. Also switches can be chosen with lower voltage rating which can save volume, cost and possibly conduction losses.

As the ZVT circuit can only achieve ZVS for the upper main switches Q_1 and Q_3, traditional unipolar modulation of the full bridge inverters cannot be used to achieve full ZVT of all 4 main switches of the full bridge inverter. Instead the bus clamping modulation is used in combination with the proposed ZVT auxiliary circuit.

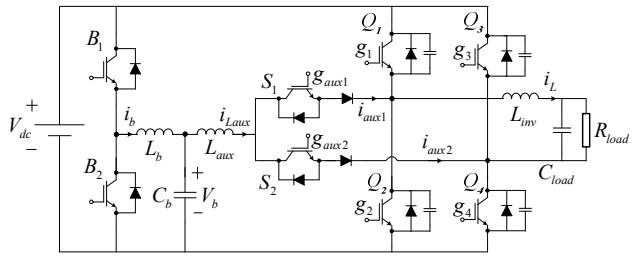


Fig. 1 Proposed topology of bus clamping modulation & ZVT technique for full bridge inverters

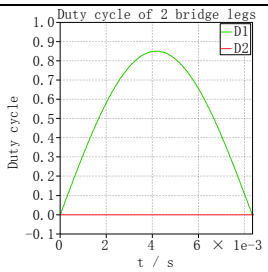
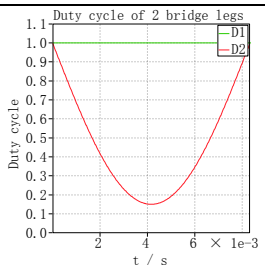
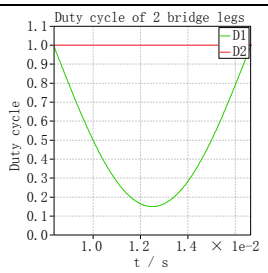
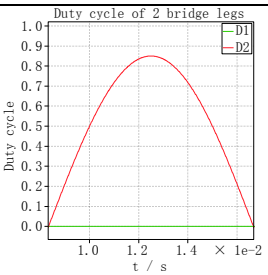
A. Bus clamping modulation with ZVT realization

The modulation scheme is shown in Table I where d is the duty cycle as same in the unipolar modulation (ranging from -1 to 1) and i_L is the output inductor current as shown in Fig. 1. The green waveforms labelled D_1 are the duty cycle given to Q_1 while the red waveforms labelled D_2 are the duty cycle given to Q_3. Q_2 and Q_4 are complementary to Q_1 and Q_3 respectively. d equals to $D_1 - D_2$.

This strategy can realize ZVS of all switches at any power factor. Take the condition of $d > 0$ and $i_L > 0$ for example, Q_2 and Q_3 can achieve natural ZVS because i_L is positive [4]. As $d > 0$ the positive state and zero state are needed which means Q_1 and Q_4 are needed. The strategy is that Q_4 is always ON which means the second bridge is bus clamped to the negative bus. Then Q_1 is ON when positive state is needed, Q_2 is ON when zero state is needed. As mentioned above, Q_2 can achieve natural ZVS by i_L while Q_1 achieves ZVT by S_1.

The scheme is capable of supporting non-unity power factors, but if the power factor is 1 the modulation strategy is relatively easier to implement compared to other power factors.

TABLE I. BUS CLAMPING MODULATION SCHEME WITH ZVT

$d > 0$ $i_L > 0$	$d > 0$ $i_L <= 0$
	
Q_4 on, Q_3 off, Q_2 achieves natural ZVS by i_L, Q_1 achieves ZVT by S_1	Q_1 on, Q_2 off, Q_4 achieves natural ZVS by i_L, Q_3 achieves ZVT by S_2
$d <= 0$ $i_L > 0$	$d <= 0$ $i_L <= 0$
	
Q_3 on, Q_4 off, Q_2 achieves natural ZVS by i_L, Q_1 achieves ZVT by S_1	Q_2 on, Q_1 off, Q_4 achieves natural ZVS by i_L, Q_3 achieves ZVT by S_2

B. Detailed analysis of commutation process

The commutation process of the ZVT will be analyzed in this section. Take the condition of $d > 0$ and $i_L > 0$ for example where Q_4 is always ON and Q_3 is always OFF and Q_1 and Q_2 are switching to generate positive and zero states. Also Q_2 can achieve natural ZVS by i_L while Q_1 achieves ZVT by S_1.

Fig. 2 shows the timing of the proposed bus clamping modulation with ZVT scheme. Fig. 3 shows commutation stages corresponding to the timing in Fig. 2.

(a) Initial stage [before t_1]. Q_2 is ON, the main inductor current i_L flows through Q_2

(b) Pre-charging stage [t_1~t_2]. S_1 is turned-on at t_1, the buck output voltage V_b is applied to the resonant inductor L_{aux}, i_{aux1} increases linearly, current in Q_2 decreases to zero at t_2.

(c) Boost-charging stage [t_2~t_3]. I_{aux1} is linearly charged to a current well above the inductor current i_L. This will make sure $V_{ds,Q1}$ (the drain to source voltage of the Q_1 switch) resonates to zero in resonant stage t_3~t_4.

(d) Resonant stage [t_3~t_4]. Q_2 is turned-off at t_3, L_{aux} starts to resonant with C_{ds1} and C_{ds2} until $V_{ds,Q1}$ resonates to zero.

(e) Clamping stage [t_4~t_5]. When $V_{ds,Q1}$ resonates to zero, D_1 (the body diode of the switch Q_1) naturally turns-on at t_4. The voltage of $-(V_{dc}-V_b)$ is applied to L_{aux}, i_{aux1} decreases. During this stage, $V_{ds,Q1}$ is clamped to 0 until t_5, Q_1 can be ZVS turned-on in this stage.

(f) Discharging stage [t_5~t_6]. I_{aux1} is discharged to zero, current in Q_1 linearly increases to i_L. S_1 can be ZCS turned-off before t_7.

(g) Steady-state stage [t_6~t_7]. Q_1 fully conducts the load current i_L.

(h) Snubber turn-off stage [t_7~t_8]. Q_1 is turned-off at t_7, i_L linearly charges C_{ds1} and discharges C_{ds2} until $V_{ds,Q1}$ reaches V_{dc}, dv/dt is limited by C_{ds1} and C_{ds2}, due to the extra C_{ds} added to the main switches, turn-off loss of Q_1 is reduced.

(i) Steady-state stage [after t_8]. When $V_{ds,Q2}$ reaches to zero, D_2 is naturally turned-on, and then Q_2 can be ZVS turned-on after t_8 resulting in natural ZVS of Q_2.

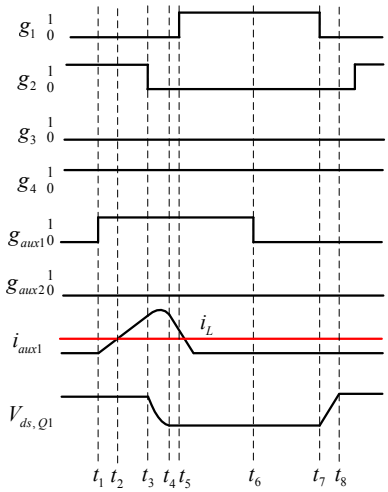


Fig. 2 Timing diagram of proposed ZVT with bus clamping modulation

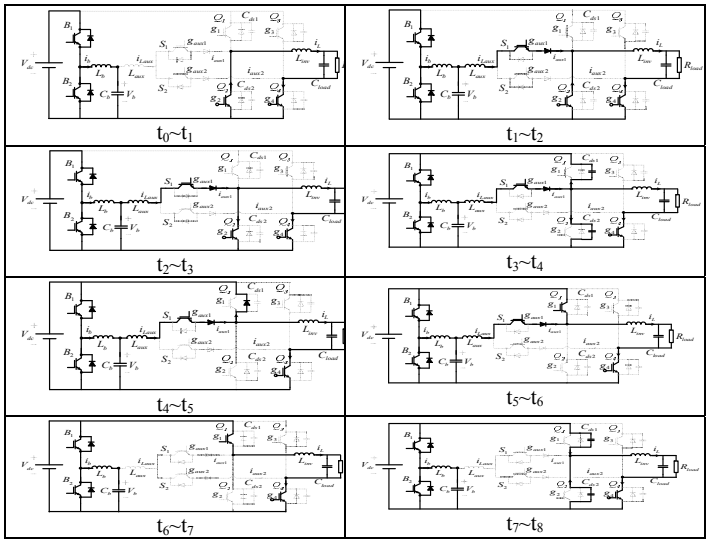


Fig. 3 Commutation stages of the proposed inverter

III. HARDWARE IMPLEMENTATION AND RESULTS

A 1kW full bridge inverter with LC filter and resistive load operating at 500 kHz switching frequency has been built to verify the proposed ZVT with bus clamping modulation technique. The power factor is 1 and the modulation ratio is 0.85 which represents a typical PV standalone application. The specifications of the inverter, the ZVT auxiliary circuit and details of switches are shown in Table II, Table III and Table IV respectively.

The blanking time which is the deadband between the gate signals of the upper switch and the lower switch (which equals to $t_5 - t_3$ in Fig. 2) is set to 90 ns. The ahead time, which is the time between the auxiliary switch gate signal and the lower switch gate signal (which is $t_3 - t_1$ in Fig. 2), is set to 210 ns in the fixed timing scheme. In the variable timing scheme, the ahead time will change with the inductor current value to further decrease the loss in the auxiliary circuit. External capacitor of 220 pF is put in parallel with C_{ds} of the main switches of the full bridge to decrease the turn-off loss of the main switches while maintaining the ZVS turn-on. The timing and auxiliary inductance, the buck output voltage are designed based on loss calculation and optimization.

SiC MOSFETS from CREE are used in full bridge main circuit, buck stage and auxiliary ZVT circuits. The driver ICs are chosen as Avago ACPL 337J. The positive gate voltage of the MOSFET (V_{gs}) is 20 V and the negative is -5V. In order to reduce the diode recovery loss, 4 SiC schottky diodes are put in parallel to the 4 main switches. LeCroy 6200A oscilloscope is used to capture waveforms. Power analyzer YOKOGAWA WT3000 is used to measure the input power at dc terminal and output power at load terminal to calculate efficiency. Ferrite core with Litz wire are used for the main output inductor.

TABLE II. MAIN CIRCUIT SPECIFICATIONS

Power	1 kW
Dc input voltage	230 V
Load voltage	140 V
Load current	8.3 A
Resistive load	17.2 Ω
Power factor	1
Switching frequency	500 kHz

TABLE III. AUXILIARY AND BUCK CIRCUIT SPECIFICATIONS

Auxiliary inductance	270 nH
Blanking time	90 ns
Ahead time	210 ns
Buck switching frequency	50 kHz
Buck inductance	260 uH
Buck output capacitance	800 nF
Buck output voltage	50 V

TABLE IV. SWITCH DETAILS

Full bridge and buck	Type	SiC MOSFET
	Manufacturer	CREE
	Part no.	C2M0080120D
	C_{ds}	73 pF
Auxiliary circuit	Type	SiC MOSFET
	Manufacturer	CREE
	Part no.	C2M0160120D
	C_{ds}	43 pF

Fig. 4 shows the full bridge power board, the buck and ZVT auxiliary board and ezDSP28335 control board.

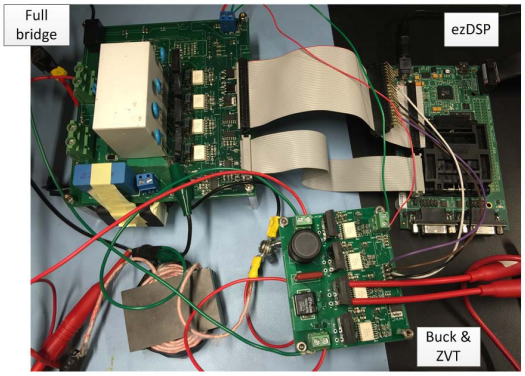


Fig. 4 H bridge, buck and ZVT board and eZDSP

Fig. 5 shows the bus clamping modulation scheme and ZVT gate signals along with the inductor current for reference. Fig. 6 shows the zoomed gate signals of the full bridge switches and the ZVT auxiliary switch. As the power factor is 1 which means the polarity of the duty ratio is almost equal to the polarity of the inductor current, the modulation strategy is easier to implement compared to other power factors though the scheme is capable of supporting other power factors as well.

It can be seen from Fig. 5 and Fig. 6 that when the inductor current is positive, for the 4 switches in the full bridge inverter, only Q_1 and Q_2 are switching while Q_4 is always ON and Q_3 is always OFF which means the midpoint of the second leg is bus clamped to the negative bus. In order to achieve ZVT for the Q_1, the auxiliary switch S_1 is switched each time before Q_1 is turned-on. While in the negative part of the inductor current, Q_2 is always ON and Q_1 is always OFF, only Q_3 and Q_4 are switching. Fig. 6 also shows that the switching frequency is 500 kHz.

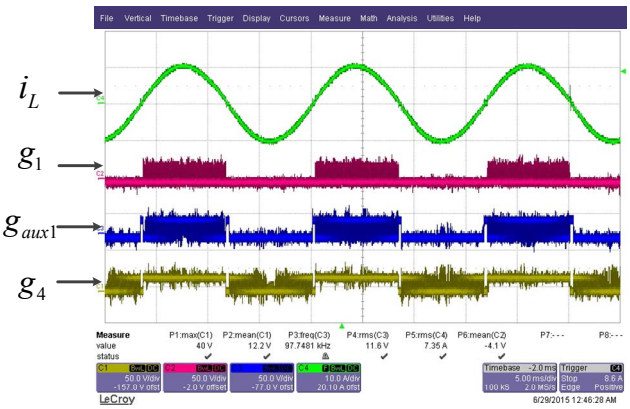


Fig. 5 ZVT with bus clamping modulation (time scale 5 ms/div, i_L scale 10 A/div, g_1, g_{aux1}, g_4 scale 50 V/div)

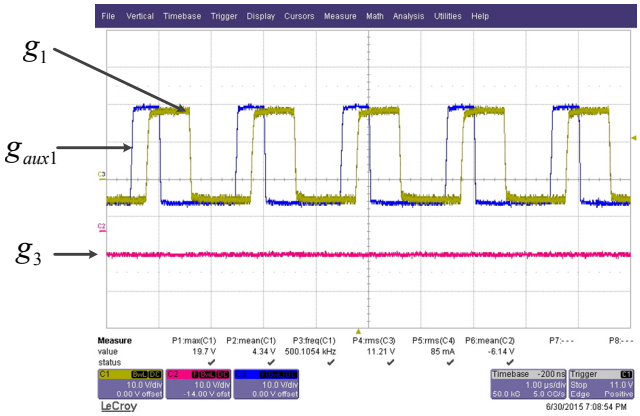


Fig. 6 Zoomed gate signal of ZVT with bus clamping modulation when inductor current is positive (time scale 1 us/div, g_1, g_{aux1}, g_3 scale 10 V/div)

Fig. 7 shows the fixed timing scheme of the ZVT where the blanking time is 90 ns and the ahead time is 210 ns. The adaptive timing method [25] is also implemented which means the ahead time changes with the inductor current adaptively to further decrease the loss in the auxiliary ZVT circuit.

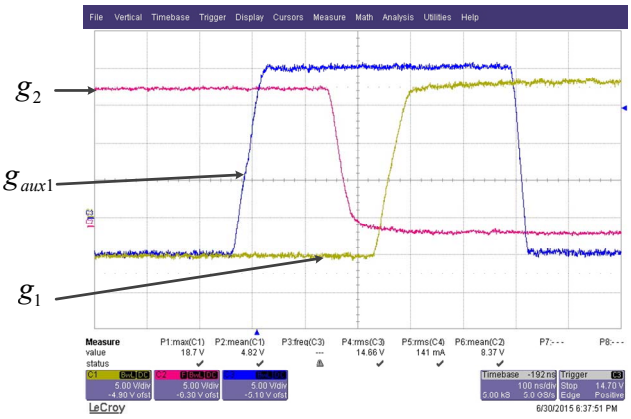


Fig. 7 ZVT timing with blanking time of 90 ns and ahead time of 210 ns (time scale 100 ns/div, g_2, g_{aux1}, g_1 scale 5 V/div)

Fig. 8 shows the waveforms of the ZVT process of the main switch Q_1 which include the drain to source voltage of the Q_1 switch ($V_{ds,Q1}$), the gate to source voltage of the Q_1 switch (g_1), the inductor current (i_L) and the auxiliary inductor current (i_{aux1}). It can be seen that the auxiliary inductor current is larger than the value of the inductor current for some time which means it can discharge the drain to source capacitance of the Q_1 switch (C_{ds1}) as analyzed in the Section II commutation stages part to achieve ZVT of Q_1. The drain to source voltage of the Q_1 switch has already fallen to 0 before the gate signal is applied proving that Q_1 realizes soft turn-on.

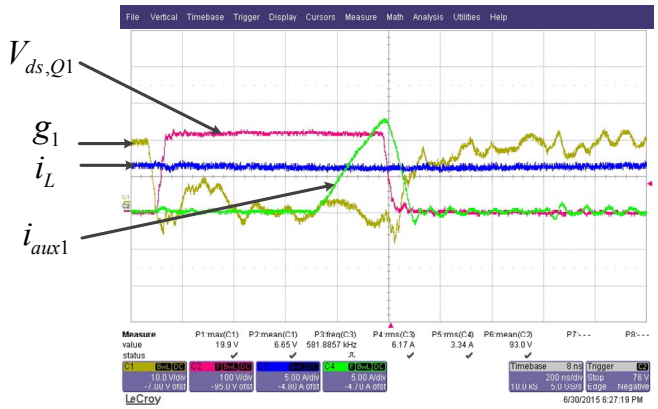


Fig. 8 ZVS of main switch (time scale 200 ns/div, $V_{ds,Q1}$ scale 100 V/div, g_1 scale 10 V/div, i_L scale 5 A/div, i_{aux1} scale 5 A/div)

Fig. 9 shows the measured loss using power analyzer YOKOGAWA WT3000 at different power levels for three different cases – base case (no ZVT), proposed ZVT with fixed timing and proposed ZVT with adaptive timing. It can be seen that the proposed ZVT can improve the system overall efficiency significantly.

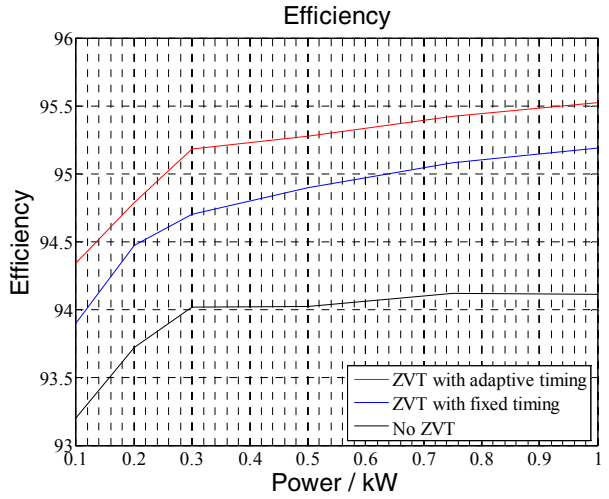


Fig. 9 Loss of full bridge without ZVT, with fixed timing ZVT and with adaptive timing ZVT proposed

The independent loss that cannot be changed by ZVT includes the switch conduction loss and inductor loss. The conduction loss of the main 4 switches which is same in all the above three schemes are calculated using $P_{con} = 2I^2R_{ds,on}{}^2 = 11.3$ W. The inductor loss is estimated to be 3 W. The core loss and copper loss are small because ferrite core with Litz wire are used and the switch frequency is high enough which results in the max current ripple of 0.2 A pk-zero.

Table V shows the calculation of the loss saving in the experimental prototype at 1 kW and 500 kHz switching frequency in which the conduction loss of the switches and inductor loss are subtracted from the total loss to obtain the rest loss for each scheme. The full bridge switching loss without ZVT is 48.3 W. The full bridge switching loss and ZVT auxiliary circuit and buck stage total loss is 36.3 W with the fixed timing ZVT and 32.6 W with the adaptive timing ZVT. After subtracting the independent loss, the fixed timing ZVT saves up to 25 % while the adaptive timing ZVT saves up to 33 % of the original switching loss of the full bridge inverter.

TABLE V. LOSS ANALYSIS IN HARDWARE PROTOTYPE

	No ZVT	**Fixed timing ZVT**	**Adaptive timing ZVT**
Total measured loss	62.6 W	50.6 W	46.9 W
Estimated conduction loss and inductor loss	11.3 W + 3 W = 14.3 W		
Switching losses and loss in ZVT circuits	48.3 W (Full bridge switching loss)	36.3 W (Full bridge switching loss & ZVT circuit & buck loss)	32.6 W (Full bridge switching loss & ZVT circuit & buck loss)
Reduction in the original switching loss	/	25 %	33 %

IV. CONCLUSION

This paper proposes a topology based on bus clamping modulation and zero voltage transition (ZVT) method to achieve zero voltage switching (ZVS) for all the main switches of the full bridge inverter. The turn-on loss of the ZVT auxiliary switches which typically is a major part of the total loss in other ZVT circuits is reduced by this strategy. The voltage rating can also be reduced which can decrease volume and cost of the auxiliary circuit. The modulation scheme under different power factor conditions and the commutation stages of the ZVT realization are analyzed in detail. A 1 kW, 500 kHz switching frequency inverter using the proposed topology and SiC MOSFETs has been built to validate the theoretical analysis. The bus clamping modulation and ZVT fixed timing and adaptive timing schemes are implemented resulting in full ZVS for the main switches in the full bridge inverter. The proposed scheme is shown in experiments to save up to 33 % of the switching loss compared with no ZVT case.

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