RADIATION HARDENED ELECTRONICS DESTINED FOR SEVERE NUCLEAR REACTOR ENVIRONMENTS

Keith E. Holbert
Lawrence T. Clark

School of Electrical, Computer and Energy Engineering
Arizona State University
Tempe, AZ 85287-5706

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EXECUTIVE SUMMARY

Post nuclear accident conditions represent a harsh environment for electronics. The full station blackout experience at Fukushima shows the necessity for emergency sensing capabilities in a radiation-enhanced environment. This NEET (Nuclear Energy Enabling Technologies) research project developed radiation hardened by design (RHBD) electronics using commercially available technology that employs commercial off-the-shelf (COTS) devices and present generation circuit fabrication techniques to improve the total ionizing dose (TID) hardness of electronics. Such technology not only has applicability to severe accident conditions but also to facilities throughout the nuclear fuel cycle in which radiation tolerance is required. For example, with TID tolerance to megarads of dose, electronics could be deployed for long-term monitoring, inspection and decontamination missions.

The present work has taken a two-pronged approach, specifically, development of both board and application-specific integrated circuit (ASIC) level RHBD techniques. The former path has focused on TID testing of representative microcontroller ICs with embedded flash (eFlash) memory, as well as standalone flash devices that utilize the same fabrication technologies. The standalone flash devices are less complicated, allowing better understanding of the TID response of the crucial circuits. Our TID experiments utilize biased components that are in-situ tested, and in full operation during irradiation. A potential pitfall in the qualification of memory circuits is the lack of rigorous testing of the possible memory states. For this reason, we employ test patterns that include all ones, all zeros, a checkerboard of zeros and ones, an inverse checkerboard, and random data. With experimental evidence of improved radiation response for unbiased versus biased conditions, a demonstration-level board using the COTS devices was constructed. Through a combination of redundancy and power gating, the demonstration board exhibits radiation resilience to over 200 krad. Furthermore, our ASIC microprocessor using RHBD techniques was shown to be fully functional after an exposure of 2.5 Mrad whereas the COTS microcontroller units failed catastrophically at <100 krad.

The methods developed in this work can facilitate the long-term viability of radiation-hard robotic systems, thereby avoiding obsolescence issues. As a case in point, the nuclear industry with its low purchasing power does not drive the semiconductor industry strategic plans, and the rapid advancements in electronics technology can leave legacy systems stranded.

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1. INTRODUCTION

The post nuclear accident conditions represent a harsh environment for electronics. Three Mile Island, Chernobyl, and Fukushima Daiichi show the necessity for emergency sensing capabilities in a radiation-enhanced environment. Each proved dangerous to workers trying to assess, control and mitigate the accidents. Robots were used in each case with limited success. Consequently, research into methods to extend the life of robots in a high radiation environment has become a priority. Robotic systems can be utilized to inspect, repair, and monitor facilities within the entire nuclear fuel cycle.

This project has developed radiation hard by design (RHBD) electronics using commercially available technology employing commercial off-the-shelf (COTS) devices and present generation circuit fabrication techniques. Such technology not only has applicability to severe accident conditions but also to facilities throughout the nuclear fuel cycle in which radiation tolerance is required. Furthermore, the methods developed in this work will facilitate the long-term viability of such radiation-hard electronic systems, thereby avoiding obsolescence issues being experienced in the nuclear power industry.

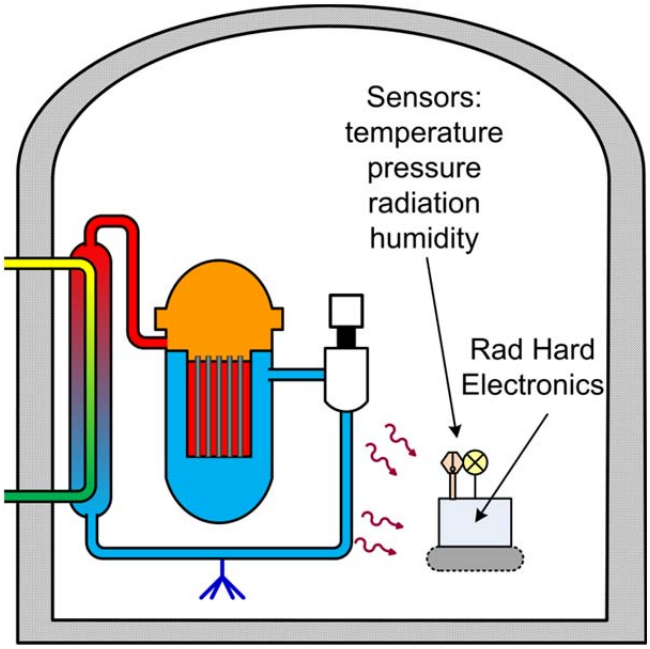


Figure 1. Depiction of a radiation hard robot for in-containment reconnaissance.

During nuclear reactor accidents, the containment building may present extreme conditions in terms of temperature, humidity and radiation, but nonetheless an environment in which electronic sensor and robotic systems must be operable. A goal of this project was to increase the radiation resilience of the more sensitive electronics such that a robot could be employed for post-accident monitoring and sensing purposes, as depicted in Figure 1, as well as for long-term inspection and decontamination missions. This two-year project has developed both board and

application-specific integrated circuit (IC) level RHBD techniques for circuits destined for severe nuclear environments, specifically those that are vital to robotic circuits. In particular, the proposed project has focused on using redundancy to achieve total ionizing dose (TID) hardness by interleaving active and recovery times for individual IC or constituent circuits.

Earlier approaches to radiation hardening ICs involved brute force techniques such as radiation shielding and use of ICs fabricated on specialized hardened processes. The limited availability and high cost of such rad-hard ICs and the reduced radiation sensitivity of advanced commercial ICs (due to process scaling) can allow use of commercial off-the-shelf (COTS) devices, after radiation testing and qualification. Application-specific IC (ASIC) efforts using radiation hardening by design (RHBD) techniques can be applied to advanced commercially available fabrication processes, at increased cost. In the present work, both board and ASIC level RHBD techniques were developed for circuits destined for severe nuclear environments, specifically those that are vital to robotic circuits.

This project was dedicated to fulfilling DOE's Nuclear Energy Enabling Technologies (NEET-2) request for "Design of a custom radiation tolerant electronics system, using the best available commercial or near-commercial technologies necessary for operation in a severe nuclear environment. The proposed system should provide observable evidence that the technology is capable of being implemented in a radiation-tolerant multi-functional robot for in-containment reconnaissance under severe accident conditions."

Chapter 2 provides brief reviews TID effects on electronics and the reactor containment radiation environment. Chapter 3 details the accomplishments in this project. Chapter 4 concludes.

2. BACKGROUND

2.1 Total Ionizing Dose Effects on Electronics

The use of electronics has become pervasive in modern society, as seen in devices ranging from musical greeting cards to cellular telephones. In contrast, the nuclear power industry has been slow to adopt electronic systems due to qualification requirements including threats from harsh ionizing radiation. Instead, sensor electronics or the transmitters themselves are generally sited away from the nuclear steam supply system. Advanced instrumentation can benefit significantly from radiation hard electronics. Consider the deployment of fiber optics and onboard instrument diagnostics for next generation sensor networks.

Ionizing radiation has the potential to degrade the performance of integrated circuits (ICs) through total ionizing dose (TID), single event effects (SEEs), and displacement damage. The latter mechanism occurs when an incident particle displaces an atom from its lattice position thereby creating a defect — categorized as non-ionizing damage. In terms of ionization effects, TID degradation is a cumulative long-term effect manifesting, for example, as device voltage threshold shifts and leakage current. A SEE happens when a single particle deposits sufficient charge to cause circuit upsets such as a bit flip or transient pulse. As an analogy using an automobile tire, TID damage may be likened to tread wear while SEE equates to a nail puncture. While TID radiation hardness is typically expressed in krad, the SEE sensitivity is measured in terms of a cross section with units such as cm^2 per bit.

Radiation tolerant electronics have been a forte of the aerospace and defense industries. Satellite electronics are exposed mostly to charged particles (electrons and protons) whereas the ex-core environment is comprised of penetrating neutral radiations (neutrons and gamma rays). Originally, brute force use of shielding was employed to reduce dose. Later, specialized semiconductor manufacturing processes were developed to fabricate radiation-hard ICs. The limited availability and high cost of radiation-hard ICs and the reduced radiation sensitivity of advanced commercial ICs can allow use of commercial off-the-shelf (COTS) devices, after radiation testing and qualification. Today's state-of-the-art approach is radiation hardening by design (RHBD), which employs circuit design techniques that mitigate the impact of ionizing radiation. Unfortunately, modern computer-aided circuit design tools have a tendency to exacerbate some radiation effects. For instance, the automatic place and route tool optimizes device siting but can locate related devices in such close proximity that multiple bits in a single word can be flipped such that error detection and correction codes (EDAC) are rendered useless.

Moore's law from the semiconductor industry states that IC transistor density doubles every two years. With this downscaling of device size, TID susceptibility has continued to decrease; conversely, SEE vulnerability has increased. TID resilience has increased because the thinner insulating oxides (e.g., SiO_2) accumulate less trapped charge than their thicker counterparts do. However, the smaller device sizes and lower operating voltages have decreased the critical charge needed for an ionizing particle to upset a circuit node.

Total ionizing dose (TID) effects are produced when ionizing radiation passing through an IC creates electron-hole pairs within the oxides. Modern sub-5 nm gate oxides allow both holes and electrons to escape the gate oxide before being trapped. Consequently, the isolation oxides, i.e., shallow trench isolation (STI), are the most vulnerable to TID effects in modern microcircuits.

In oxides, some electron-hole pairs recombine, depending on the electric field, which tends to drive the charge carriers apart. Electrons are more mobile, so they are likely to be swept out of the oxide leaving holes as trapped charge, lowering the transistor (and field isolation) threshold voltage (V_T).

While PMOS transistors are affected, it is generally not deleterious, as their parasitic devices experience a lower absolute V_T, which increases the V_T magnitude (more negative) and hence reduces leakage. There are two primary leakage paths induced by TID. NMOS transistor drain-to-source leakage is produced by a V_T reduction at the transistor edges, i.e., the interface between the thin and thick oxides. Leakage paths are also created under the STI between diffusion areas, i.e., between NMOS sources or drains at different biases or from an NMOS source/drain diffusion to the N type well. While we have developed TID hard libraries that exceed 1 Mrad hardness with minimal leakage increase, this work is focusing on mitigation techniques that are also applicable to COTS rather than hardened devices, thus allowing the widest range of devices to be used in robots aimed at nuclear accident monitoring, as well as inspection and remediation work.

TID induced leakage is extremely sensitive to the applied biases during irradiation. Measurements of old processes, e.g., with gate oxides over 45-nm thick (and presumably lower quality than on modern devices), showed significant TID effects for devices biased off as well as those biased on [15], [16]. These oxides were susceptible to "rebound", whereby positive V_T shifts occurred when alternating biases were applied, due to generation of oxide interface states and trapped hole annealing. Our own experiments on modern 130-nm and 90-nm processes (with 3.5-nm and 2.5-nm gate oxides, respectively) showed strong voltage sensitivity. Note however, that many of the interesting microcontroller components are fabricated with gate oxides thicker than this, i.e., in the greater than 5-nm range (up to 12-nm).

Studies of the radiation sensitivity of electronic components in robots have shown the expected large range of hardness, varying from less than 10 krad to multi-Mrad levels. EEPROM non-volatile (NV) memory hardness ranged from 3 to 10 krad, as did microcontrollers that presumably contain such memories. The latter are key components in robotic subsystems—they are pervasive in control circuits such as motor controllers. Research has shown that more modern flash memories also suffer from very low TID hardness. The key issue for all such memories is the relatively thick oxides required for retention time. This thickness presents scaling issues, driving the industry to NAND flash from the previously dominant NOR. The former is denser, but slower, which is less desirable in a microcontroller. However, as less than one electron can escape the cell each month to maintain data over the intended lifetime, the NAND stack permits lower drain electric fields, reducing leakage due to hot-electron effects (although NAND does require higher programming voltages) [3]. One widely assumed and cited primary circuit affecting NV memory TID hardness is leakage-induced failure of the charge pumps, although other leakage paths may contribute. Consequently, lower required voltages on those circuits are likely to be beneficial.

Embedded flash (eFlash) non-volatile memory modules generally do not use the same floating gate technologies as large capacity stand-alone flash ICs, which use expensive and specialized technologies that include buried source topologies, etc. Logic compatible eFlash is generally implemented using one of two technologies, e.g., the 1.5 transistor (1.5-T) [1] (such as the SST SuperFlash or a derivative), or the 1 or 2 transistor silicon-oxide, nitride, oxide, silicon (SONOS) charge trapping gate stack type cell [2]. The work here is centering on the former, based on our

access to the requisite IP and its easy availability in suitable microcontrollers. Both read with relatively low voltages (charge pumps are used only during erasure and programming) which should enhance hardness. However, since the primary flash memory TID weakness has consistently been the charge pump [3] [4], which is common to all the schemes, we believe the results will be readily extensible to other non-volatile memory architectures. Previous work has shown that for high-density flash devices tested in read mode, failure could occur as early as 10 to 20 krad(Si) depending on the device [3] but the effects could be delayed by 4 to 5 times when irradiating in an unbiased mode.

The prior work on stand-alone flash ICs, as well as TID testing on general devices has shown a large improvement in lifetime when irradiation occurs without bias. Consequently, by developing system and IC approaches that use redundancy and power-down operation of blocks and constituent devices, this work could dramatically extend the lifetime of such devices in TID environments. By interleaving power up and power down (recovery) cycles, we demonstrate significantly improved TID lifetime at both the board and ASIC die level. We have also more accurately determine the specific TID induced circuit failure mechanisms that must be dealt with in such systems.

2.2 Reactor Containment Radiation Environment

During nuclear reactor accidents, the containment building may present extreme conditions in terms of temperature, humidity and radiation, but an environment in which electronic sensor and robotic systems must be operable. As a case in point, failure was experienced with sophisticated robotics after Chernobyl [5]. While neutrons can cause SEEs [6] [7], the more important mechanism within the post-accident environment is TID from beta and gamma ray emissions, although a criticality accident (e.g., Tokaimura, Japan, Sept. 1999) can produce significant neutron flux. In fact, Tokaimura was the impetus in the early 2000s for developing a "radiation-proof robot," as shown in Figure 2, to operate to 10 Mrad at 1 krad/h (no neutron dose survivability specified) [8]. Remote inspection after the accident at Three Mile Island recorded radiation fields as high as 3 krad/h in containment [9]. Representative post-Fukushima Daiichi conditions as measured by a PackBot robot in April 2011 include temperatures up to 41 °C, humidity of 94% to 99%, and radiation levels of 1 to 5.7 rad/h in the unit 1 and 3 reactor buildings. A Quince robot recorded a higher reading of 25 rad/h at the lip of the unit 2 containment vessel; the Quince had been radiation tested to only 20 krad [10]. Since then, Toshiba, Mitsubishi and Hitachi have been developing robots for post-accident cleanup. The radiation tolerance of the Toshiba Tetrapod is quoted as 10 rad/h for a year (a TID of ~ 90 krad).

An issue experienced post-Fukushima was that some of the robots developed after Tokaimura had not been kept ready for utilization [11]. To overcome this, nuclear power plants could be outfitted with a robot for in-containment reconnaissance prior to any incident, serving in a standby mode either already within the containment building or outside awaiting deployment during an incident. With either approach, the instrumentation can be periodically queried to assure system operability, with the former approach, a disadvantage being long-term radiation exposure and the concomitant electronics degradation. For normal operating conditions, the annual gamma dose to instrumentation within containment has been estimated as < 2.5 Mrad between the primary and secondary shields, and < 25 krad outside the secondary shield with a nominal dose of 750 rad/y [12]; the annual neutron fluence was $< 7.5\times10^{12}$ n/cm^2 outside the secondary shield. As others have stated, the electronic components are more radiation sensitive than the sensors [5]. Prior research and experience [13] have found that worst-case post-

irradiation response varies with device voltage bias, operating frequency [14] [15], and also by technology, circuit type, and architecture [16]. With these factors in mind, one goal of this project is to increase the radiation resilience of the more sensitive electronics such that a robot could be installed in the containment building awaiting initiation instructions, since the robot circuit conditions during standby will differ from the value during operation.

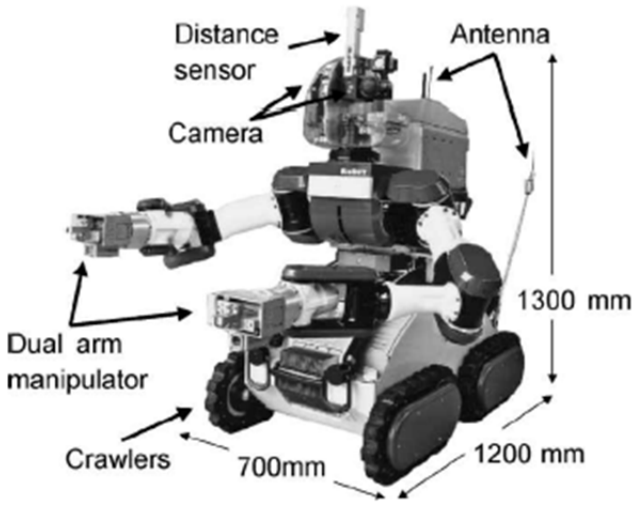


Figure 2. Japan's RaBOT [8].

In 1977, Sejvar of Westinghouse published a set of normal operating radiation exposure rates in pressurized water reactors (PWRs) [17]. Some of those data are replicated in Table 1, for the in-containment locations annotated in Figure 3. Note that 1 Roentgen (R) is equivalent to 0.877 rad(air) and 8.77 mGy. In 1983-1984, Johnson et al. provided cumulative gamma dose and neutron fluence expected within nuclear plant containments for both normal operation and accident conditions [18], see Table 2. These tabulations show that post-accident reactor containment doses could be on the order of Mrad, while present robotic circuits mentioned above are rated to <100 krad. As will be shown in the next chapter, this project successfully demonstrated microprocessor operation to the Mrad level and embedded flash memory to greater than 100 krad.

The siting of a robot within containment awaiting deployment leads to two conditions of interest: (1) the standby condition in which circuits are unbiased, and (2) the in-service state in which devices are powered. As TID damage varies according to the voltage bias, the radiation resilience must be evaluated for all cases in order to develop a proper mitigation strategy, while permitting the robot status to be queried regularly.

Table 1. Radiation Levels Inside a PWR Containment [17]

Location		Dose Rate		
Point Number	Description	Power Operation		Shutdown
		Gamma Ray (R/h)	Neutron (rem/h)	Gamma Ray (R/h)
1	Reactor vessel-primary shield annulus	1×10^4 §	3×10^5 § ($\sim 3 \times 10^4$ rad/h)	9–12
2	Reactor coolant loop area General area Contact with piping	 50 200	 0.2 —	 0.01–0.2 † 0.02–0.2
3	Outside the loop area	0.005–0.2	0.005–0.2	0.0002–0.002
4	Above the operating deck	0.005–0.05‡	0.01–0.3‡	0.0002–0.002

§ calculated values; † local levels of up to 60 R/h;
‡ local levels of up to 0.2 R/h of gamma rays and 3 rem/h of neutrons.

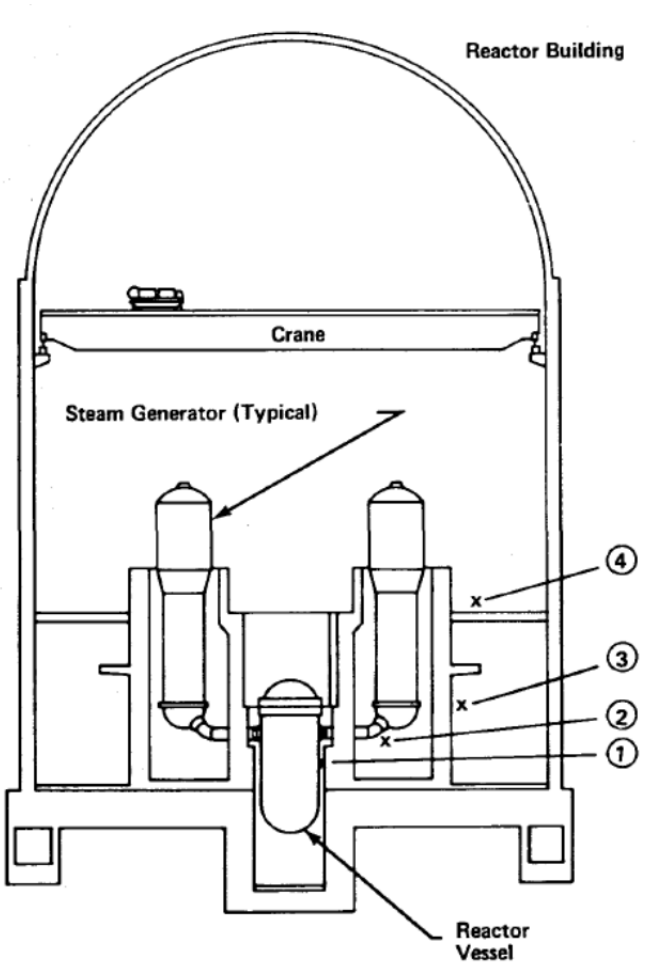


Figure 3. PWR containment building [17].

Table 2. Typical Environment in Nuclear Plant Containment Area [12], [18], [19]

Environment	Nuclear Plant Containment	
	Normal Operation (40 yr plant life)	Accident
Gamma dose, rad Gamma dose rate, rad/h	$10^3 – 10^8$ $10^{-3} – 10^2$	2×10^7 $< 10^6$
Neutron fluence, n/cm^2 Neutron flux, n/(cm^2·s)	$10^9 – 10^{14}$ $1 – 10^5$	–
Electron dose, rad	–	2×10^8
Temperature, °C	24 – 66	260
Humidity, % RH at 20°C	10 – 100	100

3. ACCOMPLISHMENTS

The project was comprised of three distinct phases, but with overlapping timeframes:

I. Microcontroller TID and elevated-temperature testing (Year 1);

II. Board level demonstration (Year 2); and

III. ASIC design (Year 1) and characterization (Year 2).

Phase I focused on in-situ TID testing of representative microcontroller ICs with embedded flash (and of course charge pumps). In our testing, we use external control and supply monitoring of devices inside a ^{60}Co irradiator (Gammacell), so the devices are in actual operation during irradiation, and device status, e.g., function and supply currents, are recorded continuously.

Phase II was practical application and proof of the Phase I results. In Year 2, we constructed a board level demonstrator that significantly improves TID lifetime using redundancy and switched supply voltages. This was accomplished with minimal external electronics, minimizing this cost and risk to hardness of the added components. This is the COTS approach, with rapid applicability to robots and other reactor environment electronics.

Phase III investigated integral power gating on ASIC devices with embedded flash. This work was facilitated by our access to the Silicon Storage Technology (SST) / Microchip embedded flash IP, which was fabricated in a 90-nm process at TSMC (Taiwan Semiconductor Manufacturing Company). Microchip Technology Inc. allowed our research designs to be fabricated on their corporate shuttle runs at TSMC, which enabled such designs at minimal budget. The test chip design incorporates power gating to the NV memory blocks to determine applicable power redundancy approaches at the on-chip level. The test chip also allowed us access to alter the programming voltages and duration. If cell data retention turns out to be a significant factor, this will enable investigation of relatively simple schemes to improve NV memory data lifetime in TID environments. Finally, use of on-die power gating is also of interest since many state-of-the-art devices incorporate power regulation and gating, which may permit pure COTS approaches as well.

The three phases of the two-year project were divided into four tasks, according to the overall project schedule given in Figure 4. The bulk of this chapter is organized according to the four tasks but with Tasks 1 and 3 results reported first. The four tasks are

1. Total ionizing dose (TID) and elevated-temperature in-situ testing of COTS microcontroller electronics with embedded flash memory;
2. ASIC (application-specific integrated circuit) design and fabrication;
3. Board-level demonstration of the COTS approach; and
4. ASIC characterization.

Besides this final report, project results have been disseminated to date at the American Nuclear Society (ANS) Nuclear Plant Instrumentation, Control & Human-Machine Interface Technologies (NPIC&HMIT) conference [20], the IEEE Nuclear and Space Radiation Effects Conference (NSREC) [21], and within the *IEEE Transactions on Nuclear Science* [22]. In addition, a provisional patent application has been filed [23].

Task	*Project Quarter*							
	Jan–Mar	Apr–June	July–Sept	Oct–Dec	Jan–Mar	Apr–June	July–Sept	Oct–Dec
1. Microcontroller TID and Elevated-Temperature Testing								
2. ASIC Design								
3. Board Level Demonstration								
4. ASIC Characterization								
5. Reporting and Dissemination								

Figure 4. Project Gantt chart.

3.1 Task 1: Testing of COTS Devices

With a variety of scientific literature indicating that the non-volatile memory and specifically the charge pump represent a significant radiation vulnerability, an a priori decision was made to dedicate the initial project efforts to evaluating the COTS flash memory.

Pursuant to the project proposal, the microcontroller TID and elevated-temperature testing focused on SST SuperFlash technology based on our access to the requisite IP and its ready availability in suitable microcontrollers. While there is substantial literature on flash memory TID response, this work focuses for the first time on 1.5 transistor per cell flash memory. We chose to study these memories due to their excellent commercial environment reliability, lower operating voltages, and efficient program and erase physics, believing that these characteristics might also manifest as greater TID hardness. The SuperFlash memories do not require iterative programming, which mandates an embedded controller, or extensive error detection and correction (EDAC) for reliable operation, as many NAND flash memories do. The latter characteristics also afford better visibility into the actual cell level behavior, despite our inability to use test modes that can measure individual cell thresholds. Finally, the SuperFlash 1.5-T cells are available as embedded intellectual property (IP) from a number of foundries, and thus may be used in radiation hardened application-specific integrated circuits (ASICs).

3.1.1 Elevated Temperature Testing

To partially assess the performance of the electronics in the post-accident environment, the microcontroller and its flash memory were subjected to elevated-temperature testing. A temperature sensor with pressure sensitive adhesive (PSA) was attached directly to the sensitive electronic device, as shown in Figure 5, and a resistive Thermofoil™ heating element with PSA was sited on the backside of the board opposite the device. Next, a layer of silicone insulating material was placed on both the front and back sides and clamped into place as exhibited in Figure 6. Although the red silicone insulation is rated to 260 °C (500 °F), the PSA is rated to only 150 °C thus motivating the use of the clamp. To ensure temperature stability during the measurements, the assembly was then wrapped in an additional overall silicone insulating blanket, as pictured in Figure 7. An off-the-shelf PID controller was programmed to permit increasing the temperature of the system gradually. According to the manufacturer data [24], the flash memory module has an operating temperature range of 0 °C to +70 °C and an absolute

maximum temperature range under bias of –55 °C to +125 °C to avoid causing permanent damage in the device. The resistive heater itself can achieve 200 °C.

Figure 5. The temperature sensor (an RTD) is directly in contact with the flash memory module on the front side of the board. The two red wires to the resistive heater on the backside of the board can be seen to the right.

The key rationale for high temperature testing is that high temperature increases transistor leakage precisely as TID does (albeit by different mechanisms). Thus, comparing TID and high temperature behavior allows us to at least correlate failures to be like or dislike each other. This is important since we do not have the ability to probe inside the flash blocks and therefore have to infer the precise failure mechanisms.

Leakage failures should produce bit failures in only one direction, and tend to affect whole bit-lines. Consequently, seeing this same symptom on TID and high temperature testing would give insight.

Moreover, reactor environments may be quite hot (Table 2) making understanding of high temperature operation interesting in and of itself.

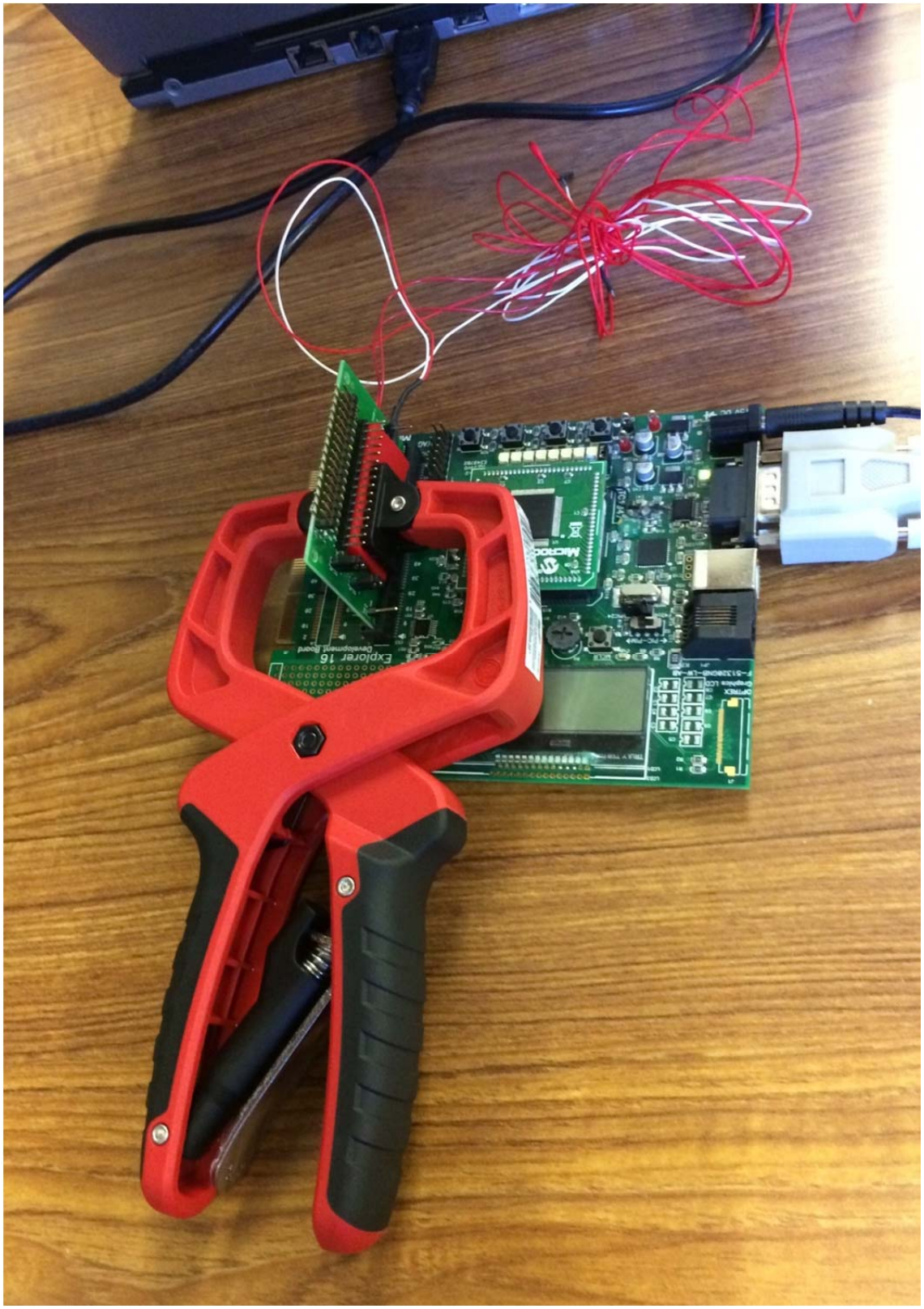


Figure 6. Front and back sides of the flash memory board to be heated are covered with (red) insulating silicone and clamped.

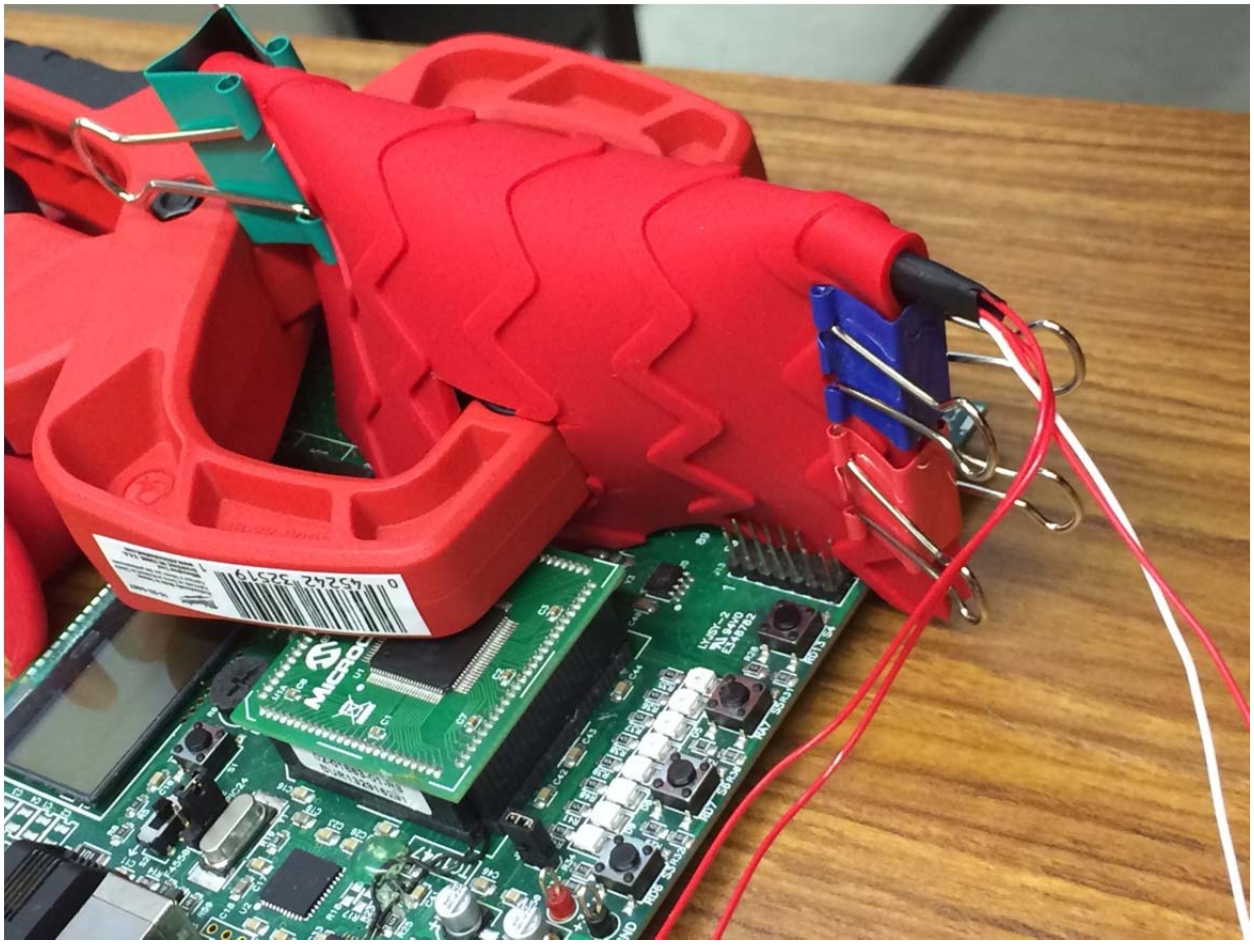


Figure 7. Final configuration of insulated flash memory board ready for heating.

Nine elevated temperature experiments were carried out, as summarized in Appendix A. Data were sampled at pre-established temperature plateaus separated by 5 °C beginning at 110 °C. Four of the 64 Mbits of the flash memory card were exercised with at least three tests of four different test patterns at each temperature step stress:

- 0x0 (0b 0000 0000 0000 0000) [all zeros];
- 0x5 (0b 0101 0101 0101 0101) [checkerboard];
- 0xA (0b 1010 1010 1010 1010) [inverse checkerboard]; and
- 0xF (0b 1111 1111 1111 1111) [all ones].

Accordingly, this SuperFlash utilizes 16-bit words. During each test, the memory was first programmed (required ~ 2 min) and then the memory read (required ~ 4 min). All bits of the 4 Mbit memory were monitored for errors and the direction of the error, that is, 0 to 1 and 1 to 0. The first error in Experiment 2 was observed at 145 °C, which is 20 °C above the manufacturer stated maximum stress limit. The elevated temperature testing results revealed errors only in the 1 to 0 direction, that is, bits that were originally zero remained zero. The results from the third

experiment are presented in Figure 8. As expected given the total number of '1' bits, the total bits in error within the 0x5 and 0xA patterns are each about half that of the 0xF pattern.

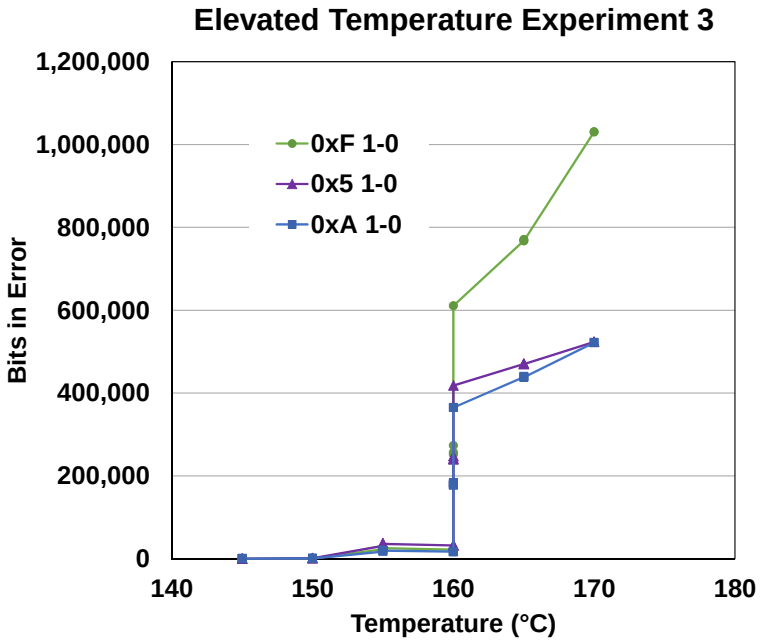


Figure 8. Elevated temperature testing results for the third experiment.

During the experiment when the temperature reached 155 °C, the board temperature was lowered to 120 °C, the memory was read again and the errors were still present. A day after the first experiment, the memory was re-written and the errors were eliminated. This latter investigation was not performed in the third experiment because the board became inoperable at 170 °C after two tests.

Overall, we conclude that the memory can be read reliably at temperatures significantly higher than the 125°C rating, that is, read-only programs can be continued to be executed in harsh environmental conditions such as those that might be experienced post-accident.

3.1.2 Radiation Testing

Experimental Setups

The total ionizing dose (TID) experiments were carried out in a Gammacell 220 Co-60 self-shielded irradiator. The Gammacell 220 allows feed through of ribbon cables thereby permitting in-situ measurements during irradiation. To accomplish the simultaneous irradiation and system testing, an Explorer 16 development board is located outside the irradiation chamber as shown in Figure 9. The Explorer 16 development board is a low-cost modular development system for Microchip 16-bit and 32-bit microcontrollers, and includes a PICtail Plus daughter card connector for expansion boards. The device under test (DUT) is then placed into a universal development board that is located in the irradiation chamber as pictured in Figure 10. In some experiments, the power to the DUT is supplied via the Explorer 16 (see Figure 11(a)) whereas in

other cases, an external dc power supply is utilized (see Figure 11(b)) so that current and voltage to the DUT may be monitored and recorded. In other instances, both a biased and unbiased DUT were irradiated simultaneously as shown in Figure 12.

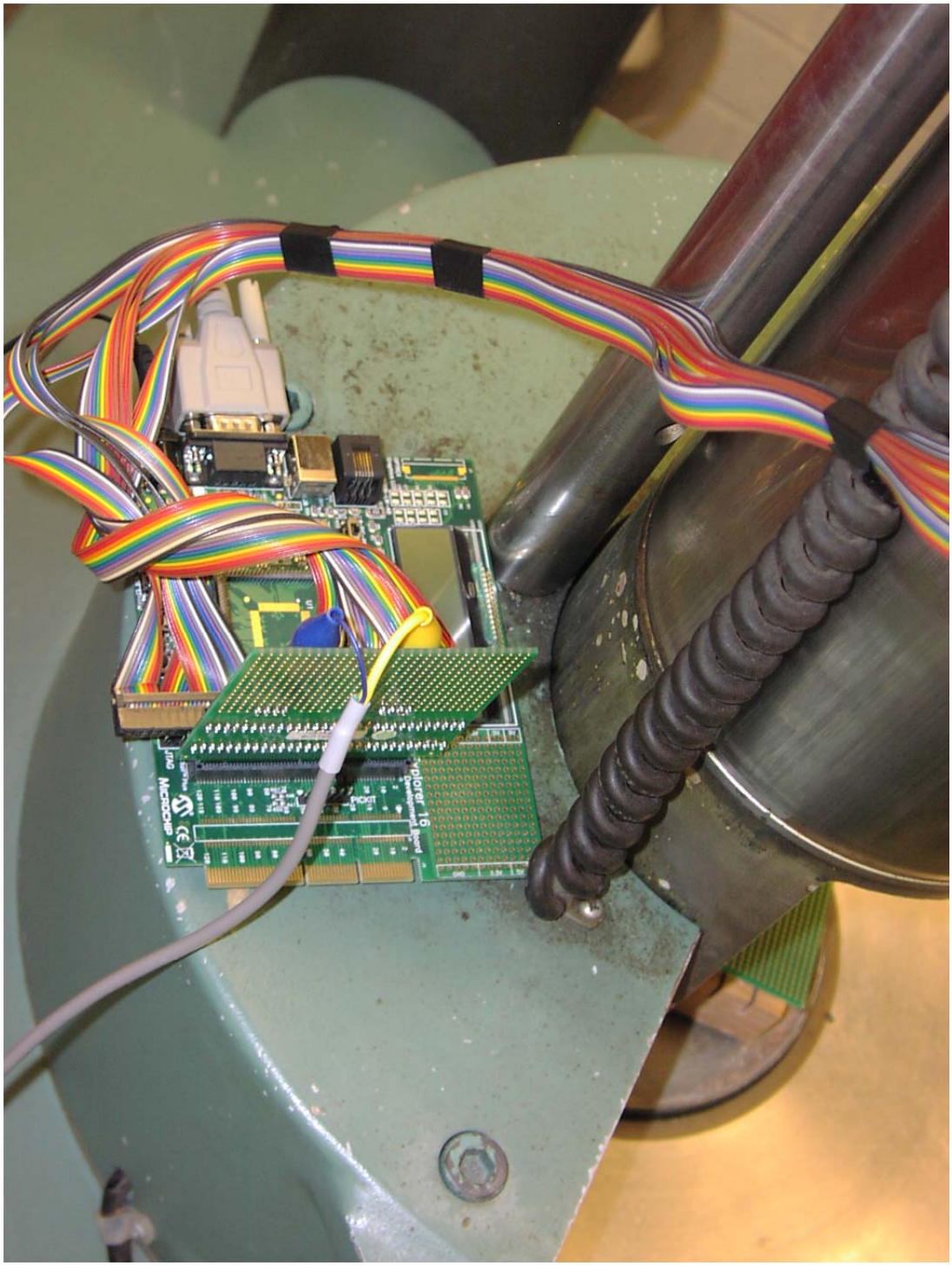
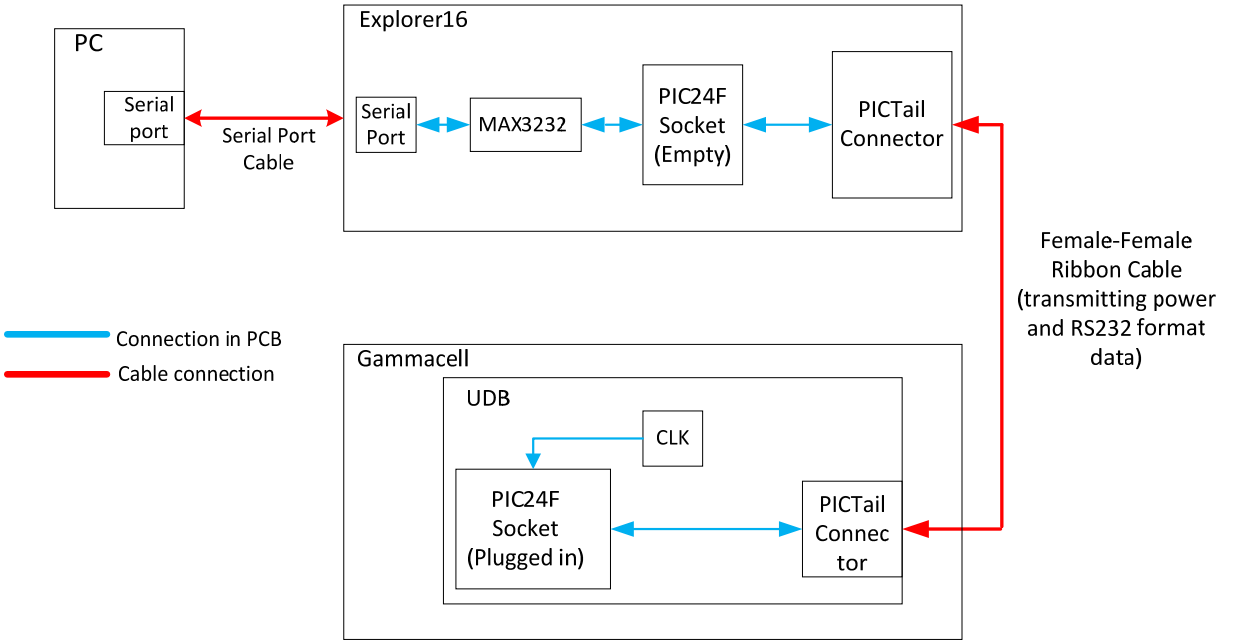
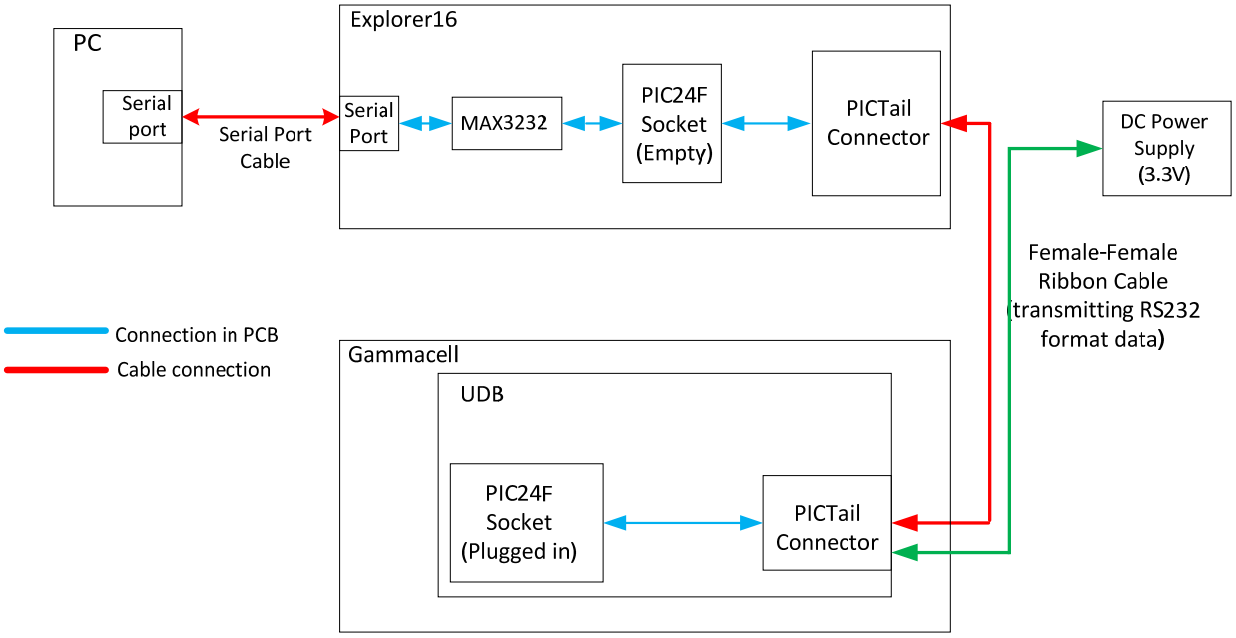


Figure 9. Explorer 16 development board located outside the irradiation chamber with ribbon cables providing signal and power transmission pathways to the device under test.

Figure 10. Universal development board with microcontroller placed within the irradiation chamber.



(a) Powering the DUT using the Explorer 16.



(b) Powering the DUT using an external dc supply.

Figure 11. Electrical connections for irradiation testing of the microcontroller.

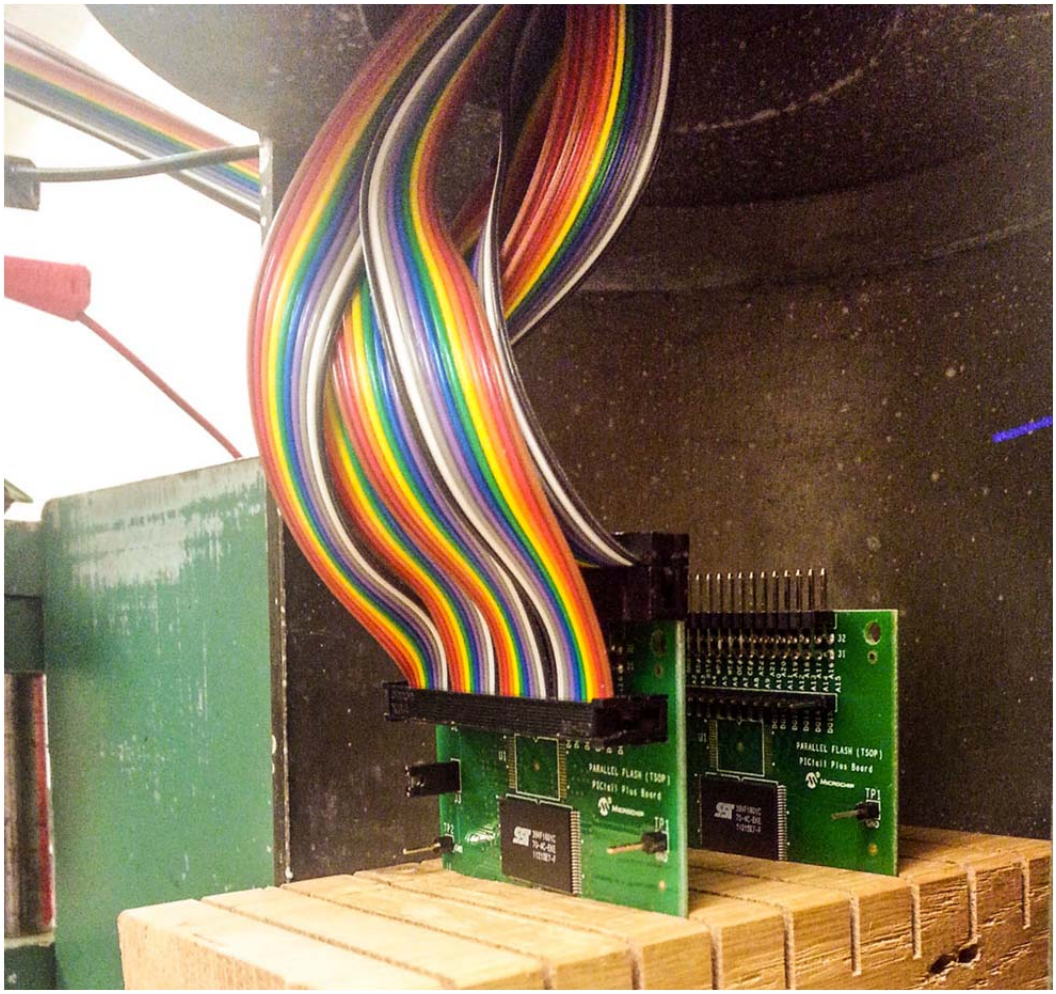


Figure 12. Biased (front) and unbiased (rear) flash memory in irradiation chamber.

Test Patterns

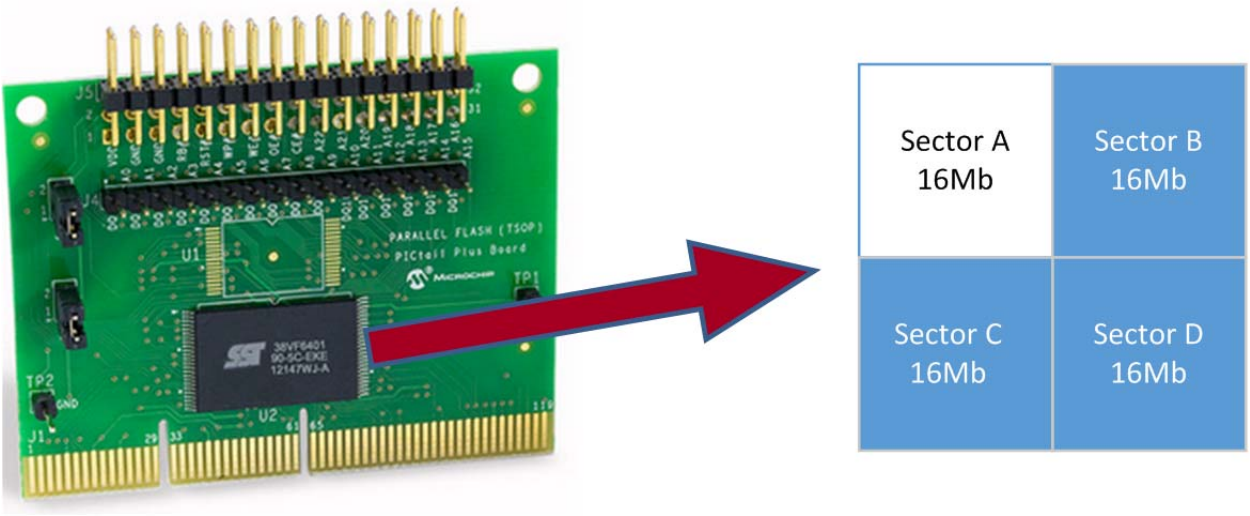
The actual irradiation experiments of the COTS devices were generally either focused exclusively on the flash memory or dedicated to the microcontroller with embedded flash. For these experiments, custom test and diagnostics codes were written to exercise the flash and microcontroller in order to assess the realistic performance of the DUT when deployed in a radiation environment. The test patterns encompassed varying the bit patterns, the activity factor in terms of the periodicity of the program and read operations, and the number of program and read operations carried out within each dose interval.

An example test pattern layout for the flash memory test is illustrated using Figure 13. First, the 64 Mbit chip is divided into four sectors of 16 Mb each (Figure 13(a)). In the testing, generally, using three of the four sectors was sufficient to accomplish the test goals. For instance, the individual sectors were programmed for different operations and intervals such as

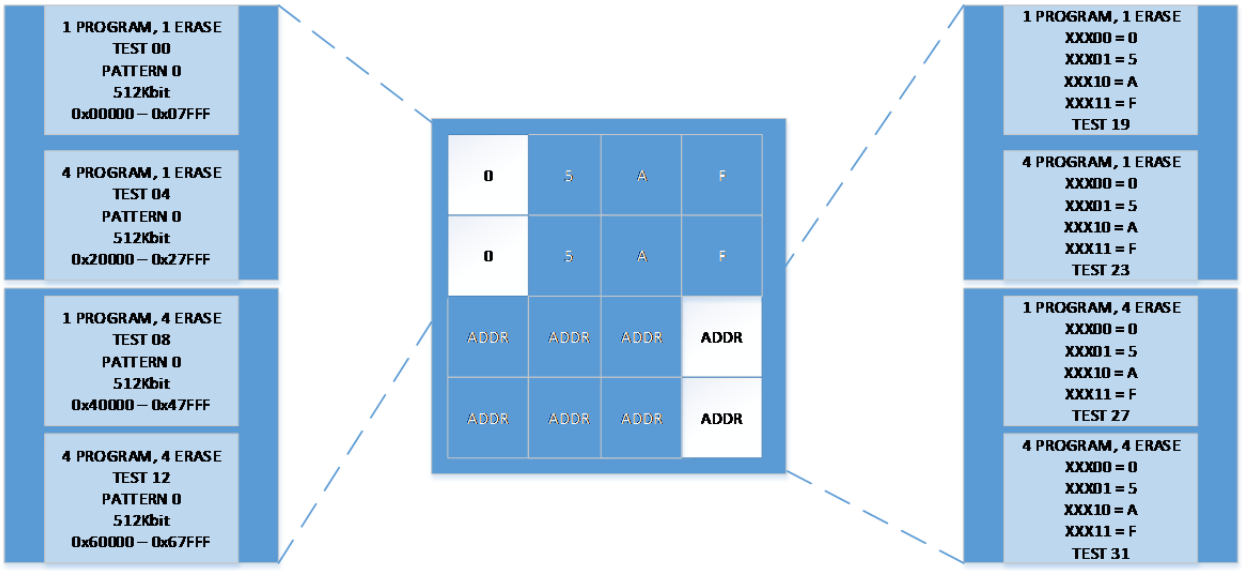
- Sector A: reprogram and read every 45 min (23 krad);
- Sector B: read only every 180 min beginning 180 min into the experiment; and

- Sector C: read only every 60 min beginning 90 min into the experiment.

Each 16 Mb sector was then further divided into 32 unique tests; see Figure 13(b). These unique tests were specific to the particular experiment. As an example, the overall test matrix for Experiment 5 is given in Figure 14. With the level of detail provided by these tests, considerable amounts of measured data were generated from each experiment for analysis.



(a) 64 Mbit chip is divided into four 16 Mb sectors.



(b) Division of a 16 Mb sector into 32 unique tests. This example is for flash experiment 5 in which the top half of the sector was programmed according to column while the bottom half was programmed with respect to address; see legends to left and right, respectively.

Figure 13. Test pattern layout for flash memory.

SECTOR A (Program/Read 4 Times Every 180-min Cycle at T=0)

00, 0x0, 1P1E	01, 0x5, 1P1E	02, 0xA, 1P1E	03, 0xF, 1P1E
04, 0x0, 4P1E	05, 0x5, 4P1E	06, 0xA, 4P1E	07, 0xF, 4P1E
08, 0x0, 1P4E	09, 0x5, 1P4E	10, 0xA, 1P4E	11, 0xF, 1P4E
12, 0x0, 4P4E	13, 0x5, 4P4E	14, 0xA, 4P4E	15, 0xF, 4P4E
16, 1P1E	17, 1P1E	18, 1P1E	19, 1P1E
20, 4P1E	21, 4P1E	22, 4P1E	23, 4P1E
24, 1P4E	25, 1P4E	26, 1P4E	27, 1P4E
28, 4P4E	29, 4P4E	30, 4P4E	31, 4P4E

SECTOR B (Read-Only Once Every 180-min Cycle at T=180 min)

32, 0x0, 1P1E	33, 0x5, 1P1E	34, 0xA, 1P1E	35, 0xF, 1P1E
36, 0x0, 4P1E	37, 0x5, 4P1E	38, 0xA, 4P1E	39, 0xF, 4P1E
40, 0x0, 1P4E	41, 0x5, 1P4E	42, 0xA, 1P4E	43, 0xF, 1P4E
44, 0x0, 4P4E	45, 0x5, 4P4E	46, 0xA, 4P4E	47, 0xF, 4P4E
48, 1P1E	49, 1P1E	50, 1P1E	51, 1P1E
52, 4P1E	53, 4P1E	54, 4P1E	55, 4P1E
56, 1P4E	57, 1P4E	58, 1P4E	59, 1P4E
60, 4P4E	61, 4P4E	62, 4P4E	63, 4P4E

SECTOR C (Read-Only 3 Times Every 180-min Cycle at T=90 min)

64, 0x0, 1P1E	65, 0x5, 1P1E	66, 0xA, 1P1E	67, 0xF, 1P1E
68, 0x0, 4P1E	69, 0x5, 4P1E	70, 0xA, 4P1E	71, 0xF, 4P1E
72, 0x0, 1P4E	73, 0x5, 1P4E	74, 0xA, 1P4E	75, 0xF, 1P4E
76, 0x0, 4P4E	77, 0x5, 4P4E	78, 0xA, 4P4E	79, 0xF, 4P4E
80, 1P1E	81, 1P1E	82, 1P1E	83, 1P1E
84, 4P1E	85, 4P1E	86, 4P1E	87, 4P1E
88, 1P4E	89, 1P4E	90, 1P4E	91, 1P4E
92, 4P4E	93, 4P4E	94, 4P4E	95, 4P4E

Figure 14. Test matrix for flash experiment 5.

Flash Irradiation Test Results

The COTS flash irradiation experiments are summarized in Appendix B. A sampling of the results is presented here to illustrate observations and conclusions that have been made as a consequence of the testing.

As seen in Figure 15, Experiment 1 established that as gamma ray dose increases linearly, the bit errors induced exhibit an exponential increase after a threshold dose is reached. Furthermore, the unbiased flash memory exhibits fewer errors at the same dose. In particular, the TID effect for

the unpowered device is delayed by at least 20 krad. It is noteworthy that unpublished data from an industrial group working on another radiation hard flash design show TID failures in the 10 krad range, such that the chosen SuperFlash far exceeds that TID.

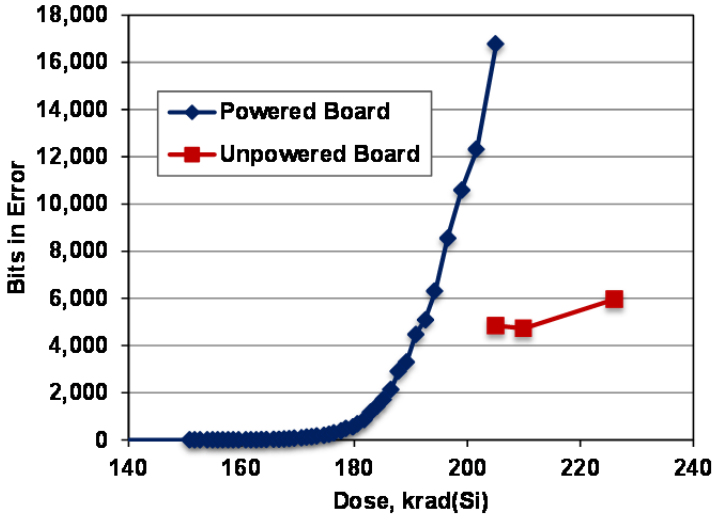


Figure 15. Exponential increase in errors with dose after onset.

Based on the results of Experiment 1, various strategies were attempted in Experiments 2 through 4. For example, in Experiment 2, the memory was operated in a read-only mode rather than also exercising the erase and program operations, as was done in Experiment 1. In Experiments 2a, 2b and 2c, the onset dose of the biased board was increased to over 200 krad, which was an almost 50 krad increase compared to Experiment 1. These first set of experiments demonstrated that the write operation (programming) appears more limiting than reading as the first error occurs at 150 krad and 250 krad, respectively.

Because of the results obtained in Experiments 1–4, a more detailed investigation was undertaken to understand the behavior of the flash memory under irradiation. Hence, the intricate test regime that was previously shown in Figure 14 was employed in Experiment 5. Immediately evident from Figure 16 is that 0 to 1 errors (solid symbols) dominate compared to 1 to 0 errors (empty symbols), that is, the programmed state (0) exhibits more errors than the erased (1) state. In Figure 17, the 0x5 pattern shows errors about half that of the 0x0 pattern as one would expect it to be, but the 0xA pattern runs one-fourth to one-third that of the 0x0 pattern. Besides examining the test patterns, this experiment undertook to determine whether repetitive (excess) programming or erasure operations might be utilized to mitigate the radiation effects. Repeated or iterative programming can mitigate TID errors in some cases [25]. However, NOR flash memory is subject to over-erase failure. Moreover, cycling, i.e. repeated write/erase in the flash chip, leads to stress-induced dielectric degradation that when combined with irradiation, leads to charge trapping induced failures [26]. Figure 18 shows that using four programming operations rather than a single programming operation actually exacerbates the impact of radiation. Likewise, it appears from that graph that the use of additional erasure

operations also serves to increase rather than decrease the number of errors. Hence, we find that a high activity factor is in fact detrimental.

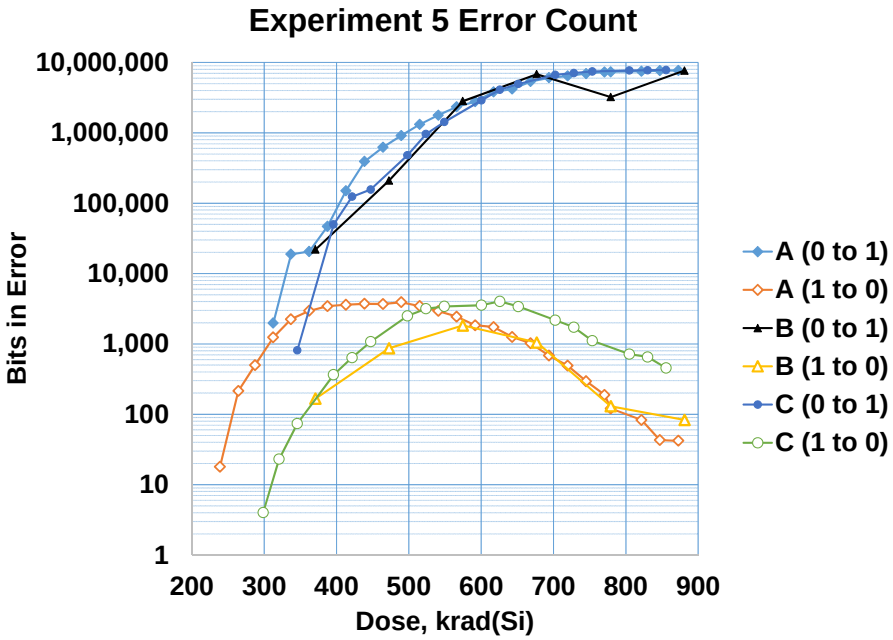


Figure 16. Bit errors with gamma ray dose in Experiment 5.

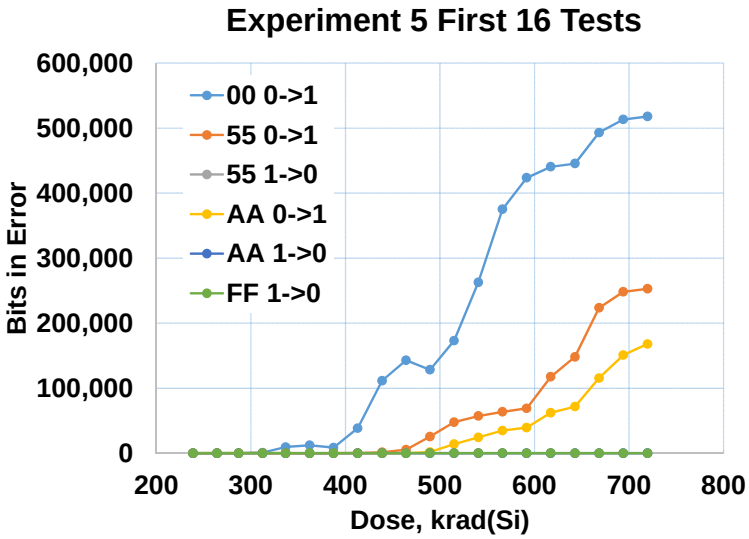


Figure 17. Errors in Experiment 5 with respect to the test pattern.

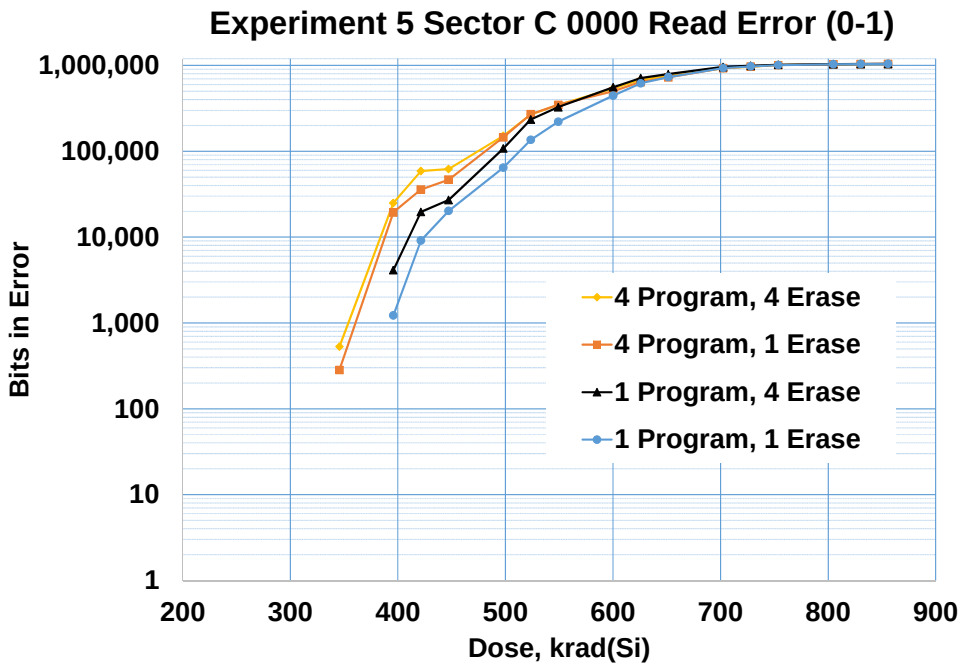


Figure 18. Impact of operation set.

Overall results from Experiment 6 are given in Figure 19. As with Experiment 5, most errors occur due to a change from 0 to 1. Since the lower numbers of 1 to 0 errors are likely correctable using EDAC, we focus on the more statically significant 0 to 1 errors which begin to occur at roughly 300 krad. Sector A 0-1 errors likely occur first because it is exercised three times every 232 min (~120 krad(Si)) with both program and read operations. Although Sector C is also cycled every 232 min, it is read only, whereas Sector B is programed and read only once during the 232 min period. Figure 20 reveals, as might be expected, that single-bit errors are typically manifest first and then with larger numbers of bit errors occurring, the multi-bit errors begin to dominate. To evaluate qualitatively the repeatability of the test results, split test comparisons were made. For example, Figure 21 shows that 0x0 pattern in the first half of Sector A exhibits initial bit flips at 370 krad while the first errors for all patterns with zero bits in the bottom half are delayed until 440 krad. Some of these split-test results led to speculation that the number of existing ones in a column might be affecting the likelihood that a bit errors, thus motivating a different test pattern for Experiment 7.

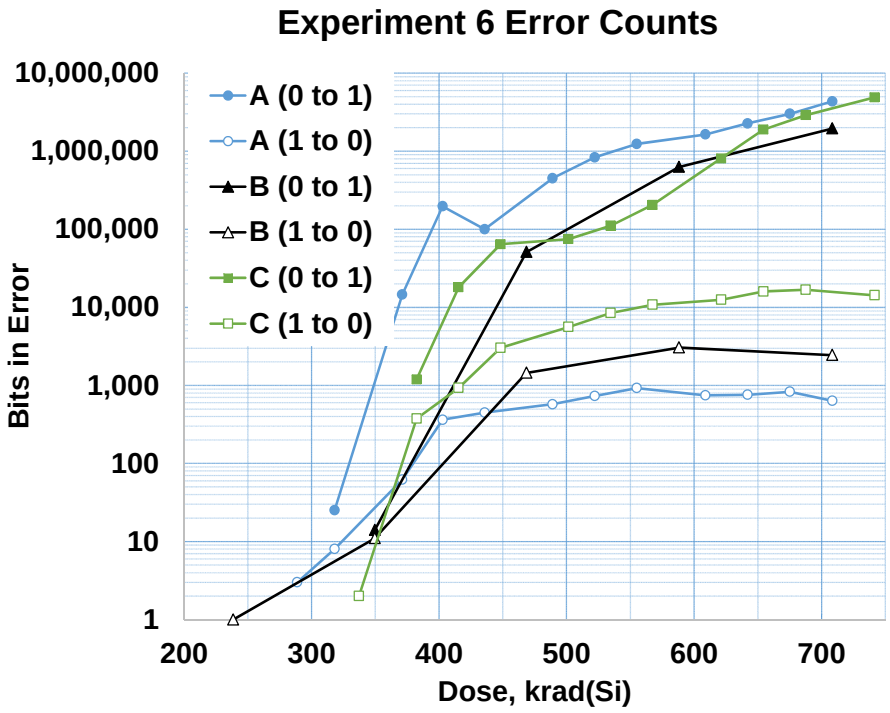


Figure 19. Comparison between errors due to three different operation sets and activity factors.

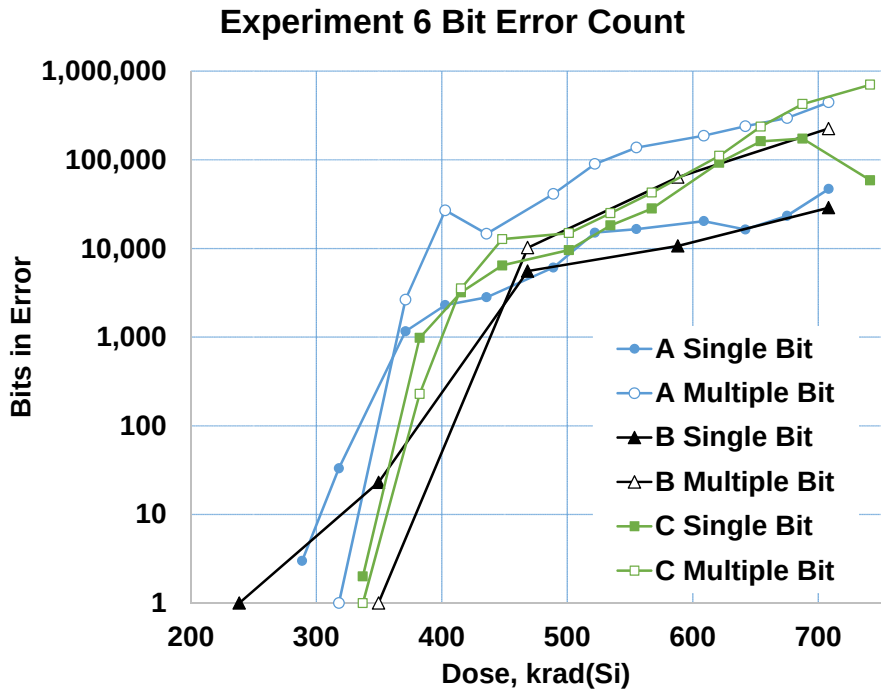


Figure 20. Occurrence of single-bit and multi-bit errors in Experiment 6.

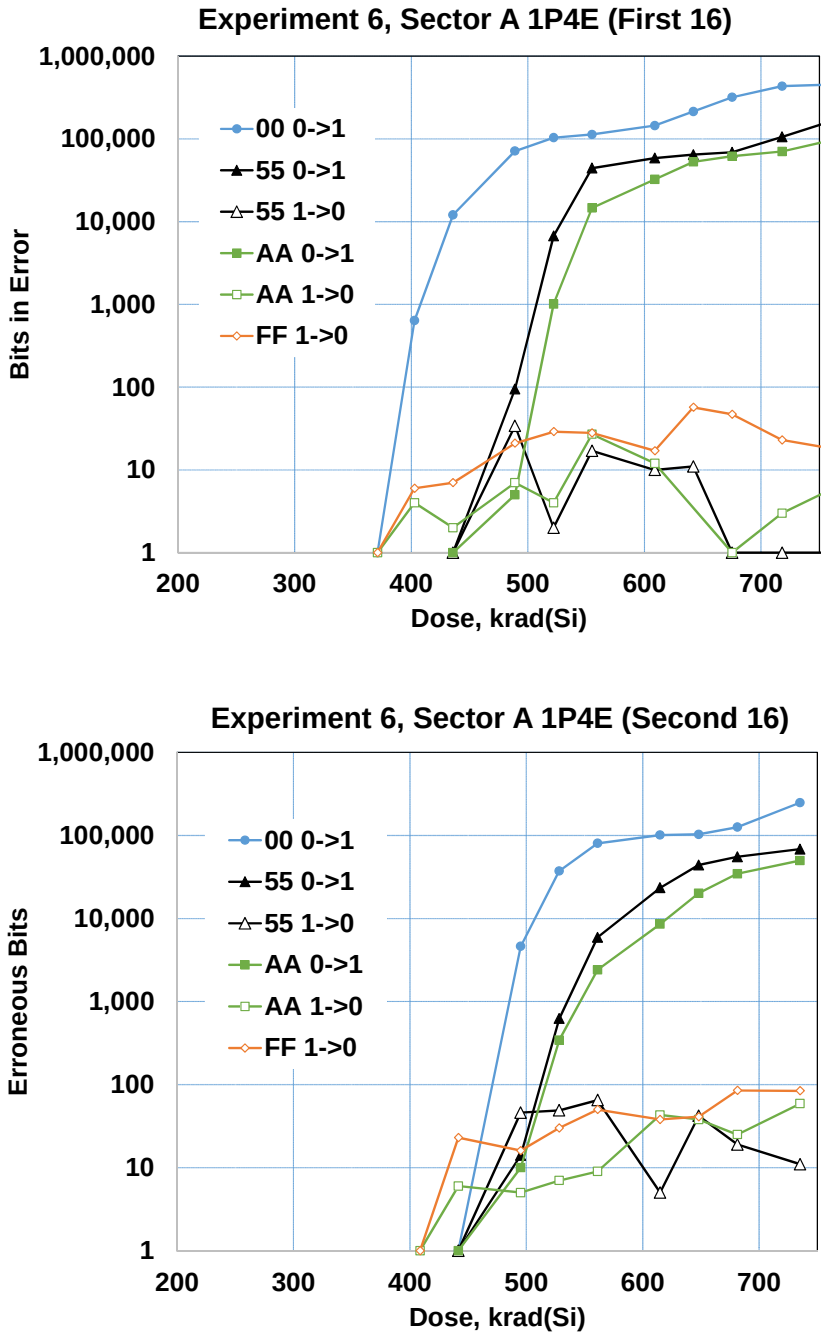


Figure 21. Representative split-test comparison from Experiment 6.

For later experiments, two other test patterns were introduced. Whereas the four patterns previously used were 0x0, 0x5, 0xA and 0xF, the first new pattern was an overall matrix composed of zeros in the top left half and ones in the bottom right half, as depicted in Figure 22, and is termed a triangle test pattern. The second new pattern, called the diagonal pattern, has ones in the top right upper half and the bottom left lower half, and zeros in the remaining diagonal from top left to bottom right. This approach was taken to assess a hypothesis that the

greater the number of existing 1's in the overall 32-bit word, the more resistant the pattern is to undergoing degradation from 0 to 1 as the latter error type dominates. These matrix patterns were subsequently deployed for both radiation and elevated temperature testing. This method allows us to correlate failures with 0 and 1 count on the column (bit line). In particular, the triangle and diagonal patterns allow determination of program disturb, which should occur directly above or below a programmed cell, on the diagonal or on the same row in the erased section (see Figure 23(d)), while the (inverse) checkerboard pattern provides indication of column level interaction between 1's and 0's.

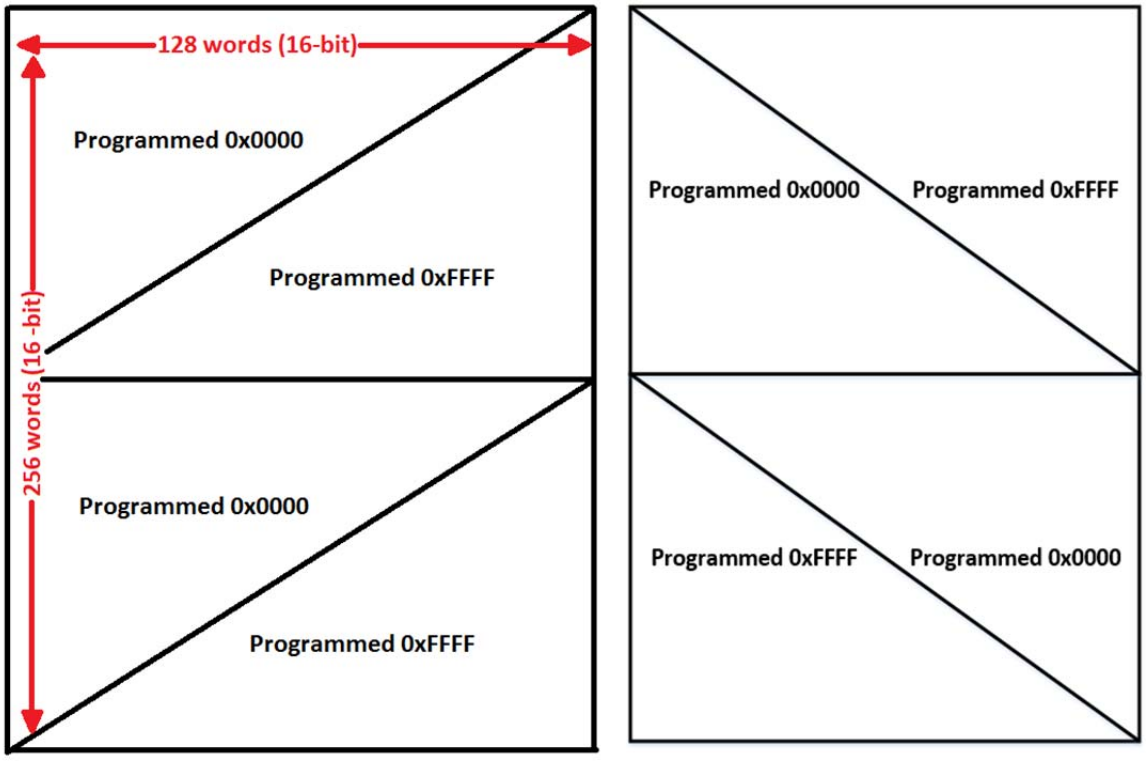


Figure 22. Triangle test pattern (left) and diagonal pattern (right).

Analysis of Flash Radiation Test Results

At this point, it is instructive to examine the behavior of a SuperFlash (SF) memory cell. The split-gate SF structure (see Figure 23(a)) is referred to as a 1.5-T cell since it has separate select gate (word line) and floating gate devices fabricated in series between the source and drain. The cell split-gate transistor pairs share a common source line (labeled source in Figure 23(a)). From a circuit point of view, the design is two series devices as in Figure 23(d)—the floating gate (FG) device at the source line (SL) provides programmability. Access through the series select gate (SG), which serves as the word line (WL) device eliminates over-erase issues, that in a conventional NOR flash would render the column inoperable [27]. The devices tested in this paper utilize the third generation cell. In this generation, the WL (SG) device can use a thin oxide, providing low voltage read operation and potentially, commensurately improved TID behavior. The source line spans a memory array row, defining the smallest erase unit, comprised

of one even and one odd row. An erase sector is generally comprised of multiple such rows (the devices used in our experiments have 16 such rows) but is bounded to be at least two WLs with a common SL. The split-gate memory cell uses poly-to-poly Fowler-Nordheim (F-N) tunneling for erasing, and source side channel hot electron injection for programming [28]. High voltages are generated by a small on-chip charge pump.

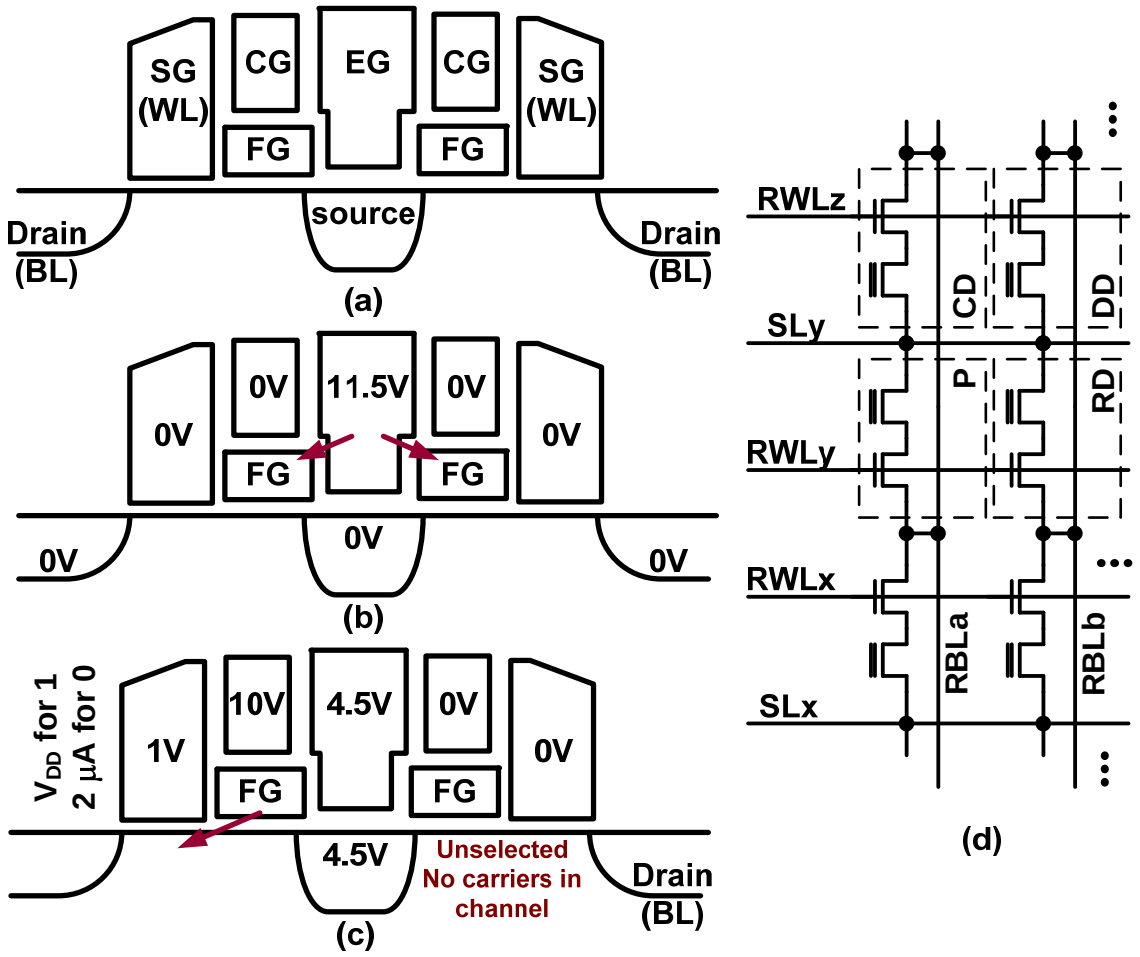


Figure 23. SuperFlash 1.5-transistor cell cross-section (a) and operating voltages in erase (b) and program (c). (d) Shows the circuit configuration; NOR bit lines are perpendicular, while the erase gate and source line are parallel to the WL. The cells are labeled by the potential program disturb positions (CD, RD, DD) while P indicates the cell being programmed.

To erase, a high voltage (11.5 V) is applied to the erase gate (EG), while the bit line (BL), WL and control gate (CG) are grounded (Figure 23(b)). The latter serve to couple the FG to a low potential, increasing the difference between it and the EG. The WL voltage capacitive coupling to the FG is less than that of the SL, producing a large potential difference. The FG is erased by removing electrons via poly-to-poly F-N tunneling, raising the FG potential. The third generation cell has a peak field at the upper corner of the FG to EG. This is a key feature of the architecture. The peak field is generated at the FG corner, which enhances the tunneling and allows a much thicker (approximately 12 nm) oxide between the EG and FG without requiring a

higher voltage on the former [29]. The electrons tunnel toward the EG, producing a current flow in the opposite direction (arrows in Figure 23(b)). The F-N process is self-limiting, controlled by the FG and EG potential difference—as the FG voltage rises, tunneling current is reduced exponentially. Erase produces the logic 1 state, which is referenced to the FG potential making the cell on (1 = conducting).

To turn the cell off, i.e., non-conducting (0 = off) it is programmed via source-side injection, where the WL is biased to about V_{th} (most efficient for hot carrier production) with a high voltage on the CG, that couples the FG high. The source connection is at 4.5 V to produce a large horizontal field in the channel. Carriers are injected by the source (here the drain end) and travel towards the source (which is biased as the drain). The voltages are optimized for hot carrier production, and scattered hot electrons are attracted towards the FG by its high potential. The resulting programming current flow is from the FG to the BL (see the arrow in Figure 23(c)) reducing the FG potential and making the cell non-conducting, i.e., to the 0 state. Programming applies to an entire row. Whether a cell is programmed (to 0) is due to carriers in the channel. A high potential on the BL turns off the device by applying a zero or negative WL to BL source potential, so there are no carriers to produce hot electrons. If a column is to be programmed, a current source at low potential provides the carriers to that column. The unselected row coupled to the same EG has a low FG potential and no carriers due to WL = 0 V (Figure 23(c)).

To read, V_{DD} is applied to the WL to turn on the access device, and $V_{CG} = V_{DD}$ to couple the FG up slightly. The source line is at ground, and the BL is biased to about 1 V (standard for flash reads). Nominal cell read current is about 38 μA in the fully erased state.

The SuperFlash cell characteristics are summarized in Table 3. Examining these properties implies that leakage from a charged floating gate (‘0’ state) could result in the shift of the logic state from ‘0’ to ‘1’, as illustrated in Figure 24.

Table 3. SuperFlash Cell Characteristics

Logic State	1 (on)	0 (off)
Voltage threshold, V_{th}	Low	High
Operation	Erase	Program
Floating gate	Conducting	Non-conducting

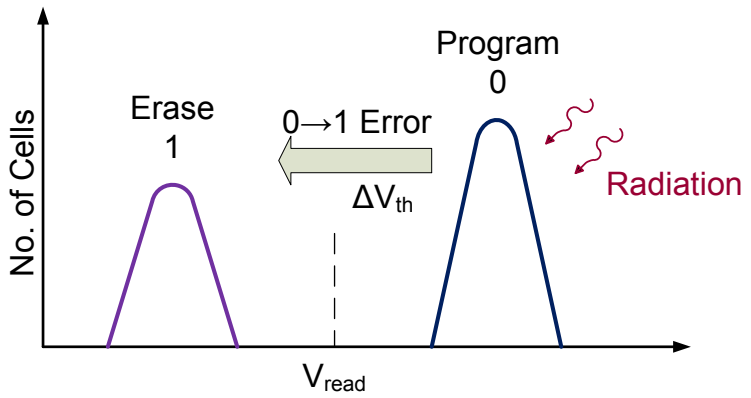


Figure 24. Irradiation-induced shift in logical state (0→1); adapted from [30].

Read Only During Irradiation

Since flash memory is frequently used as program storage in applications, a read only usage model is common. We conducted multiple tests with this usage model, and expected good results since the charge pump is not utilized for reads.

As shown in Figure 25 for one device, the memory blocks containing all 1's (erase only) and solely read during irradiation exhibited no failures in testing to 300 krad(Si). A conducting ('1') cell discharges the BL. Thus, even if a 1 (erased) cell becomes weak, TID induced leakage may take it in the correct direction. Another device tested to 500 krad(Si) showed that 288 krad(Si) was the point where failures first occur. This also indicates that the failures were not due to sensing or decoding—reads appear to be reliable through those circuits to very high dose.

Memory blocks containing all 0's, programmed before being irradiated and only read during irradiation, experienced the first failures (12 words with a single 0-1 bit error each) when read at 270 krad(Si) but had no errors at 220 krad(Si). A subsequent device tested showed remarkably similar results, reaching 271 krad(Si) before recording errors.

Read-only mode during irradiation with a checkerboard pattern had no failures until the end of that test at 241 krad(Si), where a single bit error was recorded. A subsequent test with this checkerboard pattern showed the first 1 to 0 failure at 201 krad(Si) and the first 0 to 1 failure at 265 krad(Si). Once failures begin, they increase at a rate of just under 1000 bit fails per 100 krad(Si). At 300 krad(Si), the predominant 1 to 0 failing bits are 0.15% of the total.

These results indicate that there is an effect due to interactions between cells programmed to 1 and 0. Referring again to Figure 25, the noise in the error rates was found to be due to bits reading as failed, but passing in a few subsequent reads before failing consistently. This is easily explained by a given cell reaching the band where the sensing circuits are uncertain, but then passing through this marginal point as the cell state is altered by TID.

Erase and Program During Irradiation

In a data storage application, the flash must be erased and programmed often. Particularly given the long history of charge pump induced failures, we expected this condition to be less robust to TID. Representative results for this mode are shown in Figure 31 where erase turns out to be quite limiting. Most blocks exhibited significant erase failures, primarily, but not exclusively in

the top and bottom sectors, which are the smallest erase unit. Higher activity factors did result in more rapid failures. Referring to Figure 31, the highest activity factor, which was 20x that of the lowest, exhibited an erase failure at only 50 krad(Si), which rapidly affected entire sectors. This failure mode is investigated in more detail below.

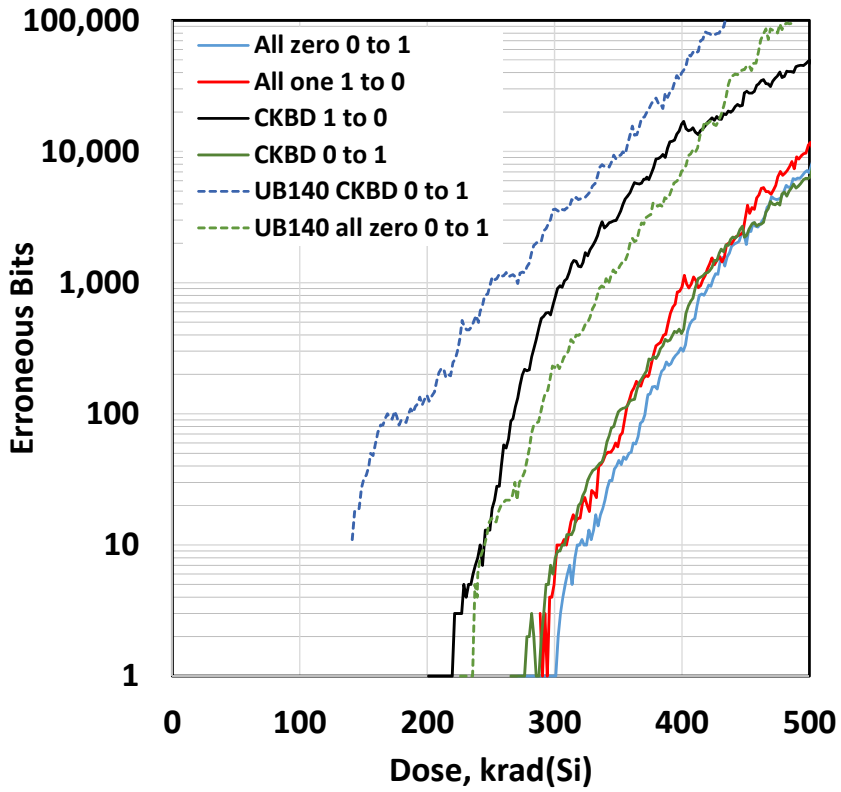


Figure 25. Read only failure response of representative 512 kilobit flash blocks in two devices in Experiments 17 and 18. The solid lines are for a device that was powered throughout the irradiation while the dashed lines are for a device that was unbiased until 140 krad (UB140).

At this point, we more carefully investigate the response to specific patterns by showing the failures graphically. We begin with the erase failures, which occur first. Figure 26(a) shows loss of a sector beginning at 109 krad(Si)—there were no errors at 88 krad(Si). Yellow indicates a 1 to 0 failure, i.e., failure to erase to a 1. The failure appears only in the triangle that was at 0 (this pattern is the triangle pattern alternating between Figure 27(f) and (g)). Other cells were already 1, so the erase failure in those bits does not emerge until the next erase cycle. At 124 krad(Si), the erase failures in sectors 0 and 15 were complete (see Figure 28(b)). Block 8 exhibited the same erase failures on sectors 0 and 15 (Figure 29(c) and (d)) at 108 krad(Si). The progression of the failures is evident in Figure 30(e)–(g). The EG organization of the arrays, i.e., two rows sharing one EG, is evident as failures follow this pattern. The progression from a few rows in the weak sector, predominantly but not exclusively the top and bottom sectors of a block, is apparent. We attribute the random patterns that preclude the full sector erase failure to random variability in the inter-poly oxide thickness causing some cells to fail earlier as the EG voltage is reduced. Other blocks exhibited almost identical failure modes (i.e., sector erase failures) and

number of failures at the same dose under the same conditions. Erase operations were successful to over 200 krad(Si) on all blocks, except for the full failing erase sectors.

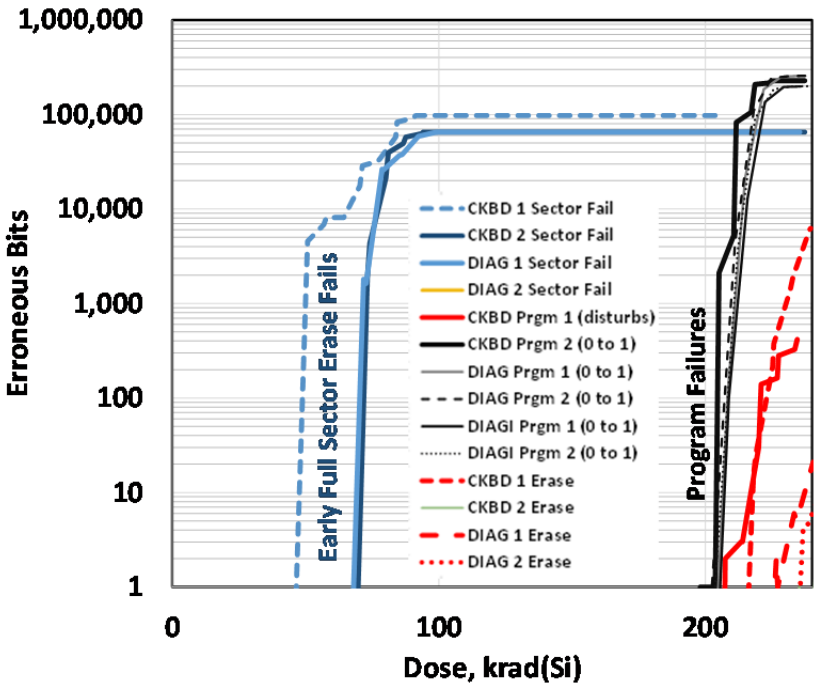


Figure 31. Erase and program failure response of multiple 512 kilobit flash blocks at high (20x) activity factor in Experiment 13. The dashed red lines are non-full sector erase (1 to 0) failures. The solid red line is due to 0 to 1 failures, but all occurred after programming, so may be program disturbs.

Block 4, programmed to all 0's, exhibited the first program (a single 0 to1) error at 220 krad(Si). This increased to 5 words (all single bit failures) and 973 words with errors at 222 and 234 krad(Si), respectively. Checkerboard patterns exhibited the same behaviors, indicating that the failures are activity and not pattern dependent (i.e., the first bit fail besides the oft-occurring sector erase failures was at 209 krad(Si)). In general, blocks experienced a very large number of program failures at some point above 200 krad(Si), with a small but detectable dependency on erase/program activity factor. Block 6 at 1x activity experienced over 13k words with errors at 234 krad(Si) (see Figure 33(a)). Block 7 at 1x activity factor, exhibited the sector erase failure mode at 149 krad(Si) and a similar failure mode to Block 6, with no other errors at 205 krad(Si), but no words could program correctly at 246 krad(Si) (Figure 33(b)).

As mentioned, a program disturb is manifested as bits changed to 0 inadvertently during a program operation. Checkerboard programmed blocks also exhibited a few apparent program disturbs beginning at 213 krad(Si), coincident in time with the onset of bit program failures (see Figure 34). At low activity factor, very few blocks showed program disturbs over many separate devices irradiated.

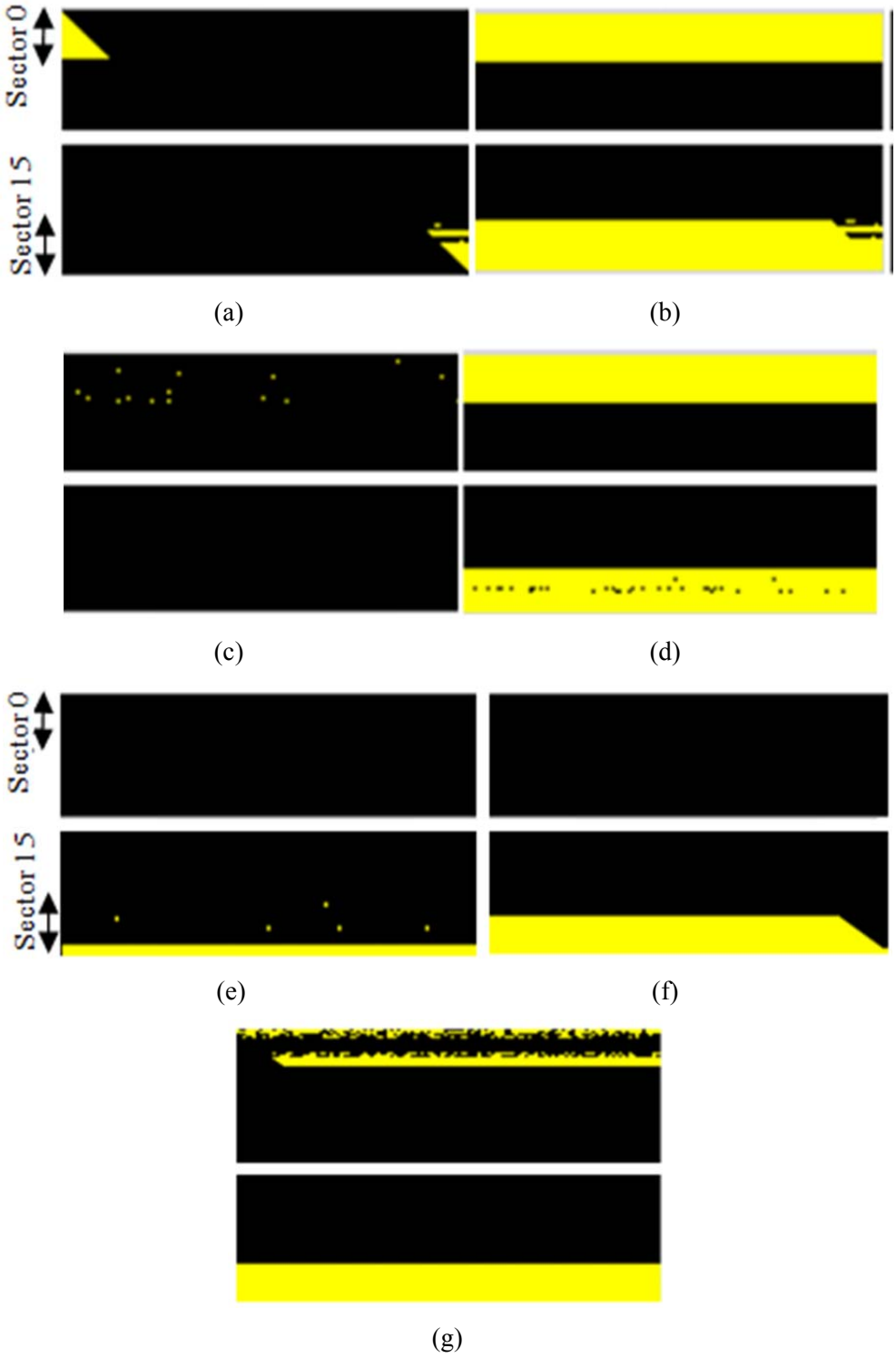
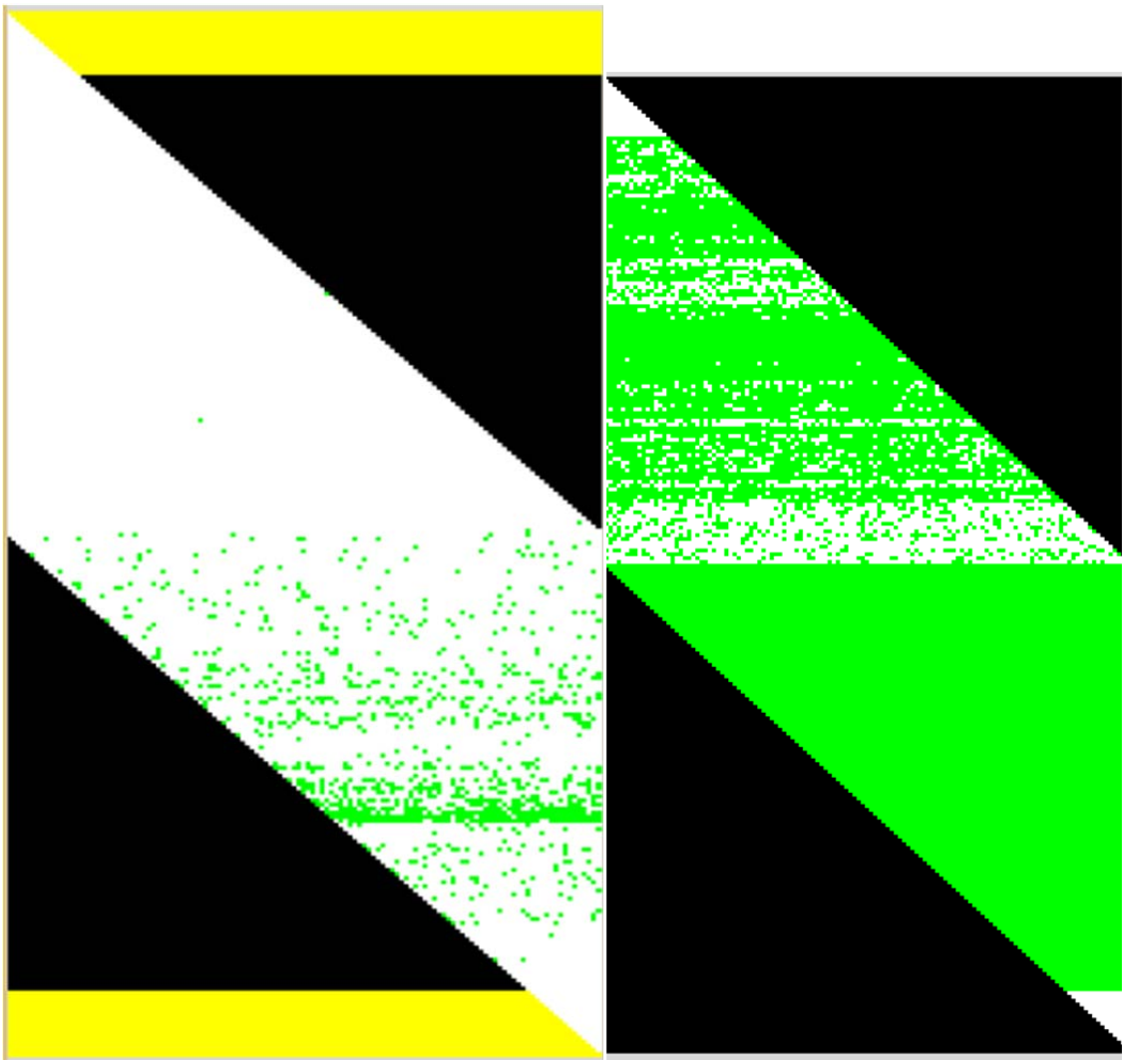
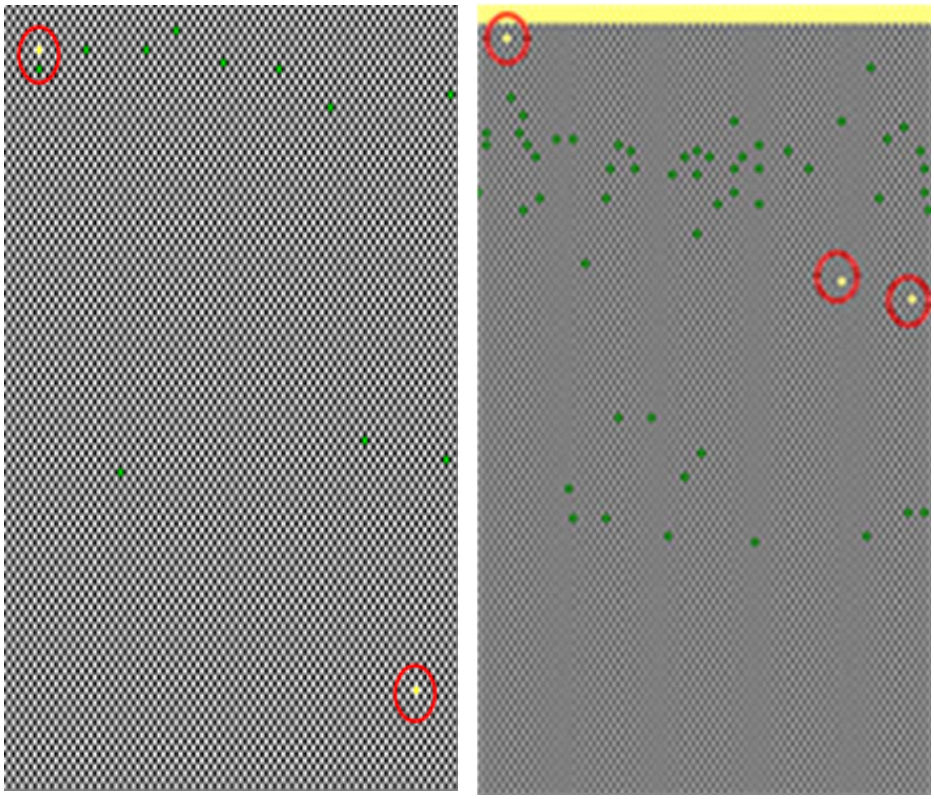


Figure 32. Erase failures for different blocks showing loss of one or two sectors and their progression. The centers of the blocks are removed since the failures occur in the top and bottom sectors. Black is a 1 bit (correct for erase) and yellow indicates a 1 to 0 failure (erase failed word). (a) Block 6 in Experiment 11 at 109 krad(Si), (b) same block at 124 krad(Si). (c) Block 8 in Experiment 11 at 100 krad(Si), (d) B8 at 108 krad(Si), (e) Block 6 in Experiment 13 at 2x activity factor—bottom rows erase fail at 73 krad(Si), (f) B6 (2x activity) bottom rows erase fail at 80 krad(Si), (g) B6 (2x activity) at 87 krad(Si).



(a) (b)

Figure 33. Program failures for different blocks at 1x program/erase activity factor in Experiment 11. (a) Block 6 at 234 krad(Si), (b) Block 7 at 246 krad(Si). Row and sector dependencies are clearly evident as the failures progress.



(a) (b)

Figure 34. Experiment 13 results (a) 2x activity factor block showing checkerboard program disturbs (circled) at 213 krad(Si) (zoomed and thus showing only part of the array); (b) another block's checkerboard program disturbs at 214 krad(Si) and many program failures. The sector erase failure occurs in this block as evident at the top of (b).

Microcontroller Irradiation Test Results

For the microcontroller experiments, in addition to exercising the embedded flash, a program was written to perform some basic mathematical operations at predetermined time intervals, and the results were continually output via a serial port to the personal computer used to monitor the DUT. In the first 16-bit microcontroller experiment, after about 1 hour in Gammacell (around 30 krad), the microprocessor rebooted itself, and remained dormant thereafter until about 150 krad at which point it did output some final data on the serial port. Post mortem analysis of the experiment revealed that an external clock IC on the universal development board had been utilized.

Given that in the previous experiment the root cause may have been the external clock IC, in subsequent microcontroller experiments, the processor internal clock was used and additionally, upon reboot, the status registers were output for diagnostic purposes. With the use of the internal clock, the failure dose was increased to 66 krad before a reboot occurred. Even so, this somewhat lackluster performance was disappointing even though it exceeds the failure TID specified for the microcontroller from several other manufacturers. The reset status register (RCON) revealed that the microprocessor rebooted because of either (a) an illegal opcode detection, or (b) an illegal address mode or uninitialized W register used as address pointer.

With anticipation that the 32-bit version of the microcontroller was fabricated using new technology, a third microcontroller experiment was carried out but the dose at which the first reboot occurred was found to be 43 krad. An unbiased 16-bit microcontroller was irradiated in parallel with the biased 32-bit unit and it was found to be functioning correctly after removal at a total dose of 68.2 krad. It was returned to the irradiation chamber for an additional 15 krad (unbiased also), and upon testing it at the 83 krad dose, it was found to be inoperable.

Eleven COTS microcontroller irradiations were carried out as summarized in Appendix C. Although the flash testing demonstrated operability to doses of a few hundred krad, the commercial off-the-shelf (COTS) 16-bit and 32-bit microcontrollers exhibited less radiation resilience than expected. In particular, catastrophic failure in the microcontrollers was experienced at doses as early as 20 krad and as late as 83 krad. However, the application-specific integrated circuit (ASIC) that we designed (see Section 3.3) provided an alternative pathway to achieve the project objectives.

Consequently, we evaluated an 8-bit processor that also utilizes the proven SuperFlash that we had successfully tested in order to ascertain whether it was a viable alternative. In an effort to extend the radiation resiliency, the supply voltage to the microcontroller was varied. This 8-bit microcontroller has a nominal voltage of 3 V with an operating voltage range of 2.7 to 3.6 V. Figure 35 shows a trend that lower bias leads to higher TID survivability; however, the increases do not achieve the overall radiation hardness desired in this application. Similarly, the 32-bit microcontroller showed a modest improvement from 42 krad to 51 krad by reducing the supply voltage from 3.3 V to 2.3 V.

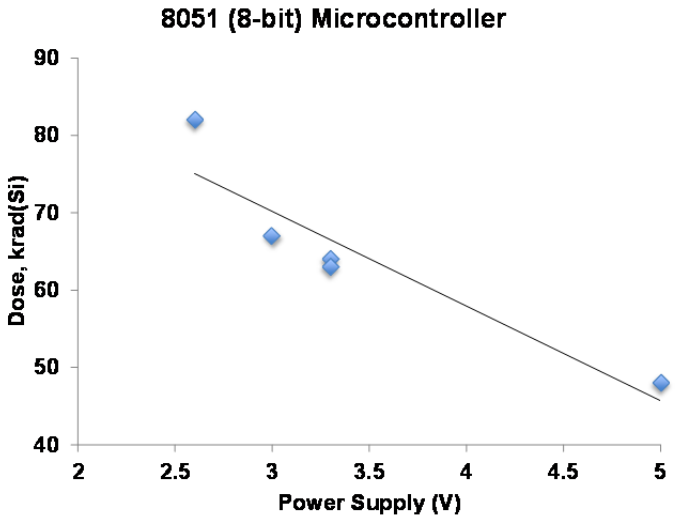


Figure 35. Catastrophic failure doses for five 8-bit microcontrollers.

3.2 Task 3: Board-level Demonstration of COTS Approach

Task 3 of the project was devoted to the construction of a demonstration board intended to establish the capability of extending the electronics lifetime in an ionizing radiation environment. With the application-specific integrated circuit (ASIC) microprocessor having survived to at

least 2.5 Mrad (see Section 3.4.1), the demonstration board was dedicated to extending the embedded flash (eFlash) memory lifetime.

The populated demonstration board is shown to the left in Figure 36. The printed circuit board layout is pictured in Figure 37. The custom demo board uses dual redundancy and power supply switching to improve the total ionizing dose (TID) lifetime of commercial off-the-shelf (COTS) eFlash (SST39VF1601C Flash daughter card). The rationale for this approach is that the high voltages experienced by the flash memory are detrimental in terms of the radiation effects, but if the chip is unbiased, such corresponding high electric fields are postponed. One obstacle to this approach is the need to electrically isolate the unbiased chip (or flash card), that is, it is necessary to place the flash card in a floating potential state. Buffering of the input/output (I/O) signal lines was necessary as we determined that the chip could be powered through the I/Os. The buffers isolating the board do not have to be hardened since leakage current through them will increase the system power slightly, but does not impact functionality. If leakage power is a concern, a hardened buffer could be used. The added system leakage of other components due to TID will dominate.

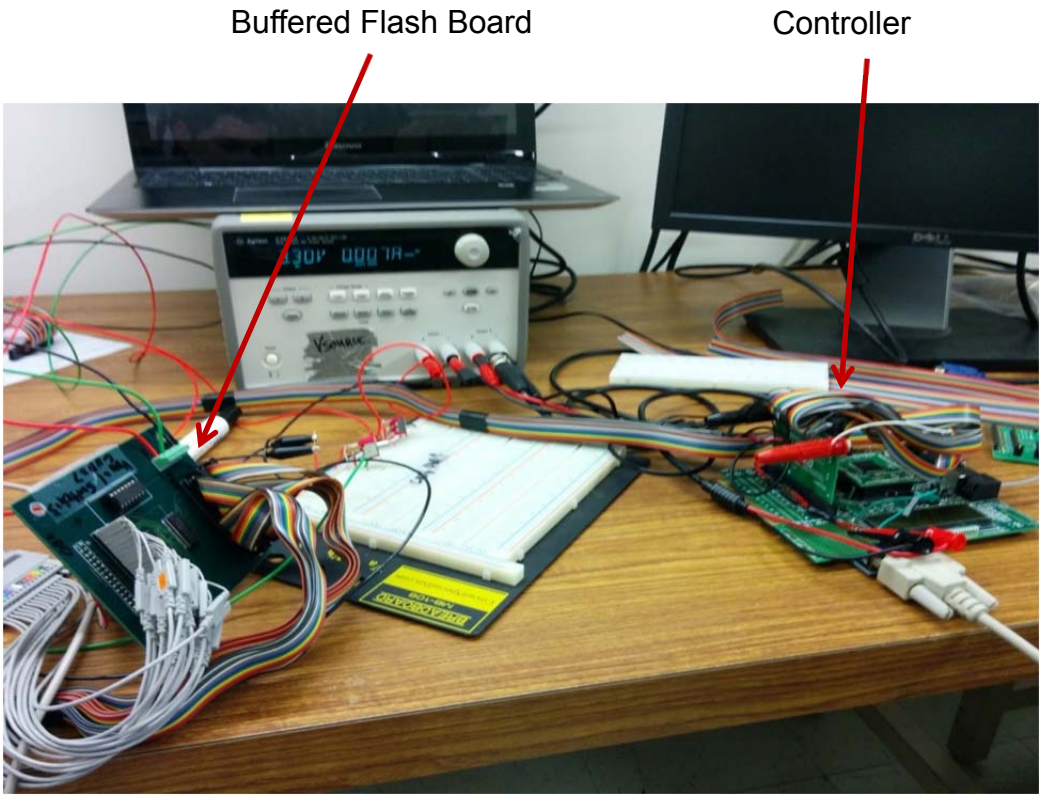


Figure 36. Demonstration board being bench tested in preparation for radiation testing.

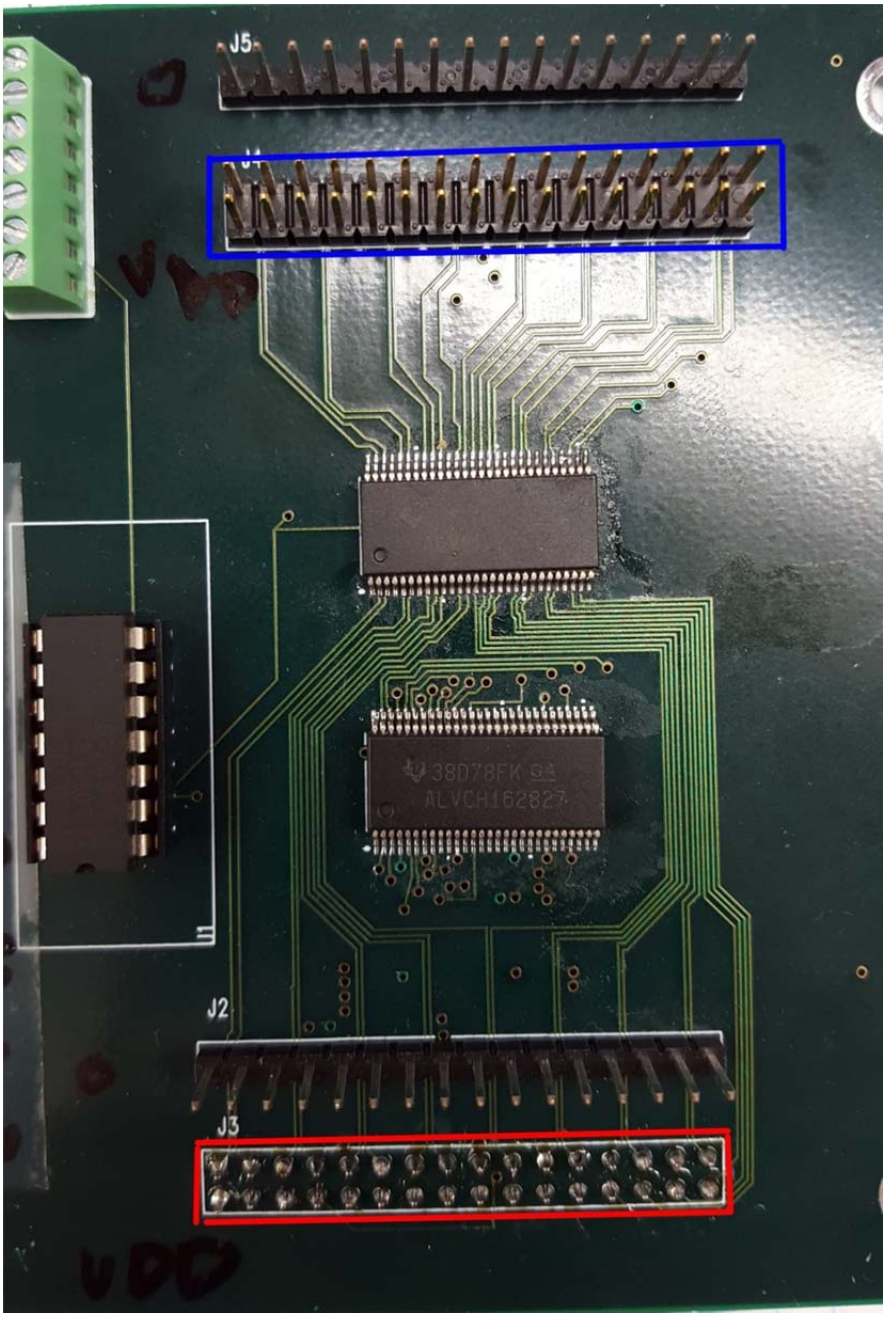


Figure 37. Populated printed circuit board of the demonstration board.

The demo board was irradiated with ^{60}Co gamma rays in early December 2015. For the radiation testing, six different data blocks were established on each chip. The programming state for each of the blocks is shown in Table 4. Blocks 7, 8 and 9 were only read at approximately 13 krad intervals (each cycle takes about 30 min) while the memory in Blocks 4, 5 and 6 were exercised according to the description in Table 4. An objective of erasing at each cycle before programming is to ensure that reinforcement of a prior programming operation does not occur, which could otherwise lead to erroneous conclusions about the measured results.

Table 4. Programming States of the Demonstration Board Data Blocks

Block	Initial Pre-irradiation State	Operations at Each Cycle
B4 (0x08000)	Programmed to checkerboard	Erased and then programmed with a checkerboard (CKBD) pattern, read to verify
B5 (0x10000)	Programmed to all zeros	Erased and then programmed with all zeros, read to verify
B6 (0x18000)	Left in erased state (ones)	Program with all zeros and then erase, read to verify
B7 (0x20000)	Programmed to checkerboard	Read only
B8 (0x28000)	Programmed to all zeros	Read only
B9 (0x30000)	Left in erased state (ones)	Read only

The first eFlash chip was powered from the onset of irradiation, while the second flash card was unbiased until a dose of 100 krad was reached, at which time chip 2 was powered on and the buffers to it were activated. The buffer tri-states the pins so the device is not powered up via the I/O electrostatic discharge (ESD) protection diodes while its power is gated off.

The radiation testing results are summarized in Table 5. The dose values for the erase, programming and read operation failures are the doses at which the first failure of that type is reported. If all flash cards were to be manufactured identically, the second eFlash chip would ideally last for 100 krad longer than the first card. However, we must bear in mind that the eFlash chips themselves have demonstrated variability in the TID response, as shown in the results presented in Section 3.1.2. Overall, these irradiation results, as discussed below, reveal this unbiased spare technique to be successful, as the TID to which this dual redundant system could be operable is essentially doubled compared to a single eFlash chip.

Table 5. Demonstration Board Radiation Testing Results

		Dose (krad)		
eFlash Chip		Chip 1	Chip 2	Life Extension
Chip Powered		0	100	
Chip Operation	**Sector**			
Erase sector failure	B4 [CKBD]	51	180	129
	B5 [All zeros]	52	181	129
	B6 [All ones]	54	170	116
Programming failure	B4 [CKBD]	91	341	250
	B5 [All zeros]	92	330	238
	B6 [All ones]	93	331	238
Read failure	B7 [CKBD]	150	210	60
	B8 [All zeros]	177	238	61
	B9 [All ones]	>600	306	n/a

Erase Operation

Table 5 and Figure 38 show that the first erase failures in Chip 1 (C1) occur at about 50 krad. These failures are observed only in the top and bottom sectors of the block (which consists of 16 sectors total) and as such, most of the memory block (14/16 = 87.5%) can continue to be erased as shown in Figure 39 and Figure 40. The dose at which the other 14 sectors began to fail varied but for all three blocks was above 100 krad, as for example can be seen in Figure 40(c). Similar

erase failure behavior is exhibited in Chip 2 (C2), although it is about 70 to 80 krad after powering (i.e., at an overall dose of 170–180 krad) before C2 experiences the sector erase failures (see Table 5) with significant non top and bottom erase failures not being seen until around 350 krad in C2.

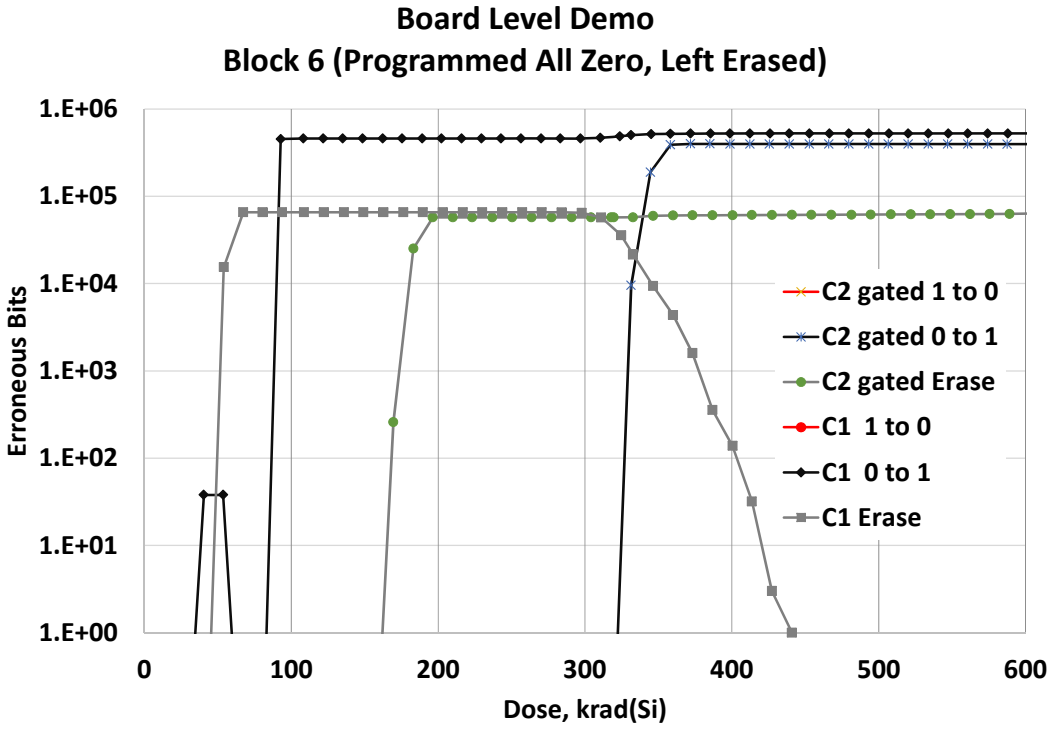
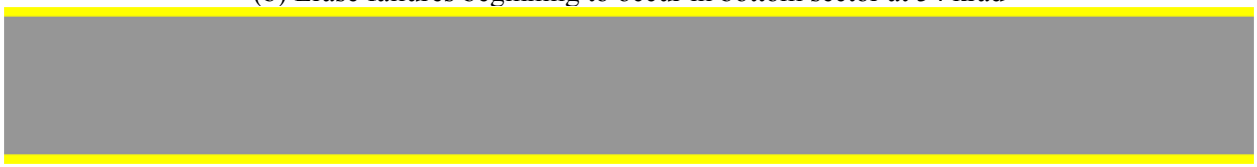


Figure 38. Representative irradiation results from both chips for Block 6, which was reprogrammed periodically. Chip 1 (C1) and Chip 2 (C2) exhibit erase failures at 54 and 170 krad, respectively. Programming (0 to 1) errors are observed in C1 and C2 at 93 and 331 krad, respectively.

(a) No failures observed at 42 krad

(b) Erase failures beginning to occur in bottom sector at 54 krad

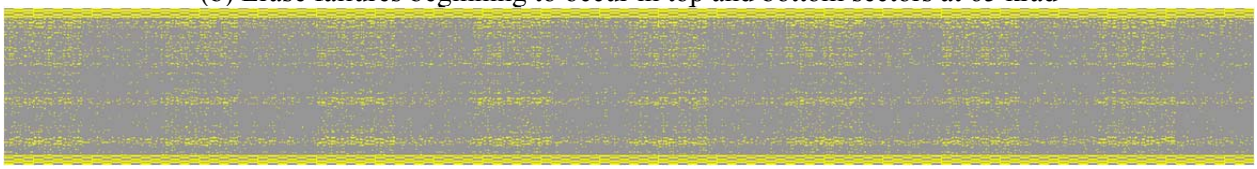


(c) Only the top and bottom sectors have failed at 68 krad

Figure 39. The erase failure monitoring (yellow dots) for block 6 (all zeros pattern) of chip 1.

(a) No failures observed at 51 krad

(b) Erase failures beginning to occur in top and bottom sectors at 65 krad

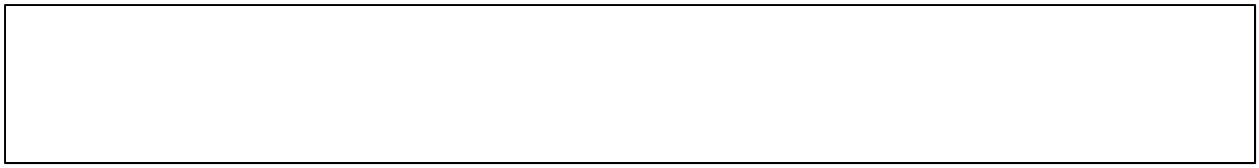


(c) Erase failures beginning to in all sectors at 106 krad

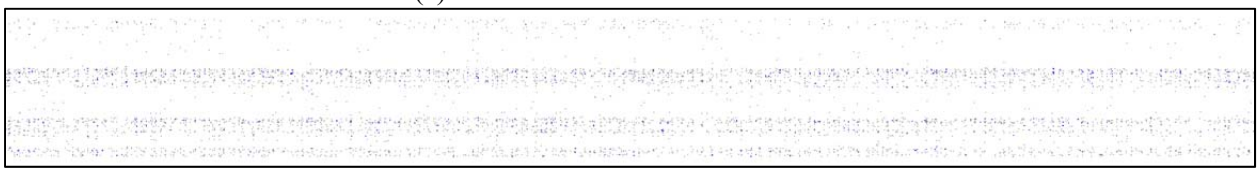
Figure 40. The erase failure monitoring for block 4 (checkerboard pattern) of chip 1.

Programming Operation

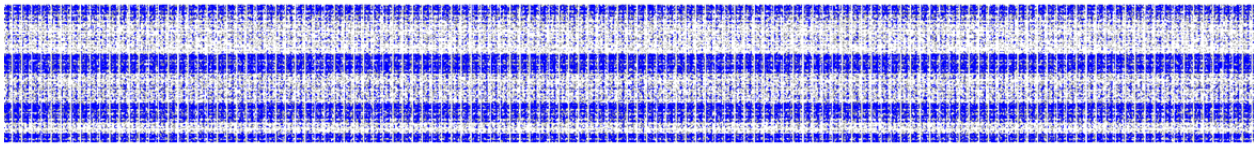
Chip 1, the initially powered chip, stopped successfully programming at around 90 krad (see Table 5 and, for example, Figure 38). This implies that had we selected a 90 krad power-on time for Chip 2 and avoided the use of the top and bottom sectors since their erase capability fails early, the programming capability could have been maintained until in excess of 300 krad (see Figure 41 and Table 5), but once again, chip-to-chip variability must be considered.



(a) No failures observed at 317 krad



(c) Significant number of programming failures at 331 krad



(c) At 344 krad, it is clearly seen that the top and bottom sectors are not logged as programming failures since the erase operation has already failed in those sectors

Figure 41. The programming failure monitoring for block 6 (all zeros pattern) of chip 2.

Read Operation

In terms of the read-only results shown in Figure 42 and Figure 43, the read failures in Blocks 7 and 8 of Chip 1 do not occur until 150 and 177 krad, which would permit activating the unbiased C2 in time to take over the functionality to ensure continuous flash memory availability. In fact, the dose required to have 1% of the C1 Blocks 7 and 8 memories unreadable was 244 and 258 krad(Si), respectively (see Figure 44 and Figure 45). This limited number of read errors could be mitigated using error detection and correction codes, which were not employed in this testing. The conclusion that extended operation of the eFlash in a read-only mode is viable is further confirmed by the fact that Blocks 7 and 8 of C2 do not exhibit their first read failures until 210 and 238 krad(Si), respectively (see Table 5).

Summary

In summary, if the top and bottom memory sectors are left unused, then the limiting operation is programming, which based on the results presented in Table 5 occurs after 90 krad to 230 krad is delivered while the chip is powered. The difference in these two dose thresholds (90 krad and 330–100 = 230 krad correspond to C1 and C2, respectively) is indicative of the potential variability in COTS device radiation response. The variability in the radiation resilience of this power gating approach is termed as the “life extension” in Table 5, which shows that the variability in individual operations results ranges from 60 krad (read) to 240 krad (program).

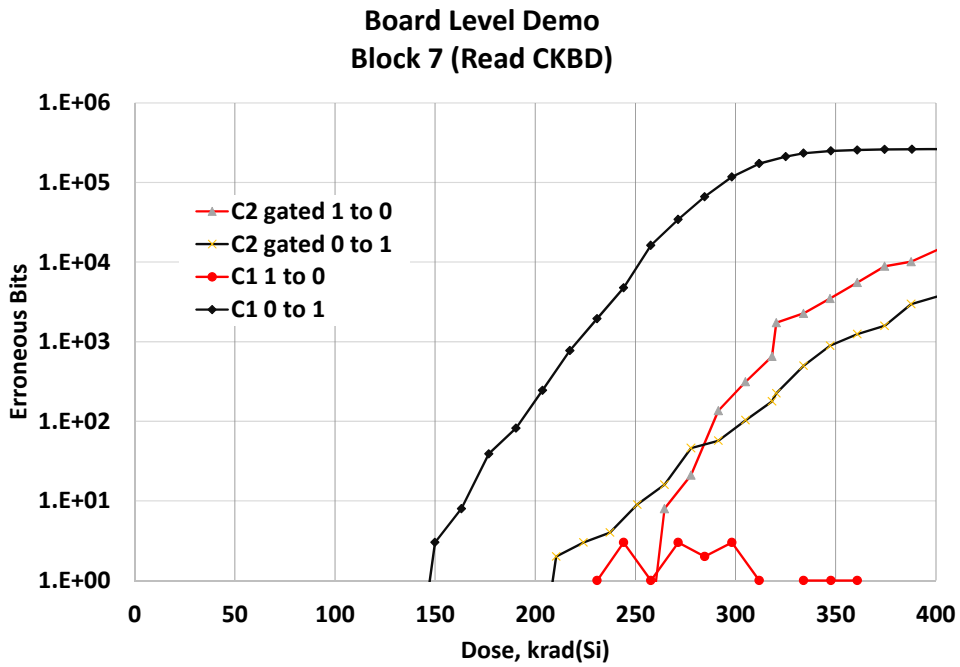


Figure 42. Representative irradiation results from both chips for Block 7, which only read periodically. Read (0 to 1) errors are observed in C1 and C2 at 150 and 210 krad, respectively.

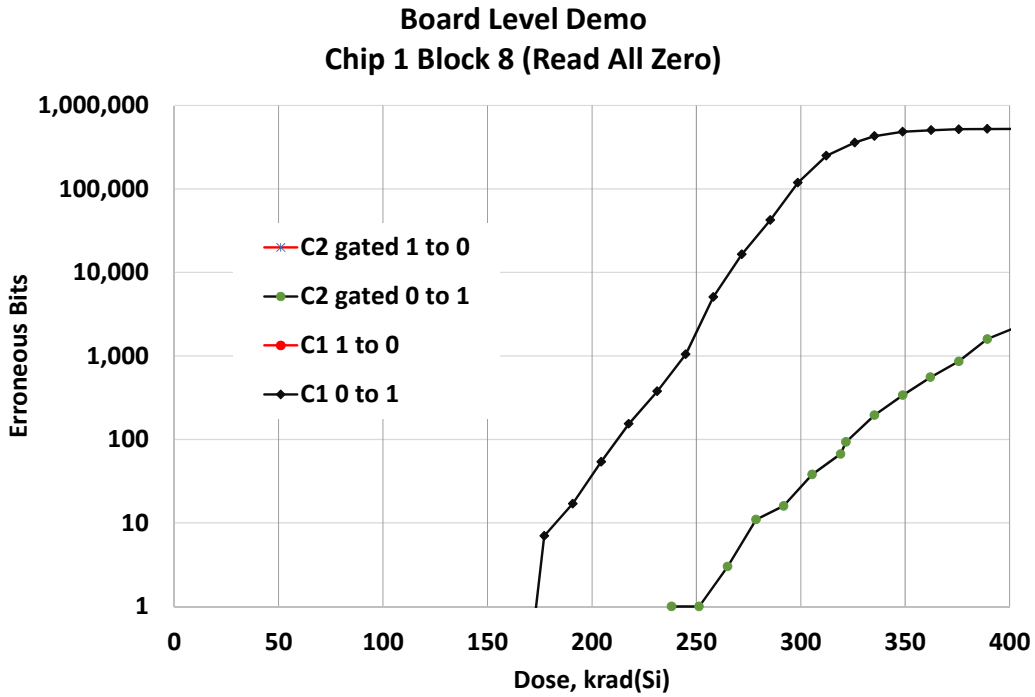
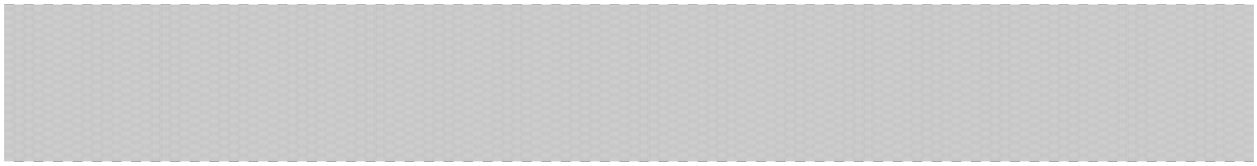
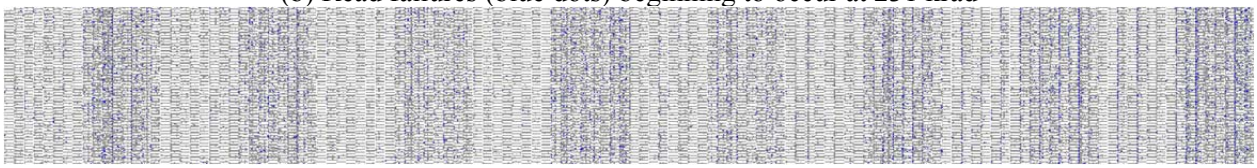


Figure 43. Representative irradiation results from both chips for Block 8, which only read periodically. Read (0 to 1) errors are observed in C1 and C2 at 177 and 238 krad, respectively.

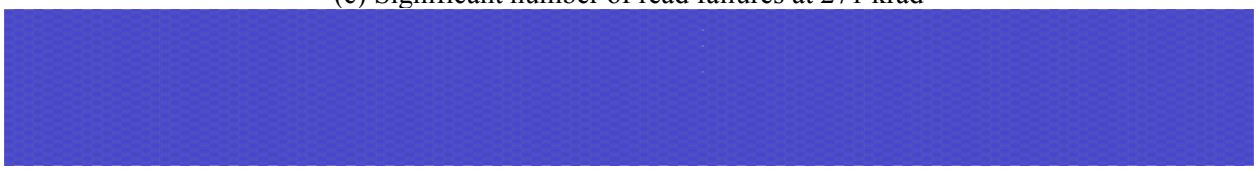


(a) No failures observed at 136 krad

(b) Read failures (blue dots) beginning to occur at 231 krad



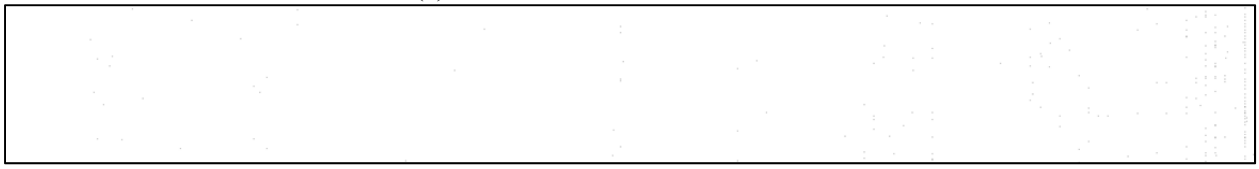
(c) Significant number of read failures at 271 krad



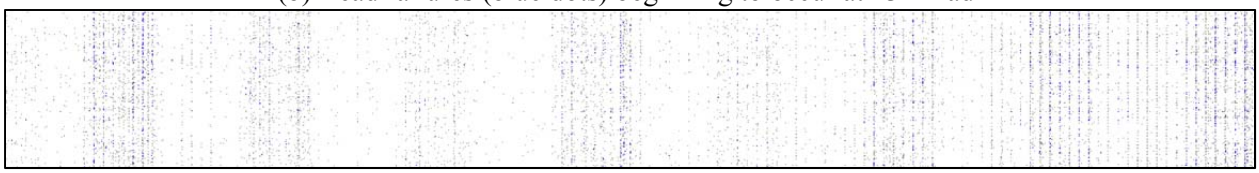
(d) All zero bits experiencing read failures (0 to 1) at 455 krad

Figure 44. The read failure monitoring for block 7 (checkerboard pattern) of chip 1.

(a) No failures observed at 164 krad



(b) Read failures (blue dots) beginning to occur at 231 krad



(c) Significant number of read failures at 271 krad

(d) All zero bits experiencing read failures (0 to 1) at 470 krad

Figure 45. The read failure monitoring for block 8 (all zeros pattern) of chip 1.

3.3 Task 2: ASIC Design and Fabrication

In parallel with the COTS effort, the application-specific integrated circuit (ASIC) provided a second pathway to ensure the success of this project. This ASIC effort was co-sponsored by Space Micro, and Microchip Inc. supported the tape-out. The ASIC itself is an extension of prior work for the Air Force [31].

The ASIC test die, shown in Figure 46, is 4 mm × 4 mm. The design uses the 90-nm TSMC LP (Taiwan Semiconductor Manufacturing Company low power) process. The design contains two Silicon Storage Technology (SST is a Microchip company) eFlash macros, shown on the left side. This work was facilitated by our access to the SST / Microchip embedded flash IP. The eFlash macros have separate power supplies to determine total ionizing dose (TID) impact independent of the surrounding logic. Each memory block includes 3.28 M-bits with 512 bytes per sector, and a 32-bit interface. The test chip rating is 100,000 minimum sector endurance (erase/program cycles), and a 100 years retention time.

The chip also incorporates EDAC and power gating features to investigate possibility of error correction. The EDAC uses the Bose, Chaudhuri, Hocquenghem (BCH) algorithm, which was chosen based on schedule rather than our confirmation that it is the best approach. Separate on-die NMOS and PMOS power gating structures are provided to determine viability of gating flash power for longer TID lifetime.

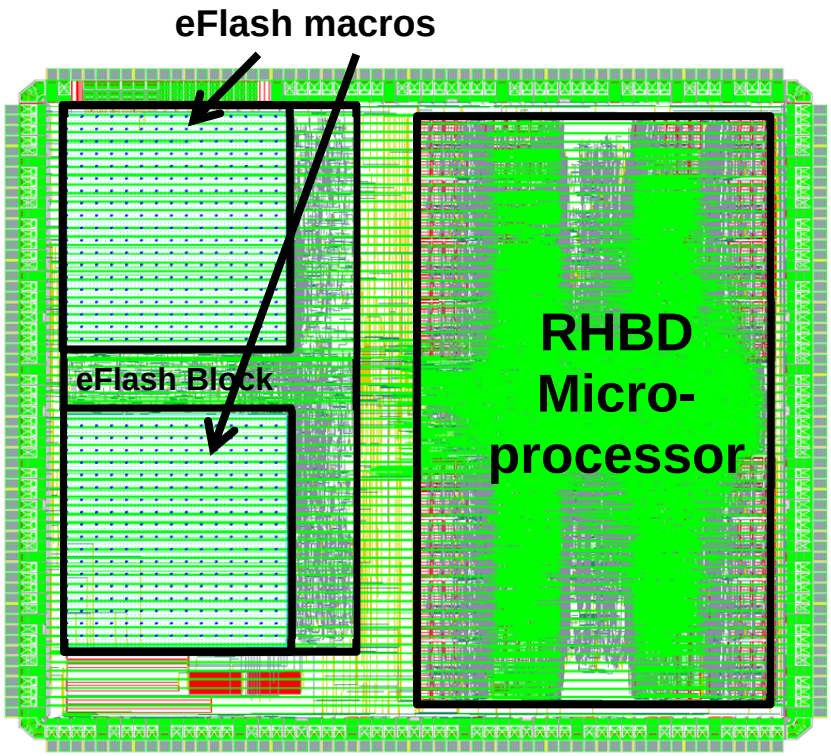


Figure 46. ASIC test die. The radiation hard by design (RHBD) processor is apparent at the right (in the black outline). At the left are two non-radiation hardened Microchip/SST flash macro blocks.

The ASIC design was fabricated at the TSMC foundry via a Microchip corporate shuttle run. The fabricated test chips were then packaged into 224 pin ceramic PGA (pin grid array), cavity up packages. The chips were tested using a field-programmable gate array (FPGA) to interface with the test chips, see Figure 47.

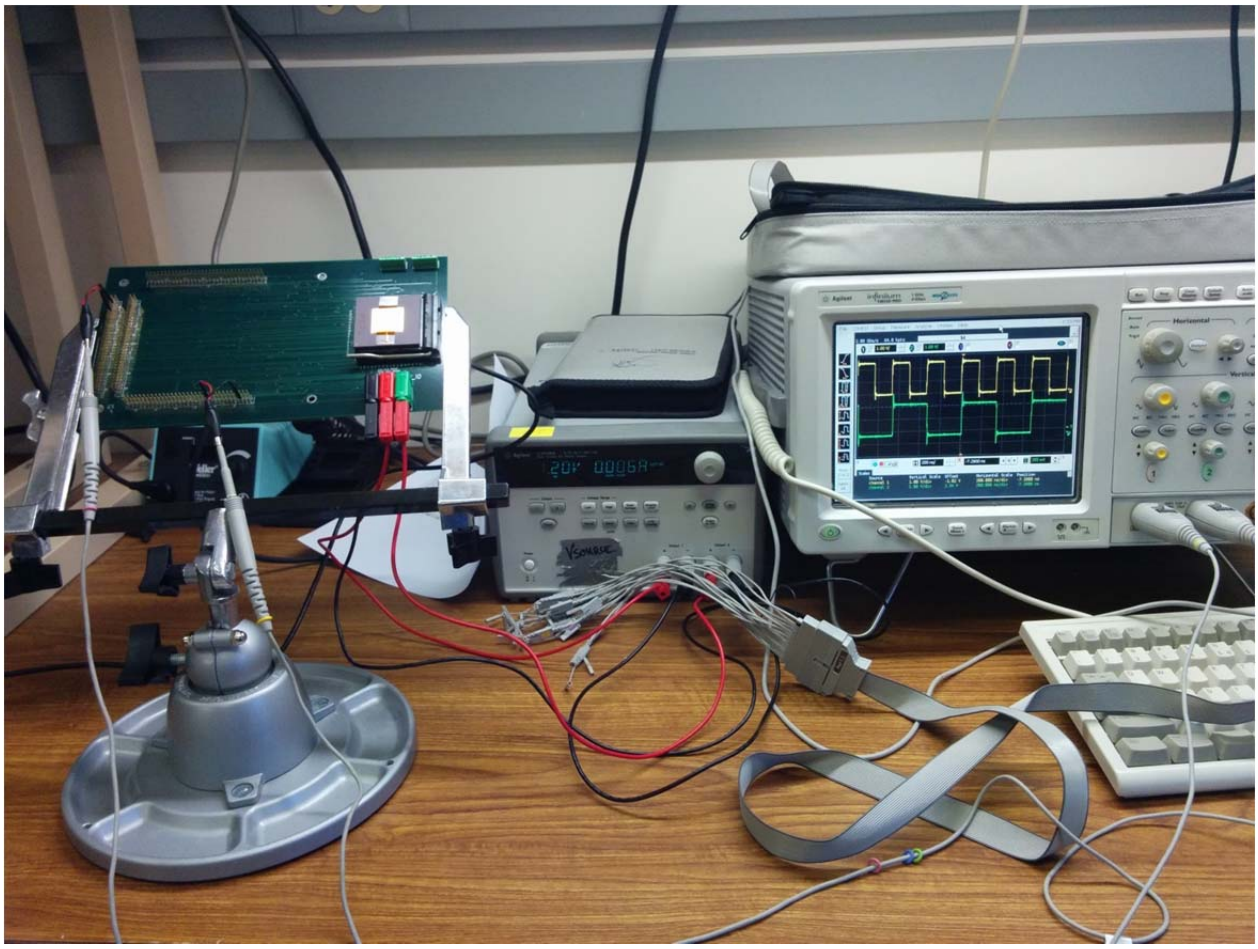


Figure 47. ASIC under bench test on a daughter card being driven by a FGPA.

3.4 Task 4: ASIC Characterization

Task 4 of the project was devoted to the characterization of the application-specific integrated circuit (ASIC) from Task 2, which comprised the ASIC design and fabrication effort.

As shown in Figure 48, the ASIC was irradiated within a ^{60}Co Gammacell with a dose rate of 430 rad(Si)/min. The FPGA used to monitor the ASIC was located outside the irradiator as pictured in Figure 49.

3.4.1 ASIC Microprocessor Radiation Performance

The radiation hard by design (RHBD) microprocessor was expected to perform well in the ionizing radiation environment as prior testing on the devices and circuits within the

microprocessor had demonstrated operation to 1 Mrad. In fact, the radiation testing here showed that the microprocessor is fully functional to at least 2.5 Mrad (whereas the COTS devices failed catastrophically at < 100 krad). Data that are more detailed are available from the eFlash testing because the amount of ribbon cabling required to pass through the irradiation access (cable feedthrough) port is limiting (see Figure 48 and Figure 49). That is, the microprocessor had to be bench tested after irradiation, whereas the in situ monitoring via the ribbon cabling was dedicated to the eFlash since earlier radiation testing in this project had shown the eFlash to be the limiting component.

In addition to the gamma-ray irradiation, several ASIC chips were subjected to neutron irradiation at the Los Alamos Neutron Science Center (LANSCE) in late 2015. That testing was funded by a different program and was dedicated to determining the impact of single event effects, rather than TID, on the chips. Those data are yet to be analyzed.

Figure 48. ASIC just before placement into the Gammacell irradiation chamber.

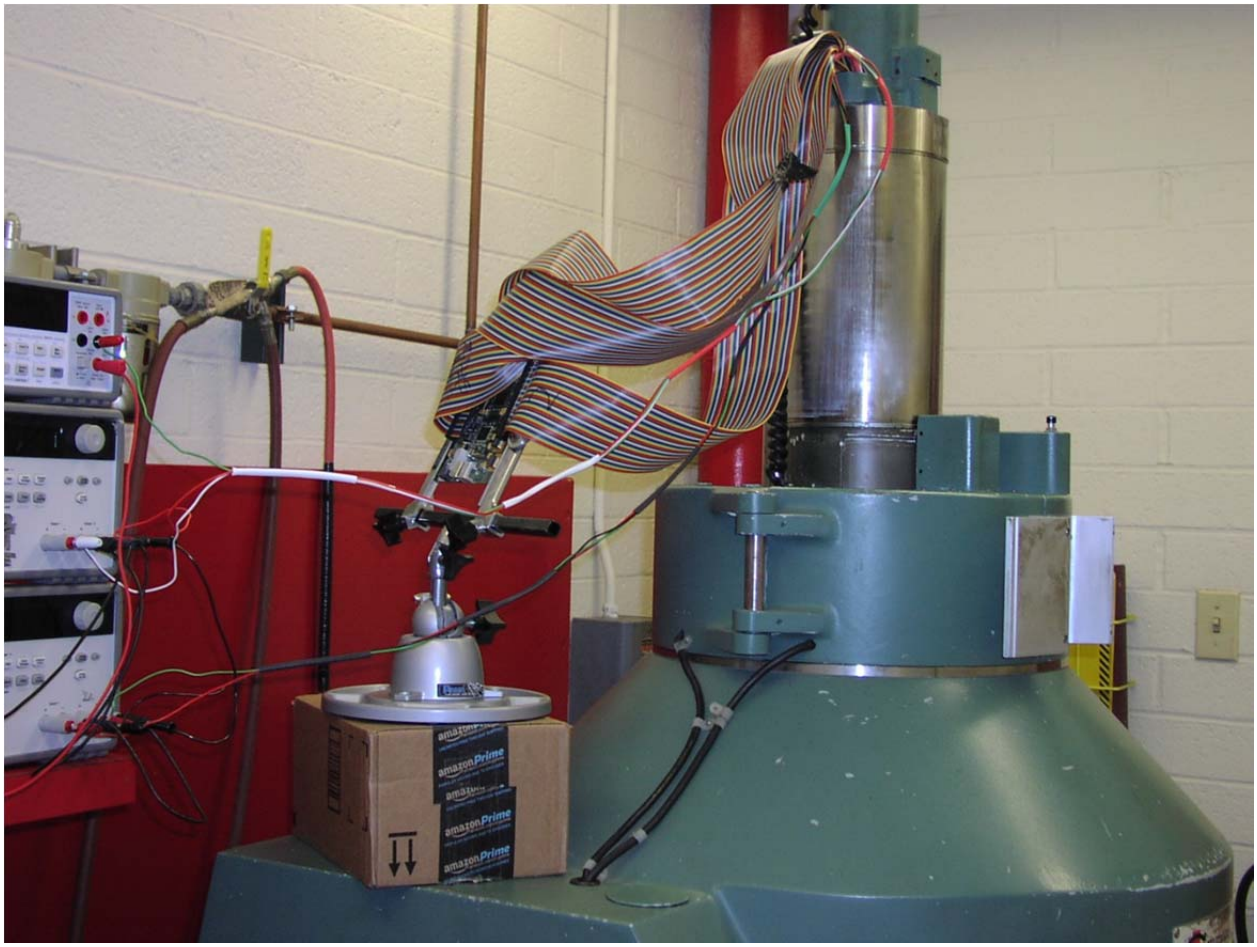


Figure 49. Using four ribbon cables, the FPGA is connected to the ASIC, which has been positioned within the irradiation chamber. Power supplies are located to the left on the red bench.

3.4.2 ASIC eFlash Radiation Performance

The eFlash was not RHBD but rather used existing IP to which we had access. For the ASIC eFlash, all memory operations (erase, program and read) were exercised and tested during the irradiation. The eFlash is divided into two memory banks with 53,247 words of 64 bits each. Prior to irradiation, the memory banks were erased, then read to verify the erase, and finally programmed and read again to verify the programming. During the irradiation, the first memory bank was erased and programmed whereas the second memory bank was read only. To better simulate the variability in bit patterns expected during operation, individual memory bytes were programmed with data equal either to their address in memory, or to the inverse of their address.

Figure 50 shows the TID test results from the second radiation test of the ASIC, dubbed TC24. The current to the chip was monitored during the TID experiments, and as seen in Figure 51, the current only increased from 0.346 mA to 0.414 mA at a dose of 435 krad(Si) indicating an acceptable amount of leakage given the substantial radiation dose.

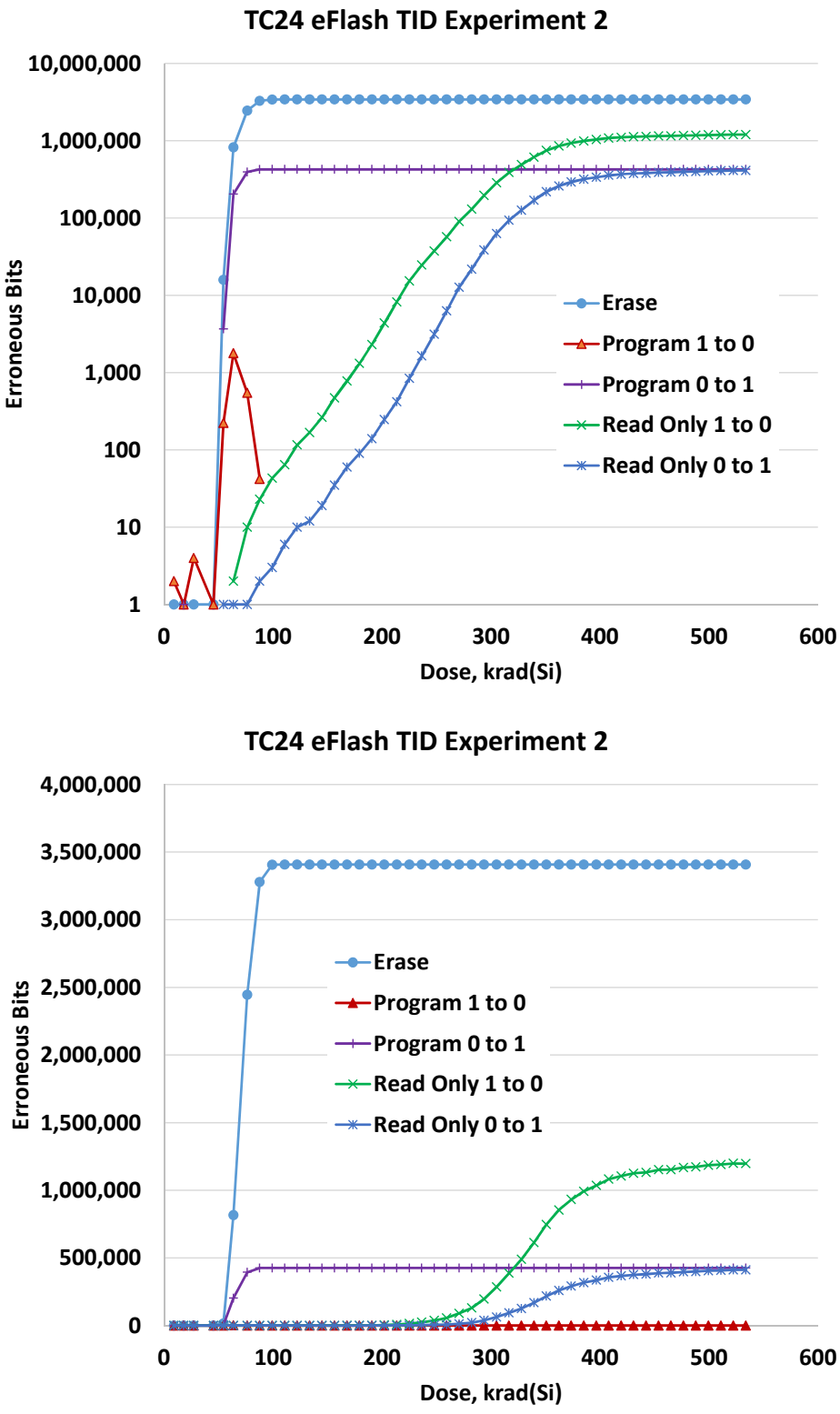


Figure 50. Embedded flash test results from the second radiation test of an ASIC chip (linear and semilogarithmic ordinate scales).

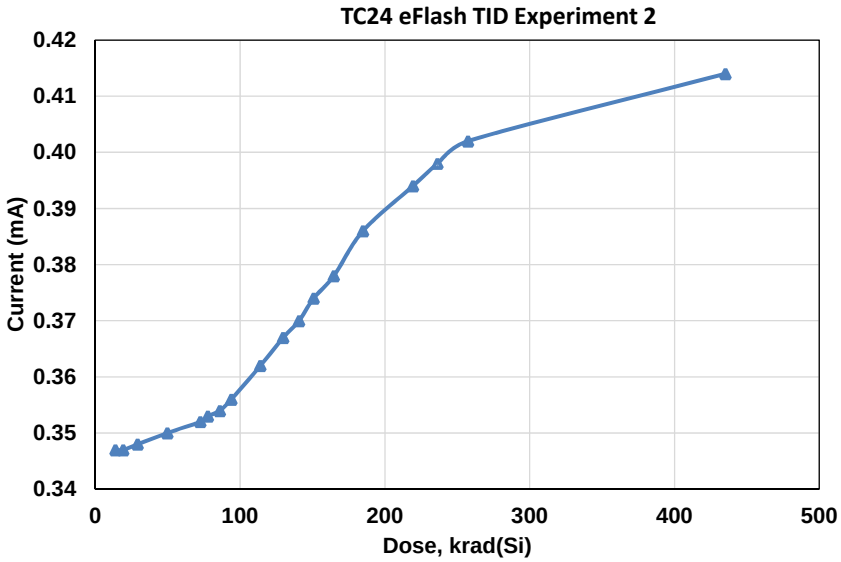


Figure 51. Measured current to chip during from the second radiation test of an ASIC chip.

Erase Operation

As seen in Figure 52, the first erase failures are recorded at 54.6 krad(Si), which is consistent with the commercial flash cards tested in Tasks 1 and 3 of this project (e.g., see Table 5). However, unlike the COTS flash cards that were previously tested, the top and bottom sectors did not experience early erase failure, rather erase failures were distributed throughout the memory, but with some rows exhibiting a pattern of failures as shown in Figure 53. This result is due to a different high voltage distribution network in the embedded IP versus the commercial product. Note also that the interface was intentionally designed with some bits reversed (to determine a locked up block due to single event latchup) and that is why there are obvious column based patterns evident.

Program Operation

As seen in Figure 50 and Figure 54, the 0 to 1 programming errors are manifest at 54.6 krad(Si), which coincides with the dose at which the erase operation begins to exhibit errors. Unlike a commercial product that omits marginal cells from usage after production, our testing utilized all memory cells from the yield regardless of their fabrication quality. This may explain some of the early 1 to 0 program failures as those cells represent about 0.05% of the entire memory (hence, a log scale is used in the upper graph of Figure 50). Because an accurate programming operation depends on the prior erasure of memory, the program operation radiation resiliency is intrinsically tied to the erase operation survivability. In the case of the COTS memory, the fact that the middle sectors (between top and bottom sectors) continued to erase properly to ~100 krad permitted a greater TID and a more exact determination of the dose at which the programming operation is no longer valid. Figure 55 shows the wide distribution of programming failures throughout the memory

Figure 52. Erase failures (a few red dots) in second radiation test of ASIC eFlash at dose of 54.6 krad(Si).

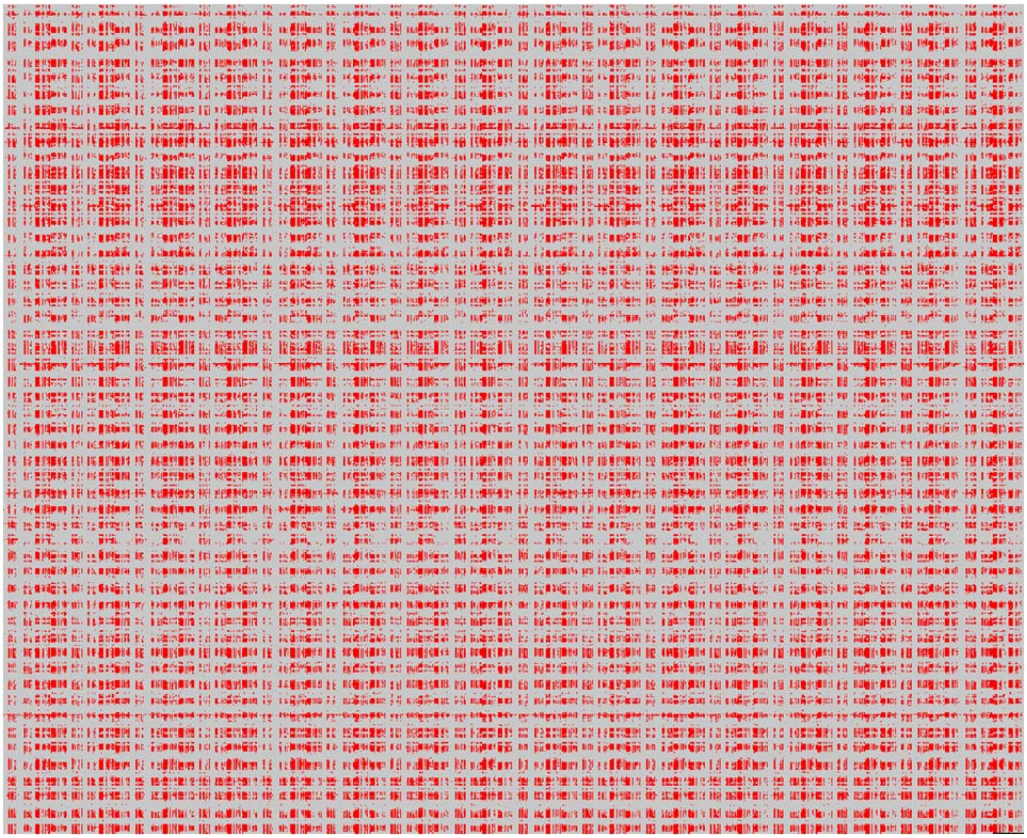


Figure 53. Erase failures (red dots) in second radiation test of ASIC eFlash at dose of 63.7 krad(Si).

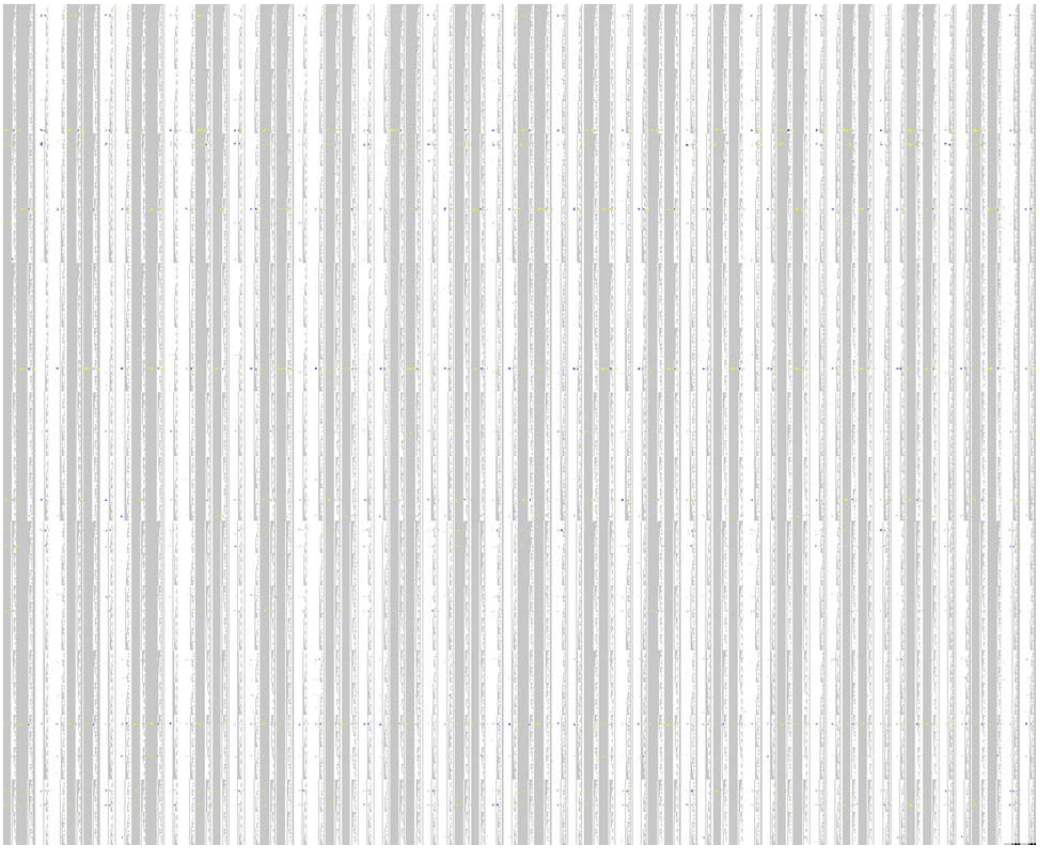


Figure 54. Program failures (the few yellow and blue dots) in second radiation test of ASIC eFlash at dose of 54.6 krad(Si).

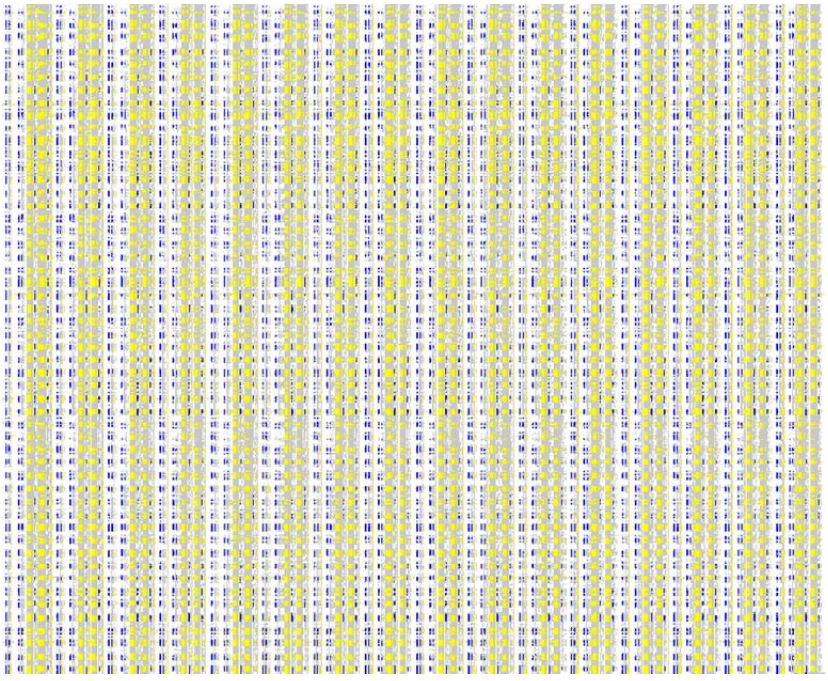


Figure 55. Program failures (yellow and blue dots) in second radiation test of ASIC eFlash at dose of 63.7 krad(Si). Yellow dots represent 0 to 1 fails; blue dots are 1 to 0 errors.

Read Operation

The first read failures from the second (read-only) memory block occur at 54.6 and 63.7 krad(Si), respectively, for 0 to 1 and 1 to 0 read errors. From Section 3.2, the dose required to have 1% of the COTS memory appear unreadable was ~250 krad(Si). Similar results were obtained for the ASIC as ~240 krad(Si) rendered about 1% of the read-only memory in error; for example see Figure 56. Although the radiation resiliency of the ASIC in the read-only access mode is not quite as good as the results from the COTS eFlash, again it should be recognized that post-production testing of commercial eFlash restricts the weak/marginal cells from being placed into use.

In order to investigate the potential usefulness of error detection and correction (EDAC) for the read-only memory, the number of bits in error within each 64-bit word of the memory was determined and graphed as shown in Figure 57. Although the first 0 to 1 and 1 to 0 read errors were recorded at 54.6 and 63.7 krad(Si), respectively, the graph shows that these initial errors are single bit errors, which are easy to correct with EDAC. The first 2-bit errors (both 0 to 1 and 1 to 0), which would require greater overhead to correct, begin to appear at 145 krad(Si). The first 3-bit errors were 1 to 0 errors and first appear at 168 krad(Si).

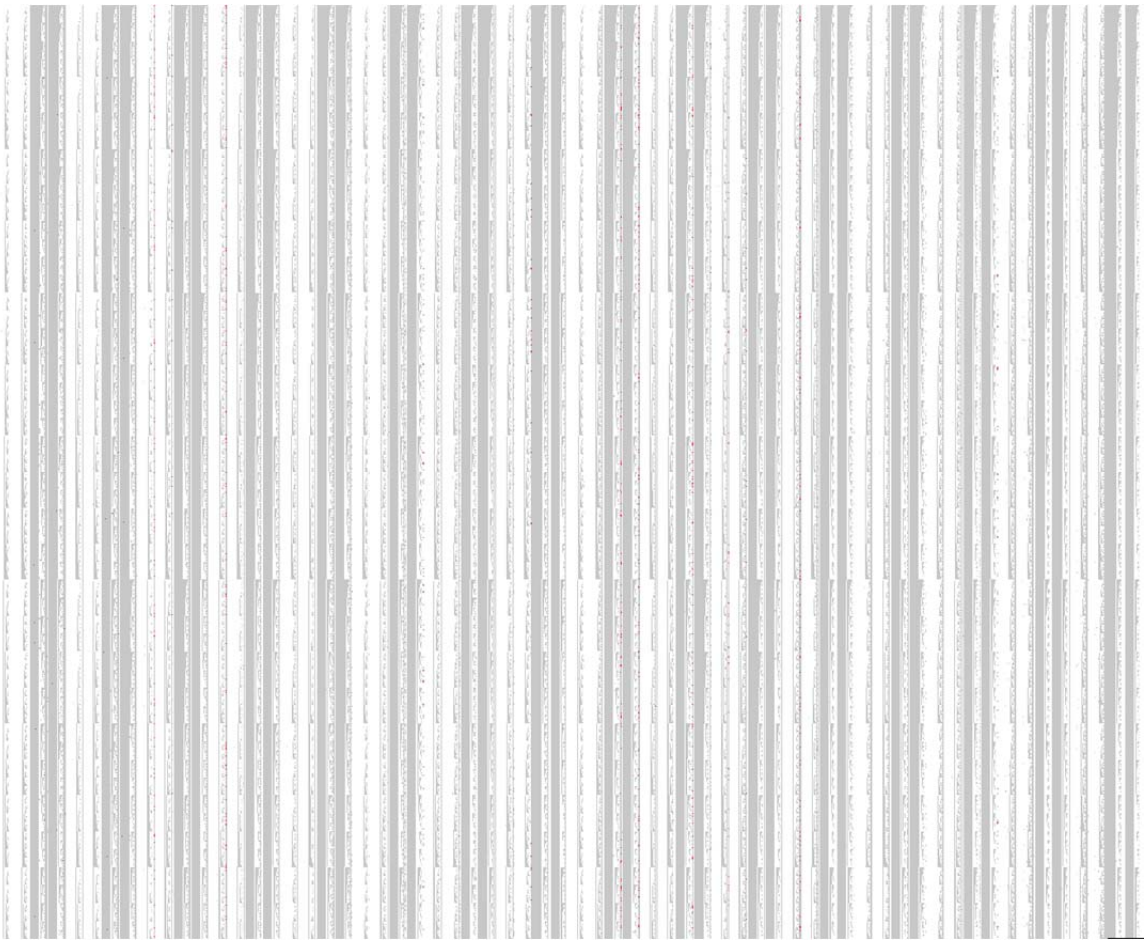


Figure 56. Read failures (the red dots) in second radiation test of ASIC eFlash at dose of 225 krad(Si).

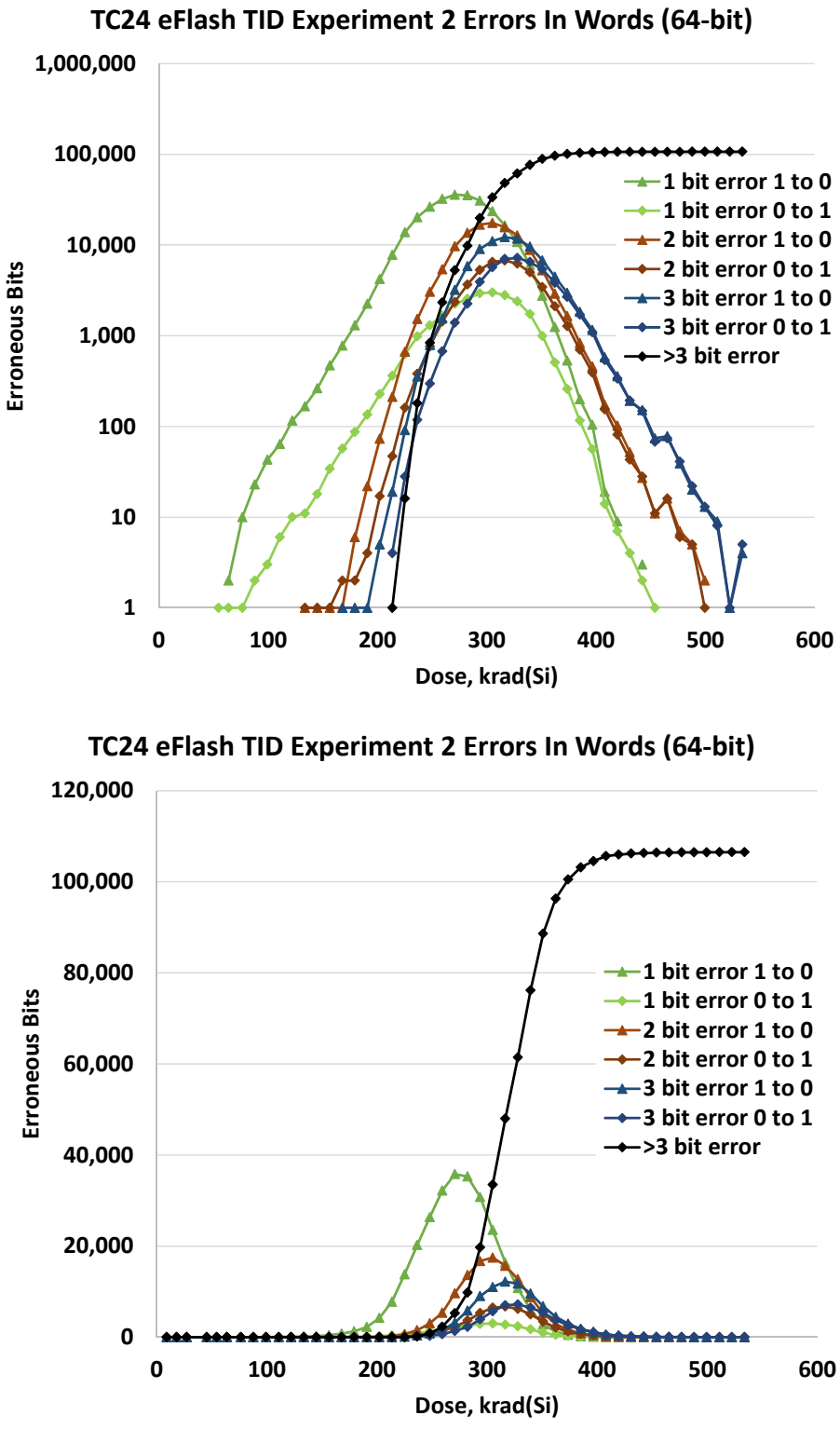


Figure 57. Read errors in the embedded flash from the second ASIC radiation test (linear and semilog scales). The read errors are categorized in terms of the error type and number of errors in a 64-bit word.

3.5 Task 5: Reporting and Dissemination

Project reporting activities included attendance and presentation at the DOE Advanced Sensors and Instrumentation (ASI) monthly review meetings held online. Similarly, presentations were made at the ASI 2-day I&C Annual Review webinars in fall 2014 and 2015. In addition, monthly reports were submitted via DOE PICS:NE. Furthermore, an article was written for the ASI Newsletter (Issue 2, February 2015).

Besides an annual report and this final report, project results have been disseminated to date at the American Nuclear Society (ANS) Nuclear Plant Instrumentation, Control & Human-Machine Interface Technologies (NPIC&HMIT) conference [20], the IEEE Nuclear and Space Radiation Effects Conference (NSREC) [21], and within the *IEEE Transactions on Nuclear Science* [22]. In addition, a provisional patent application has been filed [23].

4. SUMMARY

Ionizing radiation is intrinsic to the entire nuclear energy fuel cycle. The pervasive use of electronic systems demands devices that can withstand significant radiation exposure. The nuclear power industry needs to be able to benefit from the advancements in the semiconductor industry that have led to low-cost ubiquitous devices. This project is contributing to the deployment of state-of-the-art electronics that can improve the reliability, sustain the safety, and extend the life of current reactors. The full station blackout experience at Fukushima shows the necessity for emergency sensing capabilities in a radiation-enhanced environment.

This project developed radiation hard by design (RHBD) electronics using commercially available technology employing commercial off-the-shelf (COTS) devices and present generation circuit fabrication techniques to improve the total ionizing dose (TID) hardness of electronics. These methods will facilitate the long-term viability of radiation-hard electronics and robotic systems, thereby avoiding obsolescence issues being experienced in the nuclear power industry. For example, the nuclear industry with its low purchasing power does not drive the semiconductor industry strategic plans, and the rapid advancements in electronics technology can leave legacy systems stranded.

We have determined (physics based) specific failure mechanisms for eFlash arrays (prior work has been behavior based). We have correlated the mechanisms between temperature and radiation effects (both of which involve leakage). Determining limits to the technology and understanding the exact mechanisms have allowed better determination of the efficacy of different system level mitigation approaches for circuits destined for severe nuclear radiation environments.

Our ASIC microprocessor using RHBD techniques was irradiated and shown to be fully functional after an exposure of 2.5 Mrad whereas the COTS units failed catastrophically at <100 krad. The eFlash memory has proven less resilient with the TID limit dependent on whether the devices are operated in a read-only or fully programmable mode with the former being more rad hard due to the lower voltages required. To extend the operable life of the eFlash, a combination of power gating and redundancy were employed in a demonstration board that exhibited radiation hardness to over 200 krad.

APPENDICES

A. SUMMARY OF COTS FLASH ELEVATED TEMPERATURE TESTING

Test	Brief Test Description	Operations at Elevated Temperature Plateaus			Brief Test Results		Post Elevated Temperature Behavior
		Erase	Program	Read	First Error	Error Description	
1	64 Mbit Flash, program and read 5's, A's, 0's and F's	Once	Once	Once	125 °C*	Only 1→0 errors	n/a
2	64 Mbit Flash, program and read 5's, A's, 0's and F's Read and program separate	Once	Three times	Three times	145 °C	Only 1→0 errors	Readable after returning to room temperature.
3	64 Mbit Flash, program and read 5's, A's, 0's and F's Read and program separate	Once	Three times	Three times	145 °C	Only 1→0 errors. When temperature was temporarily reduced to 120 °C, errors remained. Experiment stopped at 175 °C.	Performed read-only operation the next day at room temperature, the errors remained. But upon re-programming, the errors were corrected.
4	Flash was divided into 8 blocks, 32K words each. Each block consists of two diagonals of 128 by 128 words each, half 0's and half 1's	Once	Three times	Three times	160 °C	Only 1→0 errors. When temperature was temporarily reduced to 120 °C, errors remain when read; however, upon re-programming at 120 °C, the errors are corrected. Experiment stopped at 175 °C.	n/a
5	One block of 32K words is exercised. The block consists of two diagonals of 128 by 128 words each, half 0's and half 1's. 0's and 1's inverse program/erase/read also performed at each temperature step.	Twice	Twice	Six times	n/a	Problem with heater. Failed to obtain any data from the experiment	n/a

* Note that a capacitor on the backside of the flash card inhibited optimal coupling between the heater and the board. This capacitor was removed for subsequent experiments, and additional silicone insulation was used in Experiments 2–4 to ensure more accurate and stabilized temperature measurements.

Test	Brief Test Description	Operations at Elevated Temperature Plateaus			Brief Test Results		Post Elevated Temperature Behavior
		Erase	Program	Read	First Error	Error Description	
6	One block of 32K words is exercised. The block consists of two diagonals of 128 by 128 words each, half 0's and half 1's. 0's and 1's inverse program/erase/read also performed in every temperature step.	Twice	Twice	Six times	165 °C	Only 1→0 errors. No errors are found caused by erasure. Data are read correctly from the prior temperature step before 165 °C. Redundant read is performed after programming at each temperature step, error count stays almost the same.	n/a
7	32K words of data are filled with pre-generated random numbers. Total number of 0's and 1's is balanced on purpose.	Once	Once	Three times	165 °C	Only 1→0 errors. No errors are found caused by erasure. Data are read correctly from the prior temperature step before 165 °C. Redundant read is performed at each temperature step, error count stays almost the same.	n/a
8	16 Mbit of 64 Mbit memory size is tested. Data are either all 0's or all 1's.	Twice	Twice	Five times	165 °C	Error appeared at the first step of 165 °C (read to verify prior temperature). 12 errors (16-bit word) are reported. Both 0 to 1 and 1 to zero errors reported in this experiment. At 175 °C, before finishing experiment, temperature from the sensor dropped to room temperature. A hole in the heater was found.	n/a
9	4 Mbit of 16 Mbit memory size is tested. Data are either all 0's or all 1's	Twice	Twice	Five times	n/a	No error is reported. Temperature dropped again when heater was set to 175°C, same problem as heater experiment 8. Checking the heater and flash daughter card, a hole on the heater was found. The copper pad from the removed capacitor may be the reason for making a hole in the heater.	n/a

B. SUMMARY OF COTS FLASH IRRADIATION EXPERIMENTS

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
1	a – Powered – 1 Mb	Once	Once	Continuous with ~ 2 min cycle			151 krad	Only 1→0 errors. Word line leakage	Errors virtually gone, but later re-use caused reappearance of the errors
	b – Unpowered – 1 Mb			None (not applicable), as board was unbiased during irradiation			At 201 krad there were already 4839 errors	Only 0→1 errors. Cell leakage	Minimal errors, but phenomenon returned and data line became stuck
2[†]	a – 16 Mb	Twice	Program	n/a	n/a	Read only with ~1 min interval	~200 krad	The first errors are 1→0, but eventually 0→1 errors dominate	n/a
	b – 16 Mb	Twice	Program	n/a	n/a		~200 krad		n/a
	c – 16 Mb	Twice	Program	n/a	n/a		~200 krad		n/a
3	Powered – 16 Mb	Twice	Program	Once	1 to 4 times	Read with ~15 min interval	~105 krad		n/a
4	Repeat of Experiment 1a, but to larger dose	Once	Once	Continuous with ~ 2 min cycle			~130 krad	Eventually 0→1 errors occurred; 0xF error rate rose more slowly	n/a
5	Sector A – 16 Mb (program and read 4 times per 180-min cycle starting at t=0)	1 to 4 times	1 to 4 times	1 to 4 times	1 to 4 times	Four per 180-min cycle	~312 krad	Errors start with 1→0 errors, but eventually 0→1 errors dominate	n/a
	Sector B – 16 Mb (read-only once per 180-min cycle starting at t=180 min)	1 to 4 times	1 to 4 times	n/a	n/a	Once per 180-min cycle	~370 krad		

[†] Experiment 2 used three different boards in succession because of an error counter problem in the diagnostic software.

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
	Sector C – 16 Mb (read-only 3 times per 180-min cycle starting at *t*=90 min)	1 to 4 times	1 to 4 times	n/a	n/a	Three per 180-min cycle	~298 krad		
6	Sector A – 16 Mb (program and read 3 times per 232-min cycle starting at *t*=0)	1 to 4 times	1 to 4 times	1 to 4 times	1 to 4 times	Three per 232-min cycle	~318 krad	Errors start with 1→0, eventually 0→1 errors dominate	n/a
	Sector B – 16 Mb (read-only once per 232-min cycle starting at *t*=450 min)	1 to 4 times	1 to 4 times	n/a	n/a	Once per 232-min cycle	~238 krad		
	Sector C – 16 Mb (read-only 3 times per 180-min cycle starting at *t*=0)	1 to 4 times	1 to 4 times	n/a	n/a	Three per 232-min cycle	~337 krad		
7	Flash was divided into 8 blocks, 32K words each. Each block consists of two diagonals of 128 by 128 words each, half 0's and half 1's	Once	None	Erase by block	By block pattern, 1; 1,2; 1,2,3…	By block pattern, 1; 1,2; 1,2,3…	From blocks 0 to 7, first-error doses are 152, 153, 158, 167, 184, 201, 202, 270 krad, respectively	Errors form unique triangles along the diagonals of the blocks	n/a
8	Flash was divided into 8 blocks, 32K words each. Each block consists of two diagonals of 128 by 128 words each, half 0's and half 1's. In addition, 0's and 1' inversed operations are performed.	Once	None	Erase by block	By block pattern, 1; 1,2; 1,2,3…	By block pattern, 1; 1,2; 1,2,3…	From blocks 0 to 7, doses are 68, 71, 73, 76, 165, 167, n/a‡, n/a, krad, respectively	Number of 1→0 errors is much larger the number of 0→1 errors	n/a
9	Flash was divided into 8 blocks, 32K words each. Memory is filled with pre-generated random numbers. Total number of 0's and 1's are balanced on purpose.	Once	None	Erase by block	By block pattern, 1; 1,2; 1,2,3…	By block pattern, 1; 1,2; 1,2,3…	From blocks 0 to 7, doses are 76, 81, 91, 111, 115, 119, 125, 319 krad, respectively	Erase errors are reported inaccurately due to program bugs.	n/a

‡ No errors from that block are reported during the experiment.

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
10	Flash was divided into 5[§] blocks, 32K words each. Memory is filled with pre-generated random numbers. Total number of 0's and 1's are balanced on purpose. In addition, 0's and 1's inversed operations performed.	Once	None	Erase by block	By block pattern, 1; 1,2; 1,2,3…	By block pattern, 1; 1,2; 1,2,3…	From block 0 to 4, first erase error doses are 67, 68, 73, 80, 90; inversed read error 70, 72, 80, 89, 98; normal read, 71, 73, 74, 82, 92 krad	Erase errors reported. First erase error appeared at 67 krad. Some data lost due terminal software problem.	n/a
11	16 MB Flash was divided into 8 blocks (4 to 11, 0 to 3 are not used due to non-uniform block size). Every block is 128 by 256 16-bit words. Patterns are as follows: block 4 to 11, (4) erased and then programmed 0x0000, read-only during experiment, (5) erase at the start, read-only during experiment, (6) erased then diagonal, erased again then inverse diagonal, (7) erase and then diagonal, (8) erase on diagonal programming, (9) erase the entire block and program to 0, then read in every cycle, (10) erase and read, program top half to 0x0000 and read, erase and read, bottom half program to 0x0000 and read, (11) erase and read every cycle	Once	None	From block 4 to 11: 1, 1, 2 per cycle, 1 per cycle, 1 per cycle, 1 per cycle, 2 per cycle, 1 per cycle	From block 4 to 11: 1, 0, 2 per cycle, 1 per cycle, 1 per cycle, 1 per cycle, 2 per cycle, 1 per cycle	From block 4 to 11: 1, 1, 2 per cycle, 1 per cycle, 1 per cycle, 1 per cycle, 2 per cycle, 1 per cycle	From block 4 to 11: 269, n/a[**], 109.5, 136.5, 100.5, 108, 108.5, n/a[††] krad	From block 4 to 11: 0 to 1 errors (read errors), n/a, erase error, erase error, erase error, erase error, n/a	Ran the whole test program again 24 hours later at room temperature after pulled up from Gammacell; it reported the blocks are F's.

[§] It will take more than 24 hours to reach block 5 due to flash programming algorithm.
[**] Block 5 stopped reporting results after 3 cycles in the Gammacell, reason still not clear.
[††] No errors are reported on block 11 before we stopped the experiment.

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
12	7 blocks of 16 MB Flash are used (4 to 10, 0 to 3 are not used due to non-uniform block size). Every block is 128 by 256 16-bit words. Patterns are as follows: block 4 to 11, (4) erased and then programmed 0x0000, read-only during experiment, (5) erase at the start, read-only during experiment, (6) erased, read then diagonal, (7) erase 2 times, read then diagonal, (8) erase 4 times then diagonal, (9) erase 16 times, read then diagonal, (10) erase and read, program with checkerboard (start with 0), erase and read, then inverse checkerboard	Once	None	Number of operations per cycle (from block 4 to 10): 1, 1, 1, 2, 4, 16, 2	Number of operations per cycle (from block 4 to 10): 1, 0, 1, 1, 1, 1, 2	Number of operations per cycle (from block 4 to 10): 2, 2, 2, 2, 2, 2, 2, 4	From block 4 to 10: 220, n/a[‡‡], 114, 115, 116, 117, 97 krad	From block 4 to 10: program failure, n/a, erase failure, erase failure, erase failure, erase failure.	Increased voltage to 4 V and erased again. Erase failure reduced.
13	6 blocks of 16 MB Flash are used (4, 5, 6, 10, 20 and 30). Every block is 128 by 256 16-bit words. Patterns are as follows: (4) checkerboard, read-only during experiment, (5) erase and read, then checkerboard erase and read, then inverse checkerboard, (6) erase and read, then diagonal, erase and read, then inverse diagonal, (10) programmed checkerboard, read-only, (20) erase and read, then checkerboard, erase and read, then inverse checkerboard, (30) erase and read, then diagonal,	Once	None	Number of operations per cycle: 0, 2, 2, 0, 2, 2	Number of operations per cycle: 0, 2, 2, 0, 2, 2	Number of operations per cycle: 1, 4, 4, 1, 4, 4	From block 4 to 30: n/a[§§], 50, 73, 241, 74, 76 krad	From block 4 to 30: n/a, erase errors, erase errors, 0 to 1, erase failure, erase failure	n/a

[‡‡] No errors observed until end of the test at 261 krad.
[§§] Date not correct due to code bugs.

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
	erase and read, then inverse diagonal								
14	Perform erase suspension experiment at low voltage while the chip is irradiated	n/a	n/a	At 80 krad, the chip is programed at 3.3 V and then an erase is initiated once the chip is powered by 2.0 V. The erase is suspended and read before being resumed. There is a 5 µs delay between erase/resume and suspension. This is done a total of 8 times.			n/a	At 2.0V and 80 krad, the chip was by mistake programmed incompletely due to there being too low a voltage. Even so, the bits that were programmed did not erase and the erase operation was non-functional. The voltage was increased to 2.5V for the next erase at 105 krad. The erase went too quickly so the voltage was reduced to 2.2V for the erase performed at 125 krad. By this point it is assumed that the charge	n/a

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
								pump was already not providing the full voltage and the erase did not occur. The voltage was brought back up to 2.6V at 150 krad but by this dose 2.6V was not enough to erase the block	
15 Trial 1	Two chips are preprogrammed before being exposed to radiation.	Blocks 5,7 left erased	Blocks 4,6 Program-med with 0X0000	Both chips are left unbiased in gamma radiation until a 60 krad dose is reached. One chip is biased and the following operations are performed: Block 4 is read, then erased 8 times, read for verification, then programmed with 0x0000 8 times, and read for verification. Block 5 is read, then erased one time and read to verify, then programmed with 0x0000 8 times, read for verification, then erased 8 times and read for verification. Block 6 is read, then erased 16 times, read for verification, then programmed with 0x0000 16 times, and read for verification. Block 7 is read, then erased one time and read to verify, then programmed with 0x0000 16 times, read for verification, then erased 16 times and read for verification. At roughly 120 krad once sufficient failure in the first chip is reached, the second chip is biased and the same above operations are			Chip 1: 1st erase errors at 120 krad At 140 krad Erase failures in complete top and bottom sectors in all blocks. Chip 2: first erase errors (not full sectors) at 197 krad in block 7, 199 krad in block 4, 204 krad in block 6 (sectors 0 and 15), and 205 krad in block 5	Conclusion inferred from two trials in test 15: Leaving the flash unbiased increases the survivability of the chip. This means that a robot can have its program on numerous chips left unbiased, swapping to a new chip at sufficient failure. This may be only up to a critical	n/a

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
				performed. Experiment concludes when sufficient failure is reached in the second chip			(sectors 0 and 15)	failure point; chip 3 did have catastrophic failure at 210 krad. The program and erase states of memory cells appeared to have no effect on the survivability.	
15 Trial 2	Three chips are preprogrammed before being exposed to radiation.	Blocks 5,7 left erased	Blocks 4,6 Program-med with 0X0000	All chips are left unbiased in gamma radiation until a ~60 krad dose is reached. One chip is biased and the following operations are performed: Block 4 is read, then erased 8 times, read for verification, then programmed with 0x0000 8 times, and read for verification. Block 5 is read, then erased one time and read to verify, then programmed with 0x0000 8 times, read for verification, then erased 8 times and read for verification. Block 6 is read, then erased 16 times, read for verification, then programmed with 0x0000 16 times, and read for verification. Block 7 is read, then erased one time and read to verify, then programmed with 0x0000 16 times, read for verification, then erased 16 times and read for verification. At roughly 120 krad once sufficient failure in the first chip is reached, the second chip is biased and the same above operations are performed. Once sufficient failure is reached in the second chip, the third chip is biased and the same previous operations are performed. Experiment concludes when sufficient failure is reached in the third chip.			Chip 1: testing begins at 55 krad (1st erase failure) B5: 130 krad Complete sector failure (top and bottom) B7: 136 krad B4: 137krad B5: 143 krad Chip 2: testing begins at 144 krad B7: 193 krad B4: 194 krad B5: 198 krad B6: 200 krad Chip 3: testing begins at 204 krad. Fails to program (catastrophic failure) after 210 krad despite no erase failures.		n/a

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
16 Trial 1	Chips are preprogrammed before being exposed to radiation. Stopped experiment at 375 krad since all computer memory used up.	Blocks 5, 7 and 9 left in the erased state	Blocks 4, 6 and 8 pre-program-med with 0x0000	Chip is left unbiased until 140 krad Chip becomes biased and the following operations are performed: Block 4 is read, then erased 8 times, read for verification, then programmed with 0x0000 8 times, and read for verification. Block 5 is read, then erased one time and read to verify, then programmed with 0x0000 8 times, read for verification, then erased 8 times and read for verification. Block 6 is read, then erased 16 times, read for verification, then programmed with 0x0000 16 times, and read for verification. Block 7 is read, then erased one time and read to verify, then programmed with 0x0000 16 times, read for verification, then erased 16 times and read for verification. Blocks 8 and 9 are read only.			Chip powered at 144 krad First Erase failures B7: 202 krad B4: 204 krad B5: 207 krad B6: 209 krad Program Failures: B4: 338 krad B5: 356 krad B6: 367 krad B7: 371 krad No read failures up to 375 krad.		n/a
16 Trial 2	Same as above	Same as above	Same as above	Same as above			Chip powered at 144 krad Erase failures B4: 200 krad B7 :208 krad B5: 212 krad B6: 216 krad Program failures B5: 356 krad B4: 381 krad B6: 410 krad B7: 414 krad Block 9 failed to read at 392 krad Block 8 not		n/a

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
							read because of typo.		
17	Test the survival of unbiased read-only memory. An unbiased period up to 150 krad. Block 4 is programmed with 0x0000 prior to radiation, block 5 is left in erased state prior to radiation, and block 6 is programmed with CKBD prior to radiation.	From block 4 to 6: once, once, once	From block 4 to 6: once, zero, once	0	0	1	From block 4 to 6: 322, n/a[***], 150 krad	From block 4 to 6: read error, n/a, read error	n/a
18	Test the survival of unbiased read-only memory. No unbiased period. Block 4 is programmed with 0x0000 prior to radiation, block 5 is left in erased state prior to radiation, and block 6 is programmed with CKBD prior to radiation.	From block 4 to 6: once, once, once	From block 4 to 6: once, zero, once	0	0	1	From block 4 to 6: 271, 289, 201 krad	For block 6 CKBD: first 1 to 0 error at 201 krad; first 0 to 1 error at 266 krad	n/a
19	To observe the effect of elevated temperature and radiation on the flash memories. The flash memory was heated up to 120 ºC in the Gammacell. Patterns are as follows: B4) erased, read, programmed with all 0x0000, read; B5) erased, read, programmed with all 0x0000, read; B6) erase, read, program with CKBD, read; B7) erase, read, program with CKBD, read; B8) programmed all 0x0000, read-only; B9) programmed	From block 4 to block 10: once, once, once, once, once, once, once	From block 4 to block 10: once, once, once, once, once, once, once	Number of operations per cycle (from block 4 to block 10): 1, 1, 1, 1, 1, 1, 1	Number of operations per cycle (from block 4 to block 10): 1, 1, 1, 1, 1, 1, 1	Number of operations per cycle (from block 4 to block 10): 2, 2, 2, 2, 1, 1, 1	From block 4 to 10: 179, 194, 125, 105, 135, 163, 164 krad	From block 4 to 10: erase error, program error, erase error, erase error, read error, read error, read error.	n/a

[***] No read errors observed.

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results		Post-Irradiation (anneal) Behavior
		Erase	Program	Erase	Program	Read	First Error	Description	
	CKBD, read-only; B10) programmed CKBD[†††], read-only.								
20	To observe the effect of elevated temperature and radiation on the flash memories. The flash memory was heated up to 120 ºC in the Gammacell. Patterns are as follows: B4) erased, read, programmed with all 0x0000, read; B5) erased, read, programmed with all 0x0000, read; B6) erase, read, program with CKBD, read; B7) erase, read, program with CKBD, read; B8) programmed all 0x0000, read-only; B9) programmed CKBD, read-only; B10) erased all 0xFFFF state, read-only.	From block 4 to block 10: once, once, once, once, once, once, once	From block 4 to block 10: once, once, once, once, once, once, once	Number of operations per cycle (from block 4 to block 10): 1, 1, 1, 1, 1, 1, 1	Number of operations per cycle (from block 4 to block 10): 1, 1, 1, 1, 1, 1, 1	Number of operations per cycle (from block 4 to block 10): 2, 2, 2, 2, 1, 1, 1	From block 4 to 10: 111, 103, 105, 108, 183, 163, 424 krad	From block 4 to 10: erase error, erase error, erase error, erase error, read error, read error, read error.	n/a

[†††] Suppose to be all 0xFFFF pattern, programmed to CKBD pattern due to a bug in the customized code.

C. SUMMARY OF COTS MICROCONTROLLER IRRADIATION EXPERIMENTS

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results
		Erase	Program	Erase	Program	Read	
1	PIC24FJ128GA010 (16-bit processor) calculating primes and summation of primes. Access to built-in flash memory with external clock.	1 to 4 times	1 to 4 times	n/a	n/a	Once every 1- min cycle	Setup runs with 3.3 V power supply. Starts reboot by itself at ~20 krad, external clock experienced catastrophic failure inside the Gammacell.
2	PIC24FJ128GA010 (16-bit processor) calculating primes and summation of primes. Access to built-in flash memory with internal clock	1 to 4 times	1 to 4 times	n/a	n/a	Once every 1-min cycle	Setup runs with 3.3 V power supply. Starts rebooting by itself at ~66 krad.
3	a. PIC32MX360F512L (32-bit processor) calculating primes and access to built-in flash memory.	1 to 4 times	1 to 4 times	n/a	n/a	Once every 1-min cycle	Setup runs with 3.3 V power supply. Starts rebooting by itself at ~42 krad.
	b. PIC24FJ128GA010 (16-bit processor), unbiased	n/a	n/a	n/a	n/a	n/a	Found to be functioning correctly after removal at a total dose of 68.2 krad. It was returned to the irradiation chamber for an additional 15 krad (unbiased also), and upon testing it at the 83 krad dose, it was found to be inoperable.
4	SST89V54RD (8-bit processor) calculating primes and summation	n/a	n/a	n/a	n/a	Once every 1 min cycle	Stopped outputting at 48 krad using 5 V supply
5	SST89V54RD (8-bit processor) calculating primes and summation	n/a	n/a	n/a	n/a	Once every 1 min cycle	Stopped outputting at 64 krad using 3.3 V supply

Test	Brief Test Description	Pre-irradiation Operations		Operations During Irradiation			Brief Results
		Erase	Program	Erase	Program	Read	
6	SST89V54RD (8-bit processor) calculating primes and summation	n/a	n/a	n/a	n/a	Once every 1 min cycle	Stopped outputting at 82 krad using 2.6 V supply
7	SST89V54RD (8-bit processor) calculating primes and summation	n/a	n/a	n/a	n/a	Once every 1 min cycle	Stopped outputting at 67 krad using 3 V supply.
8	SST89V54RD (8-bit processor) calculating primes and summation	n/a	n/a	n/a	n/a	Once every 1 min cycle	Stopped outputting at 63 krad using 3.3 V supply. Very similar failure dose as for Test 5 under the same conditions.
10	PIC32MX360F512L (32-bit processor) calculating prime numbers only.	n/a	n/a	n/a	n/a	n/a	Start reboots by itself at 50.8 krad using 2.3 V supply.

REFERENCES

1. C. Y. Wu, "A scalable split-gate flash memory cell structure and its contactless flash memory arrays," *J. Science and Engineering Tech.*, vol. 1, no. 1, 2005, pp. 5-16.
2. S. Fong, J. Ariyoshi, and T. Ema, "Embedded flash on a low-power 65-nm logic technology," *IEEE Elec. Dev. Let.*, vol. 33, no. 9, Sept. 2012, pp. 1261-1264.
3. D. N. Nguyen, S. M. Guertin, G.M. Swift, and A.H. Johnston, "Radiation effects on advanced flash memories," *IEEE Trans. on Nuclear Science*, vol. 47, no. 6, Dec. 2000, pp. 2183-2188.
4. D. N. Nguyen, C.I. Lee and A.H. Johnston, "Total ionizing dose effects on flash memories," *IEEE Radiation Effects Data Workshop Record*, 1998, p. 100.
5. P. C. Bennett, L. D. Posey, RHOBOT: Radiation Hardened Robotics, Sandia National Laboratories, SAND97-2405, October 1997.
6. W. Xin, K. E. Holbert, L. T. Clark, "Single Event Upset Mitigation Techniques for FPGAs Utilized in Nuclear Power Plant Digital Instrumentation and Control," *Nuclear Engineering and Design*, vol. 241, no. 8, pp. 3317-3324, August 2011.
7. T. Nakamura, M. Baba, E. Ibe, Y. Yahagi, H. Kameyama, *Terrestrial Neutron-Induced Soft Errors In Advanced Memory Devices*, World Scientific, 2008.
8. K. Oka, K. Shibanuma, "Development of a radiation-proof robot," *Advanced Robotics*, vol. 16, no. 6, 2002, pp. 493-496.
9. T. Moore, "Robots for nuclear power plants," *IAEA Bulletin*, vol. 27, no. 3, Autumn 1985, pp. 31-38.
10. K. Nagatani, S. Kiribayashi, Y. Okada, K. Otake, K. Yoshida, S. Tadokoro, T. Nishimura, T. Yoshida, E. Koyanagi, M. Fukushima, S. Kawatsuma, "Emergency response to the nuclear accident at the Fukushima Daiichi nuclear power plants using mobile rescue robots," *Journal of Field Robotics*, vol. 30, no. 1, 2013, pp. 44-63.
11. S. Kawatsuma, M. Fukushima, T. Okada, "Emergency response by robots to Fukushima-Daiichi accident: summary and lessons learned," *Industrial Robot: An International Journal*, vol. 39, no. 5, 2012, pp. 428-435.
12. R. T. Johnson, F. V. Thome, C. M. Craft, "A survey of aging of electronics with application to nuclear power plant instrumentation," *IEEE Trans. on Nuclear Science*, vol. 30, no. 6, Dec. 1983, pp. 4358-4362.
13. J. R. Schwank, M. R. Shaneyfelt, P. E. Dodd, Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits: Radiation Environments, Physical Mechanisms, and Foundations for Hardness Assurance, Sandia National Laboratories, SAND-2008-6851P.
14. D. M. Fleetwood, P. V. Dressendorfer, D. C. Turpin, "Reevaluation Of Worst-Case Postirradiation Response For Hardened MOS Transistors," *IEEE Trans. on Nuclear Science*, vol. 34, no. 6, Dec. 1987, pp. 1178-1183.
15. T. Stanley, D. Neamen, P. Dressendorfer, J. Schwank, P. Winokur, M. Ackermann, K. Jungling, C. Hawkins, W. Grannemann, "The effect of operating frequency in the

radiation induced buildup of trapped holes and interface states in MOS devices," *IEEE Trans. on Nuclear Science*, vol. 32, no. 6, Dec. 1985, pp. 3982-3987.

16. V. Ferlet-Cavrois, T. Colladant, P. Paillet, J. L. Leray, O. Musseau, J. R. Schwank, M. R. Shaneyfelt, J. L. Pelloie, and J. du Port de Poncharra, "Worst-case bias during total dose irradiation of SOI transistors," *IEEE Trans. on Nuclear Science*, vol. 47, no. 6, Dec. 2000, pp. 2183-2188.
17. J. Sejvar, "Normal operating radiation levels in pressurized water reactor plants," *Nuclear Technology*, vol. 36, no. 1, Nov. 1977, pp. 48-55.
18. R. T. Johnson, F. V. Thome, C. M. Craft, "Aging of electronics with application to nuclear power plant instrumentation," *IEEE Trans. on Nuclear Science*, vol. 31, no. 1, Feb. 1984, pp. 721-725.
19. R. T. Johnson, F. V. Thome, C. M. Craft, Survey of the State-of-the-Art in Aging of Electronics with Application to Nuclear Power Plant Instrumentation, NUREG/CR-3156, SABD82-2559, Sandia National Laboratories, Albuquerque, NM, 1983.
20. K. E. Holbert, L. T. Clark, Y. Chen, I. N. Zavatkay, J. W. Adams, "Rad Hardening Commercial Off-the-Shelf Microcontrollers Destined For I&C Applications In Severe Nuclear Environments," *Proceedings of the ANS International Topical Meeting on Nuclear Plant Instrumentation, Control and Human-Machine Interface Technologies*, Charlotte, NC, February 21-26, 2015, pp. 363-372.
21. L. T. Clark, K. E. Holbert, J. W. Adams, B. C. Anderson, H. Navale, "Evaluation of 1.5-T Cell Flash Memory Total Ionizing Dose Response," IEEE Nuclear and Space Radiation Effects Conference, Boston, MA, July 13-17, 2015.
22. L. T. Clark, K. E. Holbert, J. W. Adams, H. Navale, B. C. Anderson, "Evaluation of 1.5-T Cell Flash Memory Total Ionizing Dose Response," *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, December 2015, pp. 2431-2439.
23. L. T. Clark, J. Adams, K. E. Holbert, "Secure true random number generation using 1.5-T transistor flash memory," U.S. Provisional Patent Application No. 62/232,736, filed Sept. 25, 2015.
24. SST39VF1601C / SST39VF1602C Data Sheet DS-25018A, 16 Mbit Multi-Purpose Flash Plus, Silicon Storage Technology, Inc., May 2011, p. 17.
25. M. J. Kay, M. J. Gadlage, A. R. Duncan, D. Ingalls, A. Howard, and T. R. Oldham, "Effect of accumulated charge on the total ionizing dose response of a NAND flash memory," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2945-2951, Dec. 2012.
26. G. Cellere, A. Paccagnella, S. Lora, A. Pozza, G. Tao, and A. Scarpa, "Charge loss after ^{60}Co irradiation of flash arrays," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, pp. 2912-2916, Oct. 2004.
27. N. Mielke and J. Chen, "Reliability of flash nonvolatile memories," *Int. J. of High Speed Electronics and Syst.*, vol. 11, no. 3, pp. 719-750, Sept. 2001.
28. Silicon Storage Technology, Inc., SuperFlash EEPROM Technology, Revised March 1999.

29. Y. Tkachev, X. Liu, and A. Kotov, “Floating-gate corner-enhanced poly-to-poly tunneling in split-gate flash memory cells,” *IEEE Trans. Elec. Dev.*, vol. 59, no. 1, pp. 5-11, Jan. 2012.

30. S. Gerardin, M. Bagatin, A. Paccagnella, K. Grürmann, F. Gliem, T. R. Oldham, F. Irom, D. N. Nguyen, “Radiation effects in flash memories,” *IEEE Trans. Nuc. Sci.*, vol. 60, no. 3, June 2013, pp. 1953-1969.

31. L. Clark, D. Patterson, C. Ramamurthy, K. Holbert, “An Embedded Microprocessor Radiation Hardened by Microarchitecture and Circuits,” *IEEE Transactions on Computers*, vol. 65, no. 2, February 2016, pp. 382-395.