Development and Industrialization of InGaN/GaN LEDs on Patterned Sapphire Substrates for Low Cost Emitter Architecture

Final Technical Report

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1. Executive summary

Patterned sapphire substrate (PSS) technology has proven to be an effective approach to improve efficacy and reduce cost of light-emitting diodes (LEDs). The volume emission from the transparent substrate leads to high package efficiency, while the simple and robust architecture of PSS-based LEDs enables low cost. PSS substrates have gained wide use in mid-power LEDs over the past years.

In this project, Lumileds has developed and industrialized PSS and epitaxy technology for high-power flip-chip LEDs to bring these benefits to a broader range of applications and accelerate the adoption of energy-efficient solid-state lighting (SSL). PSS geometries were designed for highly efficient light extraction in a flip-chip architecture and high-volume manufacturability, and corresponding sapphire patterning and epitaxy manufacturing processes were integrally developed. Concurrently, device and package architectures were developed to take advantage of the PSS flip-chip die in different types of products that meet application needs.

The developed PSS and epitaxy technology has been fully implemented in manufacturing at Lumileds' San Jose, CA location, and incorporated in illumination-grade LED products that have been successfully introduced to the market, including LUXEON Q and LUXEON FlipChip White.

2. Objective and accomplishments

2.1. Objective

The objective of this project was to establish and industrialize a low-cost patterned sapphire substrate (PSS) high-power LED fabrication process with demonstrated epitaxial growth of InGaN layers capable of producing best-in-class lumens per dollar (lm/$) and lumens per watt (lm/W) performance when combined with low-cost packaging methods.

Lumileds' state-of-the-art InGaN high-power LED architecture involves fabricating a thin-film flip-chip device (TFFC) supported by a metalized ceramic submount. This process involves a series of steps to enable efficient light extraction including (1) flip-chip attaching the LED die, (2) under-filling the die with a reflective support material, (3) removing the sapphire substrate by laser liftoff, and (4) photo-electrochemically roughening the GaN surface. The alternative approach developed this project involves leaving the InGaN layers on their sapphire substrate to simplify the die fabrication process and enable simpler packages that utilize the sapphire as mechanical support, thereby reducing the LED package cost. Lumileds has been actively engaged in PSS die activities prior to this project. In these preceding efforts we demonstrated PSS-based emitters with efficacy performance lagging that of their TFFC counterparts by approximately 3-5%. Closing this gap was one of the aims of this project to ensure the commercial viability of the simplified PSS-based emitter architectures.

The proposed approach was to meet the project objective by (1) developing and optimizing a manufacturing process for patterning and etching sub-micron features in sapphire, (2) designing and creating PSS features tailored for highly efficient light extraction in a flip-chip architecture, (3) optimizing the epitaxial growth of GaN layers on PSS features which are aggressively designed for high light extraction, and (4) demonstrating efficient die/packaging architectures for manufacturing high-performance illumination products at a significantly reduced cost.

The final efficacy and cost targets are an efficacy of 130 lm/W at a correlated color temperature

(CCT) of 3000K, a color rendering index (CRI) greater than 80, a junction temperature of 85 °C and a current density of 35 A/cm^2 from a PSS-based LED package; and a package cost that is 25% lower than the cost of an equivalent TFFC-based LED package.

2.2. Summary of accomplishments

The PSS fabrication and epitaxial growth processes described above have been developed and industrialized in San Jose, CA. The technology enables manufacturing cost reduction at the emitter and module levels combined with best-in-class lm/W performance meeting the objectives of the project. The following significant accomplishments were made:

- Down-selection and fabrication of new PSS patterns;
- Implementation of automated visual inspection in PSS manufacturing;
- Industrialization of PSS epitaxy growth processes on all major reactor platforms;
- Wafer-level LED fabrication yield comparable to process of record epitaxial wafers;
- Realization of 4-5% gain in light output attributed to PSS improvements vs. baseline PSS performance at the beginning of the project;
- Demonstration of PSS 1 mm^2 emitter performance (in LUXEON Q package) exceeding TFFC 1 mm^2 counterparts (in LUXEON Rebel package) in multiple fabrication runs;
- Release of the developed technology into PSS-based illumination-grade LED products (LUXEON Q and LUXEON FlipChip White);
- Efficacy demonstration of 131 lm/W at a CCT of 3000K, CRI greater than 80, temperature of 85 °C and current density of 35 A/cm2 from a PSS-based LED package, meeting the final efficacy target;
- Realization of a PSS-based chip-scale package (CSP) white LED with 26% lower cost than a TFFC LED with the same die size, meeting the final cost target;
- Development of a PSS-based next-generation emitter architecture enabling further cost reduction of high-performance LEDs for directional applications.

3. Project activities

3.1. Predictive modelling of the effect of sapphire pattern geometry on the extraction efficiency of PSS flip chip devices

Simulations of light output (LOP) have been performed for PSS geometries produced in our facility by both dry- and wet-etching of sapphire. Modelling in this task has shown that the LOP performance associated with the best-known, dry-etch morphologies can be reasonably approximated with a new wet-etch methodology developed at Lumileds. LOP gains over Lumileds' baseline PSS pattern were predicted to be approximately 2.8% based on the initial simulations. These simulations guided the selection of candidate PSS geometries for experimental verification.

3.2. Optimization and characterization of photolithography for PSS fabrication

The performance of Lumileds' i-line stepper for performing photolithographic patterning prior to the wet-etch process has been mapped as a function of exposure and focus conditions. In defining submicron circular patterns, the depth of focus (DOF) for our standard PSS patterns has been determined to be approximately equal to the minimum diameter being resolved. A major challenge associated with scaling PSS features to submicron geometries therefore arises from the non-flat nature of commercially available sapphire substrates. Local thickness variation on the wafers diminishes the ability to resolve small features. Typically, this problem is most severe at wafer edges where the stepper cannot accurately measure and correct for height and tilt variations of the wafer. Software modifications to the stepper for improved measurements and corrections for wafer thickness variations were evaluated and implemented to improve manufacturability. Additionally, best conditions of focus, exposure and develop time were established to provide the maximum degree of process latitude. Despite these improvements, variability in the photolithography process continues to be a major source of the overall variation in the process and an area that warrants continuous efforts for improvement.

3.3. Optimization of the etching process parameters and PSS pattern geometry

Several promising wet-etched PSS geometries were selected for evaluation based on the simulation results. These geometries varied in terms of the feature pitch, height, footprint on the wafer (fraction of patterned area) and the relative area of different crystallographic facets. The new designs have focused on increasing the fractional area of slanted (i.e. faceted) regions of the sapphire relative to total planar area of the wafer to improve the efficiency of light extraction, and doing so without compromising the ability to grow high-quality epitaxial device layers.

In early screening experiments InGaN LED epitaxial layers were grown on PSS wafers with design variations and submitted through Lumileds' standard LED fabrication processes. Based on measured light output data, the candidate "PSS2" structure and process was identified. Additional runs focused on assessing the sensitivity of parameters of interest to expected variations in the PSS geometry. These parameters specifically include (1) the epi-growth quality, (2) the LED fabrication yield and (3) the light output flux of both blue and white (phosphor-converted) packaged LEDs. In parallel the PSS etching process was characterized to identify and minimize sources of variability. As a result of these studies process controls were implemented to minimize the etch variability associated with within-wafer uniformity, across-lot uniformity, and lot-to-lot reproducibility.

As the PSS patterning becomes more aggressive from the perspective of maximizing the light-extraction efficiency, growth of high-quality epitaxial material becomes increasingly challenging. Importantly, in this task we have identified the limits of the "aggressiveness" of the patterning which is tolerable before the quality of the epitaxial material degrades to the point of impacting yield or performance. In parallel the epitaxial growth methods were optimized for obtaining the highest quality layers possible on these substrates.

In 2014, the new "PSS2" fabrication and epitaxial growth process was transferred to manufacturing and adopted into Lumileds' LUXEON Q products. This adoption has been shown to result in an increase in light output of 4-5% compared to the prior PSS technology.

3.4. Identification of high-throughput metrology for PSS features for providing manufacturing process control

In early 2014 we obtained an optical inspection tool (on evaluation basis) to assess its capabilities for automated visual inspection (AVI) of PSS wafers to facilitate manufacturability. Our assessment showed that this tool can identify gross and fine defects on the wafer such as particles, single missing PSS features, and extended regions of missing PSS features. This capability has allowed us to reduce certain defects and improve yields through implementing improvements to the process and the processing environment. As a result of the successful demonstration of this AVI capability for defect inspection, we have now implemented this tool for quality control and monitoring in our PSS manufacturing line.

Based on this success, we have further engaged the vendor of this AVI tool to evaluate a platform for reliable submicron CD metrology for manufacturing control. Accordingly, at the vendor's site we performed a successful evaluation of the gauge repeatability and reproducibility (GR&R study) of a tool and method to measure the submicron masking features defined in our photolithography process. In these tests this tool and method were deemed to have excellent capability to measure resist and hard-mask CDs for specification tolerances down to 0.1 µm. We will continue to work with this vendor for in-house (at Lumileds) development of a technique to measure and report final PSS2 geometries in the manufacturing line.

3.5. Optimization of InGaN epitaxial growth methods and production of LED structures on PSS wafers

In early evaluations of epitaxial quality versus pattern geometry we found a measurable drop in GaN layer quality for the more aggressive PSS patterns. To address this problem, new growth template conditions were developed to optimize the nucleation and subsequent lateral overgrowth of GaN on the PSS2 substrates. The improved template is critical for enabling smooth, high-quality overgrowth of GaN. Initial development and qualification of this process focused on only one of the two major epi-growth reactor platforms used for production at Lumileds. These evaluation and qualification runs utilized co-loading of both PSS1 and PSS2 substrates for direct comparison of light output without the noise associated with run-to-run epitaxy variations. In a series of multiple runs (three epi-growth runs in each of three different reactors distributed over three different LED wafer fabrication lots) the new PSS2 pattern showed consistent gains in light output of between 3 to 4% for LEDs in a LUXEON Q package. These gains were observed in both blue and phosphor-converted (3500K, CRI>80) devices.

In the latter part of 2014, the growth process was additionally developed and qualified on a second reactor platform used for LED manufacturing. Wafers grown with further refinement to the growth template appear to have somewhat higher gains (4-5%) based on analysis of some recent data. To meet anticipated future demands for capacity we have qualified and released these growth processes on both reactor types for production in the 4th quarter of 2014.

3.6. Design, development and fabrication of die structures optimized for PSS architecture

PSS flip-chip die development was undertaken to realize a chip-scale package (CSP) die compatible both with direct-attach configurations for lowest cost and with advanced packaging architecture for highest performance.

A flip-chip contact redistribution scheme and dielectric layers were developed to optimize current

injection and thermal performance at high drive conditions. A first die design was completed in 2014 and put on high-temperature operating life (HTOL) and wet high-temperature operating life (WHTOL) tests with drive current up to 3 A. These tests revealed a failure mode in the dielectric layer, which was addressed in the next iteration of die development.

A systematic experimental study was conducted to optimize the epitaxy and die interactions in the PSS architecture. A mask set was designed and fabricated with several die design variations, and combined with variations in the epitaxy structure parameters. A total of 40 different die types were prototyped and evaluated, encompassing 10 die designs with variations in the number of n-vias, via size and die edge coverage, and 4 epitaxy designs. A sample cross-section of the data is shown in Figure 1. Based on this study, designs that optimize flux as well as designs that optimize efficacy were identified.

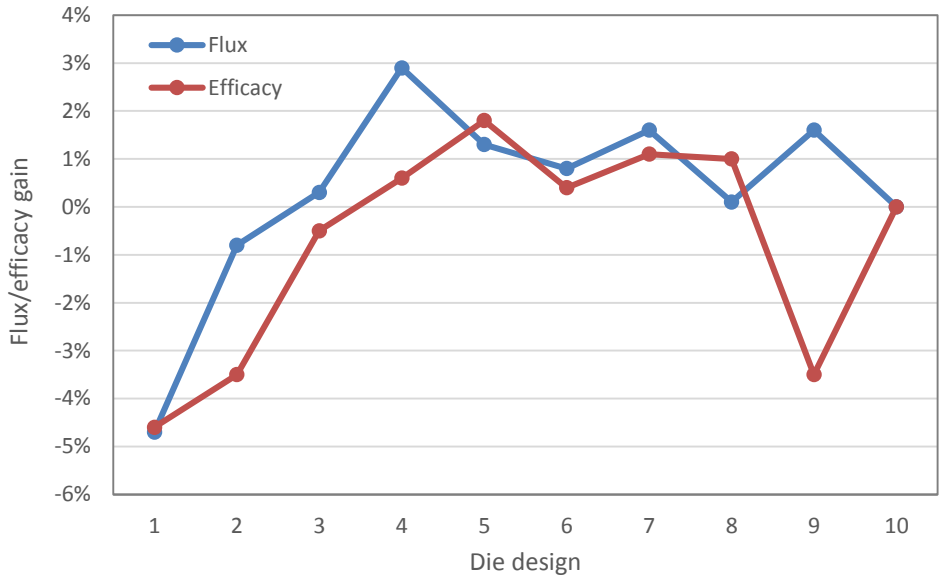
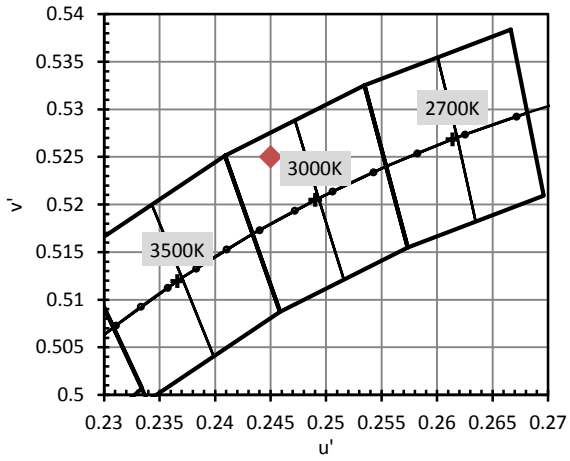


Figure 1: Relative flux and efficacy gain for different die designs for one of the evaluated epitaxy designs. Gains are relative to die design #10 which was the baseline for this evaluation.

3.7. Development of low-cost packaging architectures for manufacturing optimized PSS emitters with lm/W performance meeting or exceeding that of baseline TFFC devices

The LUXEON Q product released at the beginning of the project features a PSS flip-chip die on a ceramic submount with a conformal phosphor coating, encapsulated in a full size dome for highest flux and efficacy. This architecture serves as a baseline for further package development in this project and a vehicle for evaluating and demonstrating efficacy improvements.

In Q2-2015, the efficacy target of the project was met in a LUXEON Q package incorporating the PSS2 patterning and epitaxy process and an upgraded phosphor system. The characterization results of this package are summarized in Figure 2.



Characterization summary	
T_j (°C)	85
J (A/cm^2)	35.0
V_f (V)	2.73
Efficacy (lm/W)	131.0
CCT (K)	3116
CRI Ra	83.5
CRI R9	8.0

Figure 2: Chromaticity and characterization results of LUXEON Q package demonstration sample.

Package architecture development in the project focused on two package types for white illumination-grade LEDs leveraging the benefits of the PSS flip-chip technology:

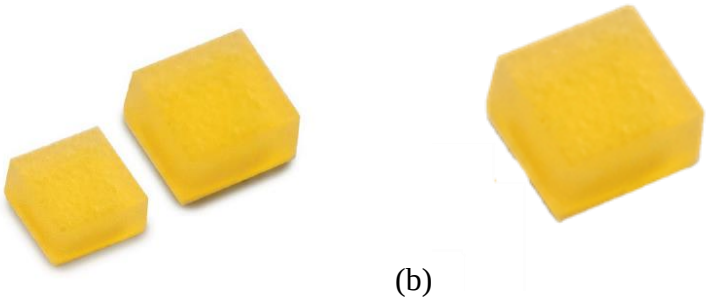
1. A chip-scale package (CSP) flip chip capable of direct attachment on a printed circuit board;
2. A fully packaged next-generation emitter (NGE) with ceramic submount, full encapsulation and tailored radiation profile.

These emitters are complementary in the application needs that they address. The CSP has the smallest form factor and lowest cost due to the minimal packaging. It is therefore an optimal solution for various cost-sensitive high-power applications as well as applications that require a close-packed array of high-power emitters for high source brightness. The fully packaged emitter uses a ceramic submount that is sized to fit a full dome encapsulant as well as other optical enhancements to create a Lambertian radiation profile from the radiation emitted by the five-sided PSS substrate. The ceramic submount also spreads the heat more effectively than typical printed circuit boards and thus enables better thermal performance. This type of package is therefore an optimal solution for directional high-power applications operating at high drive current.

To develop the CSP emitter, the die and metallization were designed to be compatible with industry standard SMT reflow processes for attachment on printed circuit boards. Application studies were performed in collaboration with customers to validate process windows for board design and assembly. Resulting recommendations were documented and published in a detailed application note. A phosphor integration and encapsulation process was developed specifically for the CSP emitter, using an intermediate carrier during these process steps in absence of a permanent ceramic submount. The intermediate carrier allows for dense packing of the dice, which reduces the process cost per die but presents process challenges in the form of a high-aspect-ratio 3D topology between the die. Process development included optimization of the process parameters to achieve high process yield at the smallest possible die spacing.

The CSP emitter was released as LUXEON FlipChip White in September 2015, with die sizes of 0.5 mm^2 and 1.0 mm^2 (shown in Figure 3a) and CCTs ranging from 2700K to 5700K. An extension to 2 mm^2 die size is under development, and prototypes have been made (Figure 3b). The manufacturing cost for the 2 mm^2 version is approximately 26% lower than the TFFC-based

LUXEON TX product, having equal die size and projected flux/efficacy performance. This achieves the cost reduction target of the project.



(a) (b)

Figure 3: (a) Released LUXEON FlipChip White products with 0.5 and 1 mm^2 die size; (b) R&D prototype with 2 mm^2 die size.

For the fully packaged next-generation emitter (NGE), system modeling was performed to predict the characteristics of various package architectures in targeted applications. Based on these predictions new submount and lens designs were down-selected and purchased. Prototypes of the designs were fabricated to allow for full characterization and model validation.

A controlled performance comparison study was completed for an experimental NGE package architecture. Packages were made both with 2 mm^2 PSS flip-chip die and 2 mm^2 TFFC die to allow for comparison to the existing LUXEON Q and LUXEON TX packages, respectively. The NGE-PSS package size was reduced relative to the LUXEON Q package to reduce cost, while the lens shape, sapphire thickness and other optical parameters were designed to achieve a suitable radiation profile while maintaining high flux in the smaller package. The LUXEON Q package (with PSS-FC die) was found to have about 2% higher flux than the LUXEON TX package (with TFFC die), in line with expectations, due to better light extraction from the PSS-FC volume emitter. However, in the experimental NGE package, the NGE-PSS was found to have about 1% lower flux than the NGE-TFFC benchmark; in other words, the package penalized the PSS-FC die relative to the TFFC die. It was determined that this flux penalty outweighed the cost benefit of the smaller package.

A new NGE design was therefore developed, reverting back to a full size dome package for highest performance. Other cost reduction opportunities were identified, including the die attach process and the phosphor integration process. The new NGE design incorporates the following elements:

- a 2 mm^2 PSS flip-chip die with key improvements in the mirror layer structure and the dielectric layer for contact redistribution, leveraging the same die design as the CSP emitter;
- a low-cost 3535 ceramic submount package with a full dome for maximum flux;
- an upgraded neutral- and cool-white phosphor/matrix system to provide maximum flux while meeting color-over-angle and reliability requirements;
- optical design enhancements in the package to redirect side-emitted light and produce a radiation pattern compatible with directional application requirements.

The internal product creation process (PCP) for the NGE has started. The program plan commitment (PPC) milestone was passed in Q4-2015, and commercial release is currently scheduled for Q3-2016. The product is positioned as a high-efficacy, directional emitter with small source size and high drive capability, with target applications including street and roadway, high-bay and arena lighting. The optical design enables a Lambertian radiation profile with <3% light emitted below the horizon and a color-over-angle variation of <35 points u'v' for maximum system performance with state-of-the-art directional optics. The maximum DC drive current will be 2 A. Initial prototypes of the emitter have been made, as shown in Figure 4, and are currently undergoing systematic characterization in order to aid the design freeze of the final product.

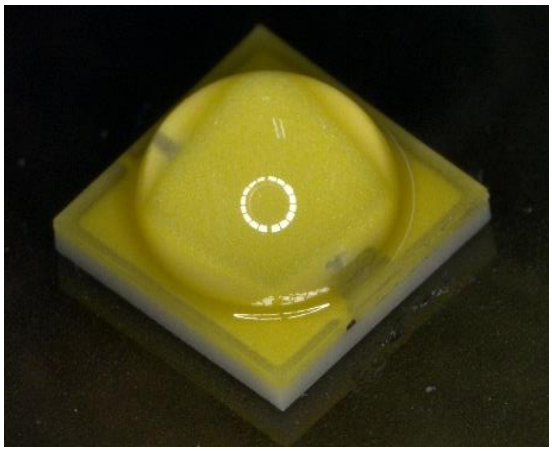


Figure 4: Prototype NGE sample with a CCT of 4000K and CRI greater than 70.

Work has also been initiated to enable further improvements in radiation pattern and flux after initial release of the NGE. One route is the application of a reflective material covering the sidewalls of the transparent sapphire substrate, enabling a top-side emitter with small source size for tighter beam control. Several materials and vendors were evaluated and a first down-selection was made. Performance was optimized based on optical simulations and confirmed by transmission/reflection measurements showing a reflectivity of >95%. The material was also tested for solder reflow compatibility and mechanical performance. An initial process has been defined and impact on upstream and downstream process has been evaluated, including opportunities for overall process cost reduction.

4. Products

4.1. LED products

Lumileds has released the developed PSS technology into several product categories addressing different application needs.

LUXEON Q was released in 2013 based on pre-existing patterned sapphire substrates at the beginning of the project. The PSS technology developed in this project was implemented in LUXEON Q in a major upgrade in 2014. The efficacy of LUXEON Q is now on par with state-of-the-art TFFC products such as LUXEON TX at comparable current density. Product information for LUXEON Q can be found at http://www.lumileds.com/products/high-power-leds/luxeon-q.

LUXEON FlipChip White was released in 2015 as a new category of direct-attach flip-chip products, epitomizing the low-cost packaging architecture afforded by the PSS technology. This

product has been released in 0.5 mm^2 and 1.0 mm^2 die sizes in a range of CCT and CRI combinations. Product information for LUXEON FlipChip White can be found at http://www.lumileds.com/products/high-power-leds/luxeon-flipchip-white. In particular, an application note covering board design, assembly and handling specific to this new product architecture is located at http://www.lumileds.com/uploads/579/AB117-pdf.

The developed PSS technology has also been proliferated into LUXEON FlipChip Royal Blue and LUXEON FlipChip UV products on the market.

4.2. Publications and presentations

Poster Presentation: "Development and Industrialization of InGaN/GaN LEDs on Patterned Sapphire Substrates for Low Cost Emitter Architecture", DOE SSL Manufacturing R&D Workshop, San Diego, CA, May 7-8, 2014

Poster Presentation: "Development and Industrialization of InGaN/GaN LEDs on Patterned Sapphire Substrates for Low Cost Emitter Architecture", DOE SSL R&D Workshop, San Francisco, CA, January 27-29, 2015

Presentation: "Will CSP LEDs Cross the Chasm Between Niche and Mainstream?", Strategies in Light, Las Vegas, NV, February 24-26, 2015

Presentation: "Development and Industrialization of InGaN/GaN LEDs on Patterned Sapphire Substrates for Low Cost Emitter Architecture", Building Technologies Office 2015 Peer Review, Vienna, VA, April 17, 2015