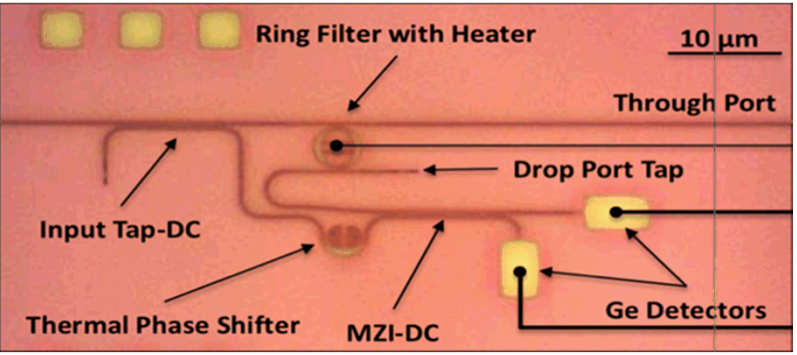
Exceptional service in the national interest

Sandia National Laboratories

SAND2015-0787PE

Sandia Silicon Photonics Update and May MPW Plans



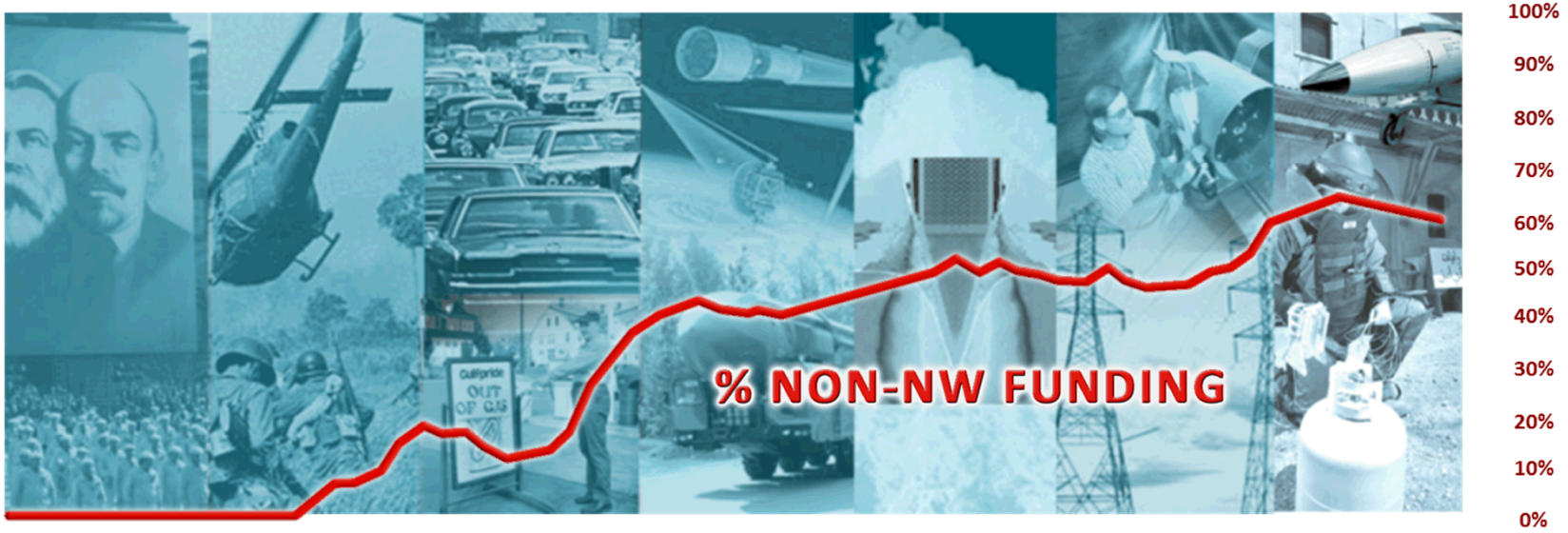
A. L. Lentine, C. T. DeRose, P. S. Davids, A. T. Pomerene, A. L. Starbuck and D. C. Trotter

Acknowledgement for background material:
F. B. McCormick, G. Keeler, A. Vawter, A. T. Pomerene: but this represents the work of many people.

What is Sandia National Lab?

Sandia National Laboratories

1950s	1960s	1970s	1980s	1990s	2000s	2010s
NW production engineering & manufacturing engineering	Development engineering Vietnam conflict	Multiprogram laboratory Energy crisis	Missile defense work Cold War	Post–Cold War transition Stockpile stewardship	Expanded national security role post 9/11	LEPs New START Evolving national security challenges



- DOE FFRDC: Initially Z-division of Manhattan Project (Non-nuclear Components, Weaponization of NEP)
- **National security tech transition**: Gov't Agencies (&/or Academia) ➔ SNL ➔ Industry
- DOE supports our "Strategic Partnership Projects" (with Industry & other gov't agencies (OGAs))
- Our Big 3: **Non-compete with Industry, Fairness of Opportunity, No Organizational Conflict of Interest**
- Managed by LMC, but see OCI above
- **CRADAs with many Defense Contractors, Many STTRs & SBIRs, BAA response teaming**
- **Experience handling sensitive & proprietary information**

Microsystems and Engineering Sciences Applications (MESA): 400,000 Sq-ft Complex with >650 Employees in Secure Facility

Sandia National Laboratories

- Trusted Digital, Analog, Mixed Signal & RF Integrated Circuits Design & Fabrication
- Custom IC Design
  - Secure microcontrollers
  - Sensor Readout ICs
  - Analog/Digital/RF
  - IBM Trusted Foundry
  - Tamper Resistant
- Micromachining
- RAD Effects and Assurance
- Failure Analysis, Reliability Physics
- Test & Validation
- 3-D Integration Features

- Advanced Computation
- Modeling & Simulation
- COTS Qualification
- Advanced Packaging
- Custom Electronic Components
- System Design & Test

- Compound Semiconductor Epitaxial Growth (UV-THz)
- Photonics: Si & III-V
- MEMS, VCSELs, Plasmonics
- Specialized Sensors, FPAs
- Materials Science, Graphene
- Nanotechnology, Chem/Bio
- Heterogeneous-Technology Integration & Processing
- III-V Semiconductor Devices
  - Rad-Hard µElectronics
  - Rad-hard Optical Links
  - Solid-State RF Devices
  - GaN Power Electronics

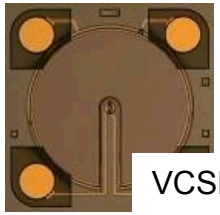
MESA is an FFRDC-based development and production facility for any microsystem component or technology that cannot or should not be obtained commercially.

Trusted Advanced Pathfinder Products: III-V Photonics

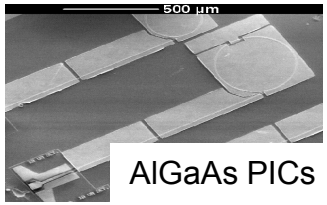
Sandia National Laboratories

2010s

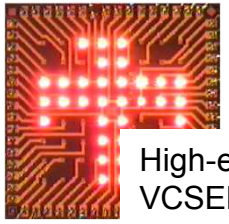
InGaAsP PICs



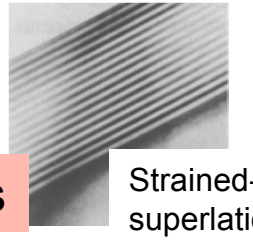
VCSEL+ PD



AlGaAs PICs

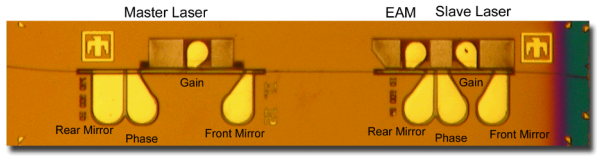


High-efficiency VCSELs

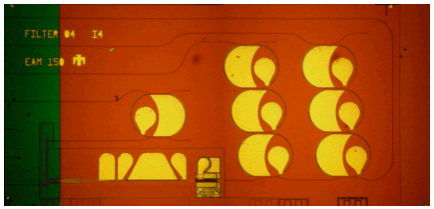


Strained-layer superlatices

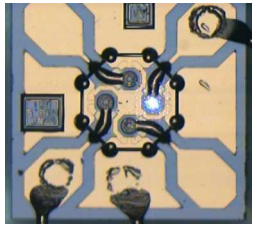
1980s



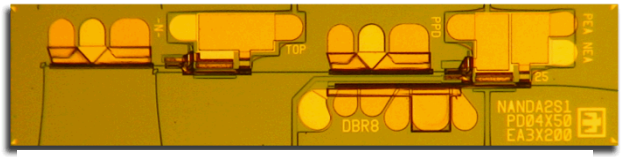
On-Chip Injection Locking
Enhanced Modulation > 50 GHz, C-Band



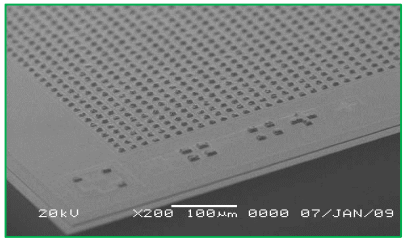
RF-Optical Channelizing Filter
1-20 GHz RF on C-Band Light



Single-Frequency Tunable VCSELs,
For atomic spectroscopy and sensors



All-Optical Logic at >40 Gb/s, C-Band



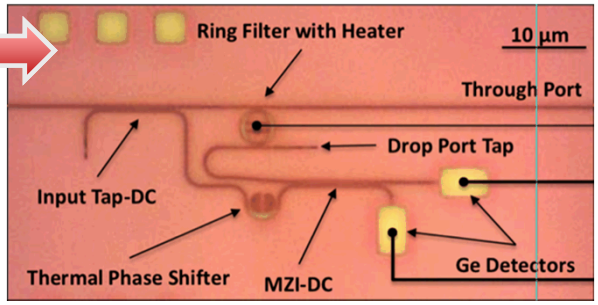
nBn FPAs in the SWIR, MWIR and LWIR,
leveraging novel III-P and III-Sb materials

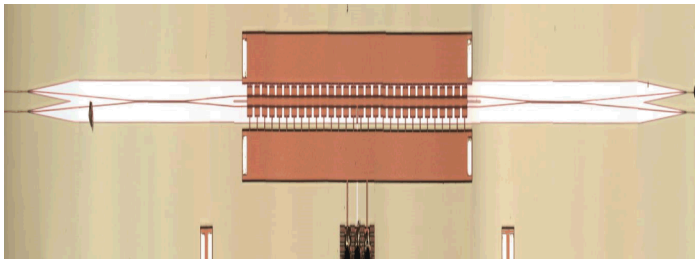
- **Foundational Capabilities**
  - **III-V compound semiconductor epitaxy, microfabrication, integration**
  - **Device physics, modeling, simulation**
  - **Microelectronics/optoelectronics, and complex mono/hetero-circuits**
- **Prove, Advance Technology Readiness Level, Productize**
  - **TRL1-6+: create, develop, prototype**
  - **NNSA QMS/QC-1-10; trusted**
- **Trusted, low-volume, high-reliability products for harsh environments**

Trusted Advanced Pathfinder Products: Si Photonics

Sandia National Laboratories

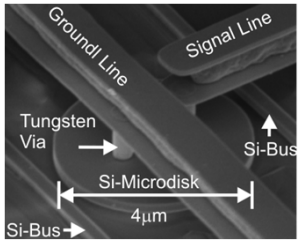
2014	*balanced homodyne resonant wavelength stabilization > 55C*
2013	*Si Photonics MPW (CIAN NSF ERC)*
2012	*24 GHz Si TW MZM*
2011	*45 GHz Ge Detector*
2010	*3 fJ/bit resonator modulator, 1V-cm MZM*
2009	*wavelength tunable rings over 35 nm*
2008	*2.4 ns Wavelength selective switch*
2007	*MicroDisk resonator infrared detector*
2005	*Si_3N_4 low-loss waveguides*
2000	*SiON / SiO2 (Clarendon Photonics)*
1990s	*Si PhC & Optical MEMS*



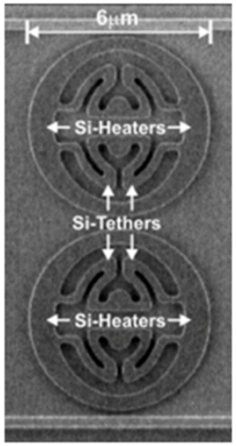


24 GHz 0.7V-cm Travelling Wave MZI Modulator

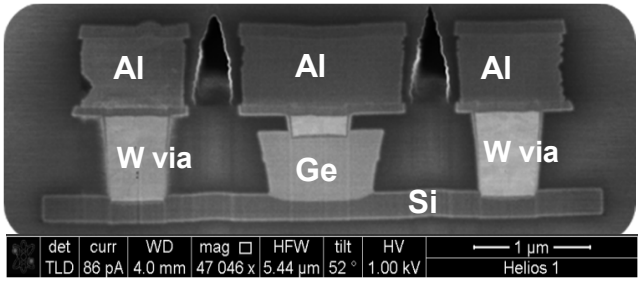
3.2fJ/bit at 12Gb/s



Resonant Optical Modulator/Filter

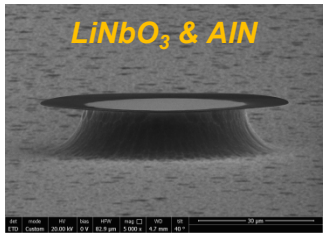


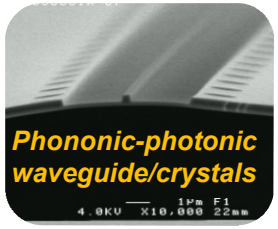
Tunable Resonant Filter



45 GHz High-speed Ge Detector on Si

MEMS process for additional capability

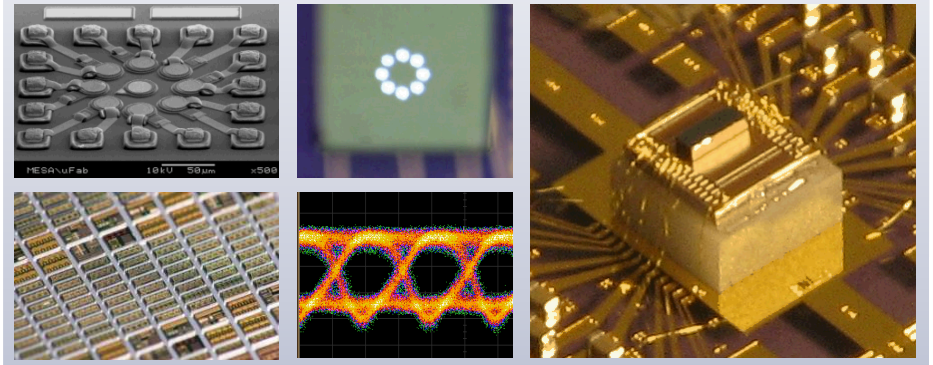




Trusted Advanced Pathfinder Products: Heterogeneous Integration

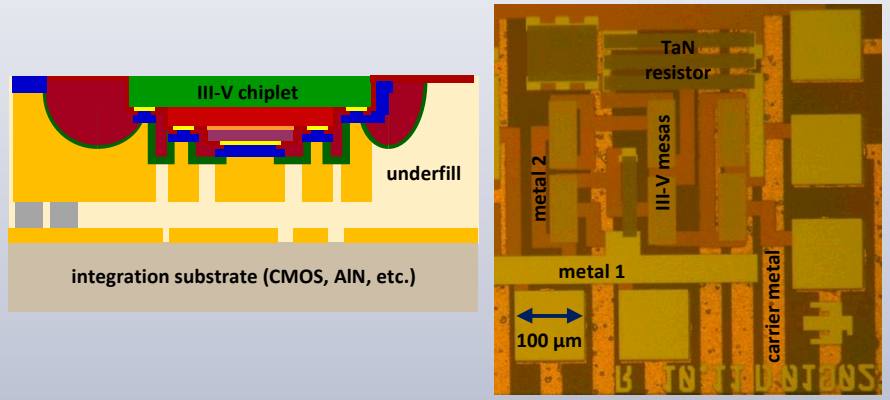
Sandia National Laboratories

Optical Data Communications



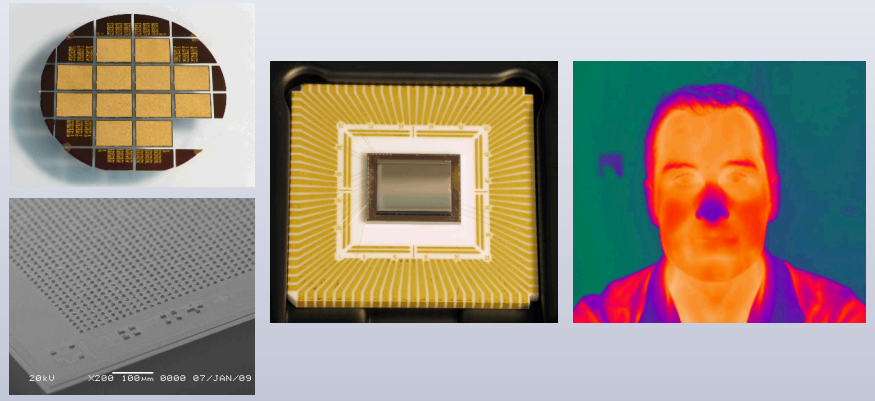
- GaAs- and InP-based devices: VCSELs, modulators, photodiodes
- dense integration onto 32-nm and 45-nm CMOS

Heterogeneous III-V/CMOS Microelectronics



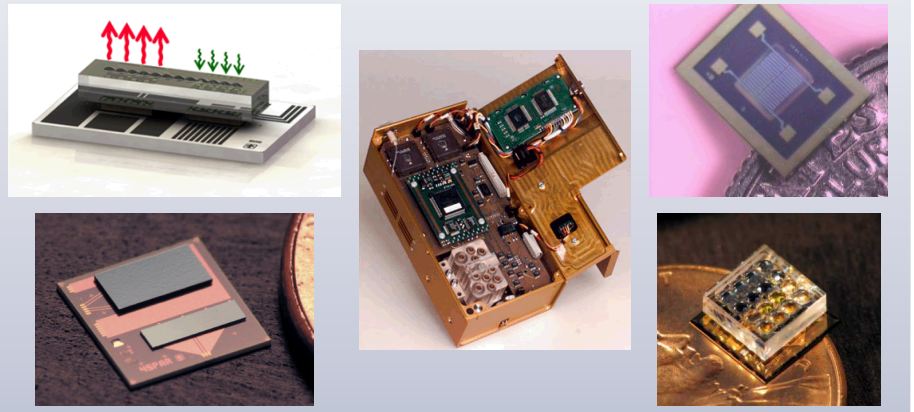
- complementary integration of GaAs and InP microelectronics
- III-V microelectronics circuitry on CMOS ASICs

IR Imagers for Remote Sensing



- nBn InAs/GaSb MWIR/LWIR detector arrays for large-format FPAs
- 10µm indium bump bonding, underfill, thinning, AR coating
- hybridization to silicon ROICs with >99.99% interconnect yield

Optical and MEMS-based Microsensors

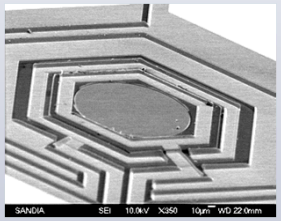
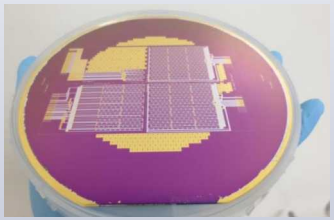
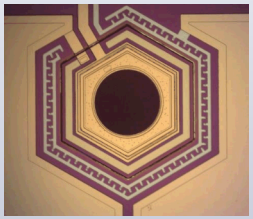


- chemical and bio sensors using MEMS and SAW devices
- g-hard optical microsensors with in-house photonics
- hybrid device integration with custom micro-optics

Trusted Advanced Pathfinder Products: Heterogeneous Integration

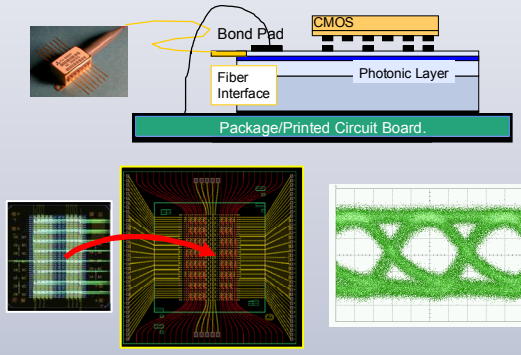
Sandia National Laboratories

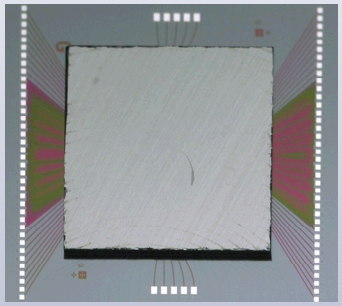
Microsystem-Enabled Photovoltaics

- wafer-level bonding for multi-junction solar cells
- InGaAsP/InP and InGaP/GaAs devices on silicon
- dielectric interfaces with III-V substrate removal
- integration with collection optics

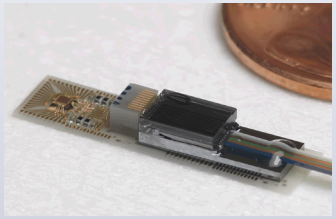
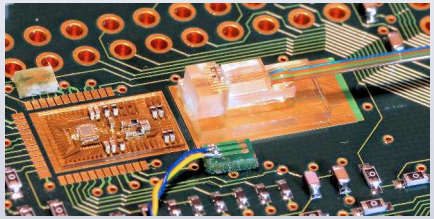
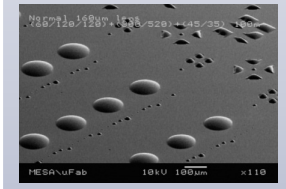
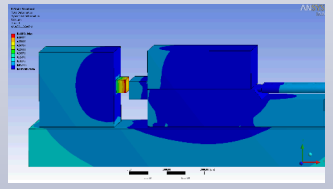
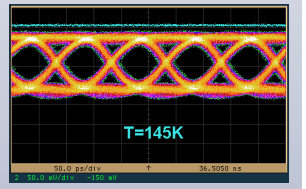
High Performance Computing





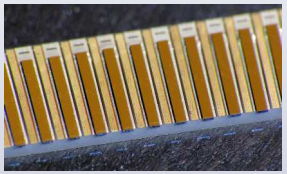
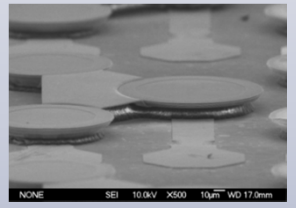
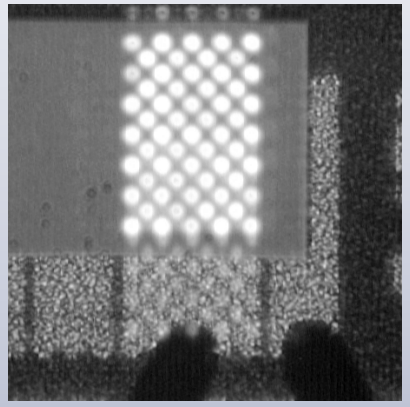
- silicon photonics on high-speed silicon ASIC
- independent optimization of electronics & photonics

Extreme Environment Applications

- custom photonics, optics, electronics for cryogenic interconnects
- advanced optoelectronics and integration for radiation hardness

High Performance Photonics

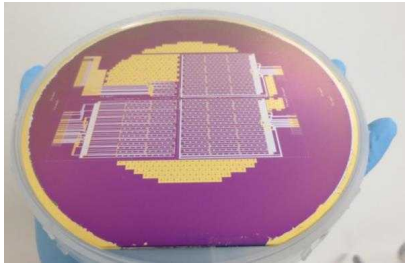




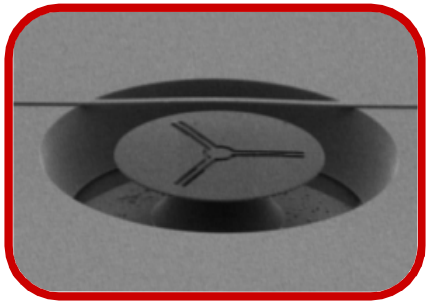
- high-power emitters on AlN and diamond
- RF packaging for high-speed test and measurement

IMI Photonics Manufacturing Hub

Sandia National Laboratories

- **What:** Heterogeneous integration of III-V, Si photonics/electronics
- **Why:** US competitiveness & military superiority
- ***Sandia's potential role:***
  - Trusted photonics
  - Research photonics incompatible with production foundries
  - Quick start



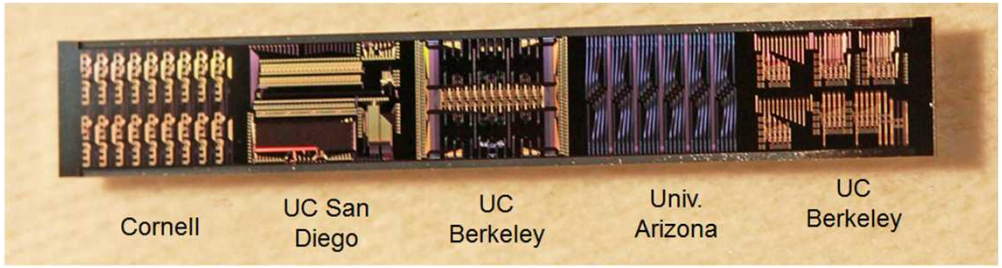


Engagement

- DOE supporting National Lab involvement in strategy and project development for *ALL* teams.
- We are available for:
  - Telecons & briefings at team meetings
  - Hosting visits to Sandia

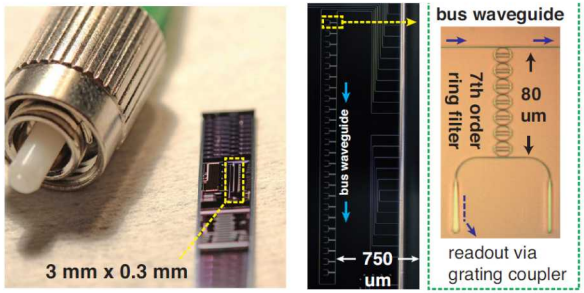
Very strong teams have formed: What gaps can we help fill?

CIAN Silicon Photonics multi-project wafer (MPW)



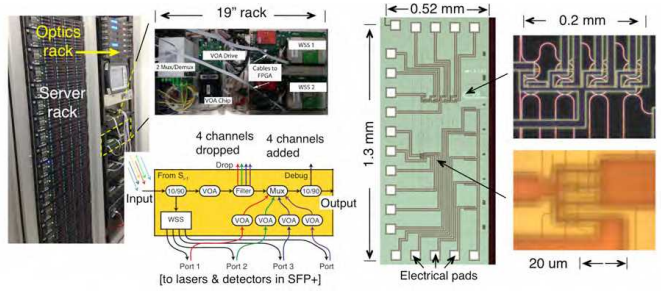
CIAN (center for integrated access networks) Si Photonics MPW Highlights

- Five university participants
- 1/7th wafer from internally funded program (XGC LDRD grand challenge)
- Sandia has delivered 100+ chips
- 6 conf. & journal papers so far



Optical Spectrum Analyzer

R. Aguinaldo et. al. OIC 2014



Network Node on a Chip

R. Aguinaldo et. el. IPC 2014

Si Photonics MPW

May, 2015

- 2 internal programs
- CIAN
- 1 confirmed customer
- 3 interested

Silicon Photonics Layer Structure

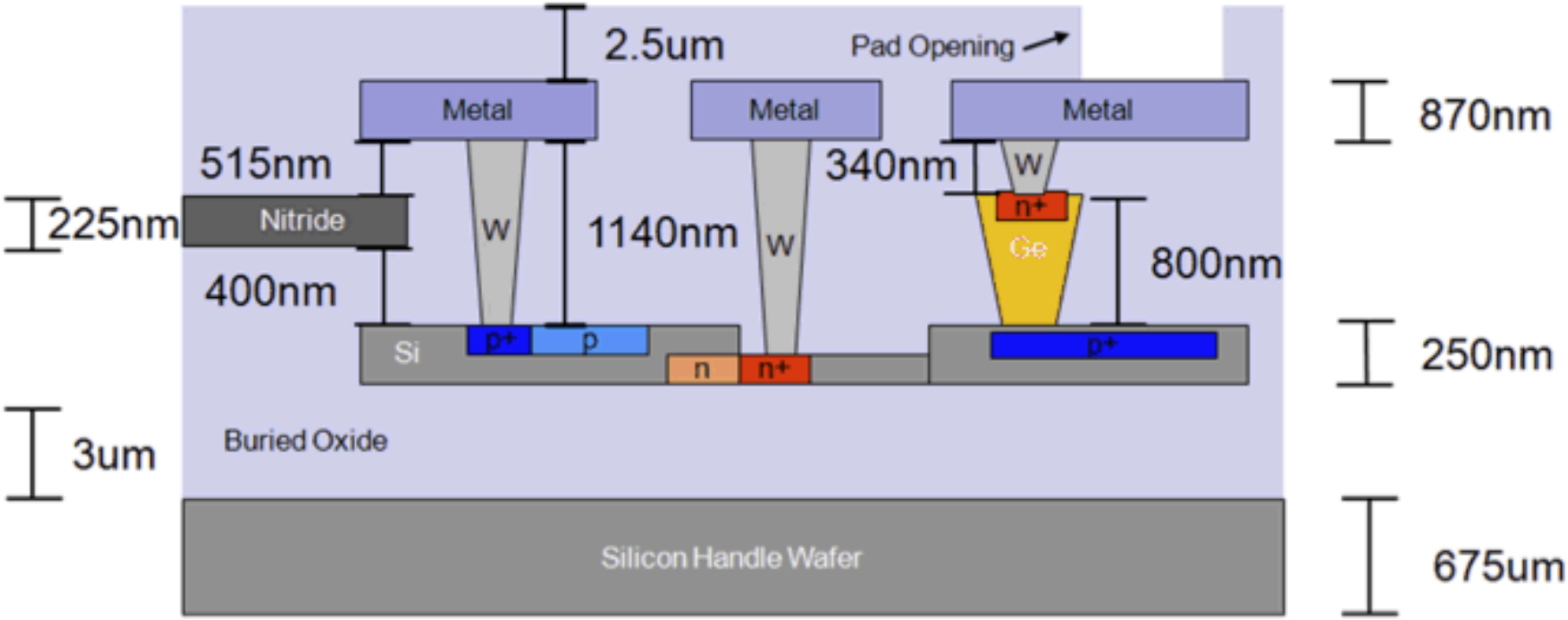
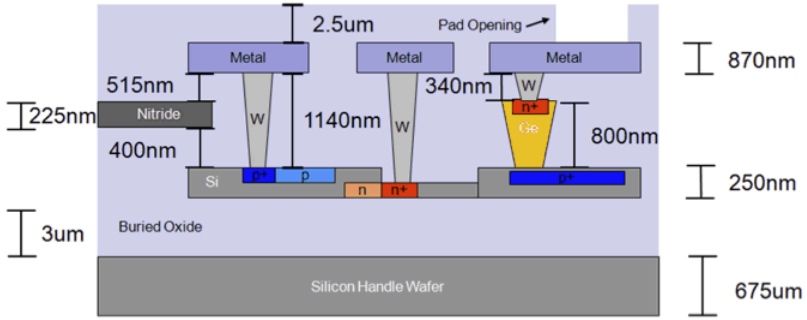


Figure 5-1 Illustration of layer thicknesses and separations between layers

Silicon Photonics Design Manual

Sandia National Laboratories



6.2.1 Si Cut (GDS layer 1)

This is layer is etched after the definition of the partial ridge etch. Fully etched waveguides, disk resonators, directional couplers, etc. are all defined in this step. The design rules for t include the following:

A. Minimum line width of 100 nm
B. Minimum space (line to line separation)of 280 nm
C. Minimum taper point 80 nm. (Note tapers coming to an 80 nm point should be less um long.
D. Minimum overlap with Ridge layer of 500 nm on all sides (Note: either Si overlaps Ridge Overlaps Si). This rule may be difficult to implement in some cases, e.g. rit waveguide transitions for this we recommend use of a library device described in sect
E. *Recommended* waveguide width of 400 nm with a minimum bend radius of 1.75 um.
F. *Recommended* waveguide width to couple to ring/disk resonators of 320 nm.

The design rules for the Si cut layer are illustrated in Figure 6-1, and SEM images of the effects rule violation are shown in Figure 6-2.

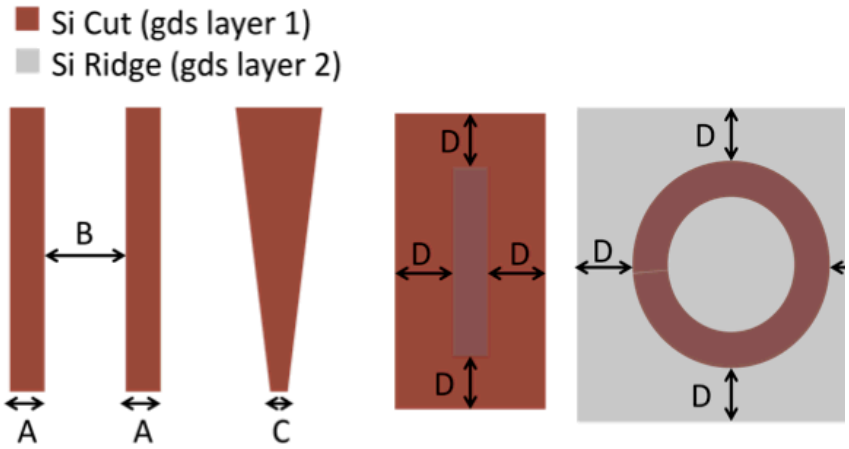
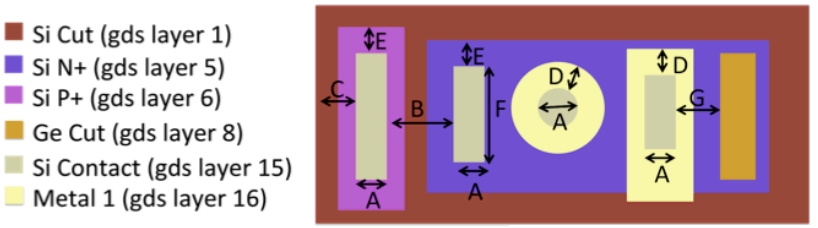


Figure 6-1 Illustration of Si cut layer design rules

6.2.12 Si Contact (GDS layer 15)

The Silicon contact layer is used for making ohmic electrical contacts to P+ and N+ doped Si. The contact width is specified to be 500 nm. The contact width is specified in order to guarantee proper filling and CMP of the Ti/TiN lined tungsten contact. For trench type contacts a rectangular shape should be used with a width of 500 nm and a length greater than 500 nm. For point type contacts, circular contacts may be used. The design rules for this layer are specified below.

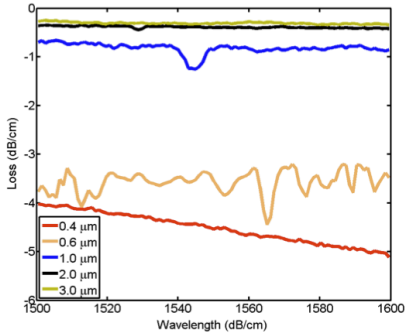
A. Contact width of 500 nm
B. Minimum space of 500 nm
C. Should be surrounded on all edges by a minimum of 150 nm of Ge cut, *Recommended* 400 nm minimum.
D. Should be surrounded on all edges by a minimum of 150 nm of Metal 1
E. Should be surrounded on all edges by a minimum of 100 nm of P+ or N+ Ge
F. Length greater than 500 nm
G. The minimum space from Ge cut is 1 um



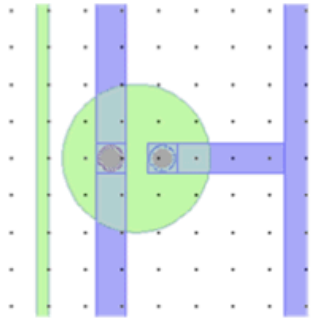
9.1 Silicon Waveguide

The silicon waveguide is the most basic element used in optoelectronic device layouts in the SPP1 platform. Since the thickness of the SOI is determined by the starting wafer selection, the silicon waveguide effectively has one parameter, its width.

Although, the width of the waveguide is the only critical parameter, it determines the propagation losses, effective index, group index, dispersion and bend radius of the waveguide. The waveguide propagation losses in the silicon waveguide are dominated by scattering from roughness at the waveguide sidewalls. Currently for our process, the rms value of the sidewall roughness is 1.2 nm with a correlation length of 100 nm and an exponential autocorrelation function. Losses for a single mode 400 nm wide waveguide are between 4 and 5 dB/cm for the TE polarization. Increasing the waveguide width results in a reduction in propagation losses but as the guide becomes multimode, coupling between the modes is induced by the line edge roughness. The losses for guides of various widths can be seen in 9-1. Typically bend radii of greater than 6 micron can be used for a 400 nm wide waveguide for the TE polarization.



9-1 Propagation loss for the TE polarization for si waveguides of various widths. Multimode phenomena is observed in the wider waveguides.



4um optical modulator

Existing design status

- Latest chip deliveries in May 2014
  - Working Ge detectors
    - Segmented contacts is now required (will update design manual)
- Out of process
  - 1 wafer waiting for test at Sandia, thin 200 layer between Oxide and Nitride (106401B)
  - 1 wafer with planar surface (but extra nitride layer); not diced yet. (106401J)
  - 2 wafers diced Sandia with higher n-type and p-type dopants (106401A, 23,24)
  - 4 additional wafers still in process, but low priority
- Please give us feedback !!

Library devices: Passive

Sandia National Laboratories

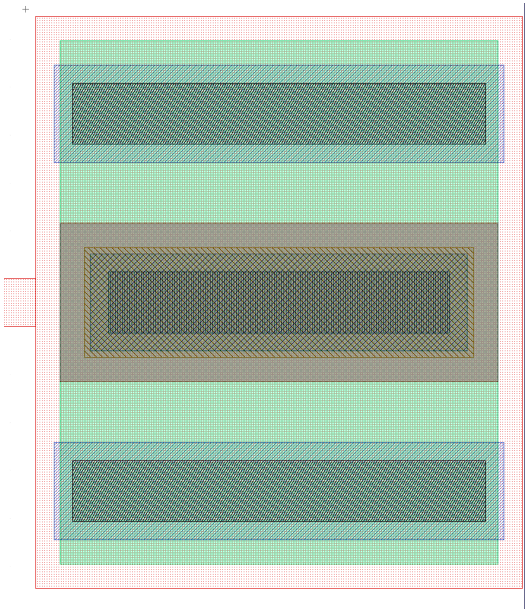
- Si rib waveguide [1]
- Si ridge waveguide [1]
- Si nitride waveguide [1]
- Si 6.0 um ring [1]
- 90 hybrids [2]
- Adiabatic hybrids [3]
- Grating coupler [4]
- Edge coupler [1]
- Two layer waveguide crossings [5]

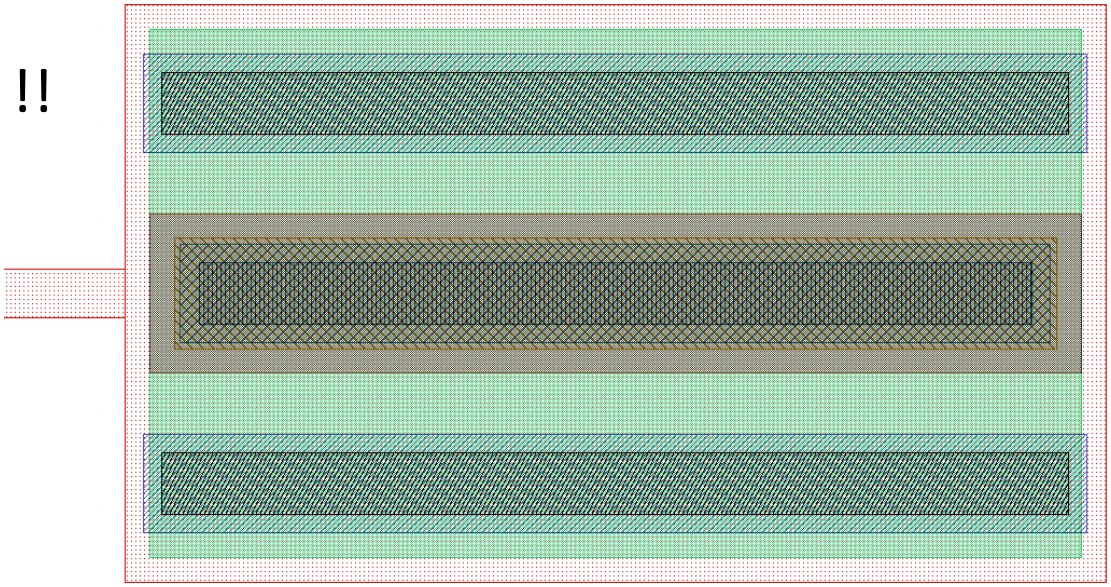
Library devices: Actives

- 3.5 um partially doped disk modulator [1,6,7]
- 4.0 um partially doped disk modulator [8]
- 4.0 um adiabatic ring high speed modulator [9]
- 4.0 um heater/modulator [10]
- 6.0 um heater/filter [11]
- Thermal phase shifter [12,13]
- Thermal MZM [12,13]
- EO phase shifter [14]
- EO MZM [14]
- Ge PIN detector [1,15]

Ge Detectors

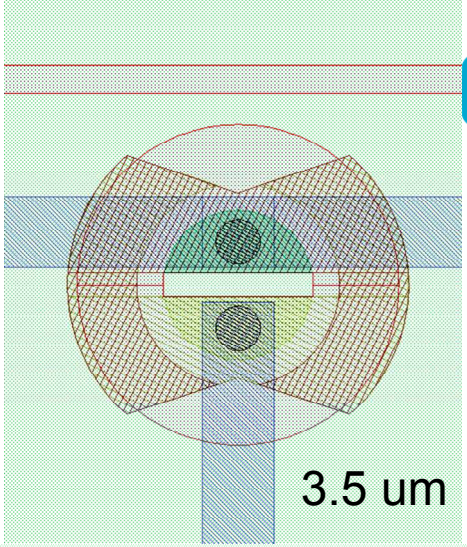
- Bandwidth to 45 GHz
- Dark current typ. 10 nA
- Responsivity 0.7 – 1.0A/W
- Length as a parameter
- Need to change to segmented contacts !!

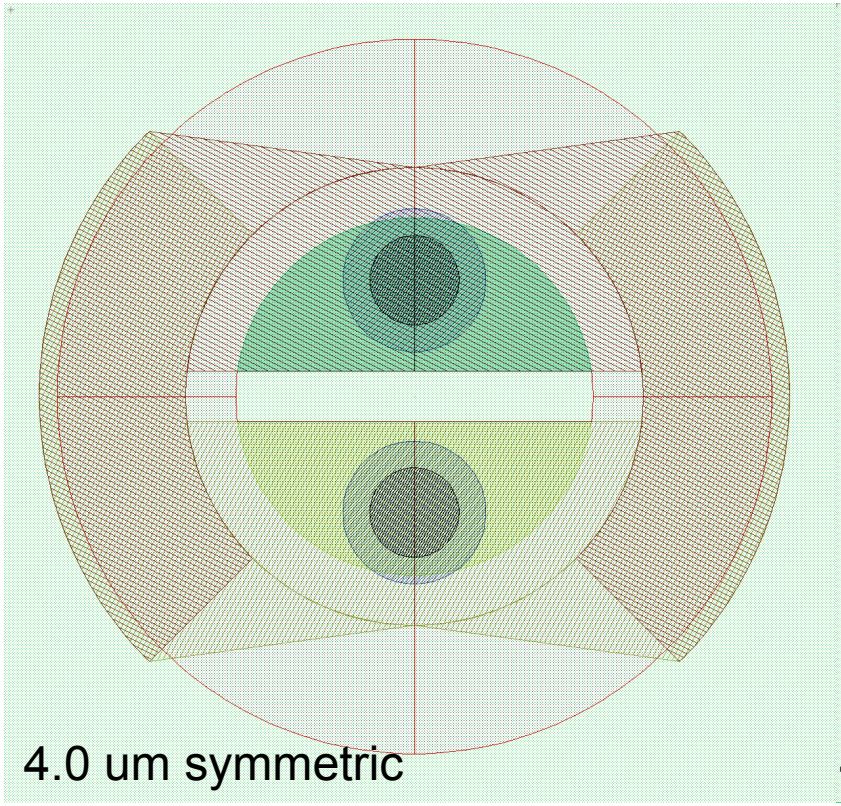


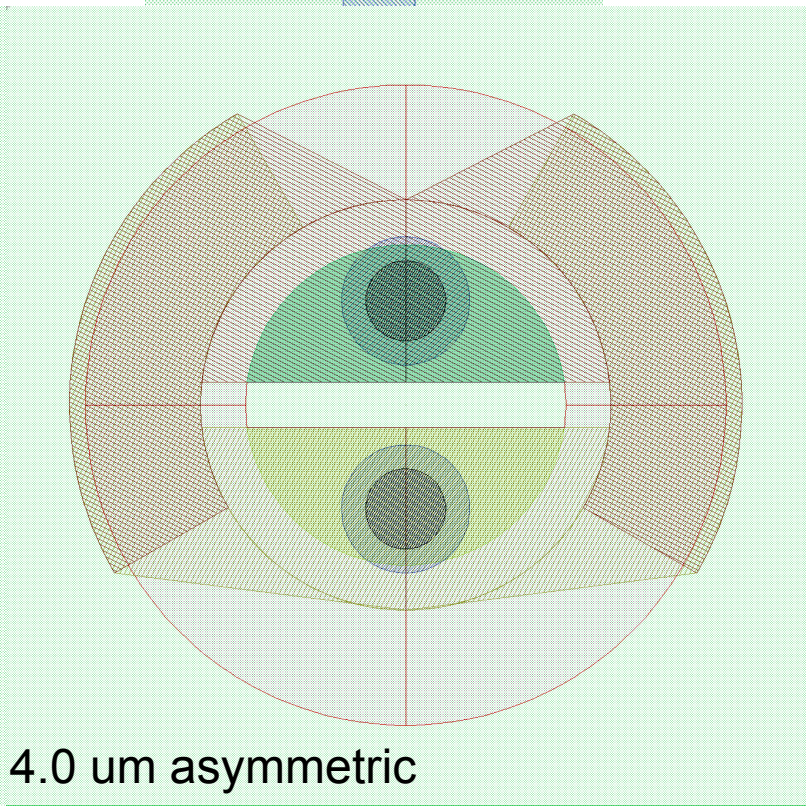


Disk modulators

- Bandwidths to 12.5+ GHz
  - Several designs from last mask still not tested
- Low voltages (+/- 0.5V @ 3:1 ER)
- FOM ~ 0.25 (Th-Tl)/2

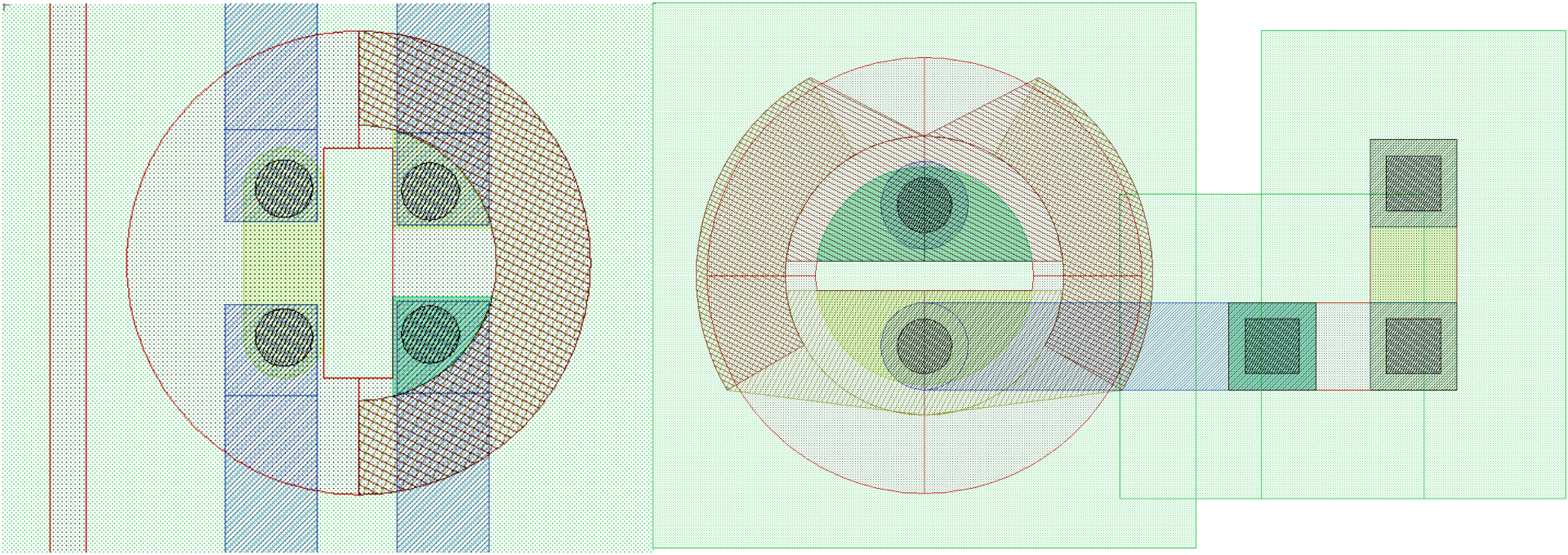






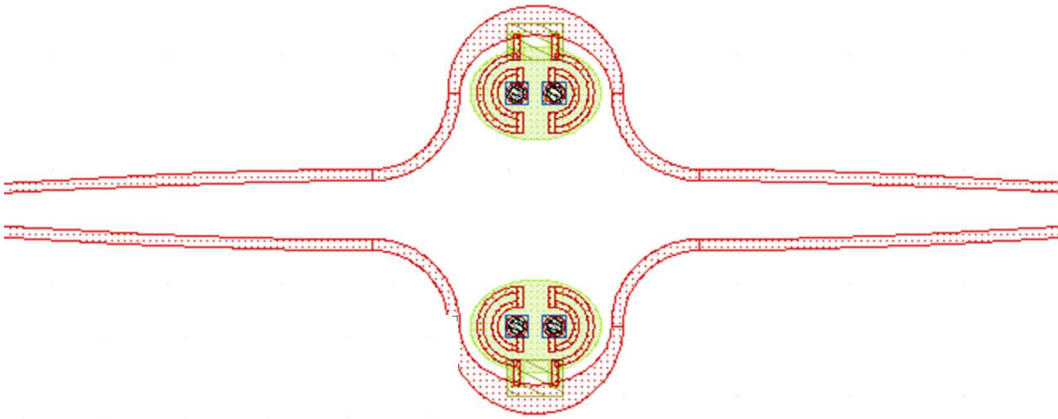
Disk Modulator with heater

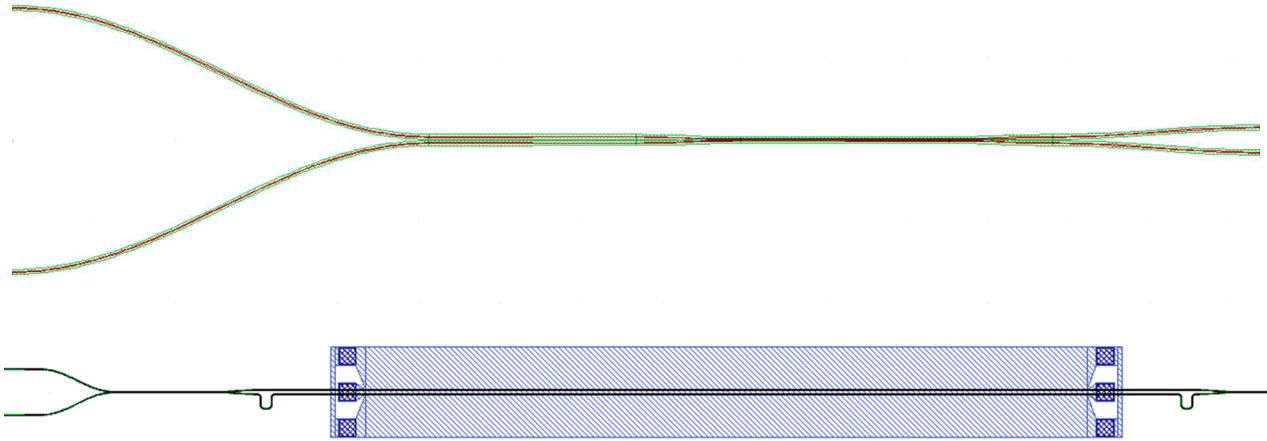
- ~ 10-12.5+ Gbps operation
- Integral heater ~ 8 uW/GHz
- External heater ~ 20 uW/GHz



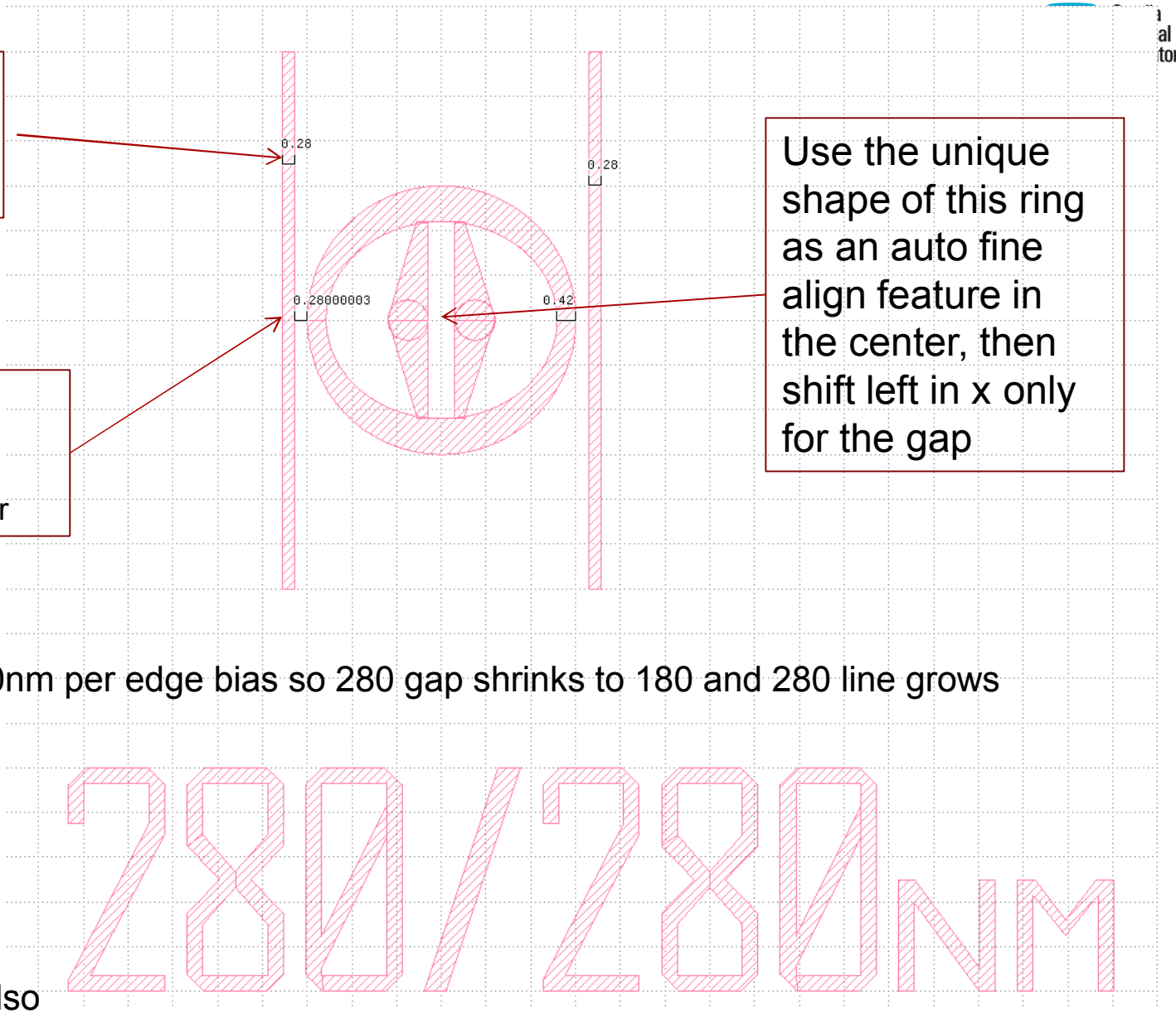
MZMs

- Bandwidth to 23 GHz
- Thermal and Carrier depletion versions
- TW and Lumped versions
- 90 degree and 0/180 degree hybrids





Measure this line
380 on mask
Expect smaller
350- 375



Use the unique shape of this ring as an auto fine align feature in the center, then shift left in x only for the gap

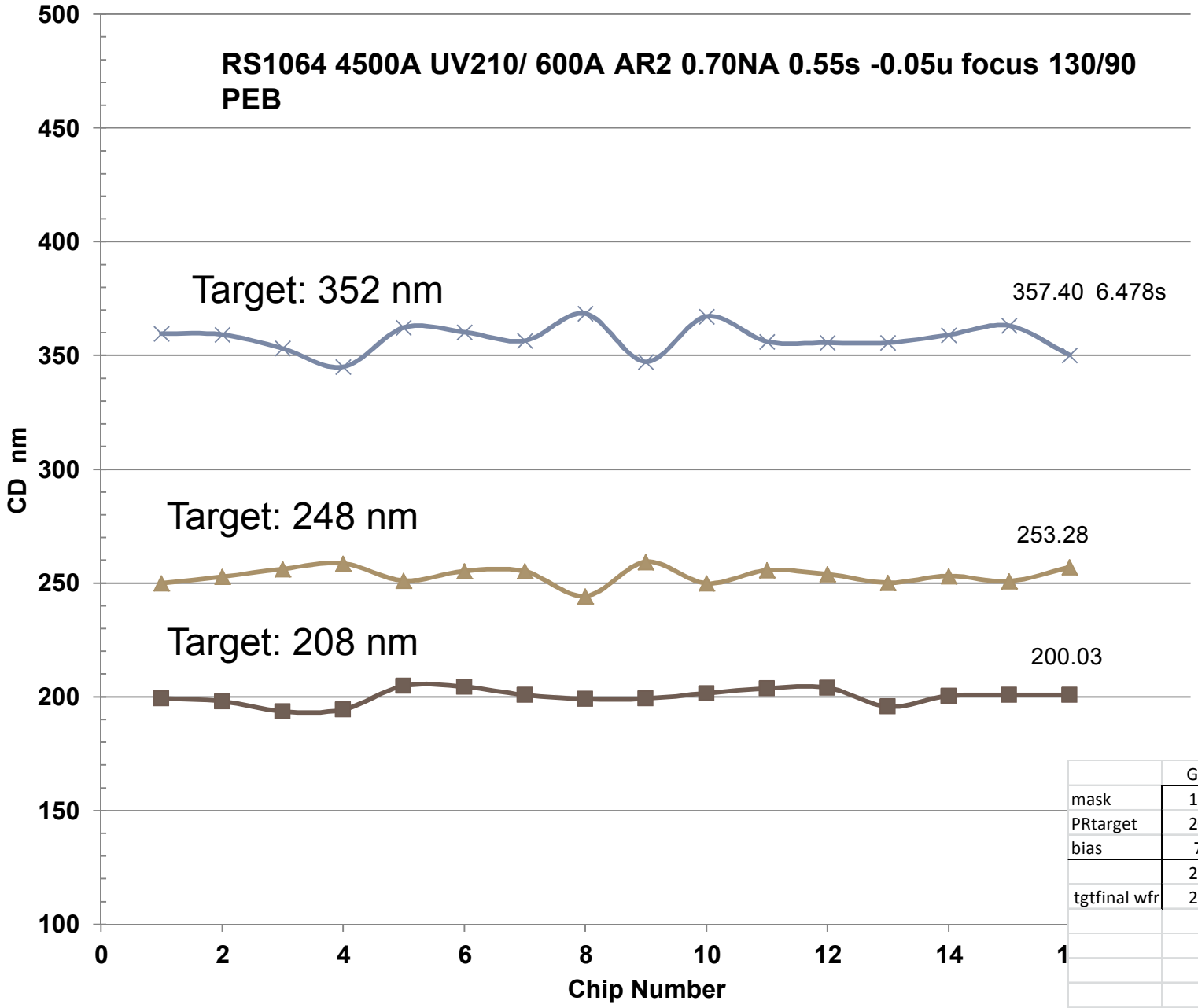
Measure this gap
180 on mask
Expect bigger
185-195

Mask has a +50nm per edge bias so 280 gap shrinks to 180 and 280 line grows to 380

280/280NM

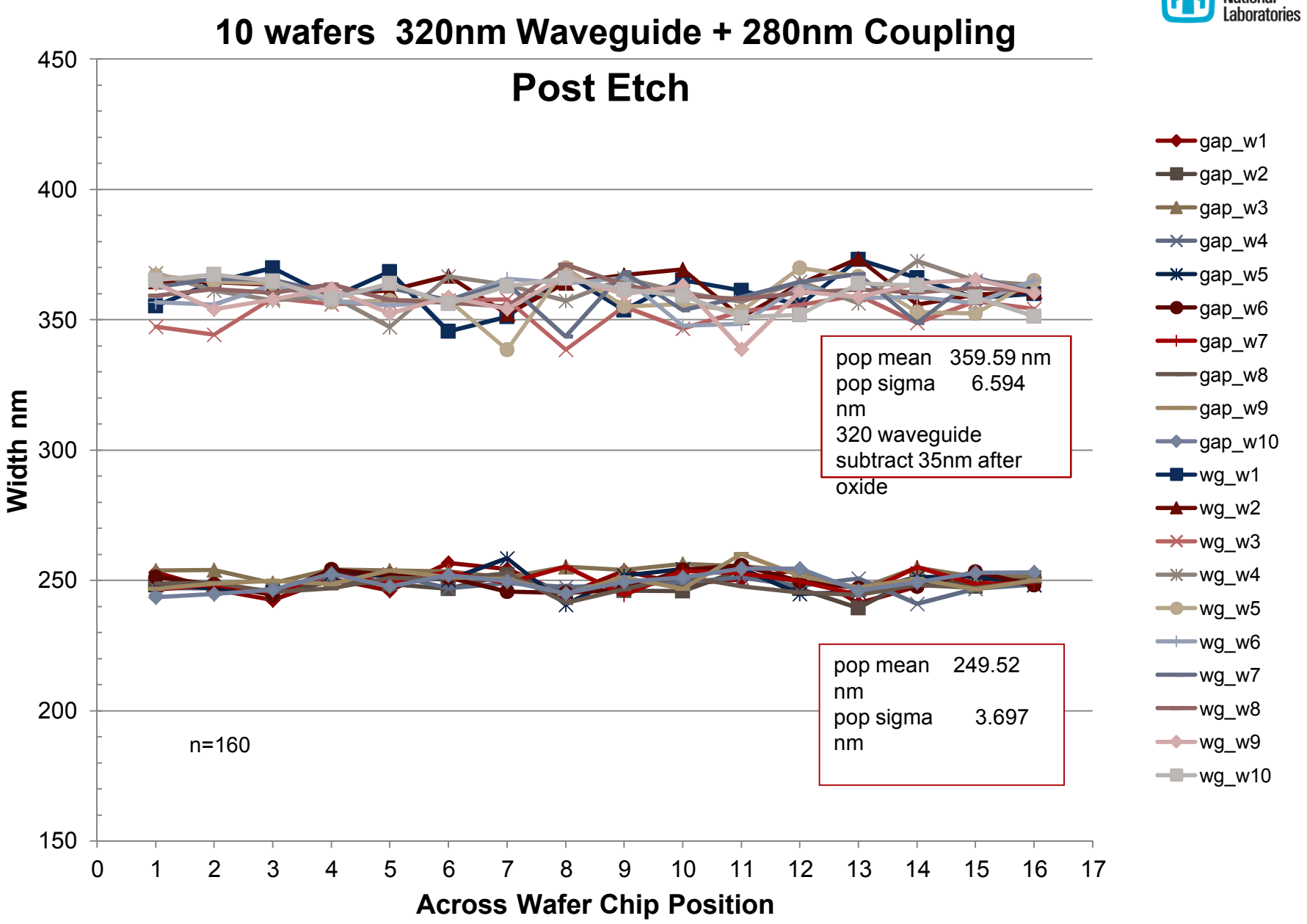
This label is unique also good for coarser align

Post Litho

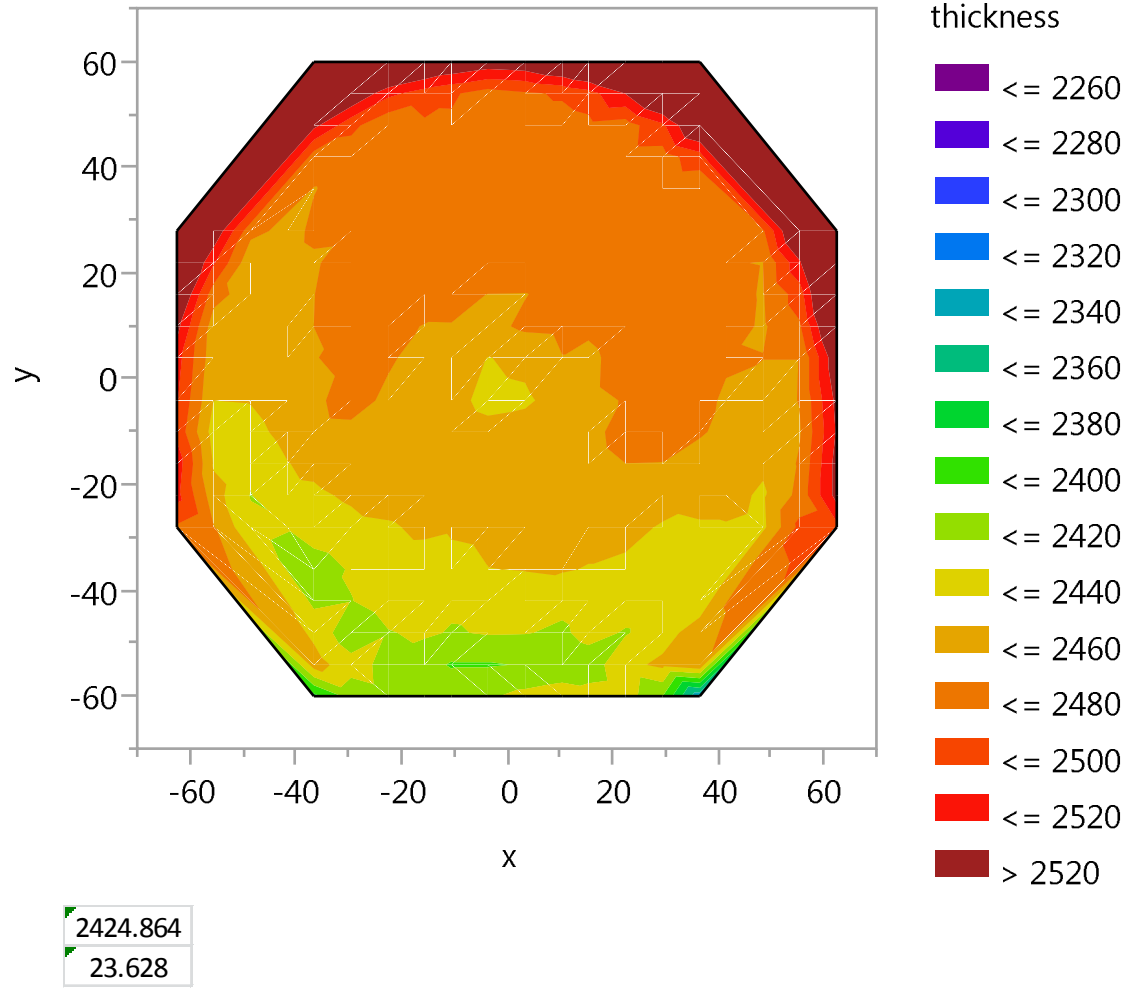


	GAP	WG	GAP
mask	180	380	220
PRtarget	200	360	240
bias	72	-72	72
	272	288	312
tgtfinal wfr	280	280	320

35nm oxide bias
37nm etch bias
72nm


10 wafers 320nm Waveguide + 280nm Coupling
Post Etch
Width nm
450
400
350
300
250
200
150
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
Across Wafer Chip Position
pop mean 359.59 nm
pop sigma 6.594 nm
320 waveguide
subtract 35nm after oxide
pop mean 249.52 nm
pop sigma 3.697 nm
n=160
gap_w1
gap_w2
gap_w3
gap_w4
gap_w5
gap_w6
gap_w7
gap_w8
gap_w9
gap_w10
wg_w1
wg_w2
wg_w3
wg_w4
wg_w5
wg_w6
wg_w7
wg_w8
wg_w9
wg_w10

Contour Plot for thicknessTK1



Schedule for next mask run

Sandia National Laboratories

- May 1: designs due
- May 15: masks in house
- September 15: Si Only expected (4 months)
- December 15: Full process with Ge (7 months) {hopeful}
- March 15 (pessimistic)

- New users must sign NDA with Sandia to get copy of design guide.
- *Existing users need to renew NDAs (all but UCSD)*
- Expect 2 – 3 external customers designing chips
- Sandia designing chips for 2 – 4 customers.

Conclusion

- Next run planned for May time frame
- NDAs new and renew
- ‘Standard cells’ should be available for your use.
- Please give us feedback along the way – if you need something, please ask!