Final Technical Report

Project Title: "100 mm Engineered InP-on-Si Laminate Substrates for InP-based Multijunction Solar Cells"

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Cost-Sharing Partners: Caltech Center for Sustainable Energy Research

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Executive Summary: This project focused on fabrication of InP/Si laminate substrates as templates for growth of InGaAsP/InGaAs and InAlAs/InGaAsP/InGaAs multijunction solar cells. InP/Si template substrates were developed and used as templates for InGaAs solar growth. A novel feature of the program was development of the virtual substrate template, which enables a substrate to be formed with a lattice constant intermediate between those of GaAs and InP. Large-area virtual substrate templates were formed by transfer and bonding of dislocation free InGaAs films wafer onto silicon substrates.

Project Objective: This program was a Caltech-led research project which expanded upon recent advances in III-V laminate substrate development for multijunction solar cell technology to achieve low-cost high efficiency multijunction solar cells fabricated on 100 mm InP/Si laminate substrates. The program comprised four major areas:

1. Scale-up of Caltech's previously-developed InP/Si laminate substrate process for III-V multijunction cell fabrication to 100 mm diameter InP/Si substrates using previously-developed InP/Si template substrates. This included developing a robust process for fabrication of 100 mm InP/Si substrates, and cost-model development for high volume manufacturing.
2. Characterization of 100 mm InP/Si laminate substrate properties, culminating in wafer specification for an InP/Si substrate that is commercially manufacturable at high volumes.
3. Validation of 100 mm InP/Si laminate substrates via fabrication of prototype InGaAsP/InGaAs and InAlAs/InGaAsP/InGaAs multijunction solar cells.
4. Development of an $In_xGa_{1-x}As$/Si "Virtual Substrate" template for growth of InAlAs/InGaAsP/InGaAs multijunction solar cells at 5.800 Å.

Project Accomplishments:

1. Growth and characterization of InGaAs single junction cell on InP/Si template: X-ray diffraction and transmission electron microscopy characterization of InGaAs solar cell grown on InP/Si templates.
2. Growth and characterization of InGaAs/InGaAsP/InAlAs triple junction cell on InP: Spectrolab performed XRD, current-voltage and quantum efficiency measurements on the triple junction cell grown on InP wafer.
3. Defect control of $In_xAl_{1-x}As$ heterostructures followed by successful fabrication and characterization of $In_xAl_{1-x}As$/InP one junction solar cell, with efficiency higher than 5%.
4. Improved InP/Si polishing: InP/Si templates consisting of InP wafer bonded to a 50 mm Si wafer were polished successfully with local surface roughness less than 2 Å. This roughness level is comparable to epi-ready bulk substrates of InP, GaAs and Ge.
5. InP/SiO_2/Si(001) template thermal stability: treatment by rapid thermal annealing (RTA) showed that the interface between InP exfoliated layer and SiO_2/Si was

stable up to 725 ^{o}C; this is the temperature corresponding to MOCVD growth of III-V photovoltaic cell active layers.

6. Demonstration of improved 100 mm InP/Si laminate fabrication: We demonstrated repeated successful generation of 100 mm InP/Si laminates through wafer bonding. There are defects remaining such that the active device-quality area is 85-90% of the total area. These defects appear to be related to incomplete particle removal prior to wafer bonding. This finding indicates that control of the particle density in the bonding ambient is the key driver for the remaining process-induced defects in InP/Si template fabrication.
7. Fabrication of large area In0.36Ga0.64As virtual substrate templates on silicon: X-ray diffraction and optical microscopy of 5.80 Å virtual substrate templates consisting of ¼ of a 2" substrate bonded to 2" silicon wafers.
8. Delivered large area virtual substrate templates for MOCVD growth: Multiple large-area virtual substrates sent to Spectrolab to allow optimization of MOCVD growth parameters and devices.
9. Characterization of surface oxide on virtual substrate and identification of wet etching treatment for oxide removal: X-ray photoelectron spectroscopy (XPS) of surface of In0.43Ga0.56As virtual substrate revealed native oxide that must be removed before MOCVD growth. Further XPS measurements validate short HF wet etch process to remove oxide.

Project Summary:

Delivery of 16 large area virtual substrate templates to Spectrolab for MOCVD growth

To prepare for MOCVD growth attempts on the virtual substrate, 16 large area templates were fabricated and delivered to Spectrolab. The large area is necessary to provide sufficient area for material samples, and the multiple templates will allow proper calibration of alloy composition, temperature and doping parameters. = All were on 2" silicon/SiO_2 substrates.

InP/Si Template Fabrication and Characterization

100 mm InP/Si Template Fabrication

Repeated fabrication of 100 mm InP/Si templates was demonstrated with the transfer of 85% and 90% complete InP layers to 100 mm Si wafers. As Figure 1 shows, the transfers, made by the process detailed in previous reports, have large continuous regions of InP, which appears grey in the images. The blue regions are voids where the InP failed to transfer to the Si/SiO_2 support, which is consequently visible. The void

regions are caused by particulate contamination of the surfaces on the wafers. The particles, which come from the cleanroom ambient, prevent contact between the wafers in their local vicinity and inhibit bonding between the InP and SiO_2 in that region.

Further work will focus on eliminating particle contamination to improve bond quality. A CO_2 "Sno Gun" has been installed in the clean room housing the bonder. This device improves particle removal in the wafer cleaning process. The Sno Gun directs a stream of frozen CO_2 crystals to the wafer surface allowing mechanical removal of particles that remain on the wafer surface after sonication and rinsing.

After the exfoliation and layer transfer process the InP/Si templates have a rough surface that is not suitable for epitaxial growth. This surface roughness and the region of ion-damaged material near the surface must be removed to present a smooth crystalline surface. Previous efforts had developed a two-step process consisting of a wet chemical etch to remove the damaged region followed by chemical mechanical polishing. This process was developed using 1cm by 1cm transfer areas. Figure 2 shows AFM images of the template surface at different stages of this process.

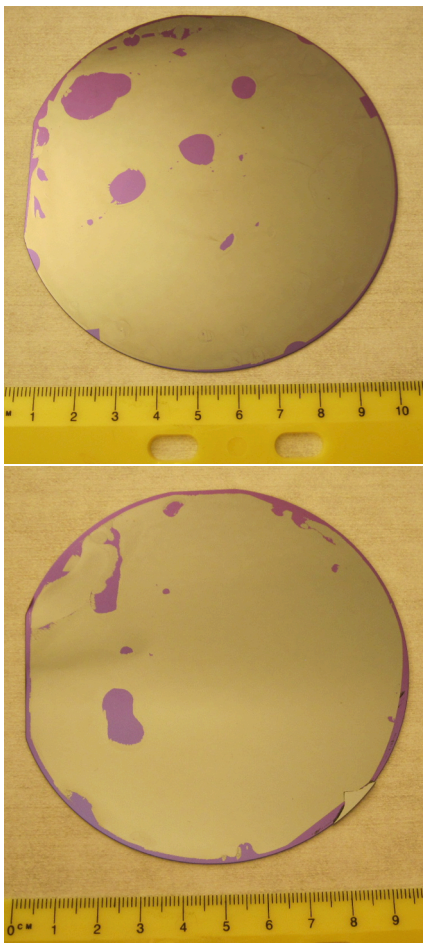

Figure 1. (a) Photograph of 100 mm InP/Si template. Blue regions are voids in the InP where it failed to transfer and Si wafer is visible. Silver regions are transferred InP. (b) Second, more complete 100 mm InP/Si template. Voids in InP are due to particle contamination of surface during bond process.

InP/Si Defect Characterization

The fabrication of InP/SiO_2/Si templates involves ion implantation, wafer bonding and layer exfoliation, which results in damaged layer and surface roughness after exfoliation. The critical Milestone 1 focused on characterizing the different types of surface defects and reducing the density of defects (dislocations, cracks, and voids) on the template surface to $<10^5/cm^2$ total defect density by chemical etching.

The H+ implantation induced exfoliation process can result in lattice damage and cause both extended and point defects. These defects coincide with the region exfoliated on the InP substrate and are most prominent on the surface of the templates. The average defect density for the InP/SiO_2/Si templates was calculated to be $7.2 \times 10^6/cm^2$.

One of the primary defects observed on the template's surface are bubbles. Figure 1 shows bubbles that can occur during the ion implantation induced exfoliation process. Using a profilometer, we were able to determine the size of the surface bubbles present on our InP/SiO_2/Si templates. The Figure 1a is a surface profile of a defect-free InP donor wafer prior to bonding. Figure 1b is a surface profile of the InP/SiO_2/Si template after the exfoliation process but before polishing. The defect density of these surface bubbles was on the average of 2.5 x 10^3 bubbles/cm^2. Future work will require determining the cause of these bubbles and how deep they extend along the template. If the bubbles are prevalent only on the template's surface then they can easily be removed by etching/polishing. However, if they are formed at the InP and SiO_2/Si interface then etching/polishing will not remove the bubbles and may cause voids.

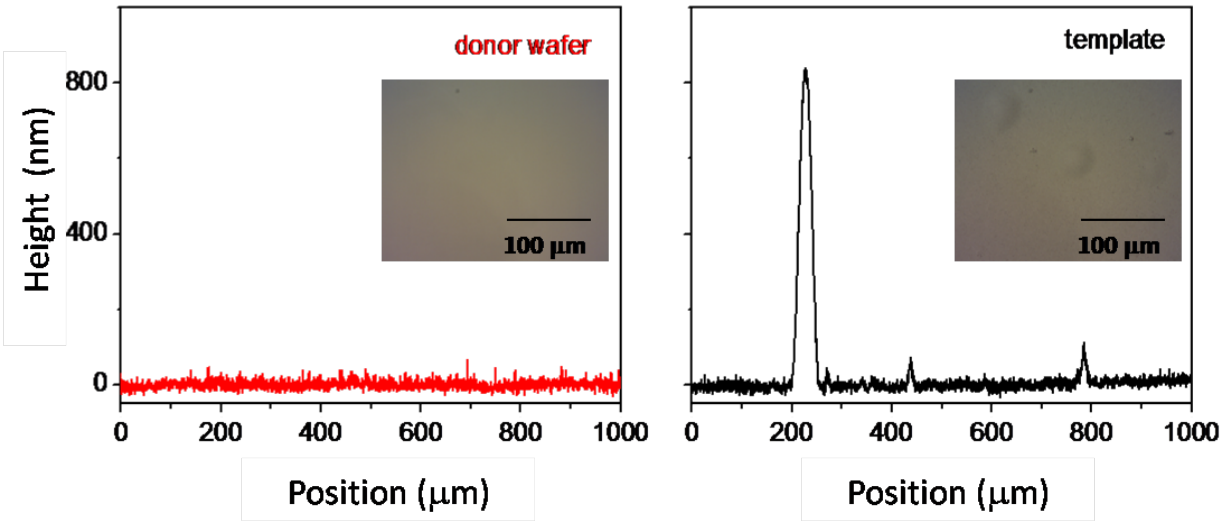

Figure 1. (a) Surface profile using profilometry of a defect-free donor wafer. The insert is an optical micrograph of the InP donor wafer. (b) Surface profile using profilometry of an InP/SiO_2/Si template after the exfoliation process and before etching/polishing. The insert is an optical micrograph of the InP/SiO_2/Si template after exfoliation.

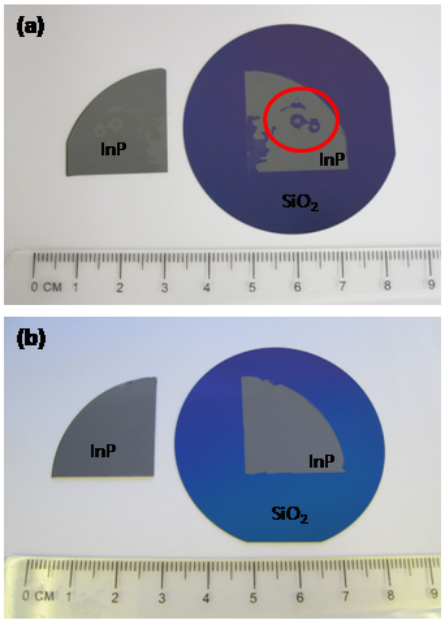

Figure 2. InP/Si/SiO2 template attempts showing (a) defects caused by center pin, (b) high quality transfer away from pin.

Analysis of surface defects revealed that the mechanical configuration of our bonder was contributing to the high defect density. The current pressure plate has a pin-hole design on the center of the plate which prevents even pressure from being applied to the wafer stack. Pressure tests using pressure sensitive papers were performed on the bonder to evaluate the uniformity of pressure. The results showed that the bonder was applying excessive pressure at the center where the pin came down, thus causing the InP substrate to not properly bond and exfoliate to the Si/SiO_2 handle (Figure 2a). In order to reduce the defect density on the $InP/SiO_2/Si$ templates we found it necessary to bond the wafer stack avoiding the center of the bonder. In addition the pressure was non-uniform in the regions away from the pin; consequently we are unable to obtain reproducible $InP/SiO_2/Si$ templates. A new set of pressure plates without the pin were obtained and installed. They demonstrate uniform pressure on the test paper. Further testing will determine if there are thermal gradients.

While awaiting the arrival of the replacement pressure plates, we began bonding three $InP/SiO_2/Si$ templates at one time, avoiding the center pin. Using this technique, better quality templates were obtained with fewer surface defects (Figure 2b).

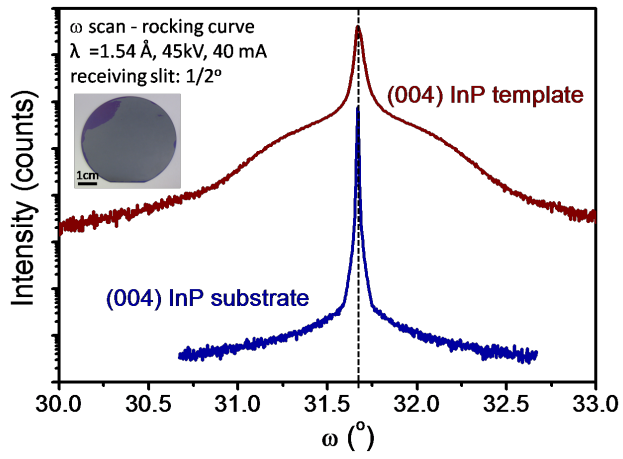

Figure 3 XRD of InP template and InP substrate showing that the direct wafer bonding procedure results in a low strained template. Inset: picture of 2 inch InP template.

X-ray diffraction measurements of the InP templates were performed to verify that the direct wafer bonding process induces low strain in the templates. Figure 3 shows rocking curves for an 800 nm thick InP template (pictured on inset) and of an InP substrate (reference). The broad peak observed for the template may be caused by the difference between the thermal expansion coefficients of InP and SiO_2/Si at 350° C or by local defects, which can be removed by polishing. Systematic etching/polishing and XRD measurements will be carried out to identify the origin of this observed signal.

Future work will involve a) re-tuning of bonding process with new pressure plates, b) characterization of interaction between post-transfer defects and etching/polishing process, c) investigation of transferred film strain state through XRD measurements after repeated etching and polishing steps.

InP/Si Roughness

InP/Si transferred films have rough surfaces to start with due to damage introduced during the fabrication process. An AFM image of as-transferred InP/Si template is shown in Fig. 4(a). Measured root-mean-square (RMS) surface roughness is 13.2 nm. As part of the exfoliation process, ions are implanted deep into the InP donor substrate. The approximately Gaussian implanted ion distribution and the stresses associated with the void and crack formation that splits off the layer result in approximately the top 300-400 nm of InP having substantial crystal damage, which must be removed for successful growth epitaxial films. A wet chemical etching process is used to remove this damaged layer. We used $HCl:H_3PO_4:H_2O_2$ with the volume ratio 1:2:6 and etched for 8 minutes with 50nm/min etching rate. This process strongly depends on the temperature of the environment in which the etching is taking place. For that reason the etching process had been carried out in a cleanroom with a precise control of room temperature. We measured the surface roughness after chemical etching and we found that the RMS surface roughness is 6.3 nm (Fig. 4(b)). Although we've been able to reduce the rms surface roughness significantly, the sample is still too rough for starting epitaxial growth. Epi-ready substrates should have a maximum surface roughness of 0.5-1 nm.

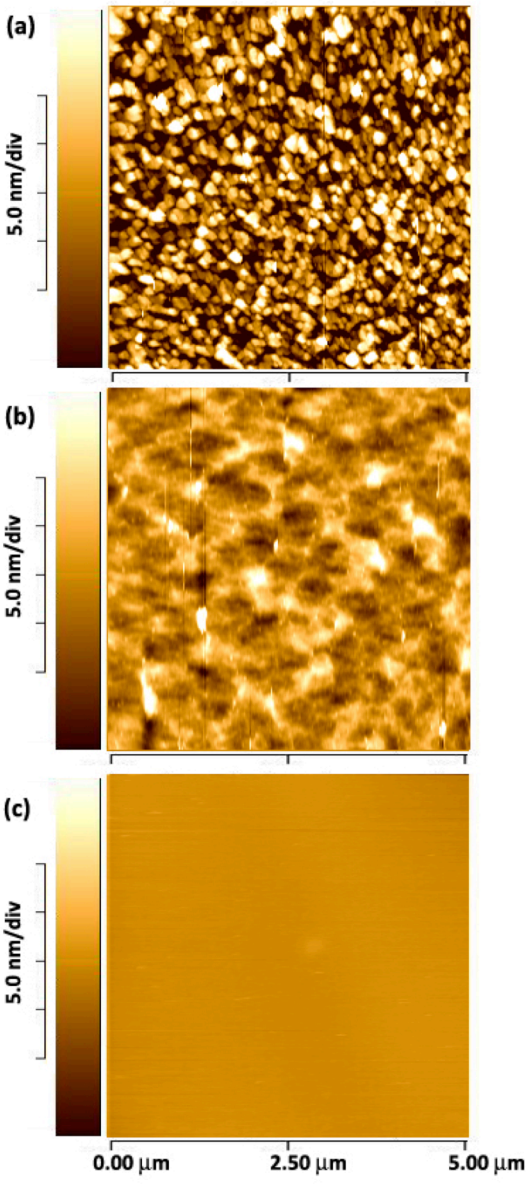

Fig. 4. AFM images of InP/Si template (a) as transferred, (b) after wet-etching, and (c) after wet etching and chemical-mechanical polishing.

We then used chemical-mechanical polishing to smooth the surface to the required values of surface roughness. In

previous studies we only performed mechanical polishing using abrasive particles and we obtained surface roughnesses on the order of ~ 3 nm. This quarter's efforts focused on the development of a chemical polishing process, using a combination of citric acid and NaOCl solution. A 1:10 NaOCl:H2O volume ratio solution is mixed with 1:2 Citric acid:H2O volume ratio solution. The chemical polishing is augmented by mechanical polishing from the rough surface of the polishing pad. The polishing disk is rotated with 30 rpm rotation for 20 minutes and the solution is constantly applied to the substrate. After the polishing we measured the surface roughness of InP/Si virtual substrate as shown in Fig. 4(c) and rms surface roughness for a 5 x5 micron area is measured to be 0.44 nm, which is suitable for epitaxial growth. Figure 4 shows the evolution of the surface roughness through the etching and polishing processes and the scale bars are intentionally kept same to compare the surface roughness of InP/Si at each process step. We've been able to polish 1 x 1 cm area substrates successfully. Future work should center on scaling up this process for larger area InP/Si templates and eventually growth of solar cells on top of fabricated substrates with surface roughness below 1 nm.

Characterization of surface oxide on virtual substrate and identification of wet etching treatment for oxide removal

In order to nucleate epitaxial growth on the virtual substrate, the surface of the template must present a clean crystalline face to the reactant gas streams. The presence of a native oxide layer can inhibit growth nucleation and is suspected as the source of failure in previous growth experiments. The virtual substrate fabrication process maintains a protective wax layer on the final exposed surface, which is the same as the exposed surface of the film as grown on the original substrate. This surface is expected to have a native oxide layer of 1-3 nm thickness as a result of contact with air after growth and during subsequent processing steps. X-ray photoelectron spectroscopy (XPS) data suggested that the majority of the native oxide had been removed from the surface, which is a necessary step for subsequent epitaxial growth. The virtual substrate template exhibited no visible change after the etching treatment under optical or scanning electron microscope inspection.

Characterization of Virtual Substrate Bond Endurance at High Temperatures

In order to serve as a template for epitaxial growth, the virtual substrate must be able to tolerate cycling up to the high temperatures used in MOCVD processes without experiencing delamination of the bond interface or degradation of the transferred film. A high temperature annealing process was used to investigate the bond integrity after such high temperature cycling. Inspection of the sample before and after annealing looked for degradation and delamination.

The test sample consisted of a virtual substrate template of 40 nm thick In0.43Ga0.57As. One quarter of a 2" wafer was used to prepare this template, and the film was bonded to an n-type silicon wafer with 100 nm of thermal oxide. X-ray diffraction measurements verified that the template was fully relaxed to its native lattice parameter, and the sample was cleaved into smaller pieces. The annealing process was conducted with a Rapid Thermal Annealer (RTA) using a susceptor under nitrogen flow and consisted of a 10 minute ramp from room temperature to 400°C, a 30 second hold at 400 followed by a 3 minute ramp to 600°C and a 30 second hold at 600. At this

point the sample was allowed to cool under the nitrogen flow, taking approximately 30 minutes to reach 100°C. The annealing process was performed on a subset of the original sample to allow comparison between annealed and un-annealed pieces in the subsequent characterization effort. Optical micrographs of the surface of the virtual substrate before and after annealing indicated that samples exhibit a slight change of appearance, mostly in the form of color difference. The crack network and overall texture of the surface seems unaffected by the heat treatment and there are no signs of gross delamination due to bubbles or thermal stresses.

Virtual substrate template fabrication

A third milestone focused on the development of a virtual substrate template for epitaxial growth of material with a lattice constant of 5.80 Å. Previous work focused on the characterization of epitaxially grown pseudomorphic $In_xGa_{1-x}As$ layers with mismatch to their InP growth substrates ranging from +0.3% to -0.7%. High resolution x-ray diffraction (XRD) measurements of these films showed that at 40 nm they exhibited negligible strain relaxation and hence low defect density. The virtual substrate concept calls for these films to be removed from their growth substrates, have their strain elastically relaxed, and then be bonded onto Si/SiO2 substrates to serve as templates for subsequent growth.

Recent work has focused on the process of removing the $In_xGa_{1-x}As$ layer from the InP and relaxing its strain in the process of bonding to Silicon. Initial efforts incorporated a 600 nm polyimide film to support the InGaAs after removal of the InP through selective chemical etching in concentrated HCl. Although the polyimide was able to support the thin InGaAs film, thermal stresses due to a mismatch in the coefficient of thermal expansion resulted in curling and buckling of the film ensemble. It was not possible to bond these films to planar substrates.

We developed an alternative process, outlined in Figure 5, which is based on the epitaxial lift-off process. First the InGaAs layers are coated with Apiezon W wax that has been dissolved in Trichloroethylene (TCE). The solvent is baked out of the wax on a hot plate to restore the rigidity of the wax. Once the coating has hardened and cooled, the InP is removed through selective etching in concentrated HCl. The wax supports the thin InGaAs yet allows the strain to be relaxed. With the InP removed, the InGaAs is placed on a Si/SiO2 substrate with a small drop of water at the interface. Left overnight, the water evaporates and leaves the InGaAs bonded to the substrate. The wax is then removed in TCE.

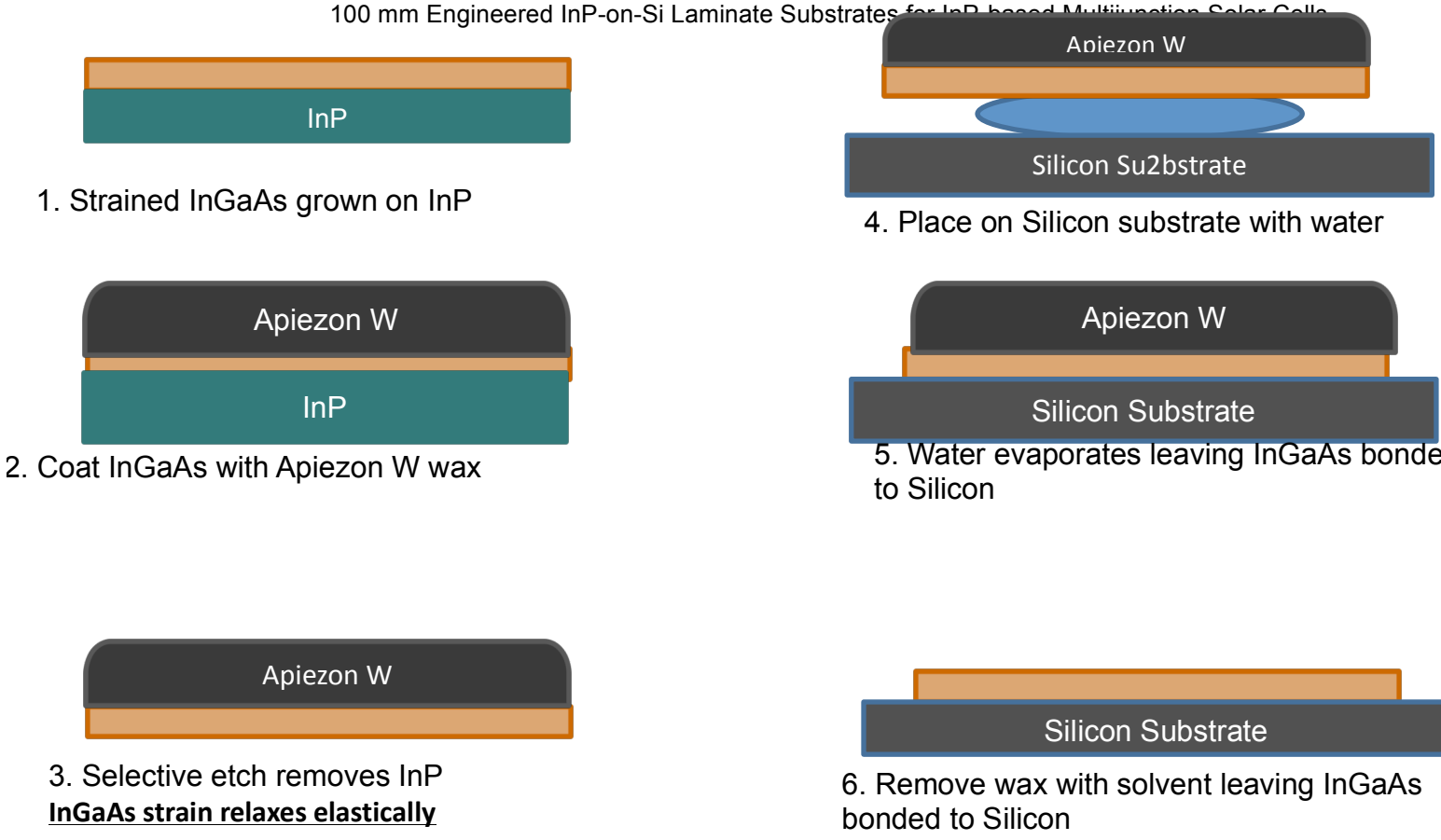

Figure 5. Process for transfer of InGaAs to Silicon

A selection of representative InGaAs films on Si/SiO_2 after transfer are shown in Figure 6. We were able to transfer areas of 1 cm^2 on a repeatable basis. The quality of the transferred films is sensitive to handling during the various stages of the process, as evidenced by areas of bare Silicon where the InGaAs failed to bond.

In addition, optical micrographs show numerous cracks in the InGaAs, perhaps resulting from stress during handling, as well as evidence of particles at the bond interface. Figure 7 shows a variety of the defects of the transferred films.

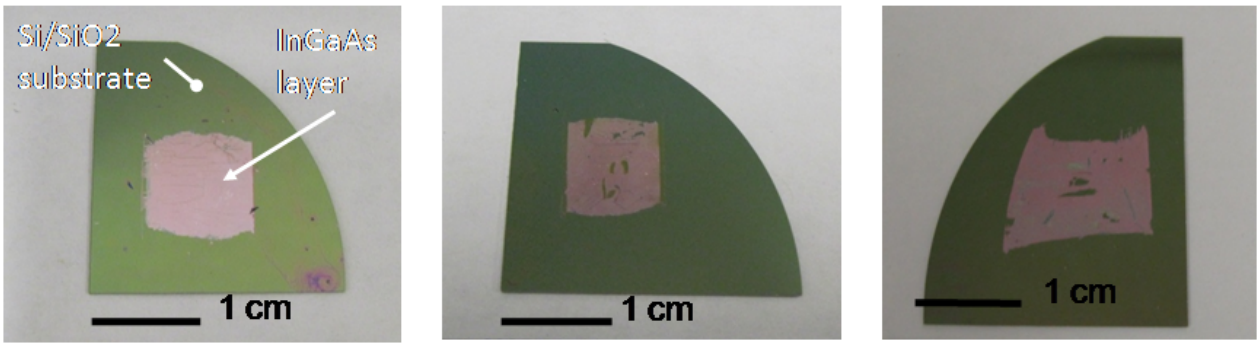

Figure 6. Transfer of $In_xGa_{1-x}As$ films onto Si/SiO_2 substrates

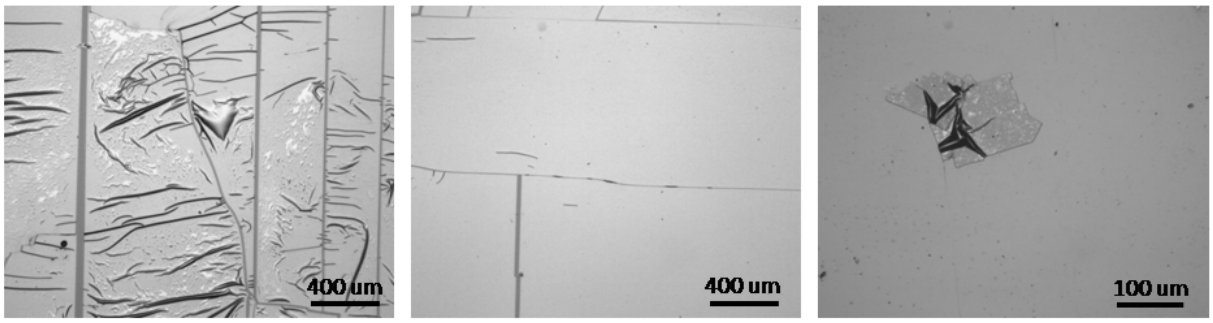

Figure 7. Optical micrographs of transferred InGaAs films. Cracks appear along crystal orientation.

XRD measurements of the (004) reflections of the transferred films were performed to determine the degree of strain relaxation. In order to serve as virtual substrates, these films must regain their native lattice constant. Measurements were taken on transferred films of each strained composition. Figure 8 shows the collected data plots for (004) reflections for the films as grown on InP and after transfer with a simulated scan for a fully relaxed film of 40 nm included for reference.

Based on the location of the film peaks, the measured lattice constant of the transferred films is equivalent to the native lattice constant as determined by the film composition. This indicates full relaxation of the strain. In addition, the width of the peak for the transferred film is not substantially larger than the peak of the film on the InP substrate or of the simulation. This suggests a high degree of uniformity of strain and a low number of dislocations generated during the transfer.

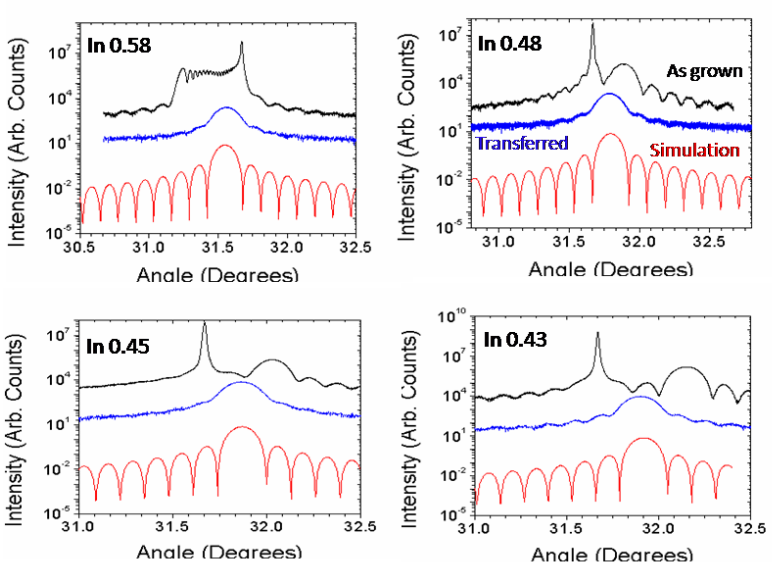

Figure 8. XRD (004) reflections for InGaAs films as grown, after transfer, and simulated

Future work should include a) further development of the transfer process to reduce cracks and defects, increase the area of transfer, and using InGaAs with a native lattice constant closer to 5.800Å, b) additional analysis of films to determine dislocation density and c) analysis of the wax/InGaAs mechanical system to better understand the strain relaxation process.

InAlAs/InP Solar Cell Fabrication

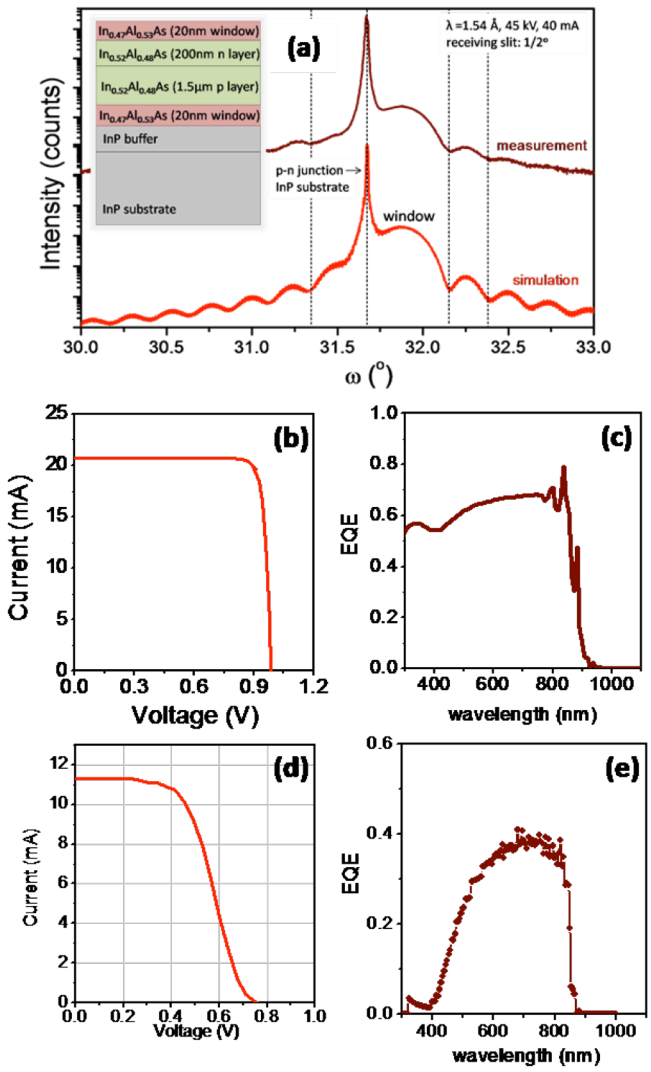

Fig. 9. (a) X-ray diffraction measurement and simulation of InAlAs solar cell sample 1. Inset: solar cell structure. (b) Light I-V curve and (c) external quantum efficiency obtained from device modeling. Experimental (d) light I-V curve and (e) spectral response of solar cell sample under 1.5AM.

One of the key milestones of this project was the design of an InAlAs/InGaAsP/InGaAs 3 junction solar cell. The $In_xAl_{1-x}As$ solar cell device that will be the top cell on the 3 junction cell was successfully fabricated and characterized. Samples are grown by MOVPE by *Spectrolab, Inc*. A first solar cell sample (1) was fabricated with p-n junction lattice matched to InP substrate (a = 5.8686 Å).

As shown on the inset of Figure 9, solar cell sample 1 is formed by an $In_{0.52}Al_{0.48}As$ (E_g = 1.47 eV) p-n junction and $In_{0.47}Al_{0.53}As$ (E_g = 1.67 eV) 20 nm top and bottom windows (highly doped layers that minimize surface recombination). X-ray diffraction measurement and simulation (Figure 9 (a)) shows coherently strained layers, in accordance with cross-section transmission electron microscopy presented in a previous report. According to the device modeling performed [Figures 9 (b) and (c)], the theoretical efficiency of this cell is 17.9%, with V_{OC} equal to 984 mV. Electrical measurements performed under AM 1.5G at Caltech showed an efficiency of 4.6 %. The external quantum efficiency obtained for sample 1 is shown in Figure 9 (e).

In order to explore the optimal InAlAs solar cells performance, a second sample was grown with the same parameters of sample 1 but different window composition. As shown on the inset of Figure 10(a) the $In_{0.35}Al_{0.65}As$ window layers (E_g = 1.98 eV) were richer in Al this time, causing more light absorption by the p-n junction but simultaneously more strain on the heterostructure. XRD measurement was in good agreement with simulation, indicating that the heterostructure is coherently strained although more strained, as shown in Figure 10(a). Cell efficiency obtained by device modeling predicts an increase in efficiency, now 19.6%. Light I-V curve and spectral response measurements showed that solar cell sample 2 is more efficient than sample 1. The external quantum efficiency enhancement [compare Figures 9(e) and 10(e)] is

due to the high band gap energy of this new window, which allows more photons to be absorbed by the p-n junction.

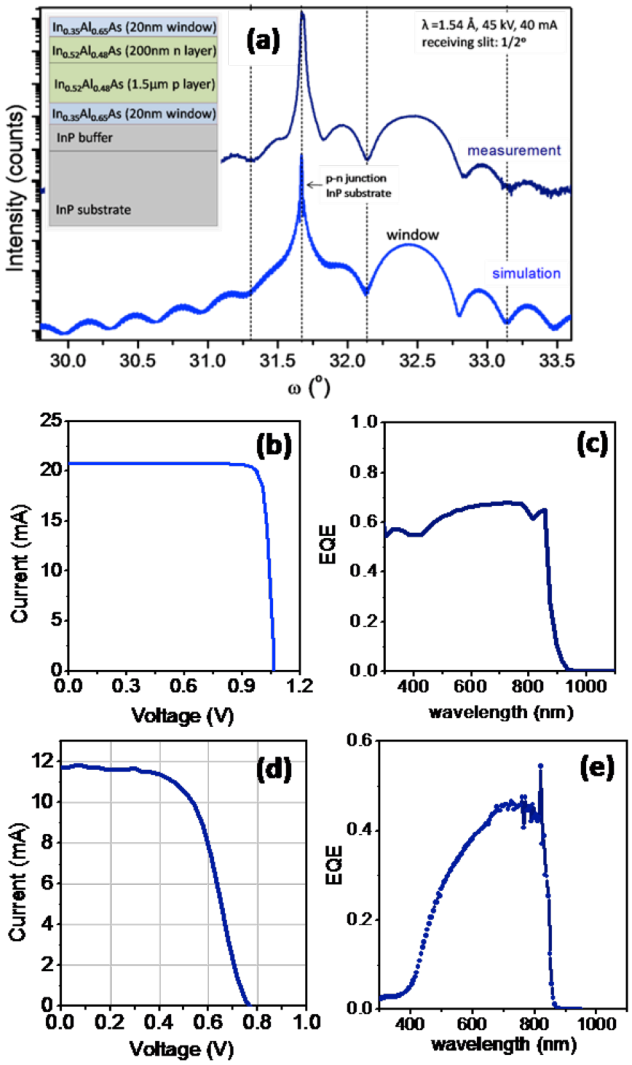

Fig. 10. (a) X-ray diffraction measurement and simulation of InAlAs solar cell sample 2. Inset: solar cell structure. (b) Light I-V curve and (c) external quantum efficiency obtained from device modeling. Experimental (d) light I-V curve and (e) spectral response of solar cell sample under 1.5AM.

Table 1 summarizes all figures of merit for the two samples, comparing device modeling and experimental results. The overall efficiency of the cells – higher than 5% for sample 2 - is currently limited by the metallic contacts used. By optimizing top and bottom contacts, an increase in V_{OC} and cell efficiency are expected. Effort will be made in the next quarter in order to optimize the Ohmic contact now used.

Sample 2 was also characterized by optical measurements. Room temperature photoluminescence (PL) measurements were performed to determine cell quality and investigate its diode behavior. By measuring the integrated PL intensity it is possible to infer the cell's external quantum efficiency and its V_{OC}; mimicking a diode under forward bias voltage.

	V_{oc} (mV)	J_{sc} (mA/cm²)	FF (%)	Eff (%)
Cell 1 modeling	984	20.7	88.0	17.9
Cell 1 experiment	756	11.3	54.0	4.6
Cell 2 modeling	1064	20.8	88.7	19.7
Cell 2 experiment	767	11.7	60	5.3

Table 1. Figures of merit obtained from device modeling and electrical measurements for InAlAs/InP solar cell samples 1 and 2.

Figure 11(a) shows the PL intensity as a function of laser excitation power. Increasing the laser power also increases PL intensity, indicating that the cell is a good diode. The pump power intensity can be easily converted into an injection current, which depends on laser energy and spot size. By integrating the PL signal from Figure 11(a) and normalizing it by the laser's scattering to compensate all losses due to optical components, one can determine the transition between radiative diffusion current and

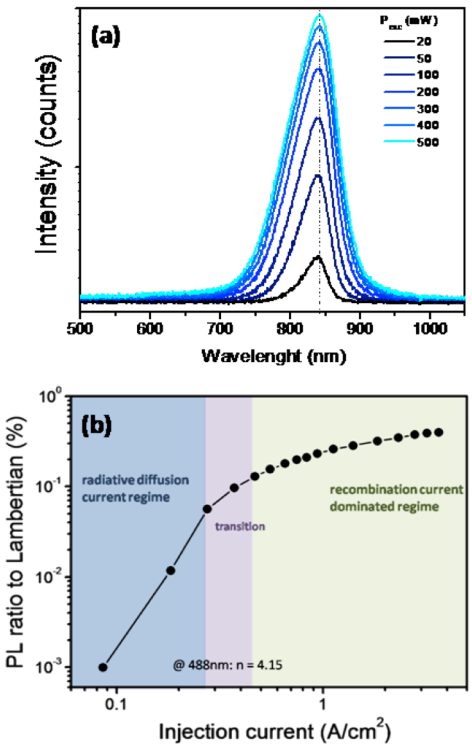

Fig. 11. (a) Photoluminescence (PL) as a function of power excitation showing the diode behavior of solar cell sample 2. (b) Ratio between integrated PL signal from (a) and a Lambertian sample as a function of injection current. Note the transition between radiative diffusion and recombination current regimes.

recombination current regimes, as shown in Figure 11(b) where each point corresponds to one excitation power. Absolute PL measurements are extremely useful to follow the cell's degradation after each processing step and will be routinely used in future device processing.

Presentations:

1. M. S. Leite *et al*. *Strain Engineering of III-V Compound Semiconductors for an Optimized Triple Junction Solar Cell.* MRS Fall meeting November 2011.
2. M. S. Leite *et al*. *A new paradigm for multijunction solar cell.* American Physical Society Meeting, March 2011.
3. M. S. Leite *et al*. *Wide band gap InAlAs solar cells for an InP-based multijunction paradigm***.** Spring MRS, April 2011.
4. M. S. Leite *et al*. *InAlAs Epitaxial Growth for Wide Bandgap Solar Cells.* PVSC, June 2011 – to be presented.
5. E. C. Warmann *et al A "Virtual Substrate" Supplies Tailored Lattice Constant Template for High Efficiency Multijunction Solar Cells.* Spring MRS, April 2011.
6. M. S. Leite *A new paradigm for multijunction solar cells.* Seminar at Mechanical Eng. Department at MIT, Nov 2010.
7. M. S. Leite. *A new paradigm for multijunction solar cells.* Seminar at Boston University. Nov 2010.
8. M. S. Leite, E. Warmann, D. Callahan, H. A. Atwater. *Virtual Substrate: a New Template for Dislocation-Free Epitaxial Growth*. Poster presented at 2010 Fall MRS – Poster Award Nominee.
9. Defect Control in InAlAs/InP Heterostructures for Multijunction Solar Cells". Presented by Marina Leite at 2010 MRS Spring Meeting, San Francisco, CA.
10. "InGaAs Virtual Substrate Templates for Low-defect Epitaxial Growth of Novel InAlAs/InGaAsP/InGaAs Multi-junction Solar Cells" Emily Warmann, MRS 2010 Spring Meeting, San Francisco, CA.
11. Harry A. Atwater, Colloquium Ehrenfestii Leiden University, Leiden, the Netherlands, 3/31/2010
12. Harry A. Atwater, American Physical Society March Meeting, Portland OR, 3/19/2010
13. Harry A. Atwater, Materials Science Colloquium, Cornell University, Ithaca NY, 3/17/2010
14. Harry A. Atwater, TED Conference on Technology, Entertainment and Design, Long Beach, CA, 2/12/2010.
15. Harry A. Atwater, Center for Energy Efficient Materials Colloquium, UC Santa Barbara, Santa Barbara, CA, 2/3/2010
16. Harry A. Atwater, Conference on Mathematics of Sustainability and Green Technology, Harvey Mudd College, Claremont, CA, 1/30/2010
17. Harry A. Atwater, Maddox Solar Energy Lecture, Texas Tech University, Lubbock, TX
18. Koray Aydin, Marina S. Leite, and Harry A. Atwater, "Increased cell efficiency in InGaAs thin film solar cells with dielectric and metal back reflectors," 34th IEEE Photovoltaics Specialists Conference, Philadelphia, PA, June 7-12, 2009

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2. Wafer-Scale Strain Engineering of Ultrathin Semiconductor Crystalline Layers, Leite, Marina S.; Warmann, Emily C.; Kimball, Gregory M.; et al., ADVANCED MATERIALS Volume: 23 Issue: 33 Pages: 3801-+ Published: SEP 1 2011

3.Wide-band-gap InAlAs solar cell for an alternative multijunction approach, Leite, Marina S.; Woo, Robyn L.; Hong, William D.; et al. APPLIED PHYSICS LETTERS Volume: 98 Issue: 9 Article Number: 093502 Published: FEB 28 2011