Amorphous silicon carbide passivating layers to enable higher processing temperature in crystalline silicon heterojunction solar cells

Very efficient crystalline silicon (c-Si) solar cells have been demonstrated when thin layers of intrinsic and doped hydrogenated amorphous silicon (a-Si:H) are used for passivation and carrier selectivity in a heterojunction device. One limitation of this device structure is the (parasitic) absorption in the front passivation/collection a-Si:H layers; another is the degradation of the a-Si:H-based passivation upon temperature, limiting the post-processes to approximately 200°C thus restricting the contacting possibilities and potential tandem device fabrication. To alleviate these two limitations, we explore the potential of amorphous silicon carbide (a-SiC:H), a widely studied material in use in standard a-Si:H thin-film solar cells, which is known for its wider bandgap, increased hydrogen content and stronger hydrogen bonding compared to a-Si:H.

We study the surface passivation of solar-grade textured n-type c-Si wafers for symmetrical stacks of 10-nm-thick intrinsic a-SiC:H with various carbon content followed by either p-doped or n-doped a-Si:H (referred to as i/p or i/n stacks). For both doping types, passivation (assessed through carrier lifetime measurements) is degraded by increasing the carbon content in the intrinsic a-SiC:H layer. Yet, this hierarchy is reversed after annealing at 350°C or more due to drastic passivation improvements upon annealing when an a-SiC:H layer is used. After annealing at 350°C, lifetimes of 0.4 ms and 2.0 ms are reported for i/p and i/n stacks, respectively, when using an intrinsic a-SiC:H layer with approximately 10% of carbon (initial lifetimes of 0.3 ms and 0.1 ms, respectively, corresponding to a 30% and 20-fold increase, respectively). For stacks of pure a-Si:H material the lifetimes degrade from 1.2 ms and 2.0 ms for i/p and i/n stacks, respectively, to less than 0.1 ms and 1.1 ms (12-fold and 2-fold decrease, respectively).

For complete solar cells using pure a-Si:H i/p and i/n stacks, the open-circuit voltage (V_{oc}) drops from 720 mV to 600 mV when annealing the device at 350°C. Yet, the V_{oc} of devices using an intrinsic a-SiC:H layer with around 10% carbon content in the i/p stack is more resilient to such process, dropping from 710 mV to 690 mV. Also, irrespective of annealing, the slightly improved transparency of a-SiC:H layers allows about 1% current gain due to a better blue-light response. Active-area efficiencies above 20% are thus obtained for particular carbon content conditions, slightly higher than for devices using only a-Si:H. Even for a-SiC:H layers with bandgaps of up to 2.1 eV, good hole collection is maintained (with fill factors of 67% for devices using intrinsic a-SiC:H in the i/p stack, compared to 73% for the reference device). However, S-shaped current-voltage curves were obtained for devices using such a-SiC:H layers in the i/n stack, indicating impeded transport, which would suggest that most of the bandgap increase translates in a conduction-band offset.