

Amorphous silicon carbide passivating layers for crystalline-silicon-based heterojunction solar cells

Mathieu Boccard¹ and Zachary Holman¹

School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, Arizona 85287-5706, USA

(Dated: August 4, 2015)

Amorphous silicon enables the fabrication of very high-efficiency crystalline-silicon-based solar cells due to its combination of excellent passivation of the crystalline silicon surface and permeability to electrical charges. Yet, amongst other limitations, the passivation it provides degrades upon high-temperature processes, limiting possible post-deposition fabrication possibilities (*e.g.* forcing the use of low-temperature silver pastes). We investigate the potential use of intrinsic amorphous silicon carbide passivating layers to sidestep this issue. The passivation obtained using device-relevant stacks of intrinsic amorphous silicon carbide with various carbon contents and doped amorphous silicon are evaluated, and their stability upon annealing assessed, amorphous silicon carbide being shown to surpass amorphous silicon for temperatures above 300 °C. We demonstrate open-circuit voltage values over 700 mV for complete cells, showing an improved temperature stability for the open-circuit voltage. Transport of electrons and holes across the hetero-interface is studied with complete cells having amorphous silicon carbide either on the hole-extracting side or on the electron-extracting side, evidencing a better transport of holes than of electrons. Also, due to slightly improved transparency, complete solar cells with slightly better performances even prior to annealing than obtained with a standard amorphous silicon layer are demonstrated using an amorphous silicon carbide passivation layer on the hole-collecting side.

I. INTRODUCTION

Very efficient crystalline silicon (*c*-Si) solar cells can be obtained when thin intrinsic and doped hydrogenated amorphous silicon (*a*-Si:H) layers are used for passivation and carrier selectivity^{1,2}. A well known loss mechanism of such *a*-Si:H / *c*-Si heterojunction devices is parasitic absorption of blue light in the *a*-Si:H layers on the light-entering side³⁻⁶. Several strategies are being followed to side-step this problem including thinner layers, wider- or indirect-bandgap materials, or interdigitated back-contact design as used in the recent world record device⁴⁻⁹.

Another less reported limitation is the observed degradation of the passivation quality provided by the *a*-Si:H layers after heating the device at elevated temperatures. This degradation typically limits all the process steps following *a*-Si:H deposition to temperatures below 250 °C. Whereas the ability to make good cells with low-temperature processing is an advantage of this technology, the inability to use higher temperatures prevents the use of high-temperature, low-resistivity silver pastes (typically requiring annealing at over 400 °C¹⁰), and of silicon-nitride passivating and anti-reflecting coatings, which could be of interest for back-contacted devices¹¹. Also, higher-temperature steps could be required in fabricating tandem devices using a heterojunction bottom cell since the process flow to fabricate most top cell candidates require high temperature steps (typically above 400 °C)¹²⁻¹⁵. The temperature-induced degradation of *a*-Si:H is especially drastic for layers with a Fermi level close to the valence band, whether because of doping (p-type layers) or the presence of an electric field (intrinsic layers adjacent to a high-work-function material). It was notably shown that, in the case of a stack of intrinsic and

p-type *a*-Si:H (i/p stack), passivation starts to degrade at lower temperatures than for an intrinsic *a*-Si:H layer only¹⁶. This effect was attributed to the fact that the nominally intrinsic layer of the i/p stack has its Fermi level shifted towards the valence band due to the presence of the p-type layer, decreasing the energy for defect creation due to bond breaking in this layer. Improving the temperature stability of the chemical passivation of such an i/p stack would thus require a modification of the intrinsic *a*-Si:H layer on which the passivation relies, since any good hole-collecting layer will shift the Fermi level in the intrinsic *a*-Si:H layer towards the valence band.

Amorphous silicon carbide (*a*-SiC_x:H) is an excellent candidate to improve temperature stability according to the studies from Beyer *et al.*^{17,18}: Upon carbon incorporation into an *a*-Si:H film, the hydrogen incorporation increases, the diffusion coefficient of hydrogen decreases, and the temperatures of both hydrogen effusion peaks increase. All these effects, linked to the stronger bonding of hydrogen to carbon than to silicon, would tend to reduce the formation of dangling bonds through hydrogen effusion upon annealing. Also, incorporating carbon in the *a*-Si:H matrix widens the bandgap, reducing parasitic absorption of short-wavelength light for a given layer thickness. The expected challenges when using intrinsic *a*-SiC_x:H in lieu of *a*-Si:H are maintaining sufficient passivation since the density of dangling bonds increases with the carbon incorporation, and good collection of carriers despite the larger band offsets resulting from the wider bandgap.

Though passivation of *c*-Si with *a*-SiC_x:H layers has been demonstrated by several groups in the last 15 years¹⁹⁻²³, the passivation quality reported has not reached that obtained with *a*-Si:H^{2,24,25}. Also, in most studies, Substantially thicker layers than typically used

in devices were used to enable efficient passivation, and the few reported results on complete silicon heterojunction solar cells showed moderate efficiencies and did not investigate improved transparency and thermal stability^{22,23,26,27}.

We investigate in this article the passivation performance of device-relevant stacks of intrinsic a -SiC_x:H and doped a -Si:H, evidencing strong annealing effects. We show that silicon-rich a -SiC_x:H can be used as a passivating layer in high-efficiency c -Si heterojunction devices with open-circuit voltages (V_{oc}) up to 730 mV. We find a slight improvement in transparency with no loss in electrical performance when using an a -SiC_x:H layer of appropriate thickness as a passivating layer below an a -Si:H p-type hole-collecting layer. These devices also exhibit improved stability upon post-fabrication annealing steps up to 350 °C.

II. EXPERIMENTAL DETAILS

We investigate intrinsic a -SiC_x:H layers deposited by plasma-enhanced chemical vapor deposition (PECVD) at a temperature of 250 °C and a pressure of 4.3 mbar from a mixture of silane, methane and hydrogen (SiH₄, CH₄ and H₂). The CH₄ to CH₄ + SiH₄ ratio (R_{CH_4}), defined as the mass flow rate of CH₄ divided by the sum of CH₄ and SiH₄ mass flow rates, was varied from 0% to 75%, and the flow of H₂ was kept at 400 sccm except when specifically mentioned. 50-nm-thick layers were used for ellipsometry characterization and some specific lifetime measurements, and 4-nm- to 10-nm-thick layers were used in cells. Except for ellipsometry measurements which were performed on a single-side-polished wafer, layers were deposited on 170-μm-thick pyramidally textured n-type wafers with resistivities of 1 Ω.cm to 10 Ω.cm that were cleaned prior to deposition with piranha, RCA-B and buffered oxide etch (BOE).

For complete silicon heterojunction cells, boron-doped and phosphorous-doped PECVD a -Si:H layers with a nominal thickness of 10 nm were used as p- and n-type contacts. The front electrode consisted of a 75-nm-thick sputtered indium tin oxide (ITO) layer followed by a silver grid with a nominal thickness of 500 nm sputtered through a shadow-mask; the back electrode consisted of a 150-nm-thick ITO layer followed by a 250-nm-thick, full-area sputtered silver layer. Whereas this metalization enables reasonably low series resistances for the 4-cm² and 1-cm² devices used here, the front-grid shadows approximately 15% of the area with 10% variability between samples. Active-area short-circuit current densities (J_{sc}) are therefore reported and were calculated by integrating the product of the external quantum efficiencies and the AM1.5G spectral irradiance. Lifetimes were measured with a Sinton lifetime tester on the samples with no ITO or silver, from which implied current-voltage (IV) parameters were extracted; a continuous-illumination Newport sun simulator was used to acquire actual IV curves. Note

that except when otherwise stated, IV measurements are reported after annealing at of the metallization at 200 °C for 20 minutes, occasionally causing V_{oc} values to exceed the corresponding implied V_{oc} values. Ellipsometry measurements of a -SiC_x:H layers were made with a Woolam M2000 system and a Cody-Lorentz model was used in the analysis, similarly to reference²⁸. A better fit of the data was obtained than with a Tauc-Lorentz model, especially for high R_{CH_4} , probably due to the large band tails in this material which are better reproduced with a Cody-Lorentz model.

III. PROPERTIES OF a -SiC_x:H LAYERS ON c -SI

A. Carbon content and optical properties

Secondary ion mass spectrometry (SIMS) analysis revealed that very little carbon is incorporated in the layer: The layer with a R_{CH_4} of 50% had an atomic ratio $C/(C + Si)$ of only 4%, and it dropped to 2% for the film with a R_{CH_4} of 25%. This poor carbon incorporation is usual for a -SiC_x:H films, and has been attributed mostly to the higher sticking coefficient of silicon radicals compared to carbon radicals¹⁷. Diluting the plasma with H₂ was shown to further reduce the carbon incorporation in the film by further lowering the sticking coefficient of the precursors, making the divergence between the gas stoichiometry and film stoichiometry larger. A stronger deviation in stoichiometry was also reported in earlier papers when increasing the deposition temperature, though no strong influence was seen in more recent work for temperatures between 130 °C and 300 °C^{22,29}. Since we did not perform SIMS analysis on all samples, R_{CH_4} (gas flow ratios) are reported instead of actual carbon content in the film throughout this paper.

Fig. 1a shows the refractive index n and the extinction coefficient k obtained from ellipsometry measurements of 50-nm-thick layers grown on polished wafers with different R_{CH_4} . Despite the aforementioned poor carbon incorporation, a significant decrease in n is seen for higher R_{CH_4} , linked with a slight decrease in k . The bandgap obtained from fitting the Cody-Lorentz model to the data increased accordingly from 1.7 eV to 2.3 eV similarly to previous reports^{18,19,29,30}.

B. Passivation

Fig. 2a shows the effective lifetime of textured wafers with both sides passivated with identical 50-nm-thick intrinsic a -SiC_x:H layers for successive 20-minute annealing steps in a furnace in ambient air. Increasing the R_{CH_4} degrades the initial (non-annealed) lifetime by up to two orders of magnitude. We attribute this to a lower-quality chemical passivation of the c -Si surface due to an increase in the mid-gap defect density in the carbon-richer a -SiC_x:H layers^{17,18}. Upon annealing, whereas the lifetime

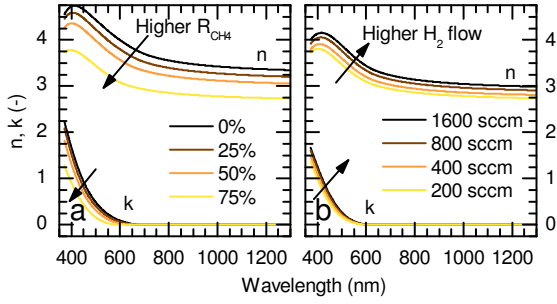


Figure 1. n and k values as a function of the wavelength for $a\text{-SiC}_x\text{:H}$ layers with a) different CH_4 to SiH_4 ratios (H_2 flow of 400 sccm) and b) different H_2 flows (R_{CH_4} of 75%).

of wafers passivated with pure $a\text{-Si:H}$ changes little below 300 °C and then decreases, an improvement is seen up to 300 °C followed by a drop when using carbon-containing layers. Changes in lifetime upon annealing are usually linked to hydrogen redistribution in the network¹⁶, so that initial improvements suggest that the initially present dangling bonds get passivated by hydrogen. The high-temperature degradation can on the other hand be attributed to hydrogen effusion¹⁶, with a lower relative degradation for higher carbon content because of stronger hydrogen bonding¹⁷. Modifying the atmosphere during annealing is expected to influence these results, and annealing under forming gas atmosphere was shown to enable a stable lifetime for carbon contents similar to the ones investigated here for higher temperatures²¹.

Fig. 2b presents lifetime evolution upon annealing of wafers having their back side passivated with a 50-nm-thick $a\text{-Si:H}$ layer and their front side passivated with a stack of two 10-nm-thick layers, each one being either $a\text{-Si:H}$ or $a\text{-SiC}_x\text{:H}$ prepared with a R_{CH_4} of 75%. $a\text{-Si:H}/a\text{-Si:H}$ stacks and $a\text{-SiC}_x\text{:H}/a\text{-SiC}_x\text{:H}$ stacks give results similar to those in Fig. 2a. The $a\text{-Si:H}$ -only and the $a\text{-Si:H}/a\text{-SiC}_x\text{:H}$ stack give similar passivation for annealing temperatures below 300 °C indicating that the passivation of a given stack is determined by the first 10 nm of material after the interface. Yet, starting at an annealing temperature of about 300 °C, passivation from the stack drops more severely, indicating that $a\text{-Si:H}$ degrades more when capped by an $a\text{-SiC}_x\text{:H}$ layer than when capped by an $a\text{-Si:H}$ layer. We speculate that such behavior can be understood from the strong decrease in the diffusion coefficient of hydrogen in $a\text{-SiC}_x\text{:H}$ compared to $a\text{-Si:H}$ (a drop by more than an order of magnitude was reported when increasing the carbon content in the $a\text{-SiC}_x\text{:H}$ layer from 0% to 10%, which corresponds to the range of carbon concentration used in this experiment^{18,31}): upon annealing, whereas an equal quantity of hydrogen is diffusing out of the first 10-nm-thick layer in both cases, it is partly compensated by hydrogen diffusing into it from the capping layer as sketched in Fig. 2c. If this layer is made of $a\text{-Si:H}$ with identical hydrogen-bonding properties, this capping layer will con-

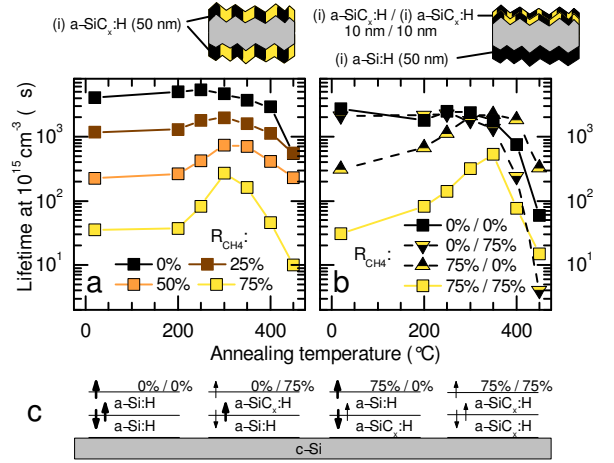


Figure 2. Lifetimes after successive 20-minute annealing steps at increasing temperatures for textured wafers with a) both sides coated with 50-nm-thick $a\text{-SiC}_x\text{:H}$ films prepared with various CH_4 ratios and b) the back side coated with a 50-nm-thick $a\text{-Si:H}$ film and the front side coated with two successive 10-nm-thick intrinsic $a\text{-SiC}_x\text{:H}$ layers with a R_{CH_4} of either 0% (pure $a\text{-Si:H}$) or 75% as sketched in c). c) Sketches of the hydrogen motion in such stacks (left to right: 0%/0%, 0%/75%, 75%/0%, 75%/75%) during the first stages of moderate-temperature annealing.

stitute a buffer preventing hydrogen loss from the interface, whereas when $a\text{-SiC}_x\text{:H}$ is used as a capping layer, much less hydrogen is coming in from the $a\text{-SiC}_x\text{:H}$ layer which has stronger hydrogen-bonding properties, reducing its protecting effect. Testing these hypothesis would require analyzing the hydrogen environment and hydrogen bonding in each case, which is delicate in view of the thin layers and layer stacks at stake. Careful measurements of dedicated samples with SIMS and Fourier-transform infrared spectroscopy (FTIR) would though be appropriate tools to probe these properties^{32,33}.

Similarly, a better lifetime is observed when the $a\text{-SiC}_x\text{:H}/a\text{-Si:H}$ stack is used compared to the pure $a\text{-SiC}_x\text{:H}$ stack, with a much improved temperature stability. The capping $a\text{-Si:H}$ layer acts in this case as a source of hydrogen at annealing temperatures below 300 °C, reducing desorption from the $a\text{-SiC}_x\text{:H}$ layer. A beneficial effect is thus seen upon annealing when using $a\text{-SiC}_x\text{:H}/a\text{-Si:H}$ stacks, similarly to recent reports³⁴. This phenomenon is already expected to happen during the hydrogen-rich plasma deposition of the $a\text{-Si:H}$ layer, explaining the higher initial lifetime of an $a\text{-SiC}_x\text{:H}/a\text{-Si:H}$ stack compared to an $a\text{-SiC}_x\text{:H}$ only stack. This particular case is to be kept in mind when considering intrinsic $a\text{-SiC}_x\text{:H}$ /doped $a\text{-Si:H}$ stacks in the following discussion.

Fig. 3a show the lifetimes of textured wafers with both sides coated with identical stacks of 10-nm-thick intrinsic $a\text{-SiC}_x\text{:H}$ and 10-nm-thick p-type $a\text{-Si:H}$ (i/p stack);

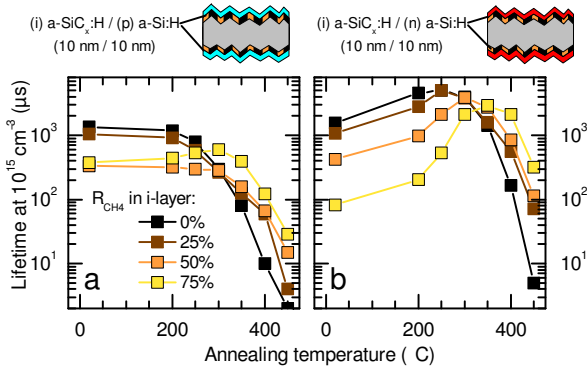


Figure 3. Lifetimes after successive 20-minute annealing steps at increasing temperatures for textured wafers with both sides coated with a stack of 10-nm-thick intrinsic $a\text{-SiC}_x\text{:H}$ prepared with different CH_4 ratios and a) a 10-nm-thick p-type $a\text{-Si:H}$ layer or b) a 10-nm-thick n-type $a\text{-Si:H}$ layer.

Fig. 3b shows the same results but when using identical stacks of 10-nm-thick intrinsic $a\text{-SiC}_x\text{:H}$ and 10-nm-thick n-type $a\text{-Si:H}$ (i/n stack). The R_{CH_4} during the deposition of the intrinsic $a\text{-SiC}_x\text{:H}$ layers was again varied between 0% and 75% (the doped layer being pure $a\text{-Si:H}$ in all cases). For the pure $a\text{-Si:H}$ i/p stack (Fig. 3a), the lifetime degrades monotonically with increasing annealing temperatures, dropping below $300 \mu\text{s}$ for 300°C . When carbon is incorporated in the intrinsic layer, a lower initial lifetime is observed but the drop upon annealing is smaller (an increase is even observed for a R_{CH_4} of 75%), making the lifetime higher for higher carbon content above 300°C . For the pure $a\text{-Si:H}$ i/n stack (Fig. 3b), the lifetime improves upon annealing up to 250°C , followed by a drop. For increased carbon content in the intrinsic layer, though the initial lifetime decreases, a stronger improvement is seen upon annealing, making the lifetimes increase with increasing R_{CH_4} above 300°C .

The lifetime behavior upon annealing for thick intrinsic, i/p and i/n $a\text{-Si:H}$ stacks is similar to that detailed by De Wolf and Kondo who observed an enhanced degradation for i/p stacks due to the position of the Fermi level close to the valence band in the intrinsic $a\text{-Si:H}$ layer¹⁶. For $a\text{-SiC}_x\text{:H}$ i/ $a\text{-Si:H}$ p stacks, the observed behavior is consistent with a superimposition of this Fermi-level effect with the influence of the carbon-content on the passivation of intrinsic $a\text{-SiC}_x\text{:H}$ / $a\text{-SiC}_x\text{:H}$ stacks detailed in the previous section.

For i/p stacks, carbon incorporation helps somewhat to maintain high lifetimes at high annealing temperatures—an order of magnitude higher lifetime is observed for a R_{CH_4} of 75% than for pure $a\text{-Si:H}$ after annealing at 400°C —but all lifetimes dive below 1 ms after annealing at temperatures higher than 200°C . As shown in Fig. 4, different injection-dependence is yet observed for different R_{CH_4} upon annealing, especially apparent after annealing at 300°C : the pure $a\text{-Si:H}$ case performs best

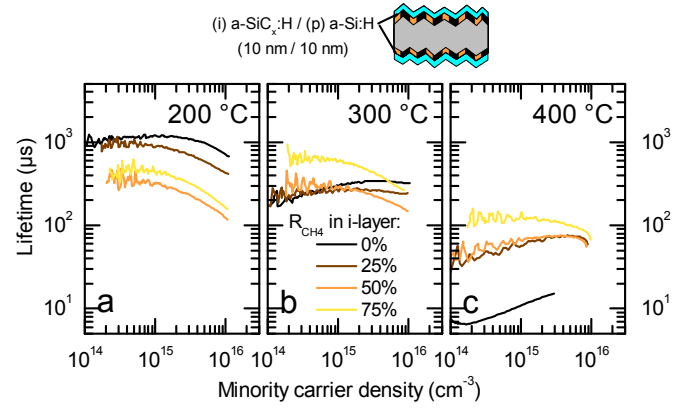


Figure 4. Lifetimes as a function of injection level for textured wafers with both sides coated with a stack of 10-nm-thick intrinsic $a\text{-SiC}_x\text{:H}$ prepared with different CH_4 ratios and a 10-nm-thick p-type $a\text{-Si:H}$ layer after successive 20-minute annealing steps at a) 200°C , b) 300°C , c) 400°C .

upon high injection, whereas it shows the poorest lifetime at low injection, possibly indicating that recombination and passivation mechanisms are different. Further analysis on a wider injection range would be required to fully analyze these behaviors³⁵. On the other hand, for i/n stacks, an initial improvement in lifetime followed by a drop is seen for all cases, with the peak value decreasing from 5 ms to 2 ms when increasing the R_{CH_4} from 0% to 75%. The position of this peak also shifts from 250°C to 350°C for increasing R_{CH_4} . This temperature shift is also present in Fig. 2 for i/i stacks, and we speculate that this is caused by diffusion of hydrogen from $a\text{-Si:H}$ to $a\text{-SiC}_x\text{:H}$. Compared to i/p stacks, the carbon incorporation helps to a larger extent to maintain high lifetimes at high annealing temperatures, with a value close to 2 ms after annealing at 400°C for the R_{CH_4} of 75% (compared to 0.2 ms for pure $a\text{-Si:H}$). No strong difference in the injection dependency (not shown) was observed for such stacks contrarily to the i/p stacks case.

IV. CELL RESULTS

A. Hole collection versus electron collection

With the increased bandgap of $a\text{-SiC}_x\text{:H}$, and thus the inevitable increase of the band offsets at the $c\text{-Si}/a\text{-SiC}_x\text{:H}$ interface, transport of charges from the wafer to the electrode might be impeded compared to $a\text{-Si:H}$. To probe the collection of holes through the $a\text{-SiC}_x\text{:H}$ layer, silicon heterojunction cells were made with a standard $a\text{-Si:H}$ i/n stack but an i/p stack consisting of an intrinsic $a\text{-SiC}_x\text{:H}$ layer with a R_{CH_4} of 0% to 75% followed by a p-type $a\text{-Si:H}$ layer. The reverse configuration was also made to probe electron transport, with a standard $a\text{-Si:H}$ i/p stack but $a\text{-SiC}_x\text{:H}$ in the intrinsic layer of the i/n stack. The V_{oc} and FF (implied values and actual

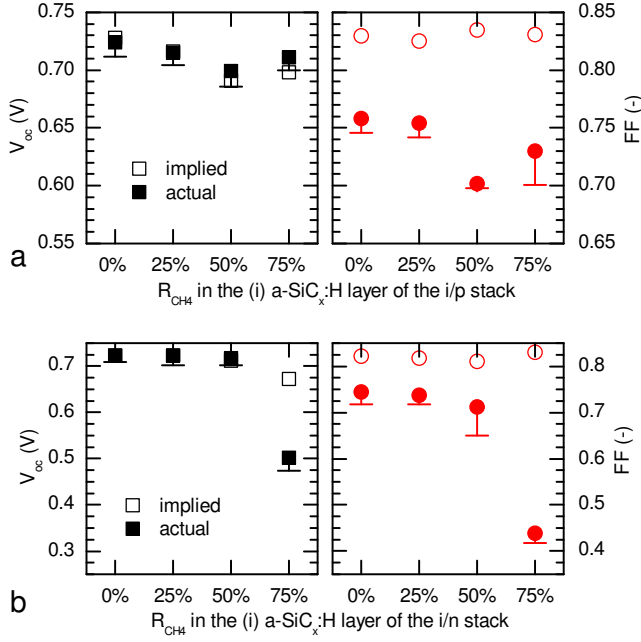


Figure 5. Implied and actual V_{oc} and FF as obtained from lifetime and IV measurements of silicon heterojunction cells with an intrinsic $a\text{-SiC}_x\text{:H}$ layer deposited between a) the p-type $a\text{-Si:H}$ layer and the n-type $c\text{-Si}$ wafer or b) the n-type $a\text{-Si:H}$ layer and the n-type $c\text{-Si}$ wafer. The 10-nm-thick $a\text{-SiC}_x\text{:H}$ layers were deposited with a R_{CH_4} of 0% to 75% and a H_2 flow of 400 sccm. Each symbol represents the best value out of three cells, and the bar indicates the average of the three cells.

values from illuminated IV measurements) after annealing at 200 °C for 20 min are shown in Fig. 5.

When using intrinsic $a\text{-SiC}_x\text{:H}$ in the i/p stack (Fig. 5a), the V_{oc} is remarkably insensitive to carbon content and remains above 700 mV. A FF above 70% is also obtained in all cases. A slight V_{oc} loss is seen for the highest R_{CH_4} , especially for a ratio of 50%, and is attributed to the poorer passivation also seen in Fig. 3. This reproducibly lowest lifetime and V_{oc} for a R_{CH_4} of 50% could be due to the competition between increased defect density and improved field-effect passivation when increasing the R_{CH_4} , the latter taking over for the R_{CH_4} of 75%¹⁹. A more detailed study of the injection-dependence of the lifetime curves would be required to analyze this effect^{36,37}.

Turning to Fig. 5b, the implied and actual V_{oc} also exceed 700 mV for low R_{CH_4} in the intrinsic layer of the i/n stack, but the actual V_{oc} degrades to 500 mV for a R_{CH_4} of 75%, the implied V_{oc} staying at 675 mV as anticipated from the lifetime in Fig. 3. A degradation of FF is also observed for increasing R_{CH_4} , associated with an S-shaped IV curve for R_{CH_4} of 50% and 75%. This indicates impeded transport of electrons through the $a\text{-SiC}_x\text{:H}$ intrinsic layer for high carbon contents, also causing the difference between the implied and actual V_{oc} values for the R_{CH_4} of 75%. Since the FF drop when

increasing the R_{CH_4} in the intrinsic layer was smaller for the i/p stack than for the i/n stack, the increased bandgap difference between $c\text{-Si}$ and the $a\text{-SiC}_x\text{:H}$ layer with increasing R_{CH_4} appears to consist mostly of a larger conduction-band offset. Different conduction-band offset values are found in literature for the $a\text{-SiC}_x\text{:H}/c\text{-Si}$ heterostructure depending on the study, with a strong dependence on the hydrogen content (as is also observed for $a\text{-Si:H}/c\text{-Si}$ heterostructures)^{30,38–43}. The large band tails and disorder of $a\text{-SiC}_x\text{:H}$, which are due to its amorphous nature, complicate the band offset definition and might also contribute to the asymmetry in performance of the cells requiring electron and hole extraction through the $a\text{-SiC}_x\text{:H}$ layer^{44,45}.

B. Influence of the hydrogen content

In an attempt to engineer the valence- and conduction-band offsets between $c\text{-Si}$ and $a\text{-SiC}_x\text{:H}$ to favor hole or electron collection through intrinsic $a\text{-SiC}_x\text{:H}$ layers, we varied the H_2 dilution during the growth of the intrinsic $a\text{-SiC}_x\text{:H}$ layers; the electron affinity of $a\text{-Si:H}$ films is known to increase with their hydrogen content accompanying the widening of the bandgap⁴⁶. Instead of a similar bandgap increase, a slight decrease was actually observed for $a\text{-SiC}_x\text{:H}$ layers, as indicated by a slight increase in both n and k for 50-nm-thick intrinsic layers deposited with a R_{CH_4} of 75% (Fig. 1b). This bandgap narrowing is attributed to lower carbon incorporation when using a higher H_2 dilution, as previously reported²⁹. Compared to the influence of the R_{CH_4} , all layers deposited with a R_{CH_4} of 75% and various H_2 dilutions exhibit optical properties that are between the ones of layers having a ratio of 75% and 50% CH_4 in Fig. 1a. The improved electrical performance when using larger H_2 flows observed in Fig. 6 can thus mostly be attributed to a slight bandgap narrowing rather than to a change in electron affinity only (without bandgap modification), since collection of both electrons and holes (though to a lesser extent) is improved. Thus, varying the H_2 dilution seems to allow little leverage in tuning the electron affinity compared to the influence of the R_{CH_4} on the overall bandgap.

C. Thickness and carbon content parallel optimization

Fig. 7 shows the electrical parameters of $c\text{-Si}$ heterojunction devices using $a\text{-Si:H}$ for the p-type layer and the i/n stack but an intrinsic $a\text{-SiC}_x\text{:H}$ passivating layer in the i/p stack with a R_{CH_4} of 0%, 25% or 75%, and a thickness of 4 nm, 7 nm or 10 nm. The J_{sc} values were extracted from EQE measurements between the front metal grid fingers and do not include the 15% shadow loss from the metal grid; the efficiencies reported in Fig. 7d were calculated based on this current density as active-area efficiencies.

Fig. 7a shows that passivation improves with $a\text{-SiC}_x\text{:H}$

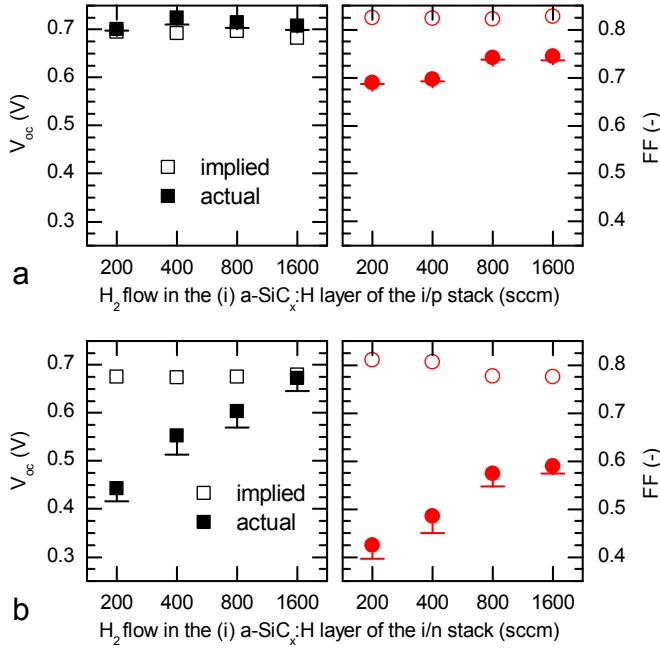


Figure 6. Implied and actual V_{oc} and FF as obtained from lifetime and IV measurements of silicon heterojunction cells with an intrinsic $a\text{-SiC}_x\text{:H}$ layer deposited between a) the p-type $a\text{-Si:H}$ layer and the n-type $c\text{-Si}$ wafer or b) the n-type $a\text{-Si:H}$ layer and the n-type $c\text{-Si}$ wafer. The 10-nm-thick $a\text{-SiC}_x\text{:H}$ layers were deposited with a H_2 flow of 200 sccm to 1600 sccm, and a R_{CH_4} of 75% to 75%. Each symbol represents the best value out of three cells, and the bar indicates the average of the three cells.

thickness for layers prepared with a R_{CH_4} of 0% or 25% but is similar for all three thicknesses for the layer prepared with a R_{CH_4} of 75%. From Fig. 7b, we can see that the FF is best for thinner layers when increasing the R_{CH_4} . For the layers deposited with a R_{CH_4} of 75%, this is due to the apparition of a barrier to charge transport arising for too thick layers, possibly due to a too small conductivity of the layer, as seen for the 10-nm-thick layers in Fig. 5 and Fig. 6. This is confirmed by the high pseudo- FF value, measured with a Sinton instrument⁴⁷, as commonly observed⁴⁸. We see here though that this barrier to hole extraction disappears for thin enough layers, with a FF of 76% for the 4-nm-thick layer. For pure $a\text{-Si:H}$, the 4-nm-thick layer appears to be too thin to ensure a high FF , at least partly due to an increase in surface recombination as indicated by the V_{oc} loss (Fig. 7a). Devices with a R_{CH_4} of 25% layer maintain high FF values above 76% for all thicknesses, with a highest value of 78% for the 4-nm-thick layer. The slight drop for increasing thicknesses is linked to a higher value of open-circuit resistance, likely due to indicate impeded charge extraction, similarly but less severely than observed for the highest R_{CH_4} due to the smaller bandgap.

The J_{sc} values shown in Fig. 7c follow the expected trend: higher current densities are obtained for thinner intrinsic layers, this gain getting lower for the most trans-

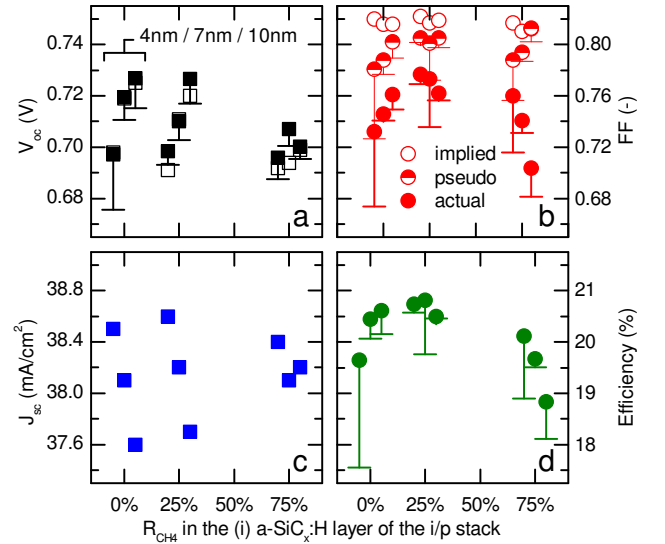


Figure 7. a) V_{oc} , b) FF , c) J_{sc} and d) active area efficiency of silicon heterojunction cells with an intrinsic $a\text{-SiC}_x\text{:H}$ layer in the i/p stack. The R_{CH_4} in this layer was varied from 0% to 75%, a H_2 flow of 400 sccm was used and for each ratio, cells with 4-, 7- and 10-nm-thick layers are shown from left to right. Implied and actual values are reported for V_{oc} and FF , and the pseudo- FF is also included. Each symbol represents the best value out of three cells, and the bar indicates the average of the three cells.

parent layers with the R_{CH_4} of 75%. For cells using a passivation layer with a R_{CH_4} of 75%, the reflection on most of the spectrum was slightly altered (by this layer due to its lower refractive index (Fig. 1), which balances the gain in the blue part of the spectrum due to improved transparency. Larger J_{sc} gains are to be expected when using a more transparent p-type (or other hole-collecting) layer, which was not investigated in this study, since most blue light is absorbed in this layer. The efficiencies in Fig. 7d mostly follow FF , and interestingly show an overall maximum for the 7-nm-thick $a\text{-SiC}_x\text{:H}$ layer with a R_{CH_4} of 25%. The optimum thickness decreases when increasing the R_{CH_4} , which can be explained by a combination of more efficient passivation for thin layers and more severe series resistance (eventually S-shape) for thick layers as the $a\text{-SiC}_x\text{:H}$ bandgap widens. Whereas these results are for room temperature, a better temperature coefficient is expected for the higher R_{CH_4} due to improved thermionic emission which might make such layers more interesting for field applications^{5,6,49}.

D. Improved temperature stability for i/p stacks

Fig. 8 shows the implied and actual V_{oc} of the complete solar cells presented in Fig. 7 after successive 20-minute annealing in ambient air at increasingly higher temperatures. As anticipated from Fig. 3, V_{oc} stability is

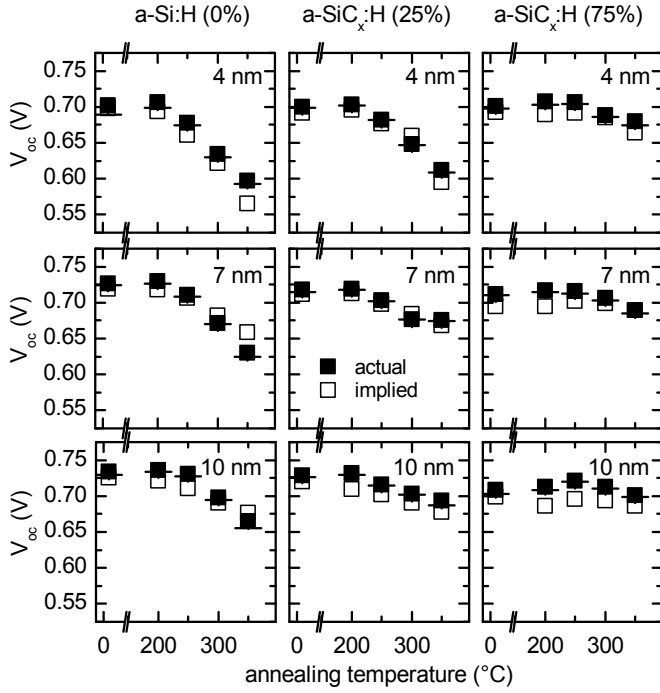


Figure 8. Implied and actual V_{oc} as a function of annealing temperature for heterojunction cells with an intrinsic $a\text{-SiC}_x\text{:H}$ layer in the i/p stack. The $a\text{-SiC}_x\text{:H}$ layers were deposited with a R_{CH_4} of 0% to 75% (variation across columns), a thickness of 4 nm to 10 nm (variation across rows), and a H_2 flow of 400 sccm. For the actual V_{oc} , each symbol represents the best value out of three cells, and the bar indicates the average of the three cells.

improved when increasing the R_{CH_4} in the intrinsic layer of the i/p stack. This is especially true for thin intrinsic layers for which the observed degradation is much more severe when no carbon is incorporated. A V_{oc} of 700 mV (680 mV) is maintained up to an annealing temperature of 350 °C when using a 10-nm-thick (4-nm-thick) intrinsic $a\text{-SiC}_x\text{:H}$ layer with a R_{CH_4} of 75%, whereas devices with a 10-nm-thick (4-nm-thick) $a\text{-Si:H}$ intrinsic layer degraded to 640 mV (600 mV). Though implied and pseudo FF values did not change much upon annealing, the actual FF degraded strongly, independently of the R_{CH_4} , which we attribute to degradation of the thin metalization also visually observable.

Note that the same temperature study applied to cells with the intrinsic $a\text{-SiC}_x\text{:H}$ layer on the i/n side (not shown here) confirms the trend observed in the lifetime study in Fig. 3: the initial implied V_{oc} decreases with increasing R_{CH_4} , but all implied V_{oc} values converge at annealing temperatures between 250 °C and 300 °C. For higher temperatures, passivation from the i/p stack begins to degrade rapidly and limits the overall V_{oc} .

V. CONCLUSION

In summary, we showed that low-carbon-content intrinsic $a\text{-SiC}_x\text{:H}$ layers can be used in high-efficiency $c\text{-Si}$ -based heterojunction cells. Lifetime obtained with using as-deposited $a\text{-SiC}_x\text{:H}$ layers was shown to get lower with increasing R_{CH_4} , but increases upon annealing at 200 °C to 400 °C were observed. When the passivating $a\text{-SiC}_x\text{:H}$ layer was capped with an $a\text{-Si:H}$ layer, a further increase in lifetime was observed upon annealing, which we attributed to hydrogen moving from the $a\text{-Si:H}$ layer to the $a\text{-SiC}_x\text{:H}$ layer. Passivation using device-relevant stacks of intrinsic $a\text{-SiC}_x\text{:H}$ and doped $a\text{-Si:H}$ are more resilient to annealing at temperatures above 250 °C compared to equivalent stacks using $a\text{-Si:H}$ only. For complete cells, poor carrier transport resulting in S-shaped IV curves was observed when increasing the carbon content in the intrinsic layer of the i/n stack. However, good FF values were maintained when using intrinsic $a\text{-SiC}_x\text{:H}$ layers in the i/p stack even for layers prepared with a R_{CH_4} of 75%, provided a thin-enough layer was used. Because of good passivation and improved transparency of the front stack, cells employing a passivating layer prepared with a R_{CH_4} of 25% reached slightly higher efficiencies than those with pure $a\text{-Si:H}$. Also, better stability of V_{oc} after annealing at elevated temperatures was shown for such carbon-containing passivating layers.

As $a\text{-SiC}_x\text{:H}$ passivating layers can withstand higher temperatures than $a\text{-Si:H}$ layers—up to 350 °C—they might allow a wider range of post-deposition cell fabrication processes. Whereas strong lifetime degradation was still observed for 20-minute annealing in air at temperatures above 400 °C, shorter exposures or different atmospheres were not investigated and $a\text{-SiC}_x\text{:H}$ layers may be beneficial in such cases. Further studies are required to fully understand the passivation mechanism for $c\text{-Si} / a\text{-SiC}_x\text{:H}$ structures and in particular the role of hydrogen, as well as carrier transport across the hetero-interface. To fully benefit from the improved transparency of intrinsic $a\text{-SiC}_x\text{:H}$ layers, more transparent hole-extracting layers would be required. Finally, $a\text{-SiC}_x\text{:H}$ passivating layers may be further improved by using multilayers, by optimizing the deposition conditions, and by investigating alternative post-deposition treatments such as annealing under controlled atmosphere or exposure to a hydrogen plasma.

VI. ACKNOWLEDGMENTS

The information, data, or work presented herein was funded in part by the U.S. Department of Energy, Energy Efficiency and Renewable Energy Program, under Award Number DE-EE0006335. We acknowledge Stanislaw Herasimenka for initial developments of the $a\text{-Si:H}$ layers used here, and Jianwei Shi and Kate Fisher for their support in wafer preparation.

REFERENCES

- ¹S. De Wolf, A. Descoeurdes, Z. C. Holman, and C. Ballif, *Green* **2**, 7 (2012).
- ²M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama, *IEEE Journal of Photovoltaics* **4**, 96 (2014).
- ³Z. C. Holman, A. Descoeurdes, L. Barraud, F. Z. Fernandez, J. P. Seif, S. De Wolf, and C. Ballif, *IEEE Journal of Photovoltaics* **2**, 7 (2012).
- ⁴K. Ding, U. Aeberhard, F. Finger, and U. Rau, *physica status solidi (RRL)-Rapid Research Letters* **6**, 193 (2012).
- ⁵J. P. Seif, A. Descoeurdes, M. Filipič, F. Smole, M. Topič, Z. C. Holman, S. De Wolf, and C. Ballif, *Journal of Applied Physics* **115**, 024502 (2014).
- ⁶C. Battaglia, S. M. De Nicolas, S. De Wolf, X. Yin, M. Zheng, C. Ballif, and A. Javey, *Applied Physics Letters* **104**, 113902 (2014).
- ⁷J. Sritharathikhun, F. Jiang, S. Miyajima, A. Yamada, and M. Konagai, *Japanese Journal of Applied Physics* **48**, 101603 (2009).
- ⁸M. Lu, S. Bowden, U. Das, and R. Birkmire, *Applied Physics Letters* **91**, 063507 (2007).
- ⁹M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, *Progress in Photovoltaics: Research and Applications* **23**, 1 (2015).
- ¹⁰N. Mizumura and K. Sasaki, in *Electronics Packaging (ICEP), 2014 International Conference on* (IEEE, 2014) pp. 526–531.
- ¹¹A. G. Aberle, B. Kuhlmann, R. Meyer, A. Hübner, C. Hampe, and R. Hezel, *Progress in Photovoltaics: Research and Applications* **4**, 193 (1996).
- ¹²J. M. Ball, M. M. Lee, A. Hey, and H. J. Snaith, *Energy & Environmental Science* **6**, 1739 (2013).
- ¹³P. Qin, S. Tanaka, S. Ito, N. Tetreault, K. Manabe, H. Nishino, M. K. Nazeeruddin, and M. Grätzel, *Nature communications* **5**, 3834 (2014).
- ¹⁴N. C. Strandwitz, D. B. Turner-Evans, A. C. Tamboli, C. T. Chen, H. A. Atwater, and N. S. Lewis, *Advanced Energy Materials* **2**, 1109 (2012).
- ¹⁵K. N. Yaung, J. R. Lang, and M. L. Lee, in *Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th* (IEEE, 2014) pp. 0831–0835.
- ¹⁶S. De Wolf and M. Kondo, *Journal of Applied Physics* **105**, 103707 (2009).
- ¹⁷W. Beyer and H. Mell, in *Disordered Semiconductors*, Institute for Amorphous Studies Series, edited by M. A. Kastner, G. A. Thomas, and S. R. Ovshinsky (Springer US, 1987) pp. 641–658.
- ¹⁸A. Shah, *Thin-film silicon solar cells* (EPFL Press, 2010).
- ¹⁹I. Martín, M. Vetter, M. Garín, A. Orpella, C. Voz, J. Puigdollers, and R. Alcubilla, *Journal of applied physics* **98**, 114912 (2005).
- ²⁰M. Vetter, I. Martín, A. Orpella, J. Puigdollers, C. Voz, and R. Alcubilla, *Thin Solid Films* **451**, 340 (2004).
- ²¹C. Ehling, J. H. Werner, and M. B. Schubert, *physica status solidi (c)* **7**, 1016 (2010).
- ²²A. Gaufrès, F. Husser, E. Fourmond, and M. Lemiti, *Energy Procedia* **38**, 823 (2013).
- ²³D. Pysch, M. Bivour, M. Hermle, and S. W. Glunz, *Thin Solid Films* **519**, 2550 (2011).
- ²⁴A. Descoeurdes, Z. C. Holman, L. Barraud, S. Morel, S. De Wolf, and C. Ballif, *IEEE Journal of Photovoltaics* **3**, 83 (2013).
- ²⁵S. Y. Herasimenka, W. J. Dauksher, and S. G. Bowden, *Applied Physics Letters* **103**, 053511 (2013).
- ²⁶R. Ferre, I. Martín, P. Ortega, M. Vetter, I. Torres, and R. Alcubilla, *Journal of Applied Physics* **100**, 073703 (2006).
- ²⁷S. Janz, S. Riepe, M. Hofmann, S. Reber, and S. Glunz, *Applied Physics Letters* **88**, 133516 (2006).
- ²⁸D. Zhang, D. Deligiannis, G. Papakonstantinou, R. van Swaaij, M. Zeman, *et al.*, *Photovoltaics, IEEE Journal of* **4**, 1326 (2014).
- ²⁹G. D. Cesare, F. Galluzzi, G. Guattari, G. Leo, R. Vincenzoni, and E. Bemporad, *Diamond and Related Materials* **2**, 773 (1993).
- ³⁰J. M. Essick, Z. Nobel, Y.-M. Li, and M. S. Bennett, *Phys. Rev. B* **54**, 4885 (1996).
- ³¹W. Beyer, *Journal of Non-Crystalline Solids* **266**, 845 (2000).
- ³²A. Smets, W. Kessels, and M. Van de Sanden, *Applied physics letters* **82**, 1547 (2003).
- ³³T. Schulze, L. Korte, and B. Rech, *Thin Solid Films* **520**, 4439 (2012).
- ³⁴I. P. Sobkowicz, *Study and optimization of the growth of a-Si:H on wet-chemically textured c-Si substrates for the enhancement of a-Si:H/c-Si heterojunction solar cells*, Theses, Ecole Doctorale Polytechnique (2014).
- ³⁵D. Suwito, T. Roth, D. Pysch, L. Korte, A. Richter, S. Janz, and S. Glunz, in *Proceedings of the 23rd European Photovoltaic Solar Energy Conference* (2008) pp. 1023–1028.
- ³⁶S. Olibet, E. Vallat-Sauvain, and C. Ballif, *Physical Review B* **76**, 035326 (2007).
- ³⁷C. Leendertz, R. Stangl, T. Schulze, M. Schmidt, and L. Korte, *physica status solidi (c)* **7**, 1005 (2010).
- ³⁸L. Martín-Moreno and J. Vergés, *Philosophical Magazine B* **61**, 237 (1990).
- ³⁹F. Evangelisti, *Journal of Non-Crystalline Solids* **7778, Part 2**, 969 (1985).
- ⁴⁰T. M. Brown, C. Bittencourt, M. Sebastiani, and F. Evangelisti, *Physical Review B* **55**, 9904 (1997).
- ⁴¹S. Knief and W. von Niessen, *Journal of Non-Crystalline Solids* **255**, 242 (1999).
- ⁴²J. Robertson, *Philosophical Magazine B* **66**, 615 (1992).
- ⁴³T. Enomoto, R. Hattori, and J. Shirafuji, *Solar Energy Materials* **23**, 340 (1991).
- ⁴⁴A. Kanevce and W. K. Metzger, *Journal of Applied Physics* **105**, 094507 (2009).
- ⁴⁵T. Schulze, L. Korte, F. Ruske, and B. Rech, *Physical Review B* **83**, 165314 (2011).
- ⁴⁶C. G. Van de Walle and L. Yang, *Journal of Vacuum Science & Technology B* **13**, 1635 (1995).
- ⁴⁷R. Sinton and A. Cuevas, in *16th European Photovoltaic Solar Energy Conference*, Vol. 25 (2000) pp. 1152–1155.
- ⁴⁸M. Bivour, M. Reusch, S. Schroer, F. Feldmann, J. Temmler, H. Steinkemper, and M. Hermle, *IEEE Journal of Photovoltaics* **4**, 566 (2014).
- ⁴⁹M. W. van Cleef, F. A. Rubinelli, R. Rizzoli, R. Pinghini, R. E. Schropp, and W. F. van der Weg, *Japanese journal of applied physics* **37**, 3926 (1998).