Research Performance FINAL Report for DOE/EERE

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Project Objective:

In this research program we will demonstrate the feasibility of thin, kerfless c-Si devices by merging thin-film cost structures with proven Si reliability and performance that provides a robust pathway to \$0.50/W_p modules. We will address the broad industry need for a high-efficiency c-Si cell that overcomes the dominant module cost barriers by 1) developing thin Si wafers synthesized by innovative, kerfless techniques; 2) integrating laser-based processing into most aspects of solar cell fabrication, ensuring low thermal budgets and high yields for thin Si; 3) developing an all back contact cell structure compatible with thin wafers using a simplified, low-temperature fabrication process; and 4) designing the contact structure to enable simplified module assembly.

Background:

Crystalline silicon-based photovoltaic (PV) technologies comprise about 90% of all solar cells currently manufactured. The success of c-Si PV is in part attributed to the robust research and development history of silicon, with over 60 years of invested experience and learning. Standardized methods of feedstock purification, crystallization, junction formation, and bulk and surface passivation were effectively transferred from the laboratory to production. Si modules have well-established field reliability, with no shortage of raw materials even at terawatt scale. Emerging device architectures on thin c-Si with kerfless wafering, leading to lower material costs, and cost-effective high throughput processing, leading to lower production costs, provide a credible technical path toward low cost high-efficiency, thin Si PV devices. In particular, an integrated back contact (IBC) solar cell with deposited a-Si heterojunction (HJ) emitter and contacts has been sited as the ultimate single junction Si wafer based solar cell design by several PV industry roadmaps and industry experts. This was confirmed in 2014 by both Panasonic and Sharp Solar producing IBC-HJ cells breaking the previous long standing record Si solar cell efficiency of 25%. Additionally, the highest efficiency module on the market for years incorporates IBC cells from SunPower although they use traditional diffused junctions not heterojunctions.

In this research program, we will address the broad industry need for a high-efficiency c-Si cell that overcomes the dominant module cost barriers by 1) developing thin Si wafers synthesized by innovative, kerfless techniques; 2) integrating laser-based processing into most aspects of solar cell fabrication, ensuring low thermal budgets and high yields for thin Si; 3) developing an all back contact cell structure compatible with thin wafers using a simplified, low-temperature fabrication process; and 4) designing the contact structure to enable simplified module assembly. The broader impacts of this work include; advances in thin crystal growth technology; development of defect characterization and passivation techniques with sub-100 nm spatial resolution; high-throughput, precision laser manufacturing on uneven surfaces; novel approaches to the manufacture of Si devices using lasers; exceeding the SunShot goal of \$0.50/W_p domestic PV manufacturing; educating the next generation of PV leaders.

Brief Summary of Highlights:

It was demonstrated that the patterning process to define the emitter and base strips and their metal contacts has a significant influence on the performance and the stability of the devices. IBC solar cells on 150 µm Si wafers were fabricated having 20% efficiency using photolithography and 16% without photolithography by using masking during the PECVD deposition. We developed laser fired contacts to n-type Si using an Al/Sb-Ti stack where the

Sb provides crucial doping allowing for contact resistances < 5mOhm-cm^2 and IBC device efficiency with LFC of 17%. However, we determined that metal-silicon interface will be strongly recombination active, even when sub-surface laser damage is minimized.

Regarding the front surface of the IBC cell, we developed a three layer front surface AR stack (a-SiC/a-SiN/a-Si on TMAH textured Si) and optimized its properties for very low front surface optical losses (reflection and absorption) while maintaining excellent surface passivation (SRV<5 cm/s). New methods to self-consistently characterize the interface state defects and capture cross-sections of holes and electrons were developed and these values were used in 2D modeling of the IBC cell structure. We investigated several different front surface doping structures to compare effect of charge vs field induced control of carrier recombination and found that the commonly used diffused front surface field was no better than the deposited a-Si passivation.

The Sentaurus 2D Device Simulator was used to provide guidance and insight into the role of various regions and designs. Recombination losses and the role of contact spacing and geometry were evaluated. The modeling was validated by close agreement of light and dark JV and QE measurements of front and rear (IBC) heterojunction cells.

Suns-Voc measurements on IBC cells prior to patterning and metallization indicated an implied efficiency of 23.7% and implied Voc of 0.745V while the final device had a measured efficiency of 19.6% and Voc of 0.682 V. The loss in Voc is significant and demonstrates that our cells have the capability to provide efficiency of 23% if we could develop patterning with less damage ot the rear surface passivation.

Significant efforts at optimization of the p-emitter doped layer deposition conditions lead to trade-offs between Voc and FF. This was solved with 2-stage high doped/low doped emitter which lead to our achieving efficiency > 20%.

Collaboration with kerfless wafer manufacturers lead to significant improvements in bulk minority-carrier lifetime of thin kerfless wafers by reducing initial impurities during growth and developing post-growth gettering techniques. Lifetimes over 1 msec were finally obtained and cells with 16% efficiency were made on 50 µm wafers.

Lessons Learned

We found that having photoresist on the device surface during PECVD resulted in inevitable contamination and degradation of performance. Significant modification of the patterning sequence lead to a more complicated procedure but improved efficiency and stability.

Damage due to laser fired contacts seem to be relatively insenstitive to the lasing conditions due to the fact that any metal-Si contact is high recombination. Thus, reducing the size of the contact with a smaller laser spot is the best approach to minimizing recombination losses.

Perhaps the biggest lesson was that the simple device structure envisioned in the original proposal has a weakness. The base contact consisted of a metal/p-i (a-Si)/ n-c-Si structure where the ohmic contact is formed by laser firing the metal through the a-Si p-I blocking junction. This lead to a very low Voc and Jsc which was determined to be due to forming a parasitic emitter junction which shunted holes from the n-Si wafer. Instead a blocking insulator such as SiN is needed between the metal and p a-Si.

Significant Accomplishments (Team members with primary responsibility are listed. Tasks 1-5 were investigated during Q1-Q6 while Tasks 6-10 were investigated during Q7-Q12):

Task 1. ***Evaluate and control defects in kerfless, thin Si wafers (MIT)***

- Worked with kerfless wafer manufacturers to apply defect-engineering techniques to improve bulk minority-carrier lifetime of thin kerfless wafers by both reducing initial impurities during growth and developing post-growth gettering techniques
- Determined kerfless material characteristics for high device performance[1] and techo-economic competitiveness[2]; work featured in The Economist.[3]
- Developed and applied novel microanalytical tools to characterize and quantify defect concentrations in kerfless materials.[4] Work recognized by an *IEEE PVSC* best poster award (2014) and led to a successful NREL NPO.
- Quantified concentration and local lifetime impacts of principal point defects and extended structural defects in as-grown epi kerfless materials.[5] Work led to successful completion of Subtasks 1.2 and 1.3.
- Work led to novel foundational insights about the kinetics of nickel[6], chromium[7], and dislocations[8] in PV-grade silicon.
- Achieved millisecond lifetimes in kerfless silicon materials.[9]
- Determined material requirements for high getterability.[10]
- The defect-engineering technologies were successfully translated to improve lifetimes in other non-traditional wafer materials.[11]
- Constructed near-IR pump-probe system to decouple τ_b and τ_s.

Task 2. ***Develop a-Si/c-Si heterojunctions (IEC)***

- Developed O_2 plasma Si surface cleaning with same performance as wet etching.
- Established relation between a-Si i-layer process conditions, material properties (i-layer bandgap, thickness, H2 content, Si-H bonding) and passivation quality (SRV or effective lifetime)[12].
- First application of a-SiGe i-layers to reduce intrinsic buffer bandgap.
- Developed and verified 2D model for IBC-SHJ device using above parameters[13].
- Developed processing for baseline front SHJ devices on 150 µm standard wafers with 17-18% efficiency.
- Fabricated front SHJ devices on ~50 µm thin wafers with 16-17% efficiency utilizing light trapping (front texture and ITO/Ag back reflector) to achieve Jsc=35 mA/cm2.

Task 3. ***Characterize and optimize front surface for IBC cell (IEC)***

- Developed 3 layer front surface AR stack: 2-5 nm wide bandgap a-Si for passivation, 40-50 nm a-SiN for index matching and fixed charge for additional passivation with thinner a-Si is used, and 40 nm a-SiC to provide chemical etch

barrier [14]

- Developed and applied new method to characterize interface recombination parameters including D_{it} and hole and electron capture cross-section using MIS admittance and QSSPC self-consistently[15]
- Used these parameters as input for 1D and 2D models[16]
- Optimize the texture and 3 layer AR stack properties for low reflection
- Obtained very low (< 6 mA/cm2) front surface optical losses (reflection and absorption) by optimizing surface texture and a-Si/a-SiN/a-SiC passivation/AR stack while maintaining excellent surface passivation (SRV<5 cm/s)[14]

Task 4. ***Laser processing for interdigitated back contacts (IEC/IPG)***

- Developed unique 3-layer metal stack (Al/Sb/Ti) for low resistance laser fired contact (LFC) to n-type Si where the 500 nm Al is the current conductor, 50 nm Sb is the n-type Si wafer dopant, and 5 nm Ti improves adhesion.[17]
- Fabricated front junction solar cells with laser fired rear contacts using unique low cost Al-Sb-Ti metal stack having same FF as standard heterojunction contact.
- Obtained contact resistance <3 Ohm/cm when Al/Sb/Ti stack is laser fired through a variety of insulators with wide window of laser parameters[17]
- Developed new 2 step laser+chemical etch isolation technique using sacrificial top coating which avoids laser damage to Si passivation
- Obtained high shunt resistance meeting goal without causing loss of passivation.

Task 5 ***Fabricate IBC-SHJ using laser fired contact with efficiency better than today's baseline (IEC)***

- Developed mutually compatible photoresist application, exposure and etching, SiN etching, and Si surface texturing processing steps with negligible residue and good uniformity, passivation and yield.[18]
- Developed simpler 1-step photolithography process which gave better FF but lower Voc than standard 2-step process[19]
- Fabricated IBC cells with 2 different wafer surface morphology and different metal contacts
- Developed and validated model for front SHJ (1D) and IBC-SHJ (2D) solar cells using same experimentally determined parameters[13], [16]
- Simulated impact of contact pitch and dimensions, wafer bulk lifetime and wafer thickness on IBC cell performance to guide thin Si wafer partners for phase 2
- Achieved steady progress in efficiency for IBC-SHJ cells by integrating new features (see figure SA.1)
- Best efficiency IBC-SHJ for Q1-Q6 with LFC was 15.0% for a device with 2.5 cm^2 area which met the Q6 go/no-go goal.

Task 6. Optimize a-Si/c-Si heterojunctions (IEC)

- Design and fabrication of solar cell test structures allowed separation of 1D vs 2D losses and explored various p and n layer deposition conditions.
- Performance of FHJ (1D) cells with range of a-Si intrinsic buffer deposition conditions found that current baseline buffer layer was optimum.

- Performance of FHJ (1D) and IBC (2D) cells with range of p-layer conditions found that 2-stage high/low doped p-layer was optimum: the low doped region has lower defects giving higher Voc and the high doped region gave a better contact to the metal [20]
- Temperature dependence of front heterojunction (FHJ) and interdigitated back contact (IBC)-HJ cells indicates that low temperature performance of cells with poor passivation is better than for well passivated high efficiency cell which form S-curves at low temperature, suggesting that valence band alignment is increasingly important as passivation improves[21]
- Loss analysis using intensity and spectral dependent JV measurements indicates our IBC cells are capable FF ~ 80% by reducing series resistance but that they still had additional ~2% loss compared to a FHJ device.

Task 7. Laser processing and patterning and defect annealing/passivation (IEC/MIT/IPG)

- Fabricated first cells using blanket p/i emitter/passivation layers, single metallization, laser patterning and laser fired contacts (LFC). They had low Voc and FF.
- Identified parasitic recombination loss in this originally proposed simplified device structure. Conclude that some patterning of the dielectric/passivation stack on back is needed to isolate p/i layers from metal with LFC.
- Established LFC through dielectric passivation stack blocking layers p a-Si/ i a-Si/ SiNx/ n a-Si/ i a-Si. [17]
- Developed 2 laser operating parameters critical for effective direct isolation: using a defocussed beam, and controlling the speed at corners and stop/start to avoid over firing the beginning and ending of a line of laser shots.
- Utilized feedback from Task 8, primarily photoluminescence imaging, to guide laser processing parameters.

Task 8. Defect engineering in thin kerfless Si wafers (MIT/IPG/IEC)

- From Gen I to Gen II materials, we improved the lifetime from ~30 µs to ~1000 µs, resulting in an increase in the device efficiency potential from ~14% to >20%. This far exceeded our stated J_{SC} and V_{OC} goals.
- Initiated development of a free-carrier-absorption-based temperature- and injection-dependent lifetime spectroscopy apparatus.
- Spatial mapping of lifetime and recombination using photoluminescence imaging has been applied to IBC-SHJ devices at various stages of processing, indicating that defects are introduced during and after the patterning stage.
- Determined that metal-silicon interface will be recombination active, even when sub-surface laser damage is minimized.
- Determined optimal laser process conditions to minimize surface recombination due to laser-fired contact.

Task 9. Optimize front surface texturing and passivation (IEC/IPG)

- As-lased texture gave slightly lower reflection than TMAH but required defect etching and possible thermal annealing of defects. Narrow process window for

etching presented significant challenge to simultaneously obtain high lifetime with low reflection.
- Decided to abandon laser texture and use our well-established TMAH texture which gives comparable reflection and passivation as commercial texture with much fewer processing steps.

Task 10. Integrate features into IBC-SHJ device platform (IEC)

- Develop new device architecture with diffused n+ front surface field (FSF)
- Investigated 4 alternative front passivation stacks: 1. diffused n+/a-Si i, 2. deposited a-Si i, 3. deposited a-Si i/n, and 4. deposited a-Si n. It was found that either configuration with the a-Si n-layers leads to a significant loss in blue QE and Voc compared to the diffused n+ consistent with the reduced effective lifetime.
- Integrate following new features into previous IBC process flow: TMAH front surface texturing, FSF, rear patterning without putting photoresist in the PECVD system, masked deposition, and thicker, more stable gap structure (i/p/SiN/i/n)[22]
- Determined that diffused FSF is irrelevant to performance
- Determined that masked deposition is currently limited by wide 100 µm gap needed for visual alignment compared to the 25 µm gap obtained with photolithography
- Obtained notable improvement in FF (74% vs <70%) and Jsc (38 vs 36 mA/cm2).
- Established reproducibility by having 4 runs with baseline cell efficiencies of 19-20% using 3 step photolithography for patterning.
- Highest in-house efficiency for IBC-HJ cell was 20.2% which had our unique 2-stage high/low doped p-layer.[23]
- A cell having 19.2% at IEC was measured at 19.7% at NREL (different areas).
- Recognizing that thin kerfless wafers would not survive baseline processing with 3 photolithography steps, intense effort made to develop to non-photolithography processing such as laser isolation (Task 7), a-Si layer deposition through masks, and metal deposition through masks. IBC cells with ~16% efficiency were made using masked deposition without photolithography.

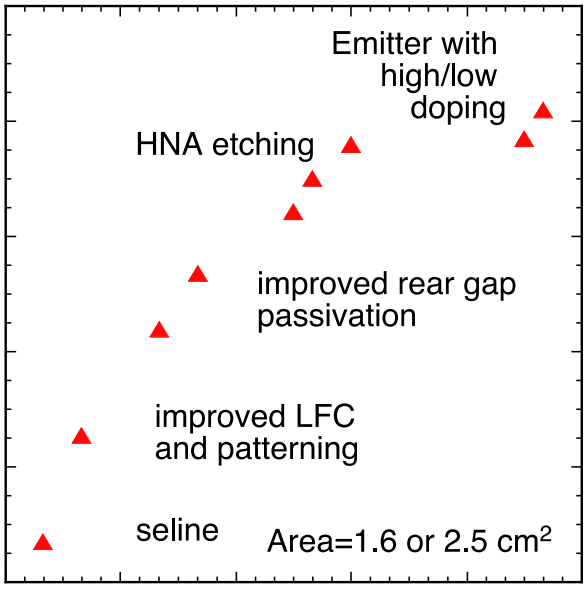


Figure SA.1 Efficiency trend for IBC-SHJ cells since January 2013.

Summary of Research Results for Tasks 1-10

Task 1. The goal of Task 1 (Subtasks 1.1 – 1.4) is to produce high-quality kerfless, thin Si wafers, by engineering minority carrier lifetimes that enable >20% device performance. Our approach involves three subtasks: 1.1. Characterize defect distributions in each of the unique Si materials from industrial partners and identifying the defects responsible for limiting cell performance; 1.2 Develop simulation/modeling tools to predict the effect of defects on cell parameters, especially V_{OC}; and 1.3 Develop engineering approaches to mitigate the most deleterious defects.

Subtask 1.1:Characterize performance-limiting defects in as-grown kerfless wafers
Subtask goal: Produce a taxonomy of defects (concentrations, types) for each of the accessible thin kerfless silicon materials (**as-grown**), correlating defect concentrations with measured bulk lifetimes and projected lifetime ceilings.
Status: Accomplished.

Subtask 1.2: Characterize performance-limiting defects in gettered and passivated kerfless wafers
Subtask goal: same as 1.1 above except **after gettering and passivation**.
Status: Accomplished.

Results

We developed a framework to determine kerfless wafer lifetime targets that can enable efficiencies commensurate with SunShot targets (>20%). We used Sentaurus Device models of standard Al-BSF, PERC, and front heterojunction (GaP/Si) solar cells to determine the injection-dependent lifetime at the maximum power point. These appear as colored lines in **Figure 1.1**, corresponding to device efficiencies shown on the right. Upon this figure, one can superimpose the injection-dependent lifetimes measured at the wafer level, before and after phosphorus diffusion. We observe that efficiencies >20% are enabled when as-processed kerfless-wafer bulk minority-carrier lifetimes approach 1 ms for PERC architecture, or exceed 0.1 ms for a HIT-like device.

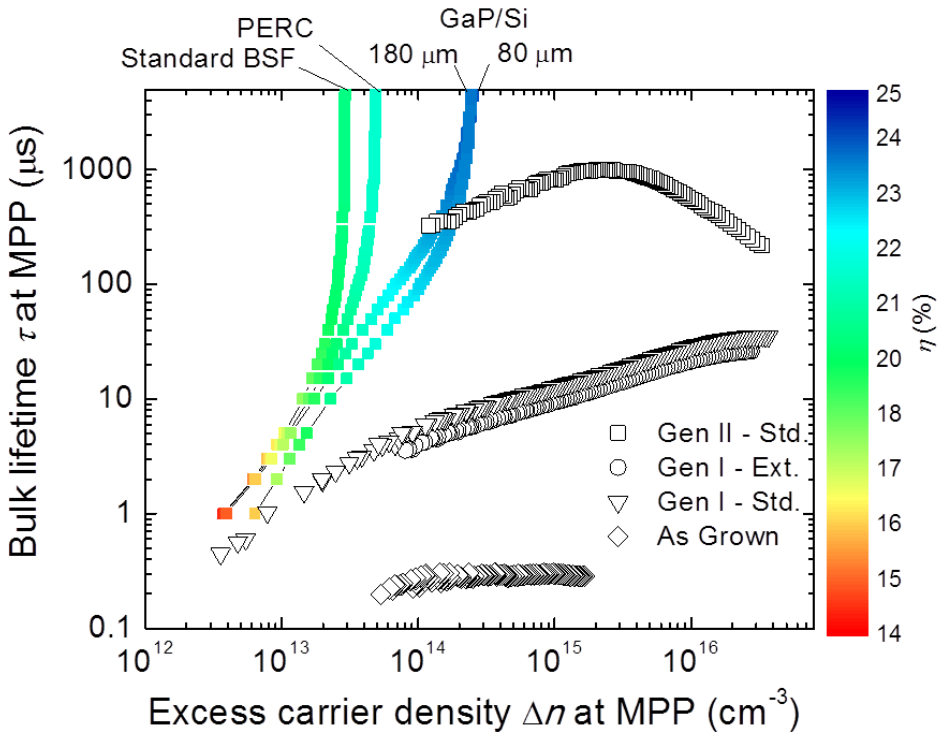


Figure 1.1: Colored curves show simulated bulk lifetime at the maximum power point (MPP) as a function of the excess carrier density at the MPP for four different device architectures. The color code indicates device efficiency. Black open symbols are measured bulk lifetime curve as a function of excess carrier density in two different generations of epi-Si wafers in the as-grown state, after standard, and after extended P-diffusion gettering.

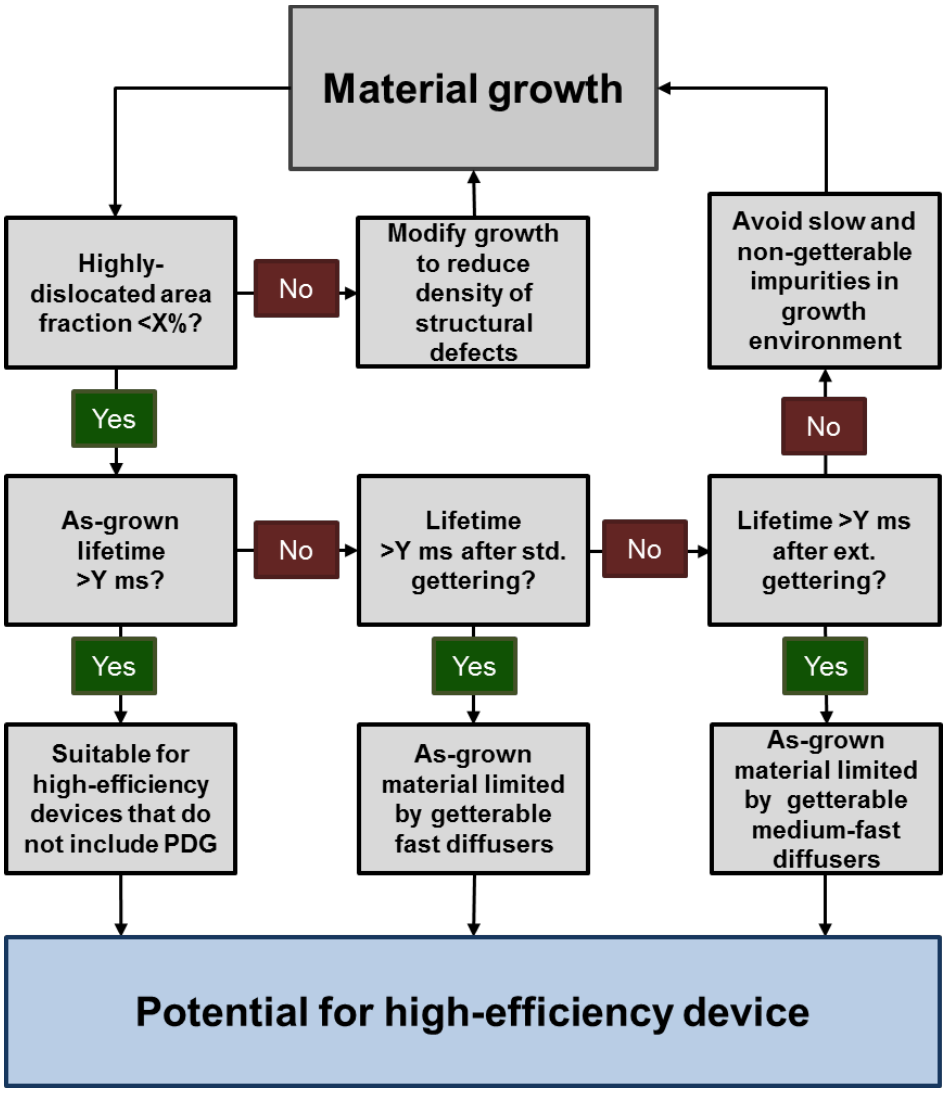


Figure 1.2: Simplified systematic approach developed over the course of this project, to determine and manage performance-limiting defects in kerfless silicon materials. *X* and *Y* are variables whose value will depend on the performance target that is set for a particular material.

Performance-limiting defects in as-grown and partially processed kerfless epi wafers were assessed. We established a continuous-improvement feedback loop, and analyzed two generations of kerfless epi material. Generation I represents the material provided to the MIT team at the onset of our collaboration within the context of the F-PACE project. Two company visits and several teleconferences were conducted to provide feedback from Gen I characterization, leading to a second generation of material (Generation II) that resulted from modifications made during the growth process used to fabricate the material. Both Gen I and Gen II materials were analyzed in an as-grown state, after standard gettering, and after an extended gettering designed using our I2E simulator to mitigate bulk impurity point-defect concentrations (**Figure 1.1**).

Materials: Epi wafers were exfoliated from their substrates, which consisted of a porous silicon release layer. Individual samples of approximately 40 × 40 mm^2 were laser cut from these samples. Four samples were obtained from the first generation (Gen I) material, while nine were obtained from the second generation (Gen II) material. The Gen I samples had an average estimated thickness of 63 μm, while the Gen II samples had an average estimated thickness of 99 μm, after an initial silicon-removing etch. An image of a similar sample from the epi material can be seen in **Figure 1.3**. Additional wafers from both generations were prepared for bulk impurity measurements.

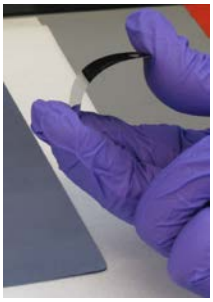


Figure 1.3. Photo of sample from kerfless epi wafer. Photo credit: David Berney Needleman

Impurity Measurements: Both slow- and fast-diffusing impurity point defects can limit performance of as-grown material. However, fast-diffusing impurities can often be removed *via* gettering. Thus, there is motivation to quantify the concentration of slowly diffusing impurities, and endeavor to reduce their concentration by engineering the feedstock and growth environment. This methodology is presented graphically in **Figure 1.2**.

Total bulk impurity concentrations for both samples were assessed by the inductively coupled plasma mass spectrometry (ICP-MS) method. Although subject to significant uncertainty, the ICP-MS analysis showed that contaminants in Gen I material include Cr, Fe, Mo, Ti, Mg, Al, Mn, Ni, Cu, Zn, Zr, and Nb. From Gen I to Gen II materials, slowly diffusing molybdenum and vanadium contamination levels decreased by up to 80%, suggesting a market improvement in as-grown crystal quality. This translated to improved performance (**Figure 1.1**).

Iron-boron (Fe_i-B_s) pair measurements after gettering suggest concentrations in the mid-10^9 to mid-10^{10} cm^{-3} levels, which implies an iron-limited lifetime entitlement above 1 ms. Thus, we conclude that iron point defects do not limit Gen II gettered lifetimes.

Deep-level transient spectroscopy (DLTS) was also performed *via* collaboration with Prof. Tony Peaker's group at the University of Manchester. Deep levels detected in as-grown materials were compared to literature, and appear consistent with platinum. After gettering, the concentration of this defect was below detection limits (**Figure 1.4**), consistent with lifetime improvement observed in **Figure 1.1**.

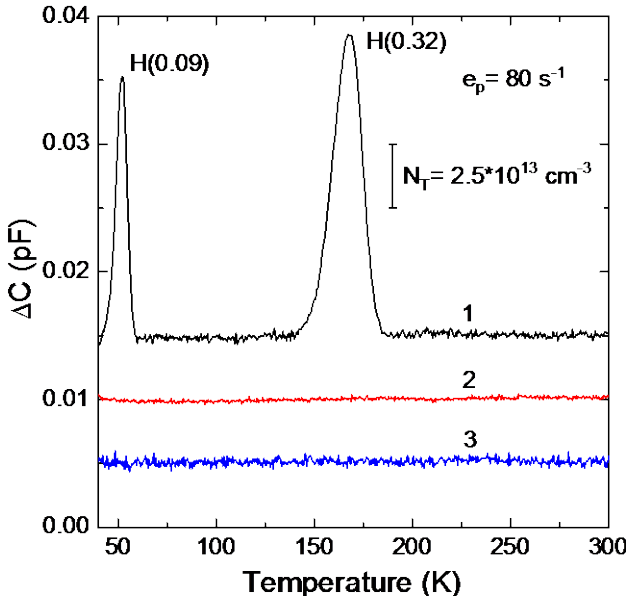


Figure 1.4. DLTS spectra for as-grown *p*-type epi material shows the presence of two peaks corresponding to Pt_s (1, black). After standard (2, red) and extended (3, blue) gettering, the peaks are no longer above detection limits. Measurement settings were: bias –9.0 –7.0 V for spectrum 1, bias –9.0 –4.0 V for spectra 2 and 3, emission rate e_p = 80 s^{-1} and pulse duration 1 ms for all the spectra. The spectra are shifted on the vertical axis for clarity.

Extended defects: Characterization of structural defects is vital for understanding their impact on materials performance and for developing techniques for mitigation. We analyzed structural defects in kerfless materials by employing a combination of defect etches to reveal structural defects, and scanning electron microscopy and/or automated optical microscopy to quantify defect concentrations. These measurements were then correlated with electrical measurements, to determine the impact of extended defects on bulk minority-carrier lifetime. This activity is coupled to **subtask 1.4**, which envisions developing simulations to predict the device impact of extended defects percolating through the junction region.

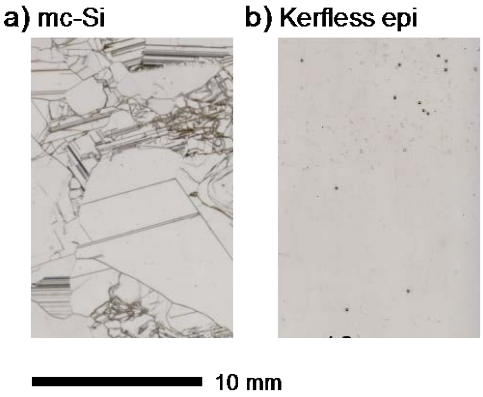


Figure 1.5. High-resolution flatbed scanner images comparing representative regions of (a) a mc-Si ingot and (b) single-crystalline kerfless epi silicon. Defect etching reveals an average dislocation density of $\leq 10^4$ cm^{-2} for the epi, and 10^5 cm^{-2} for mc-Si.

We find that the concentration of structural defects in epi silicon, while comparatively lower than traditionally multicrystalline silicon ingot material (**Figure 1.5**), can locally impact minority-carrier lifetime (**Figure 1.6**).

We investigated the origins of these structural defects in epi wafers. Through electron microscopy and defect etching, we found that many dislocation clusters originated at the porous silicon layer, suggesting that improved control of this layer may assist in minimizing structural defect density (**Figures 1.7** and **1.8**), which in turn affects the distribution of precipitated impurities (**Figure 1.9**).

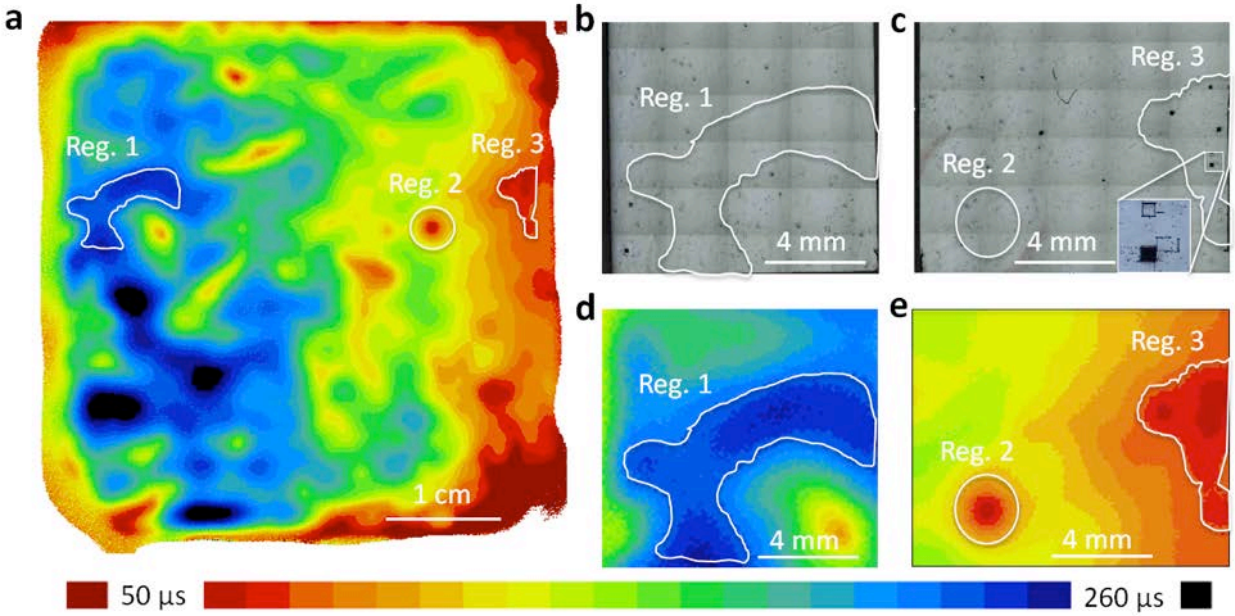


Figure 1.6. µ-PCD maps of effective lifetime exhibiting inhomogeneity after P-gettering. The full-wafer µ-PCD map appears in (a), with magnified scans in Regions, 1, 2, and 3 (d, e). The recombination activity of the sample corresponds to structural defects in Regions 1 and 3 (b, c). In Region 2, where no observable structural defects are observed on the lifetime map, we observe evidence of porous silicon collapse in the adjacent substrate.

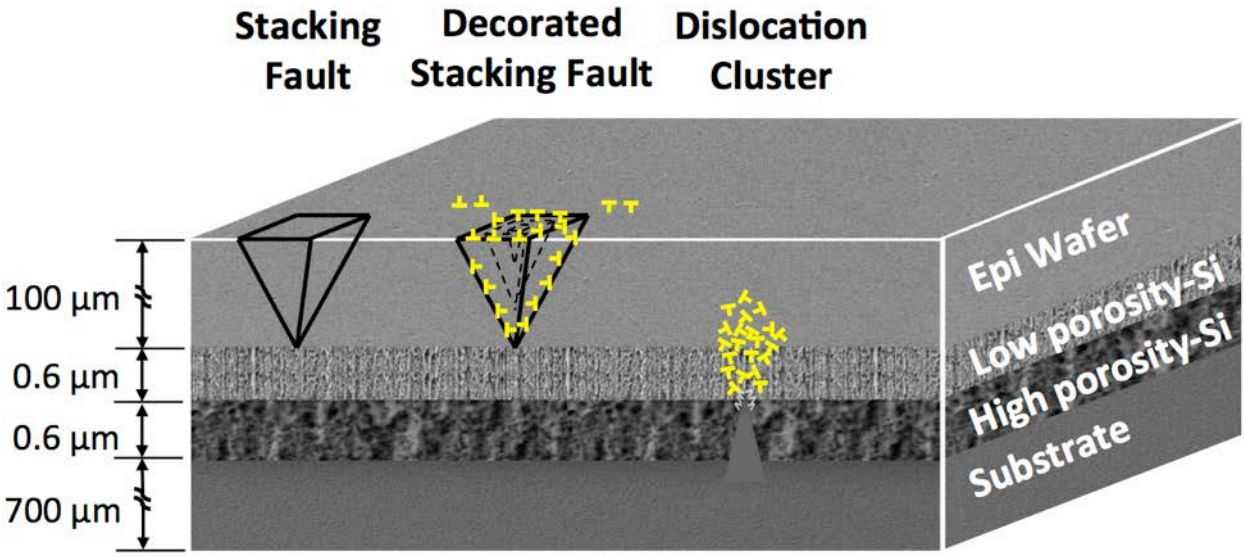


Figure 1.7. Schematic of epitaxial silicon on porous silicon bi-layer. Three categories of structural defects are shown: stacking faults, concentric stacking faults decorated with dislocations, and dislocation clusters. The defects are not to scale.

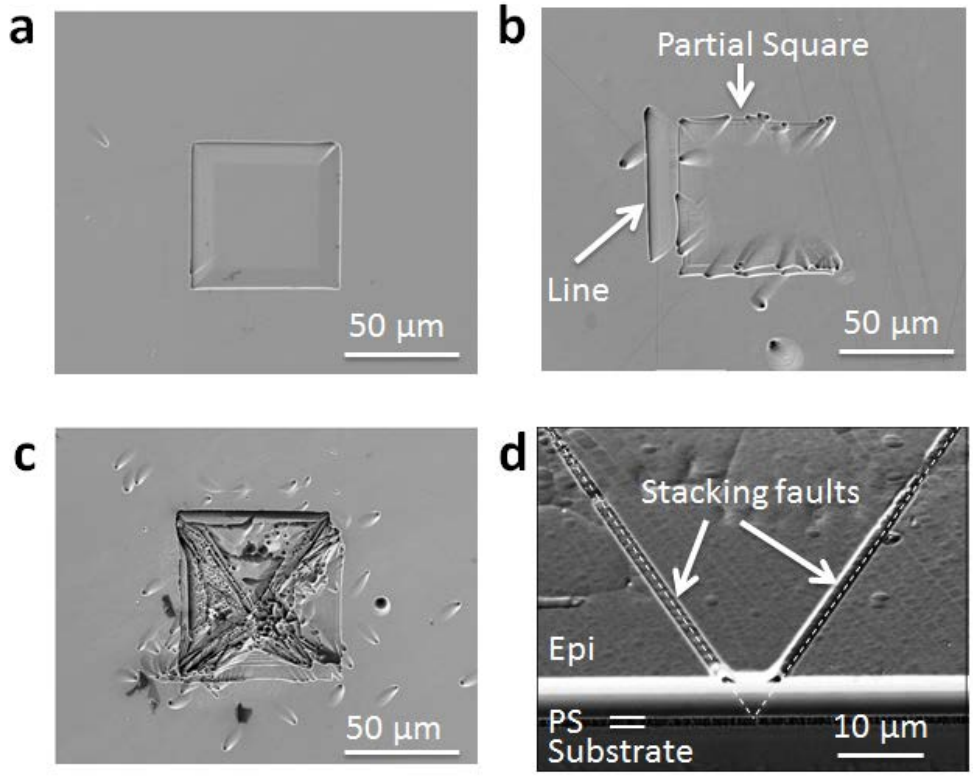


Figure 1.8. (a–c) SEM plan view of stacking faults (a) Square and free from dislocations (b) line and partial-square stacking faults, (c) concentric squares stacking faults and heavily decorated with dislocations. (d) A cross-sectional SEM image of a stacking fault projected to show its origin at the porous silicon/epi interface.

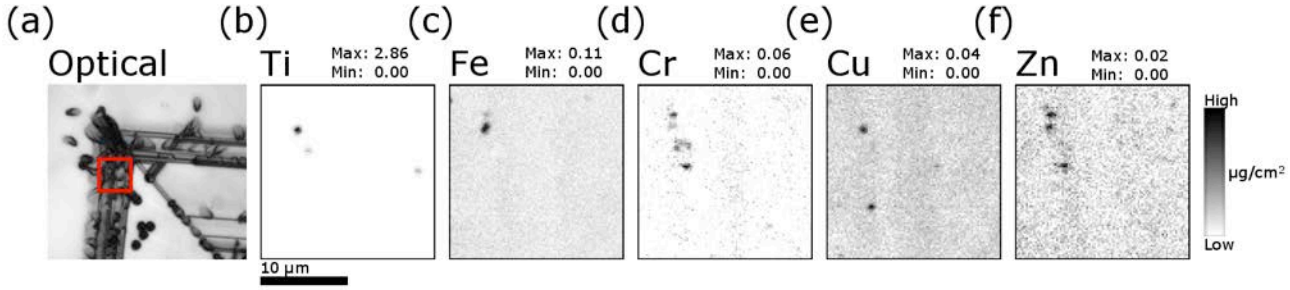


Figure 1.9. Synchrotron-based micro X-ray fluorescence map of as-grown *p*-type material. (a) At a stacking fault, particles of (b) Ti, (c) Fe, (d) Cr, (e) Cu, and (f) Zn are observed. The approximate scanned area is indicated in red in the optical image (a). The maximum radius of Fe particles observed in the sampled area is 16 nm.

Subtask 1.3: Develop and apply defect-engineering techniques to improve processed bulk minority carrier lifetimes of kerfless wafers.
Subtask goal: Demonstrate bulk lifetimes in excess of 100 µs over limited wafer areas, and average bulk lifetimes in excess of 60 µs.
Status: Accomplished.

Results

We developed enhanced annealing profiles during phosphorus diffusion, to mitigate the effect of fast-diffusing impurities during device processing. Samples from the two generations of epi kerfless material were gettered in a phosphorous diffusion furnace, following the as-grown characterization. Two time temperature profiles were employed (**Figure 1.10**). Two samples from each generation were used for each time-temperature profile. The first process consisted of a "Standard" recipe with an 845°C 25-minute plateau (with 12-minute $POCl_3$ deposition) that ended with unloading of the furnace at the plateau temperature and air-cooling of the wafers. The second process added a slow cool of the wafers down to 575°C, and an additional 2 hour anneal at 575°C that ended with the unloading of the furnace at 575°C and air-cooling. A low temperature anneal (LTA) has been shown to be effective through experiment and simulation at reducing iron concentration. The cost trade-off of reduced throughput for enhanced efficiency has been evaluated, and there is a strong incentive to enable higher efficiencies.

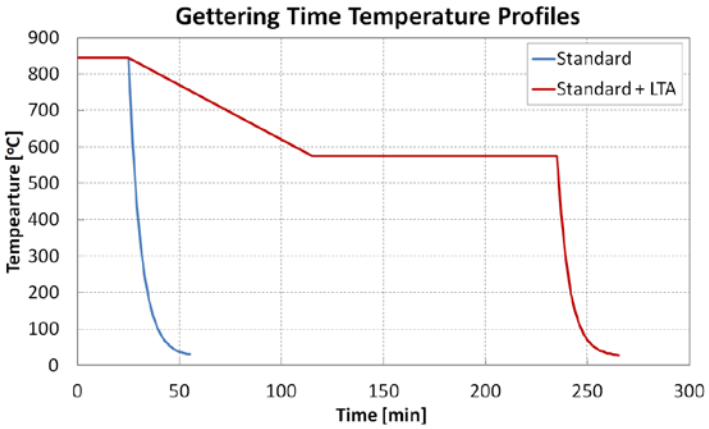


Figure 1.10. Idealized gettering time temperature profiles for epi wafer gettering: standard annealing and standard plus a low-temperature anneal (LTA). Samples were cooled in air to room temperature.

After phosphorus diffusion, lifetimes achieved in Gen II material (~ 1 ms in both *n*- and *p*-type materials) correspond to diffusion lengths that are >10x greater than the sample thickness (~87 μm), an important metric for advanced devices.

Subtask 1.4: Develop 2D and 3D models for predicting defect impact on V_{OC}.
Subtask goal: Develop 2D and 3D models predicting V_{OC}-impact of extended defects in thin silicon cells.
Status: Accomplished.
Highlights:

- Simulated impact of extended defects on solar cell V_{OC} and efficiency.[24]
- Determined that absorbers with extended defects can still reach efficiencies >20%, provided the density of deep levels along the grain boundary (N_{deep}) is lower than ~106 cm^{-2}.

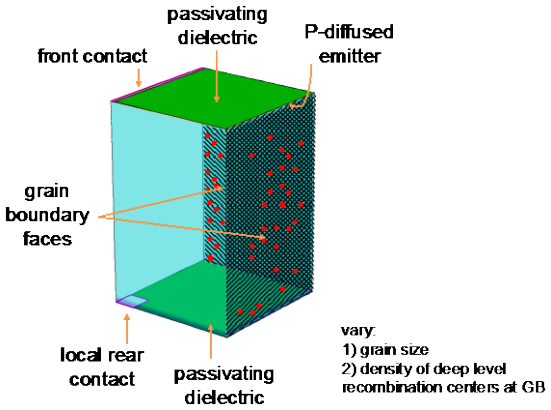


Figure 1.11. Simulation domain that we used to calculate the impact of extended defects on high-efficiency device performance. This Sentaurus Device simulation domain includes a grain boundary decorated with recombination centers.

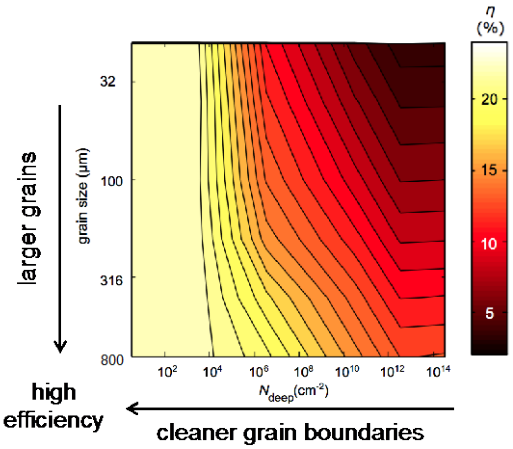


Figure 1.12. Simulation output. This phase space presents the simulated PERC cell efficiency as a function of grain size (*y*-axis) and areal density of deep levels along the grain boundary (N_{deep}, *x*-axis)

Device simulation: Effect of extended defects. For a kerfless silicon device, extended defects (like stacking faults) may not only affect minority-carrier lifetime, they may affect V_{OC} by enhancing diffusion/saturation current (J_0). With the intent of defining defect tolerances for kerfless materials, we selected Synopsys Sentaurus as a simulation platform due to its wide use in the field, including within the research team, its superior meshing capabilities, and the ease with which models can be modified to include processing steps and to convert between 2D and 3D. A model was developed in Sentaurus to simulate the impact of dislocations on device performance at room temperature. This model matches the recombination activity described by the model of Kveder *et al.*, *Phys. Rev. B* **63**, 115208, 2001, using a single mid-gap donor and acceptor trap state. We assumed that grain boundaries can be modeled as dense rows of dislocations, pursuant to Stokkan *et al.*, *J. Appl. Phys*. **101**, 053515, 2007. V_{OC} and efficiency losses were predicted, assuming a grain size and density of recombination centers along the grain boundaries (**Figure 1.11**). Emitter depth did not affect the impact of the dislocation on device performance, but wafer thickness did. Results are summarized in **Figure 1.12**, indicating that for grain sizes >1 mm^2 and $N_{deep} < 10^6$ cm^{-2}, efficiencies >20% are in principle accomplished even with a standard PERC architecture. Note that to accomplish Ndeep < 10^6 cm^{-2}, which corresponds to an SRV of a few hundred cm/s, excellent gettering and passivation is required. The simulated data herein assumes 180 μm wafer thickness; tolerances relax for thinner wafers.

Task 2. ***Develop a-Si/c-Si heterojunctions***

Subtask 2.1 (Q1-Q4) Optimize conventional front heterojunction emitter / back contacts separately

Subtask Goal: Standard front junction SHJ with FF>77%

Results:
There are several practical aspects to fabricating high quality a-Si/c-Si heterojunctions. Since we use CZ or FZ wafers with bulk lifetime > 4000 usec, effective lifetime is largely controlled by the surface passivation. Thus, wafer cleaning and a-Si deposition, and a-Si film properties are critical. Their mutual optimization is complicated by dependence on the specific surface texture of the wafer. Next, the a-Si/c-Si band alignment is important to facilitate efficient carrier transport since wider bandgap leads to an increasingly higher valence band offset (VBO). Modeling has consistently shown that lower-than-normal bandgap (<1.72 eV) and relatively thin (<10 nm) a-Si is needed for high FF[25]. Methods to reduce the buffer layer bandgap are well known, such as increasing deposition temperature and increasing the H dilution. But they tend to lead to formation of nanocrystalline or highly defective a-Si phases which severely degrade the passivation quality. Thus optimization of any of these process steps is sensitive to the other process steps.

We will discuss efforts to improve the performance to optimize the emitter by moving sequentially from the wafer surface outwards to the TCO contact.

It is well established that excellent Si wafer surface cleaning is required to produce high lifetime and high Voc. Our standard cleaning process (solvent clean, etch in TMAH, piranha H_2SO_4:H_2O_2 in 2:1 ratio, finally 1 minute in 10% HF) typically results in lifetimes > 1500 usec with implied Voc (iVoc) > 710 mV on 2 or 10 Ohm-cm^2 Cz wafers when passivated with 10 nm a-Si buffer layers. In this phase IEC investigated a ‘dry’ pre-cleaning process using O_2 plasma as a viable alternative to the piranha etch. IEC invested in a RF plasma cleaning system to study its use for the pre-HF oxide growth as well as for photoresist removal. We varied the RF power and duration keeping O_2 flow rate and pressure constant at 10 sccm and 240 mT, respectively. Front SHJ devices were made on textured Cz wafers with 8 nm i-layer passivation on front and back side with different plasma oxide time and power. Their efficiency is shown in Figure 2.1 plotted against RF power. The results indicate a clear optimum at 75 W for 2 minutes where baseline performance, i.e. 17% efficiency, was obtained. The plasma conditions seem to primarily affect the FF not Voc. We achieved these results only at the very end of this reporting period so all further device performance discussed in this report were obtained with the standard piranha+HF cleaning. We plan to incorporate the plasma etching more routinely in the future.

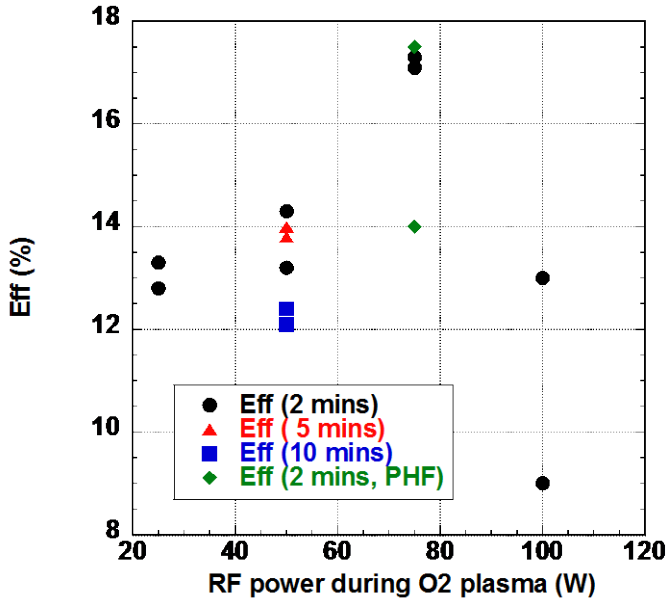


Figure 2.1: Efficiency vs RF power for different O_2 plasma exposure time. Each symbol is average of 4 cells. The green diamonds represent pieces which received 75W plasma for 2 minutes followed by standard piranha etch. Pieces receiving only the standard piranha clean also had ~ 17.2% efficiency which matched the results with O_2 plasma for 2 minutes at 75W.

The i-layer bandgap (E_G) is known to have a critical impact in front SHJ cells. With increasing E_G, the FF decreases due to poor hole transport over an increasingly higher valence band offset (VBO). A series of runs were made exploring a wider a-Si i-layer deposition parameter space around our previous baseline (pressure 1.25 or 1.5 T, T=175-250°C, ratio R=H_2/SiH_4=2.0 or 2.5, total flow (TF) rates of 28-56 sccm). FTIR and ellipsometry were used to characterize bandgap, thickness and H2 bonding. QSSPC was used to evaluate passivation quality via the effective lifetime. While we could obtain high lifetime (>700 usec) under a range of conditions, the bandgap and growth rates were often too high. As temperature increased with constant total flow (TF) rate of 16 sccm SiH_4 and 40 sccm H_2, Eg decreased as expected but still remained too high even at 250°C. Reducing total flow rate (75% or SiH_4/H_2=12/30 sccm) reduced the bandgap to an acceptable value. Reducing the total flow at a constant pressure increases the residence time for each species in the plasma. Based on these results, we selected SiH_4= 10 sccm, H_2= 25 sccm at 250°C for our new i-layer conditions. More details including device results from IBC cells with different i-layer bandgaps has been published elsewhere[26]. Further buffer layer optimization is reported under Task 6 including comparison of DC and RF plasma deposition.

Doped layer conditions were similarly adjusted. We found that the device performance was more sensitive to the p-layer than n-layer conditions. This is discussed further in Task 6. During the second half of the project, we developed an HNA (HF/HNO3 acid mixture) etch which removed more defects and created a better surface for passivation and emitter formation. This is discussed in Task 10.

The above discussion summarized our results to reduce the bandgap of a-Si buffer layers by varying the deposition conditions, specifically H_2 dilution and temperature. While we were able to reduce E_G as low as 1.65 eV, these conditions often produce films on the edge of nanocrystallinity, which negatively impacts their ability to passivate the Si. Instead, we looked to alloying with Ge to reduce E_G. We have installed a

cylinder of 20% GeH_4/80% SiH_4 after upgrading our hydride gas control facility in consultation with the university EHS safety committee for handling such extremely toxic GeH_4 gas. Accordingly, our gas monitoring system is set to the detection threshold for the SiH_4 level corresponding to the TLV of the 20% GeH_4 mixture. We estimated that deposition from the pure 20/80% mixture should have enough GeH_4 to reduce E_G to ~1.5 eV.

A series of studies were made to evaluate the bandgap reduction and passivation using various GeH_4/SiH_4 mixtures. A 10% GeH_4 concentration in the plasma yielded E_G <1.60 eV. Front SHJ solar cells were fabricated on planar Fz wafers with 8nm thick passivation layer on both surfaces having three different bandgaps. Table 2.1 summarizes their passivation quality and solar cell parameters. The lifetime and iVoc decrease with decrease in bandgap consistent with the actual Voc. The Jsc decreases as well, probably due to increased absorption of short wavelengths in the a-SiGe. But the FF is not affected by E_G or GeH_4 flow. This suggests the FF is not reduced by the increased interface defects. Light JV curves were analyzed to obtain series resistance R, diode quality n, and recombination current J_o. The Table shows that R decreased with bandgap, while n and J_o increased.

Table 2.1 Effect of reducing the front and rear buffer layer (8nm) bandgap by alloying with Ge on passivation quality and front SHJ solar cells.

Material	E_G (eV)	Lifetime (usec)	iVoc (V)	Voc (V)	Jsc (mA/cm2)	FF (%)	Eff (%)	R_s (Ω.cm2)	n	J_0 (mA/cm2)
a-Si	1.72	1302	0.715	0.687	30.9	73.0	15.5	1.7	1.5	**6.0E-07**
a-SiGe	1.60	201	0.660	0.630	29.9	71.0	13.4	1.0	1.8	**4.0E-05**
a-SiGe	1.56	76	0.631	0.604	28.7	72.8	12.6	0.7	1.8	**6.0E-05**

The emitter thickness was varied from 6 to 16 nm in a series of front SHJ solar cells over several months (runs MC1216, 1223, 1228, 1270, 1284, and 1295). Buffer layer conditions were SiH_4= 10 sccm, H_2= 25 sccm at 250°C as discussed above. Table 2.2 lists the best cell performance having variation in p-layer thickness. The maximum appears to broadly span 9-13 nm with no strong trend. Figure 2.2 shows the QE with decreasing blue QE with increasing p-thickness.

Table 2.2 Performance of front SHJ solar cells having different p-layer thicknesses. All pieces had symmetric 8 nm a-Si buffer. Values are average of 4 cells per piece.

Piece	P-layer (nm)	Si wafer	Voc	Jsc	FF	Eff
MC1284-06	16	10 Ω Cz	0.656	33.1	66.4	14.4
MC1270-01	13	10 Ω Cz	0.698	32.3	73.6	16.6
MC1284-03	9	10 Ω Cz	0.690	34.1	74.6	17.6

MC1270-19	6	3 Ω FZ	0.676	35.5	70.0	16.8

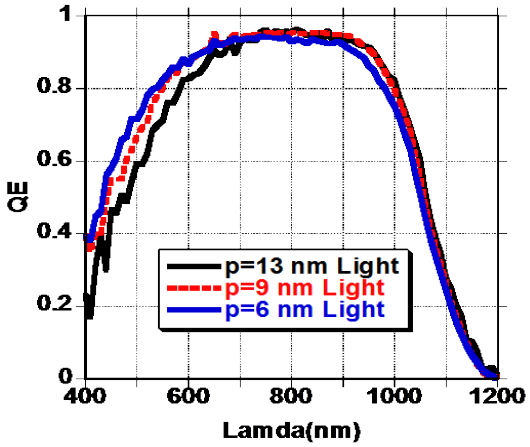


Figure 2.2: QE for 3 different p-layer thicknesses.

The milestone for Task 2 was standard front junction device with area > 1cm^2 and FF>77% and Voc>680 mV. Table 2.3 shows performance of devices from 3 different runs meeting the Voc and FF goals. Overall, the highest efficiency front junction SHJ device made this period was MC1228-13. However, slightly higher Voc was obtained later in the program.

Table 2.3. JV performance for 'best' FHJ devices during this period. IQE is the QE integrated with AM1.5G spectrum to validate the Jsc value

Cell	Area cm^2	Voc V	Jsc mA/cm^2	FF %	Eff %	IQE mA/cm^2
MC1228-13	0.56	0.687	34.7	77.2	18.4	35.1
MC1254-01	0.56	0.700	33.0	76.1	17.5	33.7
MC1284-03	0.56	0.690	34.1	74.6	17.6	n/a

Subtask 2.2 (Q3-Q6) Develop enhanced models of c-Si heterojunction devices

Subtask goal: Model quantitatively predicts measured IV trends with i-layer thickness, defects, bandgap within ±5%.

Results: This work produced a new procedure to self-consistently derive model input parameters such as interface state density (D_{it}) and electron/hole recombination cross section from SRV and admittance was developed. These parameters were then used as inputs to model FJ and IBC-SHJ solar cells using a two-dimensional (2D) simulation software package. The methodology and results in this section represent an original and unique approach to extract experimentally-grounded input parameters for simulation. It has been submitted for publication. The model has been validated by comparison with measured front SHJ and IBC-SHJ JV and QE performance. Excellent agreement is obtained. This work was described in more detail in publications[27],[28].

In order to investigate both the front and back surface recombination processes for front SHJ and IBC-SHJ solar cells (figure 2.3), five relevant passivation structures with symmetrical configuration were made on both sides of n-type c-Si wafer. Effective lifetimes of the symmetrical passivation structures as functions of excess minority

carrier density were measured by quasi steady state photoconductivity (QSSPC) using a Sinton tester. The SRVs for the five symmetrical passivation structures are plotted as open symbols in Figure 2.4.

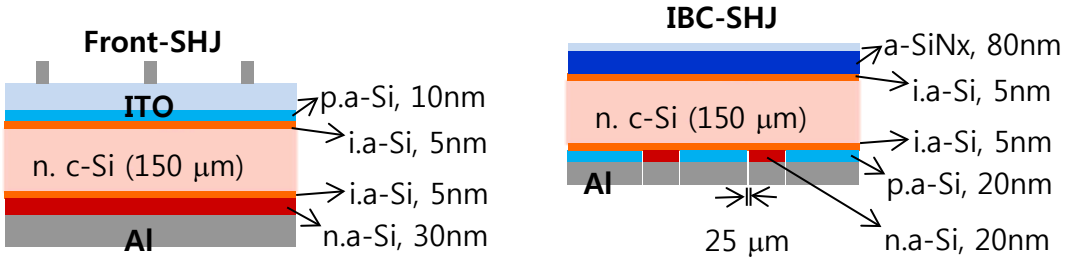


Figure 2.3: Schematic pictures of front SHJ (left) and IBC-SHJ (right) solar cells.

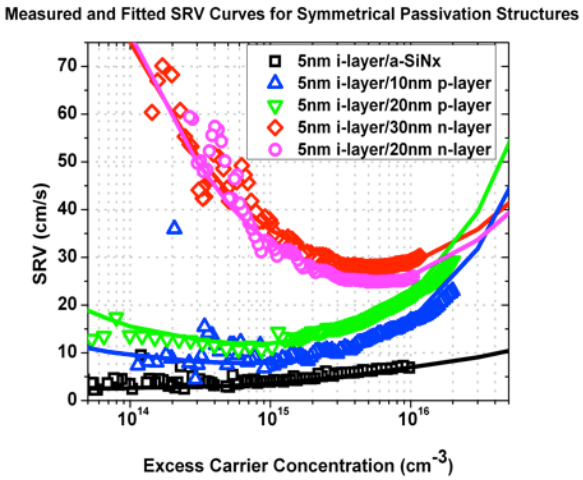


Figure 2.4: Measured (symbols) and fitted (lines) SRV curves for five symmetrical passivation structures. These represent all 5 types of interfaces with c-Si found in front SHJ and IBC-SHJ cells.

The hole and electron capture cross sections (σ_p, σ_n), $D_{it}(E)$, and the interface charge (N_{Fit}) were treated as adjustable parameters and determined by fitting the experimentally measured SRV curves for the five passivation structures. A numerical procedure[29] was performed with the help of a computer program developed by IEC. The distribution of $D_{it}(E)$ and fixed charge in a-SiNx layer were also obtained from the metal-insulator-semiconductor (MIS) device containing the i-layer/a-SiNx stack as described in Task 3.2. There is excellent agreement between the modeled (solid lines) and measured (open symbols) SRV curves for the five symmetrical passivation structures as shown in Figure 2.4. The interface defect distribution $D_{it}(E)$ and the carrier capture cross sections σ_p and σ_n, and N_{fit} for each passivation structure are listed in Table 2.4 and were input for the TCAD tool to simulate our baseline front SHJ and IBC-SHJ solar cells. The other parameters for each of our baseline a-Si layers were listed in our publications[28],[27].

Table 2.4 Parameters in extended Shockley-Read Hall (SRH) model used to fit measured SRV curves in Figure 2.4. D_{it} is given as the value at the mid band gap of c-Si (see text). These values were used as input for the Sentaurus device model.

Structure	D_{it}	σ_n	σ_p	N_{fit}

	($cm^{-2}eV^{-1}$)	(cm^2)	(cm^2)	(cm^{-3})
i/a-SiN_x	$4.4x10^{10}$	$3x10^{-18}$	$6x10^{-17}$	N/A
i/10nm p	$1.4x10^{11}$	$2x10^{-17}$	$1x10^{-15}$	$-4.0x10^{18}$
i/20nm p	$3.1x10^{11}$	$8x10^{-18}$	$2x10^{-15}$	
i/20nm n	$1.6x10^{11}$	$1x10^{-18}$	$3x10^{-16}$	$5.4x10^{18}$
i/30nm n	$1.6x10^{11}$	$1x10^{-18}$	$3x10^{-16}$	

We used "*Sentaurus Device*" TCAD package from *Synopsys Inc.* to simulate both front SHJ and IBC-SHJ solar cells. To validate the accuracy of the simulation, dark and light JV curves were simulated and compared with the baseline experimental devices. As seen in Table 2.5 and Figure 2.5, Voc, Jsc, FF, and efficiency as well as the shapes of the JV and QE curves, were well matched, thus validating the physical models and parameters used in simulations. The good agreement between simulation and experiment confirms accuracy of the simulation routine and procedure to obtain the input parameters.

Table 2.5: Comparison of baseline and simulated FHJ and IBC-HJ solar cell performance. Simulations used the same models and parameters for the two types of devices.

Device Structure	Voc (mV)	Jsc (mA/cm^2)	FF (%)	Eff. (%)
Front SHJ (exp.)	682	31.3	76.8	16.4
Front SHJ (sim.)	683	31.3	77.2	16.5
IBC-SHJ (exp.)	670	34.2	65.2	15.0
IBC-SHJ (sim.)	674	34.1	64.8	14.9

The model has subsequently been used to provide valuable insight into front and IBC SHJ devices. We show here one example. The effect of buffer band-gap and thickness on FF is shown in Figure 2.6. Changes in Voc and Jsc with band-gap were minimal, but significant changes of FF were observed for both cells with similar trends. The primary impact of buffer layer band-gap on FF is caused by the band misalignment at p-n HJ interface. This band offset acts as potential barrier to the carrier transport at the hetero-interface. Since the electron affinities are kept constant, the valence band offset (VBO) at a-Si/c-Si interface will be increased if i-layer's band-gap is increased. This inhibits hole transport. Since holes are minority carriers, this impacts the photo-carrier collection. Hole transport can be inhibited not only by increasing the height of the potential barrier but also by widening it. Figure 2.6 shows that FF can be improved by an absolute ~20% if the buffer layer is narrowed from 10nm down to 2nm, for both cell structures but this is not practical plus it typically leads to lower Voc. Slightly weaker dependence of FF on buffer thickness has also been observed in experiments at IEC and elsewhere. Another crucial observation from Figure 2.6 is that the FF difference

between FJ and IBC-SHJ devices becomes smaller with narrower bandgap of i-layer, which was the motivation for investigating a-SiGe as a low bandgap passivation layer as described in previous section.

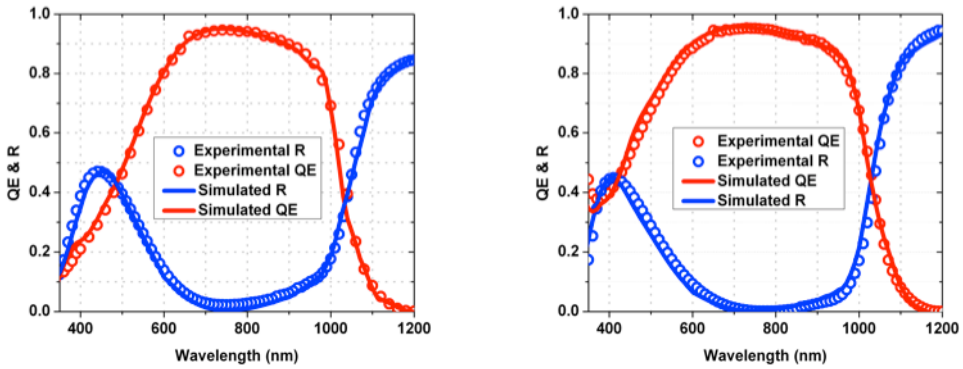


Figure 2.5 Simulated and experimental quantum efficiency and reflectance curves for Front SHJ solar cell (left) and IBC-SHJ solar cell (right).Symbols are data, solid lines are simulation.

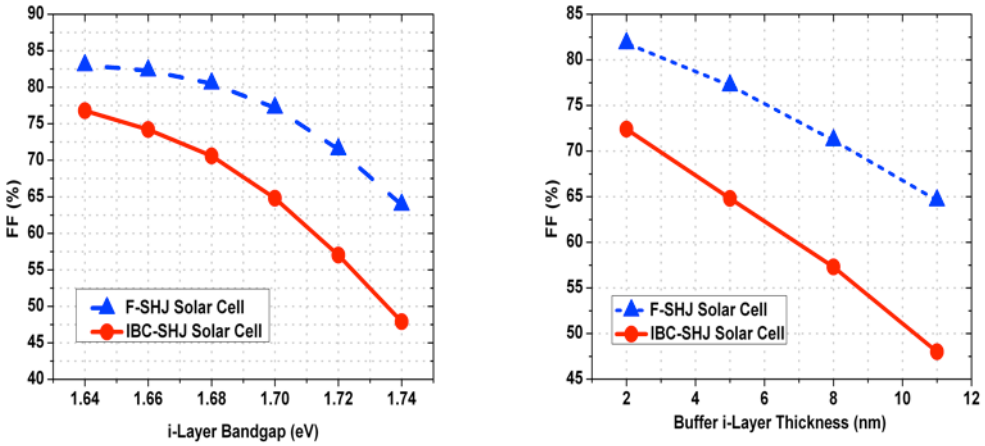


Figure 2.6: (left) Effect of buffer i-layer band gap on FF of FJ and IBC-SHJ solar cells. (right) Effect of buffer i-layer thickness on FF of FJ and IBC-SHJ solar cells.

Using this model, we studied the impact on device performance of c-Si surface recombination, interface defect density D_{it}, a-Si doped and intrinsic layer defect levels, and intrinsic buffer a-Si layer band-gap and thickness. The difference in FF between the two types of cells is related to the 2D nature of the IBC cell. This work provided a guide for optimization of both vertical and horizontal design IBC-SHJ solar cells and for diagnosis of both FJ and IBC-SHJ solar cell performance. More complete results are presented in our publications[27],[30] and in Tasks 5 and 6.

Task 3. Characterize and optimize front surface for IBC cell

Subtask 3.1 Optimize conventional front-surface texturing and passivation.

Under a previous DOE-SAI program, IEC developed a stack structure consisting of a intrinsic a-Si, silicon nitride (a-SiN_x) and silicon carbide (a-SiC) layers to provide front surface passivation as well as anti-reflection (AR) coating in IBC solar cells for polished c-Si wafers[31]. The 2-5 nm a-Si passivates the c-Si surface, the a-SiN_x is the primary AR layer, and the a-SiC is an etch barrier to protect the a-Si and a-SiN_x from subsequent chemical exposure. This stack layer has demonstrated excellent passivation on n-type c-Si and low absorption loss due to the transparency of a-SiN_x and a-SiC, as well as the ultra-thinness of a-Si layer. To further reduce front reflection losses, surface texturing of c-Si is necessary. To avoid potassium contamination from the standard KOH etching, an alternative wet etchant, tetramethyl ammonium hydroxide (TMAH) has been studied[32]. The stack structure process conditions must be reoptimized for the new surface texture. This work was presented in more detail in a conference publication[33].

Polished FZ n-type c-Si wafers (300µm thick <100>) were cut into 1"x1" pieces, given standard cleaning (Piranha+HF), then immersed into the etching solution of TMAH, DI water and isopropyl alcohol (IPA) in an ultrasonic bath. Samples were textured in TMAH for a period of time at 70^{o}C ~ 90^{o}C under ultrasonic agitation. Three variables, TMAH concentration (1 wt.% or 2 wt.%), etching temperature (70^{o}C, 80^{o}C, or 90^{o}C), and agitation time (10 min or 20 min) were studied. The concentration of IPA was 9%. The weighted reflectance for each sample was calculated by normalizing reflectance spectra with air mass 1.5 solar spectrum to quantify the effectiveness of surface texturing. Surface morphology of the optimized textured sample was characterized by SEM, to provide a guideline for modeling of surface geometry.

AR coating layers were grown by plasma enhanced chemical vapor deposition (PECVD) on polished wafers and glass for optical characterization. The intrinsic a-Si layer was deposited at 200^{o}C with a gas flow ratio of H_2/SiH_4=4. The a-SiN_x layer was deposited at 300^{o}C, using NH_3, SiH_4 and H_2 as precursor gases with a flow ratio of $R_{SiNx}=NH_3/SiH_4$. The a-SiC layer was deposited at 200^{o}C with a gas flow ratio $R_{SiC}=CH_4/SiH_4$, using CH_4, SiH_4 and H_2 as precursor gases. R_{SiNx} in a-SiN_x deposition, R_{SiC} and H_2 flow rate in a-SiC deposition were varied to adjust the refractive index and absorption coefficient of each layer, which were measured by variable angle spectral ellipsometry (VASE).

The full reflectance spectra of several textured samples are shown in Figure 3.1. Weighted reflectance ranged from 16 to 22%. SEM images of the sample with the lowest weighted reflectance (16%), which was textured by 1% TMAH for 20 minutues at 70^{o}C, is shown in Figure 3.2.

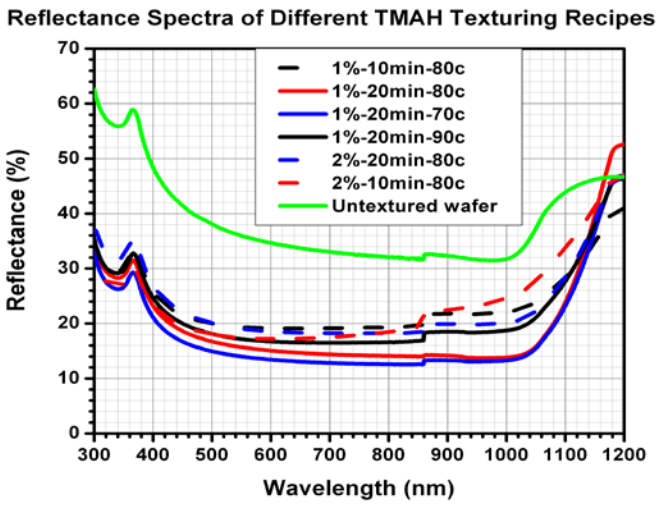


Figure 3.1: Reflectance spectra of bare c-Si samples with both sides texturization using different TMAH recipes (no AR stack).

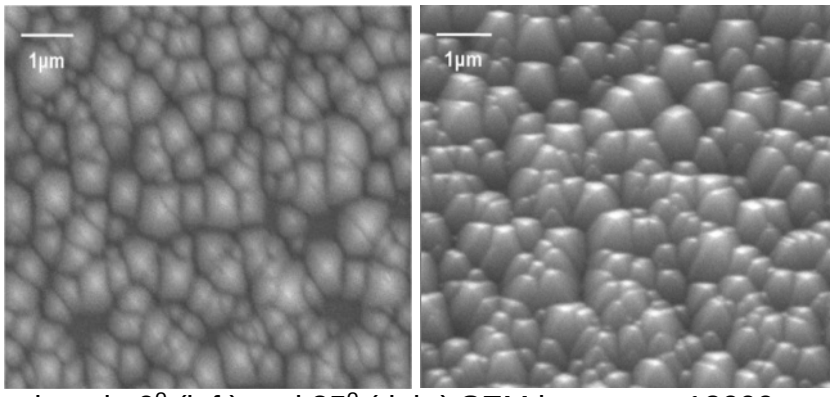


Figure 3.2: Tilted angle 0^{o} (left) and 35^{o} (right) SEM images at 12000 magnification of c-Si surface textured by 1% TMAH etchant at 70^{o}C for 20 min agitation.

High resolution SEM images in Figure 3.2 clearly show random pyramid-like textures resulting from anisotropic etching by TMAH solution. One can roughly estimate that both the bottom face length and the height of pyramid are 1μm or less.

The a-Si deposition condition giving bandgap = 1.8 eV and thickness of 5 nm had been previously optimized for high passivation quality and were unchanged for optical optimization described above, to ensure excellent surface passivation as characterized by a surface recombination velocity less than 10 cm/s. The optical constants of a-SiN_x and a-SiC layers were varied by the processing gas flow ratio and plasma type (DC and RF), as shown in Figure 3.3. These indices were used in the optical simulator to obtain an optimized growth condition for each layer.

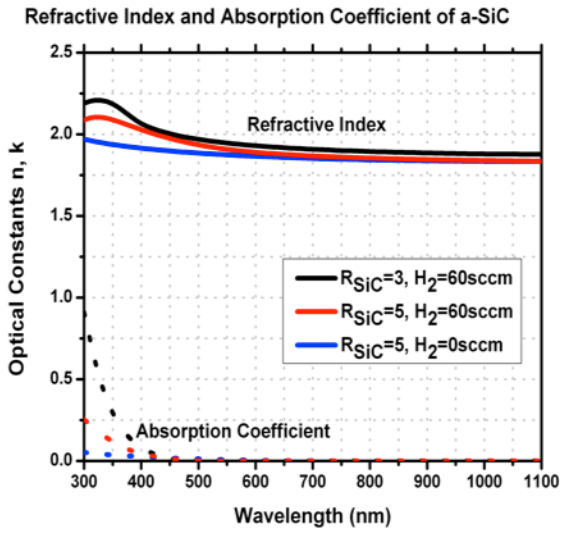


Figure 3.3a) Optical constants of a-SiC grown with different process gas flow ratios.

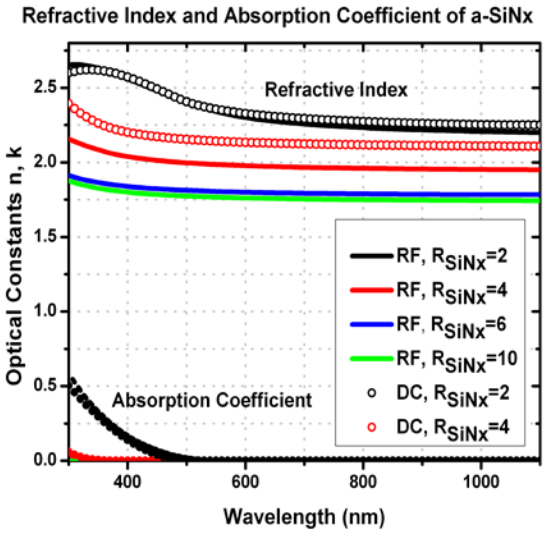


Figure 3.3b) Optical constants of a-SiN_x each grown with different process gas flow ratios and deposited by RF or DC plasma.

A simple 2D geometry which consists of 2 types of triangles periodically arranged with each other was used to analytically model the random pyramid-like textures with the heights of triangles of 1 µm or less. The ray tracing procedure and AR stack optimization was performed with Sentaurus TCAD tools, a package developed by Synopsys Corp. The geometry was verified by fitting the calculated reflectance of bare textured wafer with experiments, as shown in Figure 3.4.

AR stacks with different thicknesses as well as the optical constants (Figure 3.3) of a-SiN_x and a-SiC, were input into ray tracer to optimize for the maximum photo current J_{max}, assuming there is no electrical loss in the device and a total reflection on the back textured surface (by a back surface mirror). Simulation shows that the AR stack which consists of a 40nm thick DC a-SiN_x layer with R_{SiNx}=4 and a 40nm thick a-SiC layer with R_{SiC}=5 and no H_2 dilution is optimal for light trapping, giving a J_{max} of 40.1mA/cm^2. Figure 3.4 also shows the reflection and ideal quantum efficiency (QE) curves of an IBC solar cell having an optimized AR stack. By integrating the reflectance and absorption with the AM1.5 spectra, the total reflection loss (from ARC and back surface reflector) and absorption loss of current in AR stack were found to be 5.0mA/cm^2 and 1.7mA/cm^2, respectively. This is close to the milestone of obtaining integrated losses < 6mA/cm^2.

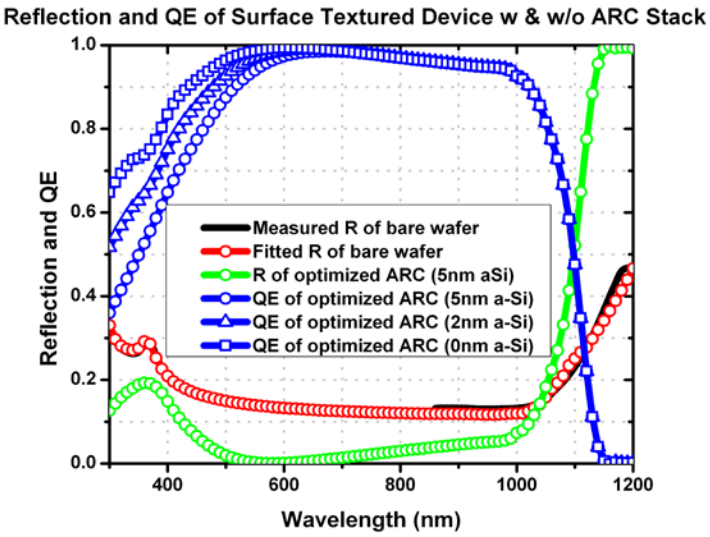
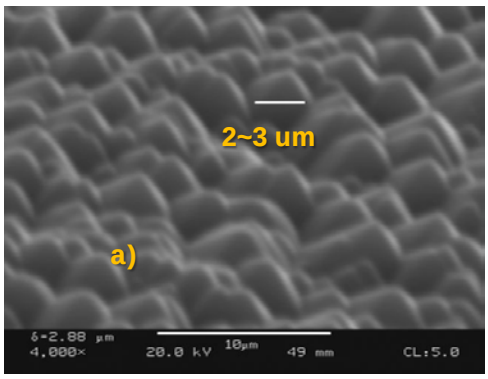


Figure 3.4: Measured and fitted reflection of textured bare Si wafer and calculated QE of surface textured c-Si device with and without optimized ARC stack.

The 5 nm a-Si layer is responsible for 1.3 mA/cm^2 of the absorption loss. Eliminating it increases J_{max} to 41.5mA/cm^2. Although the thickness of a-Si is only 5 nm, it is responsible for 75% of absorption loss in optimized AR stack, due to the multiple reflection and refraction of the random pyramid-like textures. However, the 5 nm thickness is crucial to passivate the surface and increase the effective lifetime and V_{oc}.

We re-optimized the TMAH texture process (time, temperature, TMAH concentration) to apply it to polished wafers in order to determine if a different texture would improve the photolithography processing and reduce optical losses even further. Figure 3.5a shows the surface after etching with the new optimized TMAH process. Note that the features are about 2-3 times larger and slightly sharper than those in Figure 3.2. Figure 3.5b shows the steady improvement in front surface reflection losses during this contract. As expected, the textured wafers (blue and green) have substantially lower reflection. Using the same low temperature deposited a-Si/SiN/SiC stack, the device with IEC textured surface has very low reflection, less than 5% between 500 and 1050 nm. Table 3.1 quantifies the key deposition variables and optical losses for these structures. The last entry (green data) verifies optical losses and SRV which meet the Task 3 goals. These processing and TMAH texture conditions were used for several of the IBC cells described in Task 5.



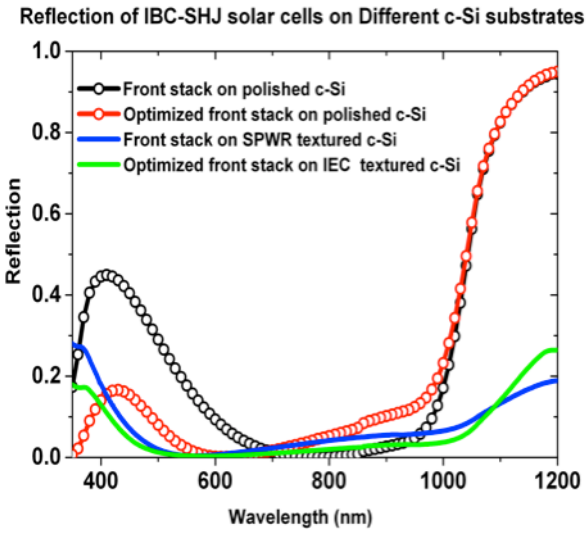


Figure 3.5. a) SEM of Si surface after optimized TMAH texture. b) Reflection for 4 combinations of polished and textured wafer. The black and red curves are on polished Si and the blue and green curves are on textured Si wafers.

Table 3.1. Deposition conditions and critical metrics for front surface processing of test structures whose reflection is shown in figure 3.5b. The gas flow ratios and thicknesses for SiN and SiC layers in the stack are shown along with the front surface optical losses and SRV. The optical losses are converted to current by integration of reflection (from figure 3.5b) and absorption (AR stack plus 5 nm a-Si passivation layer) with AM1.5 spectra from 300-1100 nm. SRV is converted from the measured lifetime at an excess carrier density of $10^{15}cm^{-3}$ by assuming the bulk lifetime of FZ c-Si substrate is 5 ms. Colors match those of figure 3.5b.

Sample Description	NH_3/ SiH_4 flow	CH_4/SiH_4 flow	a-Si/SiN/ a-SiC thickness (nm)	Front optical losses (AM1.5 mA/cm^2)	SRV cm/s
AR stack on pol Si	4	3	5/60/20	12.4	4.3
Optimized AR stack on pol Si	2	5	5/40/50	9.7	3.8
AR stack on commercial textured Si	4	3	5/60/20	4.4	7.6
AR stack on IEC textured Si	4	3	5/60/20	3.7	3.7

Subtask 3.2 (Q3-Q4) Fundamental characterization of front passivation

Subtask Goal: Obtain D_{IT} for front contact from CV for front multilayers from Subtask 3.1

Results:

Frequency and voltage dependent capacitance and conductance measurements of MIS structures having a-SiN_x/ a-Si passivation stacks were analyzed to obtain various fixed and voltage dependent charges including the interface state density D_{it}. These were then used to parameterize the QSSPC lifetime vs intensity to uniquely determine electron and hole capture cross sections. We applied existing techniques and developed new ones to characterize the mid gap heterojunction interface defect density D_{it} . Based upon the parameterization of the measured $D_{it}(E)$ distributions, modeling of the injection level dependent lifetime curves was developed and applied self-consistently to extract carrier capture cross sections σ_p and σ_n of interface defect states. The 2 nm a-Si layer significantly changes the magnitude and ratio of σ_p and σ_n states at the a-SiNx/a-Si/c-Si stack interface (σ_p~$5x10^{17}cm^{-2}$ and σ_n~$3x10^{18}cm^{-2}$) compared to an a-SiNx/c-Si interface which explains its critical role in surface passivation.

Metal-insulator-semiconductor (MIS)-like devices were fabricated for capacitance (C-V) and conductance (G-ω) characterization. The insulating layers were a-SiNx/a-Si passivation stacks on n-type c-Si wafers with Ohmic back contact. Details of the measurement and samples are published elsewhere[34]. Variables included the a-SiNx thickness, deposition temperature (300 or 380°C) and N-concentration, and a-Si thickness (2-20 nm). Figure 3.1 (left) shows the effective excess minority carrier lifetime and the corresponding SRV from QSSPC at the injection level of $10^{15}cm^{-3}$. The solid lines represent samples with both sides passivated by a-SiNx/a-Si stack with different a-Si layer thickness. Without any a-Si layer ($d_{a\text{-}Si}$=0 nm), the effective lifetime of a-SiNx passivated wafer is very low ~ 15µs. Inserting a 2 or 5 nm a-Si:H layer improves the lifetime by over 2 orders of magnitude to 2.2 or 2.8 ms, respectively. Without a-SiNx, a 20 nm thick a-Si layer would be required to provide the same effective lifetime (>2 ms) as obtained with a 2-5 nm a-Si layer together with a-SiNx. The thicker a-Si layer would cause 1-2 mA/cm^2 higher absorption loss compared to the stack with thinner a-Si layers. This data confirms that we can obtain SRV< 5 cm/s for the front a-SiNx/a-Si stack when the a-Si > 3 nm, meeting the subtask milestone.

a)	b)

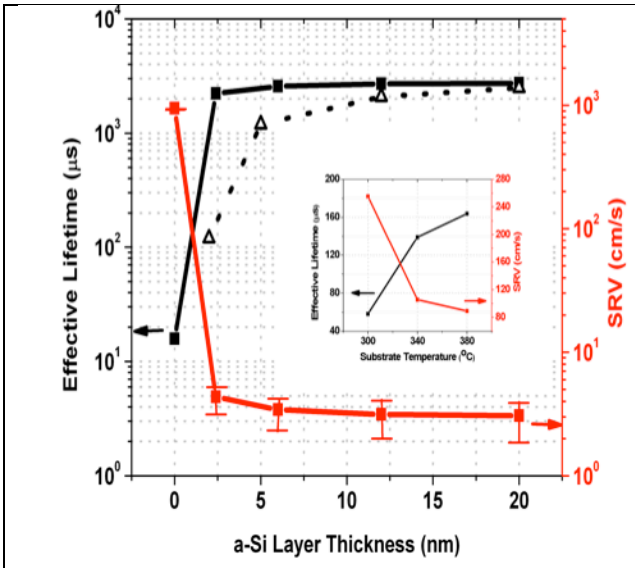


Figure 3.6a: Effective lifetime and SRV of $R_{a\text{-}SiNx}$=4 a-SiN_x:H/a-Si:H stack passivated 300μm FZ n-type c-Si wafer with varied thickness of a-Si:H layer (solid symbols), as compared with single a-Si layer passivation (open symbols). Inset: Single $R_{a\text{-}SiNx}$=1 a-SiNx layer ($d_{a\text{-}Si}$=0nm) passivation for 3 substrate temperatures. Values are given at the injection level of $10^{15}cm^{-3}$.

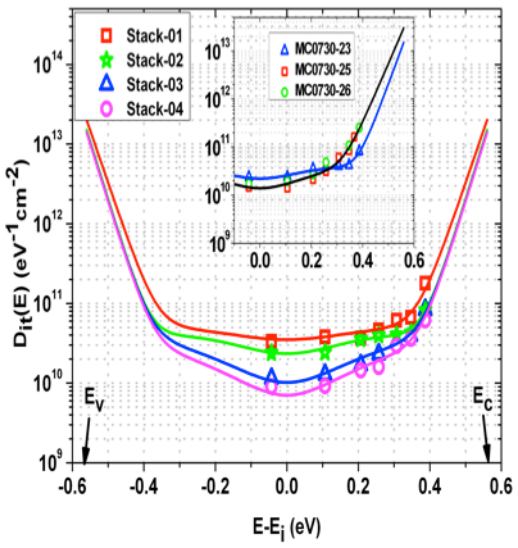


Figure 3.6b. Measured (open symbol) and parameterized (lines, see text) interface defect density distributions $D_{it}(E)$ at stack/c-Si interfaces with varied a-Si layer thickness. Inset: with varied a-SiNx growth gas flow ratio $R_{a\text{-}SiNx}$.

Other important conclusions are that the 2 nm a-Si layer reduced the fixed a-SiNx charge from $9x10^{11}cm^{-2}$ to $1x10^{11}cm^{-2}$ suggesting that bulk defects (DBs) in the a-Si layer contribute a negative charge. $D_{it}(E)$ distributions for all of our stack samples measured from conductance techniques (C vs V and G_p/ω vs ω) are shown as open symbols in Figure 3.6b. $D_{it}(E)$ increases dramatically toward the conduction band edge, exhibiting an exponential tail and an approximately constant distribution near the mid-gap. The insertion of 2nm thick a-Si layer in between a-SiNx and c-Si greatly decreases the interface defect near mid-gap from $1x10^{12}eV^{-1}cm^{-2}$ to $5x10^{10}eV^{-1}cm^{-2}$.

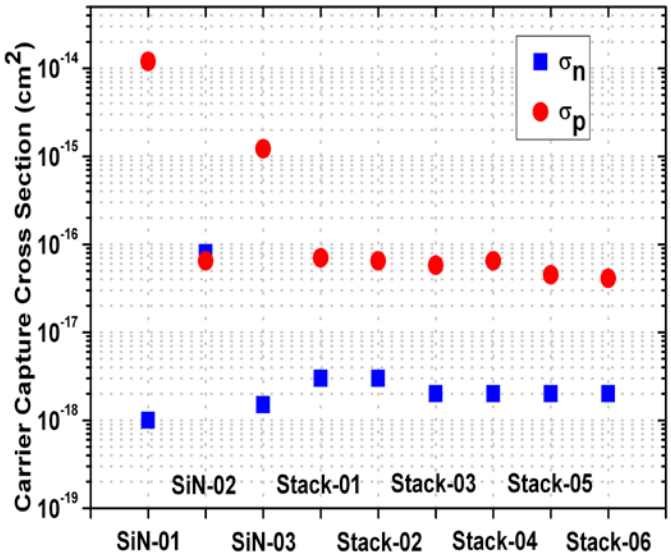


Figure 3.7. Electron and hole capture cross sections determined from modeling of different surface passivations of c-Si wafers. Samples SiN-01 to -03 have single layer a-SiNx insulator with different SiN composition and samples Stack 01 to 06 have a-SiNx/a-Si stack insulators with varying a-Si thickness and SiN properties.

Applying a model developed to fit the measured injection-dependent lifetime allows extracting carrier capture cross sections σ_n and σ_p of the interface defects (Figure 3.7). For a-SiNx/c-Si interface, the ratios of capture cross sections are dependent on a-SiNx layer growth conditions. The physical nature of these different defect types was believed to be extrinsic silicon DBs with different back bond configurations. For stack/c-Si interface, the defect state (σ_p=6.5x10^{-17}cm^{-2}, σ_p/σ_n~30) is very different from that at a-SiNx/c-Si interface and independent of a-Si thickness and a-SiNx layer growth condition, implying that the properties of these interface defect states are basically determined by a-Si buffer. The higher effective lifetime yielded by stack passivation can be attributed to the significantly lowered defect state density at stack/c-Si interface and its lowered capturing capability for minority carriers σ_p. The parameters resulting from this unique characterization procedure provide inputs to the Sentaurus modeling of FHJ and IBC-HJ devices described in several other tasks and publications.

Task 4. Laser processing for interdigitated back contacts

Subtask 4.1 Develop base contact laser process by firing through the i-p a-Si.

This task involved design and fabrication of a wide range of LFC test structures, developing electrical and structure characterization methods, and preliminary exploration of a wide laser parameter space. While laser firing of Al metal through SiN/SiO_2 to make ohmic contacts to p-Si has been widely reported, laser fired contacts (LFC) on n-Si is much less common. At the beginning of this project, we had investigated firing Al, Ag or Ni (all 500 nm) directly on bare n-type Si wafer. Ag gave the best result with a 7 ns pulse width giving a contact resistance ~20 mOhm-cm^2. The other metals had very high resistance. At the start of this program, we began to

investigate firing the metal through p or i a-Si layers. We could not get any reasonable Ohmic or low resistance contact with Al or Ag when fired through the amorphous layer. So we added a 50 nm Sb layer under the Al or Ag. This showed promise but had adhesion problems. So we added a 5 nm Ti layer under the Sb which greatly enhanced the adhesion. The incorporation of an Sb layer between the top metal (Al or Ag) and the a-Si / Si wafer heterojunction was a critical aspect enabling progress on this task.

Subtasks 4.1 and 4.2 were collaborations between IEC and JPSA. IEC had responsibility to design and fabricate test structures, develop characterization and analysis techniques, provide JPSA with samples for laser process development, and optimize laser processing using a laser tool with limited capability. JPSA, which has a wide range of laser tools available which can be operated in various modes with sophisticated controls, has responsibility to map out a wider parameter space and analyze the laser-solid interaction according to their considerable experience. Table 4.1 compares the sole IEC laser and one of the systems at JPSA for LFC work reported here. During this program, JPSA was renamed IPG Photonics, and so JPSA and IPG are both used to refer to the same team and tool sets.

Table 4.1. Comparison of IEC's sole laser and one of the JPSA lasers used for LFC.

Laser	IEC	JPSA
Pulse Width (ns)	**7**	**150**
Wavelength (nm)	**532**	**1064**
Spot Size (μm)	**~30**	**~60**
Typical Power (W)	**< 1**	**4-5**
Typical Number of Pulses per LFC	**<10000**	**<100**

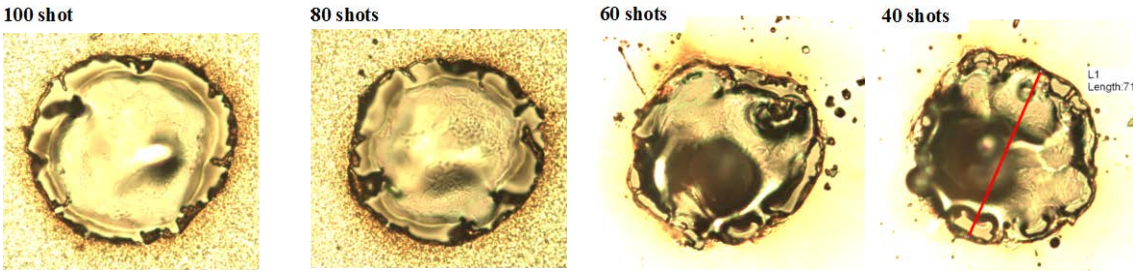
The goal of this subtask was to conduct preliminary investigation of laser processing to form an ohmic contact by driving metal through the i-p a-Si or SiN to contact the n wafer and allow melting/alloying/doping. Laser parameters would include: laser wavelength, pulse duration, energy density, average peak power, number of shots per location, spot size, energy distribution (beam shaping), and machining techniques.

Samples fabricated at IEC and laser processed at JPSA and IEC include structures such as : Ag/ n c-Si/ n a-Si/ Al; Ag-Sb-Ti/ p a-Si/ i a-Si/ n c-Si/ n a-Si / Al; Al-Sb-Ti/ p a-Si/ i a-Si/ n c-Si/ n a-Si; Al-Sb-Ti/ SiNx/ n c-Si/ n a-Si. Some samples have Al or Al / n a-Si as the ohmic back contact to the n-Si wafer. Initial samples all had Ag as the outer layer since it is supposed a better ohmic contact to n-type Si and Al is known as a p-type dopant. However it was eventually found that the high reflection from Ag was problematic, leading to a narrow process window for lasing, and the counter-doping of Al was not a problem, thus most of our later samples and all IBC cells had Al as the thicker current carrying metal.

Optimization of process parameters to achieve typical LFC topology was performed with two different 1064 nm laser sources at JPSA having pulse widths of approximately 20 ns or 150 ns. The use of short ns pulses typically results in ablation with crater formation due to pulses with high peak intensity. Tests with this type of laser source were conducted such that the effects of ablation were minimized by generating melting effects through accumulation of heat from a large number of shots at low power levels (slightly below the damage threshold).

A different 1064 nm laser source generating long pulses of approximately 150 ns was used to investigate the capability of creating LFC topology more typical of what is reported in the literature. Studies using MC0960-02 (Ag strips/i a-Si/ n c-Si/n a-Si/Al) and MC0815-14 (Ag strips/n c-Si/n a-Si/Al) indicate that the laser material interaction is different between long or short pulsed lasers. Tests were done by a) focusing the laser beam on the sample surface without any beam shaping (Figure 4.1) and b) using a shaped beam/imaging technique (Figure 4.2). Results indicate that a longer pulse duration with a relative low number of shots (below 100 shots), leads to a desired topology with melting of the top metal layer and hydrodynamic effects leading to alloying. Unlike the short pulse tests the exposed areas have a smoother aspect and indicate that ablation effects leading to crater formation are minimized. The electrical characteristics were tested before and after the LFC formation using 4-wire JV tests. High resistance values ranging from 2700 to 7300 Ohms were measured prior to laserprocessing and low resistance values ranging from 6 to 13.5 Ohms were obtained after processing, indicating that LFC contacts were formed upon laser exposure.

In order to get a better control of the size and shape of the contacts, samples were lased with a 50 microns diameter circular beam with a flat top intensity profile generated through an imaging technique. By using this approach, the control over the shape of the exposed area as well as the topology can be improved.



MC0815-14 **MC0960-02**

Figure 4.1. Results obtained using a longer laser pulse (~ 150 ns) in two different samples (see text for description) without beam shaping

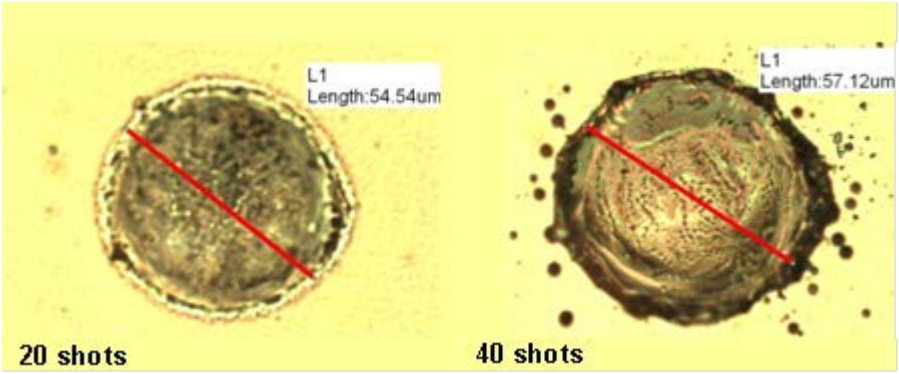
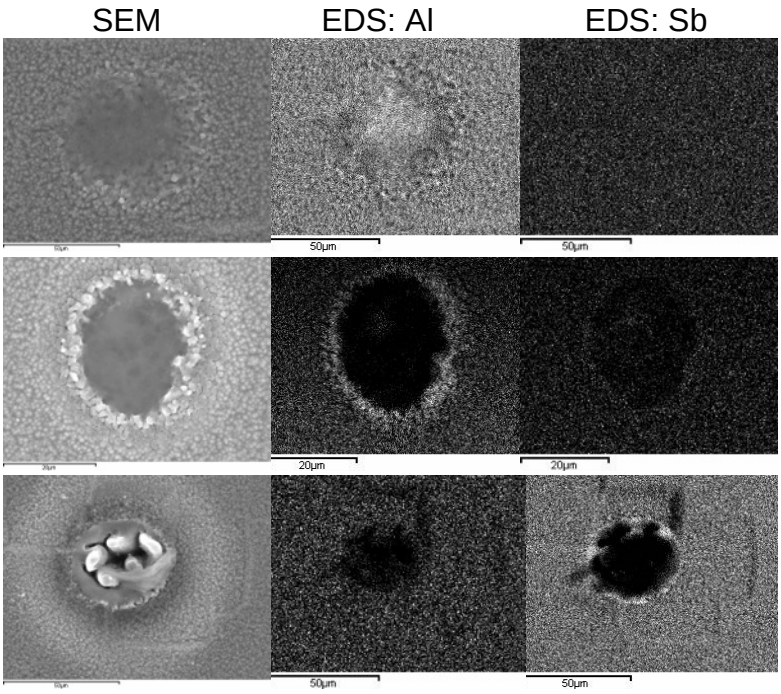


Figure 4.2. Circular spots generated with 20 and 40 shots at optimum laser fluence with 150 ns laser with beam shaping.

We developed visual criteria to categorize under-fired, over-fired, and properly fired contacts. Figure 4.3 shows the SEM image and the composition map for Al and Sb for three qualitatively different conditions. Continuity of Al at the edge of the spot and appearance of Sb in the middle of the spot (doping of the Si) is critical to achieving low resistance.



Under-Fired: Al not completely ablated, Sb intact; no or minimal increased conductance;

Properly-fired: Al ablated, highest increase in conductance;

Over-fired: Noticeable damage to bulk silicon.

Figure 4.3. SEM image and energy dispersive spectroscopy (EDS) map for Al and Sb for three types of contacts. Top: under-fired, middle: properly fired, bottom: over-fired.

More precise values of Rc can be obtained when Rc is small from transfer length method (TLM) measurements using lateral current flow through a series of identically lased contact pads. Figure 4.2 shows the TLM structure and sample. The intercept of plotting Rs vs pad distance is 2Rc as is well known for semiconductor contact measurements.

Test structures were designed and fabricated to evaluate LFC contact resistance (Rc) with vertical current flow, as will occur in the IBC, and with lateral current flow, as in traditional transfer length method (TLM). Figure 4.4 shows the side view and top photo of a simple structure used for both vertical measurements. After lasing the individual top contact strips, measurements are made in the vertical direction between the LFC and the rear ohmic contact. This resistance includes contact and spreading resistance (Rsp) in the Si wafer. Rc is extracted from the measured total resistance according to these relations:

$$R_{LFC} = R_c + R_s + R_{bc}$$

$$R_s = \frac{\rho_b}{2\pi r} \tan^{-1} \frac{2t}{r}$$

$$\rho_c = \pi r^2 \times R_c$$

where Rs is the spreading resistance in the bulk wafer and Rbc is the back contact resistance assumed to be 0. Uncertainty results from this structure when Rc is small and small variations in bulk wafer resistivity give large variation in Rc. However this structure was very useful for rapid screening of a large matrix of lasing and metal or dielectric conditions since we could evaluate 12 different conditions per sample.

More precise values of Rc can be obtained when Rc is small from transfer length method (TLM) measurements using lateral current flow through a series of identically lased contact pads. Figure 4.5 shows the TLM structure and sample. The intercept of plotting Rs vs pad distance is 2Rc as is well known for semiconductor contact measurements.

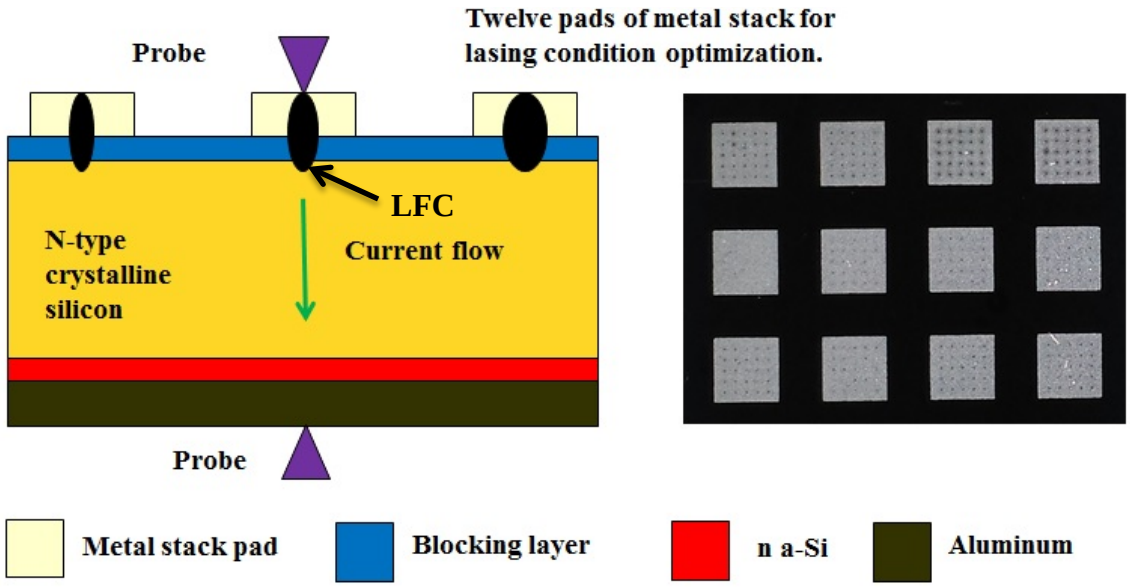


Figure 4.4. Left: Cross section of vertical test structure and probe arrangement for obtaining Rc. Current flow through the wafer is subject to spreading resistance correction. Right: Photo of sample with 12 pads (3x3 mm) each with 5x5 array of LFC having different lasing conditions, hence 12 different conditions could be explored per sample.

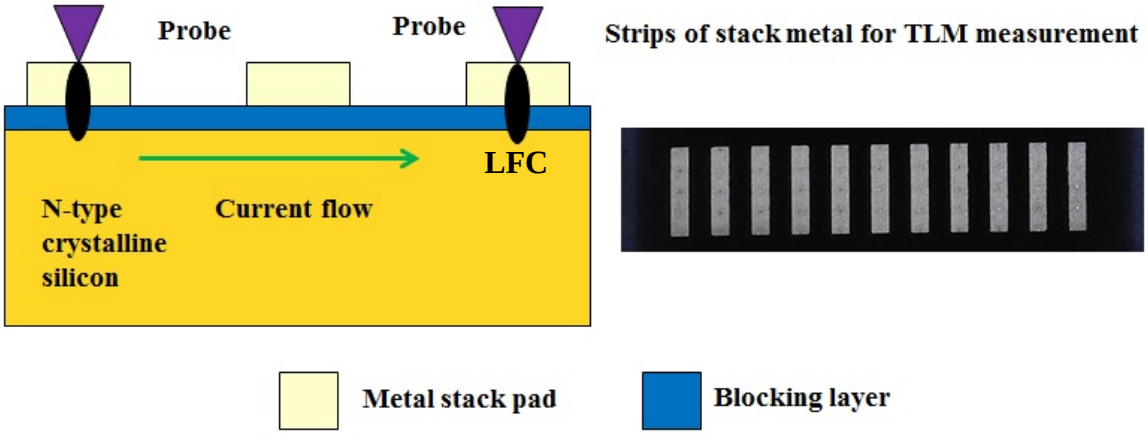


Figure 4.5. Left: Cross section of horizontal test structure and probe arrangement for obtaining Rc from TLM measurements. Current flow through the wafer is subject to spreading resistance correction. Right: Photo of sample with 11 pads each with 5 LFC shots having identical lasing conditions.

Figure 4.6a (left) shows the ohmic behavior from the vertical measurements for a sample with Al (500 nm) /Sb (50 nm)/Ti (5 nm) stack deposited on a p-i a-Si / n c-Si heterojunction. Clearly the LFC has shorted out the junction. The average resistance for 5 LFC spots of 76±3 Ohms with 25 µm diameter can be reduced to Rc= 0.24±0.08

mΩcm^2 for each spo . Figure 4.6b (right) shows the TLM analysis from a line of contact pads on this same sample lased with same conditions. The intercept of 157±2 Ω represents twice the resistance of 5 LFC contacts (since the 2 contacts are in series) yielding Rc=1.9 mΩcm^2.

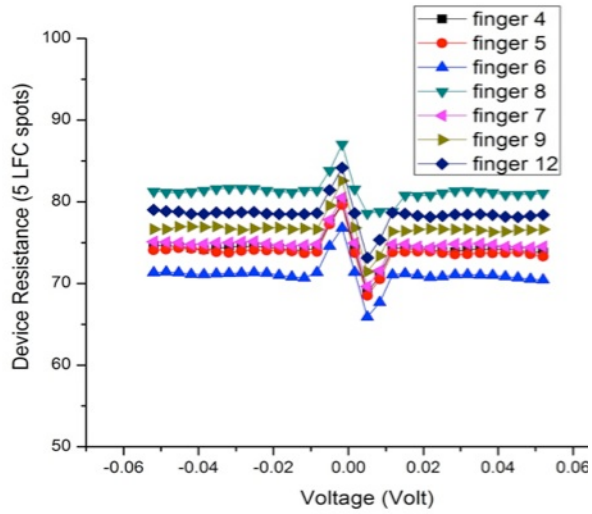


Figure 4.6a. Vertical resistance-voltage curves for 7 fingers with same lasing conditions. Metal Al/Sb/Ti stack was fired through a-Si p-i layers with only 5 spots per finger. Average resistance is 76±3 Ohm. Discontinuity around 0V due to resolution limits of I measurement.

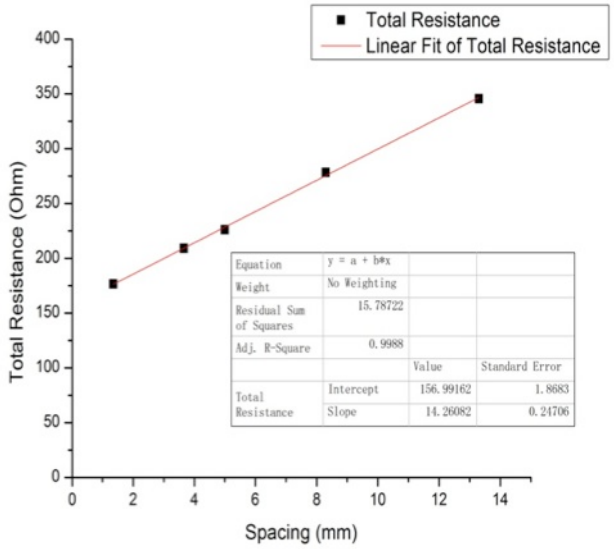


Figure 4.6b. Lateral TLM analysis from same sample after etching bottom Al contact measured across pairs of contacts on the top surface. The intercept is 157 Ohms which corresponds to Rc=1.9 mΩcm^2.

Identifying the need for Sb doping from the metal stack and demonstrating its critical role in obtaining a low contact resistance on n-type Si is one of the key achievements of this project. Figure 4.7 shows the JV curves for vertical test structures before and after LFC for metal stacks with and without Sb. Without Sb, the resistance remains extremely high after LFC, > 1E4Ohms, for both types of dielectric. With Sb, a linear JV with low resistance results. Note that Figure 4.7b shows that the Sb effectively shorts out the HJ formed with an a-Si p-layer.

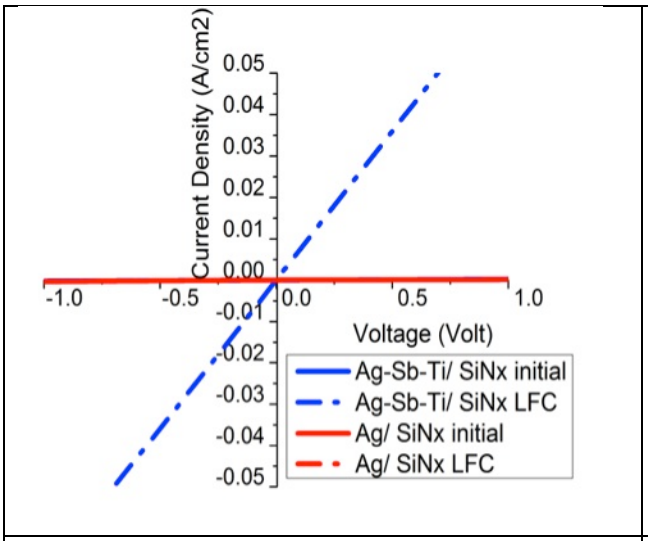


Figure 4.7a JV curve before and after LFC for Ag and Ag-Sb-Ti stack on SiN insulator. Measured on vertical test structure (Figure 4.4)

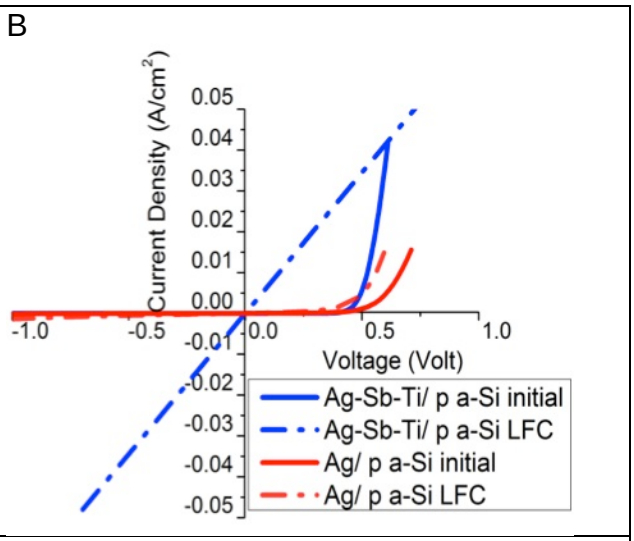


Figure 4.7b JV curve before and after LFC for Ag and Ag-Sb-Ti stack on a-Si p-layer. Measured on vertical test structure (Figure 4.4)

Having identified the critical role of Sb and the advantage of using Al compared to Ag, it was necessary to refine the LFC process development on this new metal stack with different dielectric layers underneath. Figure 4.8 shows optical microscope images of the 1064 nm laser fired spots for 10 kHz repetition rate with pulse duration around 150 ns at powers from 0.5 to 5.0 W. The metal stack starts melting at 0.5W, and is fully melted at 1.0W. The SiNx/p a-Si layers is removed at 1.5W, and the n c-Si layer is ablated with >1.5W laser pulses. The c-Si layer becomes rough when power is over 4.0W.

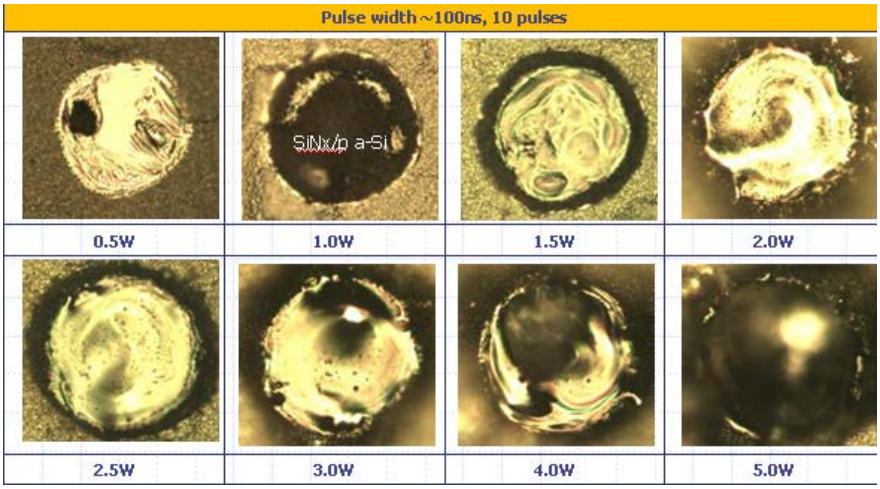


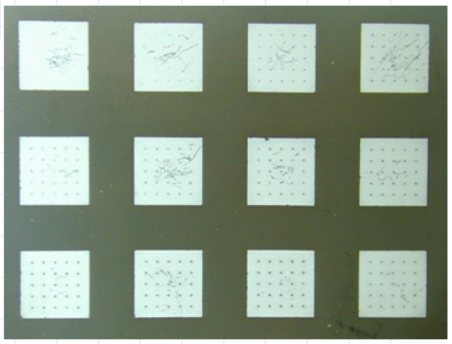
Figure 4.8: Ablation testing with different powers at 10kHz on MC 1215 - 01

A similar range of laser powers were used at IPG on sample MC1215-05 having Al/Sb-Ti stack on a-SiNx. Figure 4.9 shows the pads obtained with the new mask designed for this task, the JV curves, and the resistance R_{LFC} . Each pad had a 5x5 array of laser fired spots. Before LFC, the resistances were ~ 10 M Ohm. After LFC, the JV

characteristics are all linear and Ohmic with resistances < 10 Ohms with optimum lasing power of 2.8-3.2 W. Values of R_C were calculated for these conditions to be <3 mΩcm^2 assuming a conservative nominal wafer resistivity of 1 ohm-cm.

Table 4.2 compares Rc from vertical and TLM structures. Regardless of measurement geometry, data in this table confirms that *we have achieved the milestone of R_C< 3 mOhm-cm^2* on several combinations of metal and dielectric structures.

Pad	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12
R (MΩ)	10	6.7	10	10	10	6.7	0.07	6.7	6.7	10	10	10
LFC Condition	0.5W, 10kHz	1.0W, 10kHz	1.5W, 10kHz	2.0W, 10kHz	2.5W, 10kHz	3.0W, 10kHz	3.2W, 10kHz	3.4W, 10kHz	3.6W, 10kHz	3.8W, 10kHz	4.0W, 10kHz	2.8W, 10kHz
R_{LFC}(Ω)	1066	10.31	7.78	6.45	6.42	5.65	5.75	6.10	7.08	7.26	7.25	5.64



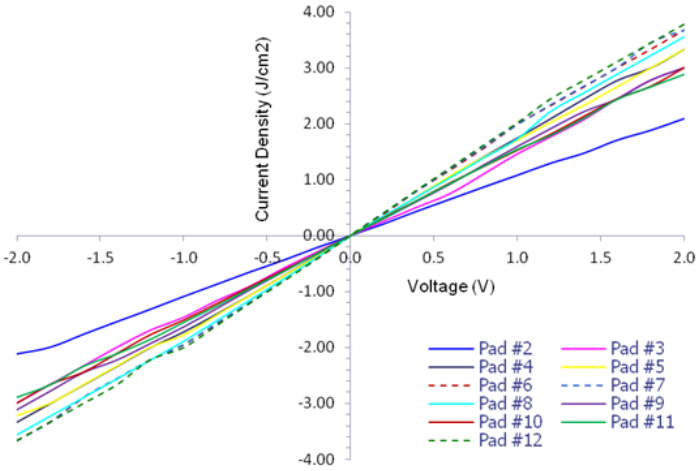


Figure 4.9: JV curve on MC1215-05 without a-Si p-layer for various test pads having different laser power. R_{LFC} of pads 6, 7 and 12 is <6 ohm with lasing condition 2.8-3.2 W power, 10 kHz rep. rate, 10 pulses per spot.

Table 4.2. Comparison of R_C from vertical or horizontal test structures for various combinations of metal and dielectric stacks. Lasing at IPG or IEC. NA means no samples available.

Structure	Rc from IEC Vertical ($m\Omega cm^2$)	Rc from IPG Vertical ($m\Omega cm^2$)	Rc from IEC TLM ($m\Omega cm^2$)	Rc from IPG TLM ($m\Omega cm^2$)
Ag-Sb-Ti/ p a-Si/ i a-Si/ pol n c-Si/ n a-Si/ Al	<1.0	<3.3	5.0	NA
Al-Sb-Ti/ p a-Si/ i a-Si/ pol n c-Si/ n a-Si/ Al	<1.1	<3.3	NA	NA
Al-Sb-Ti/ p a-Si/ i a-Si/ text n c-Si/ n a-Si/ Al	<0.3	NA	1.9	NA
Al-Sb-Ti/ SiNx/ text n c-Si/ n a-Si/ Al	<0.7	<3	7.1	12.5

Front SHJ solar cells were processed with rear LFC to evaluate electrical properties after LFC processing at either IEC or IPG. Run MC1221 and MC1226 had slightly different rear dielectric stacks as shown. Of interest in Table 4.3 is the reasonably high FF (~73%) on all three pieces confirming that the LFC made a low resistance ohmic contact. MC1226 had the highest efficiency for a LFC back contact so far (15.2%). These initial results for unoptimized LFC show great promise for one of the key concepts of the proposed IBC design, namely the ability to create an Ohmic contact by firing through a blocking junction.

Table 4.3 Device performance and lasing parameters for front SHJ cells with rear LFC. All had Al-Sb-Ti metal stack.

parameter	MC1221-01-04	MC1221-02-03	MC1226-02-03
LFC location	IPG	IEC	IEC
Dielectric layers	a-SiN/a-Si i	a-SiN/a-Si i	a-SiN/a-Si n /a-Si i
Initial lifetime (us)	130	110	100
Implied Voc (mV)	644	637	630
LFC area fraction (%)	0.75	0.35	0.3
Actual Voc (mV)	609	624	639
Jsc (mA/cm2)	31.6	32.4	33.2
FF (%)	73	72	72
Roc (Ohm*cm2)	2.4	2.7	2.7
Eff (%)	14.0	14.4	15.2

Subtask 4.2 Laser isolation of base and emitter contacts

The goal of this subtask is to develop the capability to cleanly isolate two interdigitated contacts with minimal underlying damage to the Si and to evaluate lateral shunt resistance and compare to existing IBC-SHJ. There was no baseline. The subtask interim goal is to obtain laser process repeatability regarding heat affected zone/debris field and material removal depth within nominal +- 20%. The overall goal subtask goal is to obtain shunt resistance >1 KOhm-cm^2 and SRV<100 cm/s from test structures.

Samples processed at IEC and jointly processed with JPSA for isolation studies include: Ag/ n c-Si/ n a-Si/ Al; Al/ p a-Si/ i a-Si/ n c-Si/ n a-Si/ Al; Ag-Sb-Ti/ p a-Si/ i a-Si/ n c-Si/ n a-Si; Al-Sb-Ti/ p a-Si/ i a-Si/ n c-Si/ n a-Si; bare wafer.

Past experience at JPSA indicated very short pulse (<10 ps) lasers are well suited for ablation with minimal damage to underlying surfaces. Several coupons with different stack structures were processed with various conditions using a 515 nm 10 picosecond pulse-width disk laser, with average power of 30W. For Al/p a-Si/i a-Si/n structures (Type 1 samples), the goal was to achieve isolation on the metal fingers with as little damage on the wafer as possible. For bare silicon wafers (textured and polished, Type 2 samples), the goal was to generate trenches/isolation patterns on the bare wafer for further process development, before any passivation or metallization. The target was to make a trench less than 10µm deep, around 5 to 40 µm wide with the wall as vertical as possible. This aspect ratio might allow finger isolation using a single metal layer. There would be no risk of damage to the passivating a-Si since it would be deposited after the lasing.

In order to improve the removal selectivity and the edge definition of the isolation lines the beam was conditioned to achieve a flat top intensity profile vs. a focused beam. The variation of the scribing depth and the shunt resistance (shown in Figure 4.10) with the laser fluence was determined using Type 1 stack structures. The fluence required for complete isolation (saturation >10K) depended on the scan speed and line width.

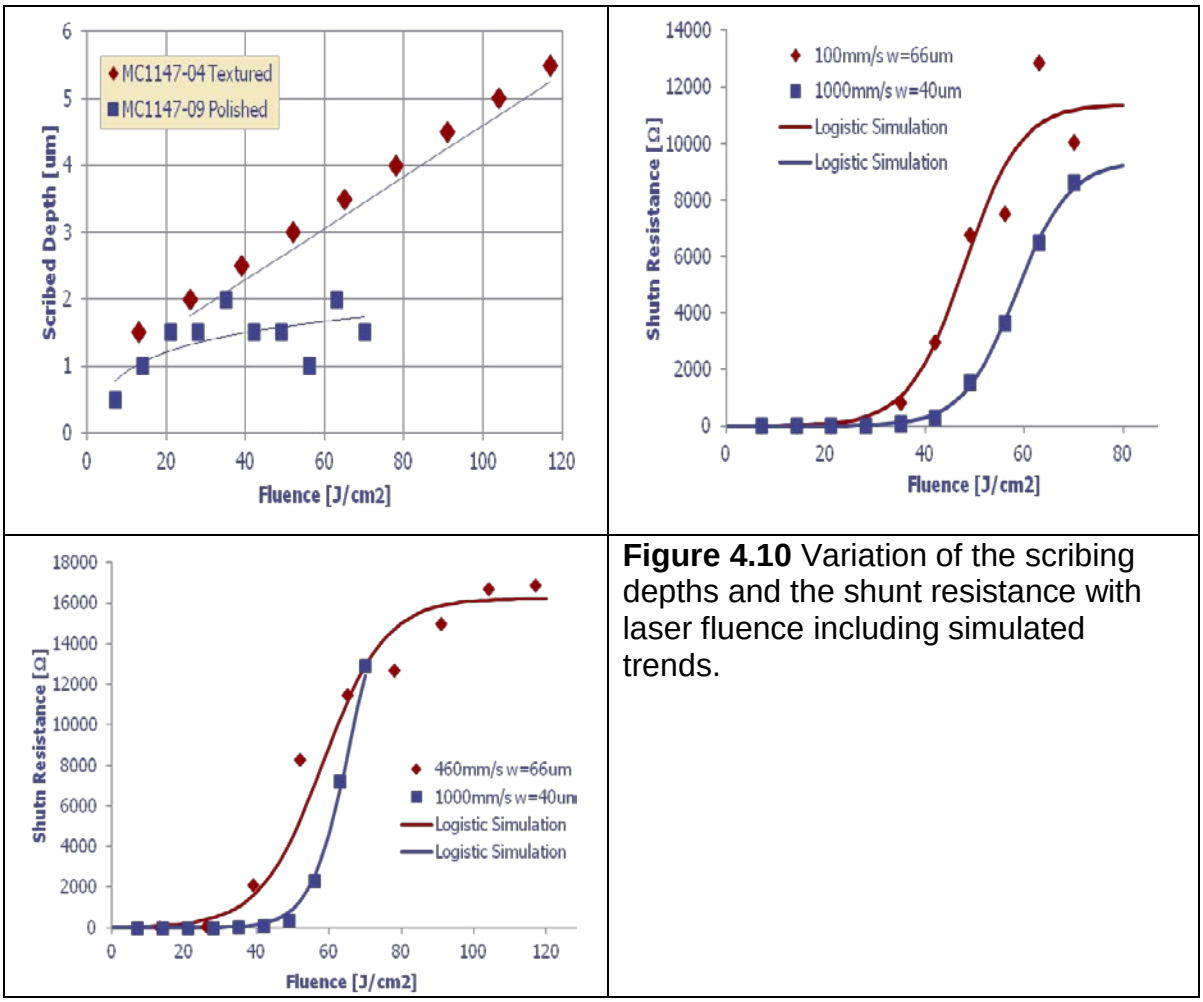


Figure 4.10 Variation of the scribing depths and the shunt resistance with laser fluence including simulated trends.

To compare the lateral shunt resistance after isolation, we normalize the values by the length of the isolation scribe which was 8 mm for JPSA and 23 mm for IEC. For the textured wafer isolated at JPSA using the ps laser, the measured maximum resistance was 2.1 kΩ/mm and 1.6 kΩ/mm for 66μm and 40μm wide line, respectively. The maximum resistance for the polished sample was 1.6 kΩ/mm and 1.1 kΩ/mm for 66μm and 40μm wide line respectively. At IEC, resistance was 1.1 kΩ/mm with a 25 μm beam. Thus, there appears to be an inverse relation between beam width and shunt resistance.

The quality of the isolation lines with good edge definition and minimal heat affected zone is shown in Figure 4.11 for the Type I samples.

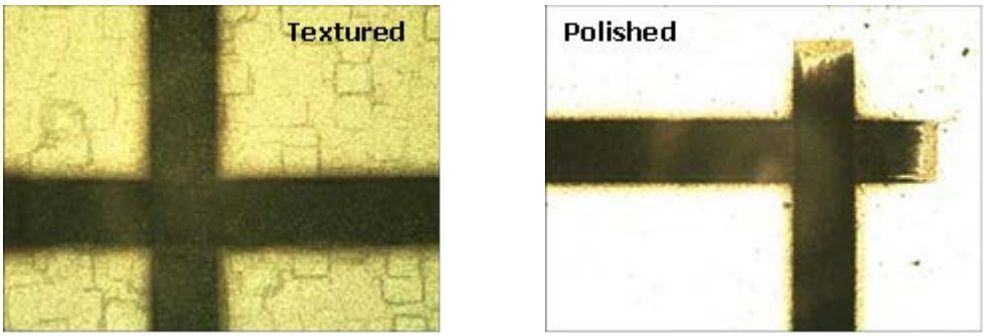


Figure 4.11. Typical isolation quality achieved using a conditioned (flat top intensity profile) beam to ablate the Al.

Successful laser patterning with sharp edges and no HAZ was also performed on the textured or polished (Type II) bare silicon wafers for future metallization steps. Pictures below (Figure 4.12) show the edge quality achieved by patterning the wafers with an optimized flat top beam at an effective speed of 1 m/sec.

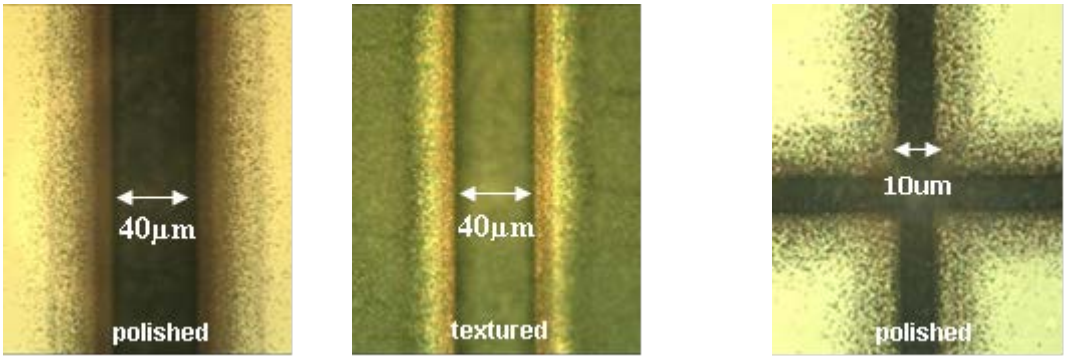


Figure 4.12. Patterning trenches on polished and textured wafers

The use of an imaging beam allows for an easy adjustment of the trench width down to 10 microns wide with identical exposure across the trench.

High resistance has been achieved using ps lasing to ablate and isolate metal contacts. The use of an ultra short picosecond laser allowed for isolation to be achieved. An imaging technique allows for better process control than a standard focusing technique

Another option for laser isolation which avoids laser ablation of the passivation and subsequent lifetime degradation was proposed and first realized at IEC as shown in figure 4.13. It is a laser assisted etching isolation called “laser+chemical etching”. Photoresist (PR) was applied on top of the metal stack and the UV laser was used to remove it. Then the metal in the opening was chemically etched while the remaining PR was used as an etching resistant layer. The transition from Al to the more relevant Al-Sb-Ti or Sb-Ti-Ag has proved to be challenging because of the need for selective etchants depending on which metal was on top. IPG evaluated various lasing

conditions using two pulsed lasers: 10 nsec at 266 nm and 10 psec at 515 nm. IEC investigated several different metal stacks and etchants using photoresist (PR) as the etch resistant sacrificial coating. Figure 4.14 shows an optical image of the laser isolated surface of a PR/metal stack sample. EDS mapping confirmed that the PR is removed in the laser scribed area.

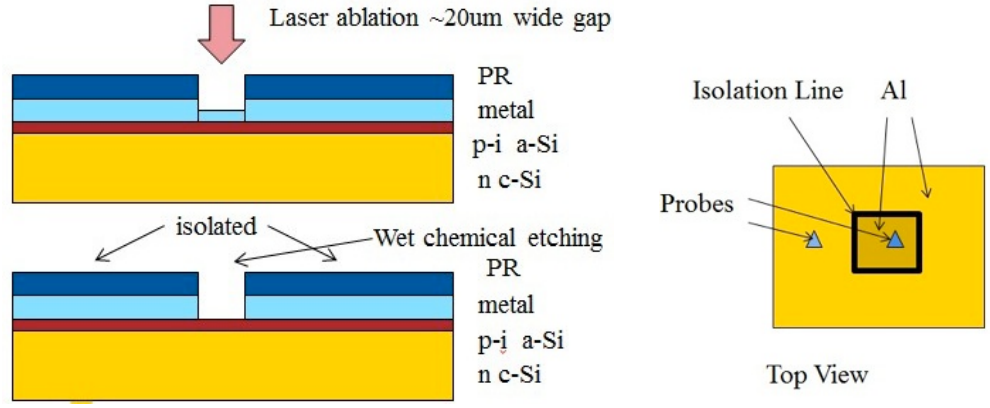


Figure 4.13. (Left) Diagram showing vertical structure during laser-guided chemical isolation. (Right) Horizontal layout for electrical test.

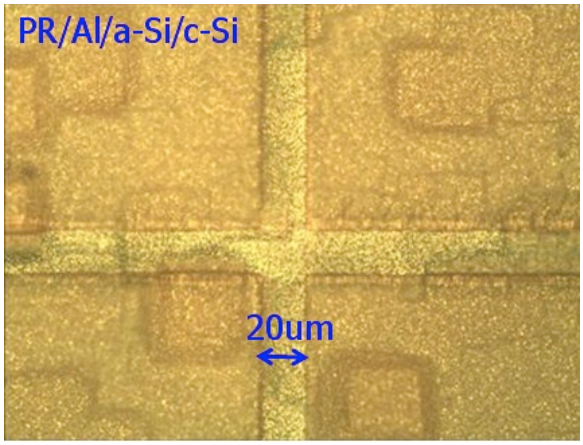


Figure 4.14 : Optical image of laser ablated PR on MC1268-04, Total energy dose 5 J/cm2, 0.25 J/cm2 single pulse fluence , 100 kHz, 20x20 microns beam, 0.1 W, 100 mm/sec, 95% overlap, 20 pulses per location.

It is common to express shunt resistance in units of kOhm-cm^2 where the area is the horizontal area of the device. However, in the IBC application, a more meaningful parameter is the linear shunt resistance in kOhm/mm of isolation. After chemical etching at IEC, results on several samples proved that the 2 step laser-chemical isolation was successful: for an isolation area of 0.1 cm^2 a shunt resistance of 2.3*10^4 Ω cm^2 or 1.6*10^4 Ω per mm isolation line length was achieved. Clearly this exceeds the milestone goal of > 1 KOhm-cm^2.

Subsequent measurements of lifetime by QSSPC after etching away the metal, or by photoluminescence mapping (Task 8) confirms that there is no damage to the underlying passivation layers. The lasing damage is confined to the sacrificial photoresist and a thin region of the metal. With the laser+chemical etch approach, the passivation remains intact, in contrast to the direct laser isolation.

The use of etch resistant sacrificial coating eliminates the HAZ/DF in underlying a-Si/c-Si surfaces, since the laser beam does not penetrate entirely the metal layer and debris is removed when the PR is stripped. An alternate approach for reduction of HAZ/DF for the direct laser isolation without the sacrificial layer has also been developed by IPG using an appropriate beam shaper. With this beam imaging technique the debris field was limited to well within 20 % of the spot diameter for various substrates and process condition. For identical samples and process conditions the debris field was repeatable contact to contact. Analysis of the isolation scribes indicates a very repeatable process regarding affected zone/debris field with a (max-min) width variation at less than 5% of average isolation width.

Task 5. Fabricate IBC-SHJ using laser fired contact with efficiency better than today's baseline

Goal: Produce a IBC-SHJ device with laser fired contact having efficiency >15% and area > 1 cm2 (Phase 1 go/no-go metric)

Results: In c-Si/a-Si:H heterojunction solar cells, the junction formation and its properties are extremely sensitive to the surface cleanliness and interface qualities between different semiconductors (interfaces of c-Si/passivating i.a-Si:H layer, passivating i.a-Si:H layer/doped a-Si:H layers and doped a-Si:H layers/metal contacts). All IBC cells require an interdigitated pattern with alternating regions of doped layers and their metal contacts that are formed using multiple lithography/masking, alignment, etching and/or deposition steps. Process induced damage reduces the surface passivation and carrier transport, leading to low V_{OC}, and FF, respectively. We have simulated the impact on Voc and FF of interface defects at the p/i, n/i and gap regions using the model described above and elsewhere [35]. These results confirm the importance of minimizing Dit not only under the emitter p-strip but also in the gap between the p and n strips. Several other observations confirmed to us that the back contact patterning was the source of our low efficiencies. Prior to any patterning, the double side passivated wafers typically have high effective lifetime and implied Voc, even afer the first doped layer deposition. This indicates standard Si cleaning and a-Si/a-SiN deposition were of high quality. But visual inspection of the p and n gap openings after photolithography showed evidence of incomplete photoresist (PR) removal in the large texture pits on the surface (such texture features can be seen in figures 4.4 and 4.6 and are on the wafers as-received). LBIC images of competed cells consistently show poor collection under the n-strip but not the p-strip. And there was indirect evidence that etching the a-SiN under the p and n strips was too aggressive, leading to unpassivated or even bare Si in the gap between p and n strips. Preliminary investigations into the sources and solutions for removing residue and improving the interface quality have been published[36].

During this project we developed 3 process flows for the IBC-SHJ cells. The main difference between them is in the patterning and passivation of the p and n heterojunction strips on the rear of the cell. Two of them are identical except for formation of the rear n-contact: one has a standard a-Si i/n heterojunction and the other

is a LFC. They are described more completely elsewhere[37]. Here we focus on the baseline two step photolithography (2-PL) process. The cross section of a IBC-SHJ cell as fabricated at IEC is shown in Figure 5.1 and Table 5.1 gives the process steps for our baseline IBC-SHJ cell using 2 photolithography steps. It can affect both the i/p and i/n interface quality since the thin a-Si passivation in both is exposed to photoresist (PR) and chemical processing. Two step photolithography with laser fired base contact (2-PL-LFC) avoids the n-type a-Si:H deposition but can affect i/p a-Si:H interface.

We have invested significant effort in process optimization, repeatability, and off-line studies using various test structures and front SHJ devices. We quickly came to focus on the patterning and etching of the p and n strip windows and how it was influenced by the wafer surface texture. Repeatability had been an issue due to poor control of the interaction between surface texture and patterning and due to materials compatibility limiting the process window. For example, the 2-PL process has potential contamination at the i/p and i/n a-Si:H interfaces, since the photoresist was applied at both interfaces and subsequent doped a-Si:H layers were deposited in the gap between photoresist at 175°C in PECVD. The photoresist material in such thermal and plasma environment can out-gas impurities to contaminate the interface and doped a-Si:H films. Contamination or damage at the i/doped a-Si:H layer interface and/or doped a-Si:H layers will have a severe impact on the solar cell FF. We consistently made devices from several different runs with ~14% with low FF as the primary weakness. By integrating several of the process improvements, **we recently achieved the 15% target for an IBC cell having a LFC with area 2.5 cm2.**

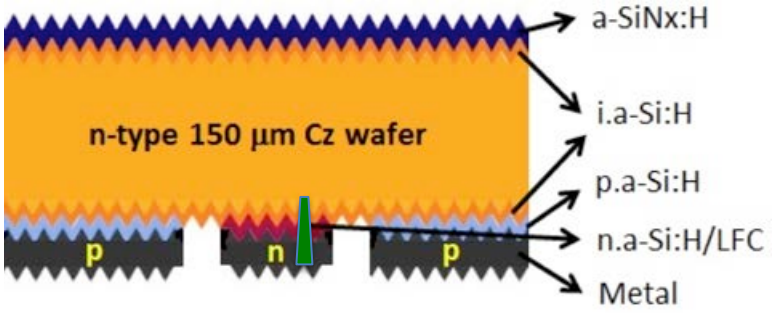


Figure 5.1 The cross section of a IBC-SHJ cell as fabricated at IEC. Table 5.1 gives the process steps for our baseline IBC-SHJ cell using 2 photolithography steps. The optional LFC on the n-strip is indicated by the green cone.

Table 5.1 Process flow for baseline 2-PL and 2-PL-LFC process. Optional steps in red were investigated to improve the yield and reproducibility.

Baseline IBC-SHJ Process: 2-photolithography steps

1. Clean commercial textured wafer (organic/TMAH smoothing/piranha/HF) followed by TMAH texture
2. Passivate surfaces (front and back a-Si i-layer)
3. Front AR stack (PECVD a-SiN/a-SiC)
4. Photolithography: open emitter p-strip
   - Spin coating
   - Soft bake
   - Exposure (double time for textured Si surface)
   - Development
   - Rinse
   - Option: UV exposure or hardbake
5. Chemical Etching (10% HF, 1 minute)
6. Deposit PECVD a-Si p-layer (emitter) at 175°C
7. E-Beam p-layer Al contacts
8. Lift off
   - Option: O_2 plasma surface treatment
9. Photolithography: n-strip
   - Spin coating
   - Soft bake
   - Exposure
   - Development
   - Rinse
   - Option: UV exposure or hardbake
10. Chemical Etching (10% HF, 1 minute)
11. Deposit PECVD a-Si n-layer at 175°C (2-PL only)
12. E-beam n-layer metal contacts (either Al or Al/Sb/Ti)
13. Lift off
14. JV test, anneal, retest; optional LFC optimization

Figure 5.2a shows the initial and post-HT JV curves for baseline 2-PL device having 14.5% efficiency. There is little change in the Voc and Jsc with heat treatment while the FF increases significantly. The initial S-shaped light curve with FF=40% evolves into an acceptable JV curve with FF=67%. QE bias light dependence determined that the source of low Voc after heat treatment was not due to poor front passivation and therefore likely to be the rear. This increase in FF with HT is very similar to our F-SHJ cells. However, the Voc of F-SHJ cells also increases 30-50 mV upon heat treatment. This difference suggests that the IBC cell Voc is limited by a mechanism not occurring in F-SHJ cells such as PR residue or etching damage at the p or n contact strip. Figure 5.2b shows the LBIC image for a cell from this piece. There is low collection over the n-contact. This suggests the loss of Voc and Jsc is likely due to higher recombination at the n-contact. This sort of LBIC image was commonly seen in our IBC-SHJ cells.

We have investigated several new process options to minimize the potential for contamination after the PL step and to maintain good passivation under the n-strip. For

example we tried the following: 1) applied UV exposure for organic removal; 2) used O2 plasma to grow thin oxide followed by HF stripping to remove oxide and contaminants; and 3) hard-baked the PR prior to placing samples in PECVD chamber for a-Si film deposition at 175 or 200°C, which is well above the recommended temperature range for the resist. Efforts to identify and quantify the effect of cleaning and residual photoresist due to the extreme hardbake in the PECVD system were discussed elsewhere[36]. None of these had statistically meaningful effect on the device performance although occasionally they resulted in better performance, as indicated by MC1364-02 seen in figure 5.2 and Table 5.3. The LBIC image confirms that we had good uniformity across the piece except for the difference between the p and n strips. This occasional jump in efficiency suggested we were on the right track but were still limited by an uncontrolled variable which affected each piece individually. This excluded the PECVD deposition. So we turned our focus to the PR thickness and application method , PR exposure time, a-SiN etching and how they were influenced by the Si surface texture. These efforts lead us just recently to replace the previous baseline unpolished wafers with polished wafers which we textured internally using TMAH as described in Task 3. This produced devices with high Voc and Jsc but low FF as shown by MC1366-02 as shown in Table 5.2. A key observation comes from the LBIC scans for this cell seen in Figure 5.3 which indicate very uniform collection between p and n strips. Thus, the internally textured polished wafer had negligible loss in passivation with processing. But the very poor FF suggested we were still not removing all residue. So we switched to the polished wafers with internal TMAH texture to optimize the PR application and exposure for this new texture to eliminate visible pockets of PR and also reduced the time and concentration of the HF etch.

We found that when S-curves and low FF result, applying the LFC helps to improve the FF with only minimal loss in Voc or Jsc. This is confirmed by the LBIC line scan for MC1364-06 in Figure 5.3. It shows much higher collection over the n-layer than any other cells with the same processing and wafer. The LFC establishes a direct ohmic contact between the metal and Si while still allowing the a-Si heterojunction passivation to operate. Therefore we started making all IBC-SHJ cells with the Al/Sb/Ti stack. By integrating the improved patterning, TMAH textured polished wafers, less aggressive SiN etch (HF=2% for 15 sec instead of 10% for 60 sec) and LFC, we obtained device MC1390-06 having 15% efficiency as shown in figure 5.4 and Table 5.2. Note the significant improvement with heat treatment and then with LFC, taking the FF from 26% to 67% with negligible change in Voc or Jsc.

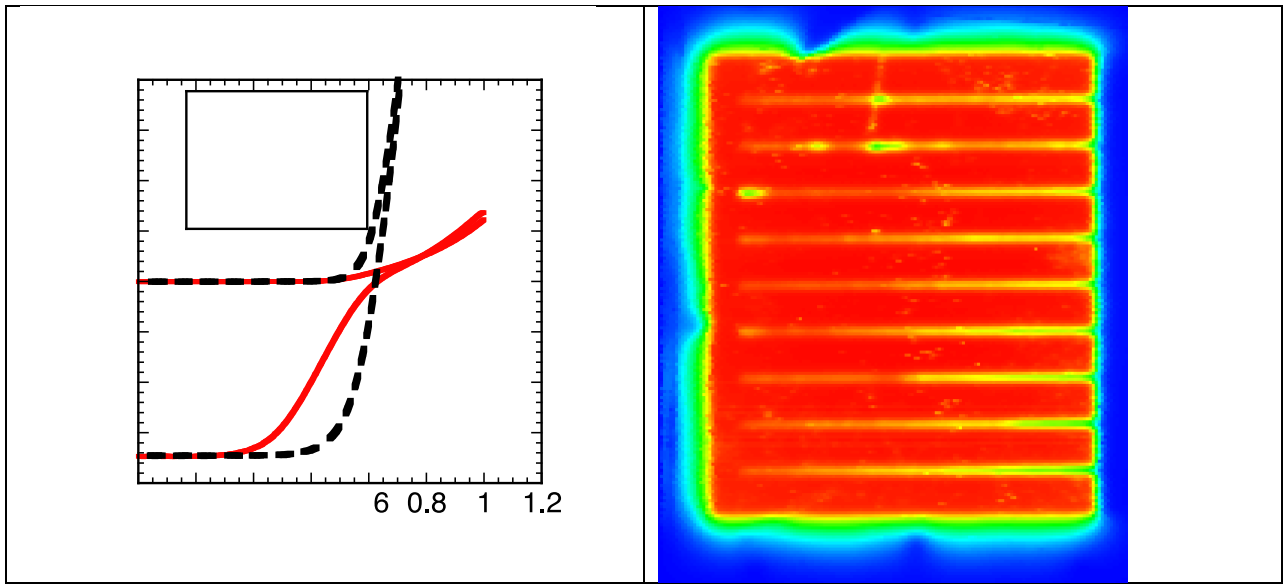


Figure 5.2a) JV curves and performance from MC1364-02 baseline device fabricated on a commercially available textured Cz wafers wafer before and after annealing. b) LBIC response from the device after annealing. Red corresponds high collection over the p-emitter, blue is low response over the n-base contact. Difference in response magnitude between p and n strip is shown in figure 5.3.

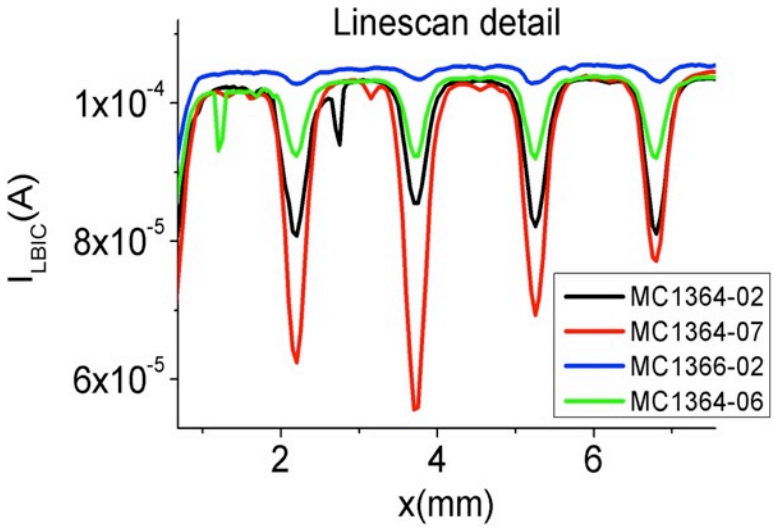


Figure 5.3 LBIC line scans of 4 IBC cells described in Table 5.2. Complete LBIC image for MC1364-02 is shown above in Figure 5.2. The narrow valleys are over the n-strip and wider peaks are over the p-strip.

Table 5.2 JV results for several process variations of IBC-SHJ with or without LFC. Text colors match LBIC scans in Figure 5.3.

Piece	Description	Voc (V)	Jsc (mA/cm^2)	FF (%)	Eff (%)
MC1364-07	Baseline process and wafer	0.63	33	65	13.5
MC1364-02	Baseline wafer, baseline process with PR hard-bake and O2 plasma clean	0.62	35	67	14.5
MC1366-02	Baseline process with polished wafer +TMAH texture	0.69	37	27	6.9
MC1364-06	Baseline process •after HT •after LFC of n-strip	 0.66 0.64	 35 34	 55 62	 12.7 13.6
MC1390-06	Polished wafer with TMAH texture, p and n dep@200°C SiN HF etch=2%, 60 Sec •after HT •after LFC1 •after LFC3	 0.68 0.65 0.65	 35.7 35.1 34.7	 40.1 58.5 67.0	 9.7 13.4 15.0

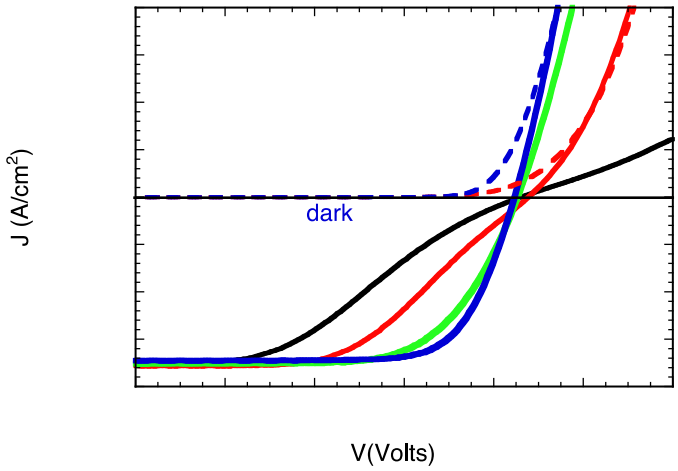


Figure 5.4 Light and dark JV curves for IBC-SHJ MC1390-06 showing the evolution from initial, heat treated (150°C, 2 min), and then after the 1st and 3rd LFC step. Values of FF are shown. Dark JV curves for HT and LFC also shown. After the 3rd LFC, the efficiency was 15.0%.

Finally, having characterized and modeled the electronic structure of the various heterojunction interfaces and the device structure as described in Task 2.2, we used our IBC model[35] to investigate the impact of geometry (characterized as fraction of emitter coverage) and Si wafer properties on the IBC-SHJ performance. Figure 5.5 shows some of the key results of the simulation by comparing the role of emitter coverage on efficiency for 50 um wafer with different bulk lifetime using realistic passivation. This

latter figure indicates that we need bulk lifetimes >200 usec to meet the 20% goal this thin kerfless wafers.

Overall, the 2D simulations show that V_{oc} has a strong dependence on front and back (i)a-Si:H/c-Si interface defect densities in IBC-SHJ solar cells, since the total recombination is limited by the surface passivation quality for high wafer lifetime (FZ wafer) solar cells. The simulations clearly suggest areas for immediate experimental attention to improve performance. An increase of D_{it} in the gap between p- and n-strips decreases all parameters, implying the importance of the gap region passivation in IBC-SHJ solar cells. This is difficult to control in our current 2-step photolithography process. Simulation shows that by either lowering the dangling bond density D_{DB} (deep defects) of (p)a-Si:H emitter or narrowing its band tails (shallow defects), the FF can be improved without losing V_{oc} and J_{sc}, and the sensitivity of FF to the (i)a-Si:H buffer layer band gap can be reduced. The band diagram analysis shows that the FF dependence on both D_{it} and D_{DB} is related to the interface recombination losses under forward bias.

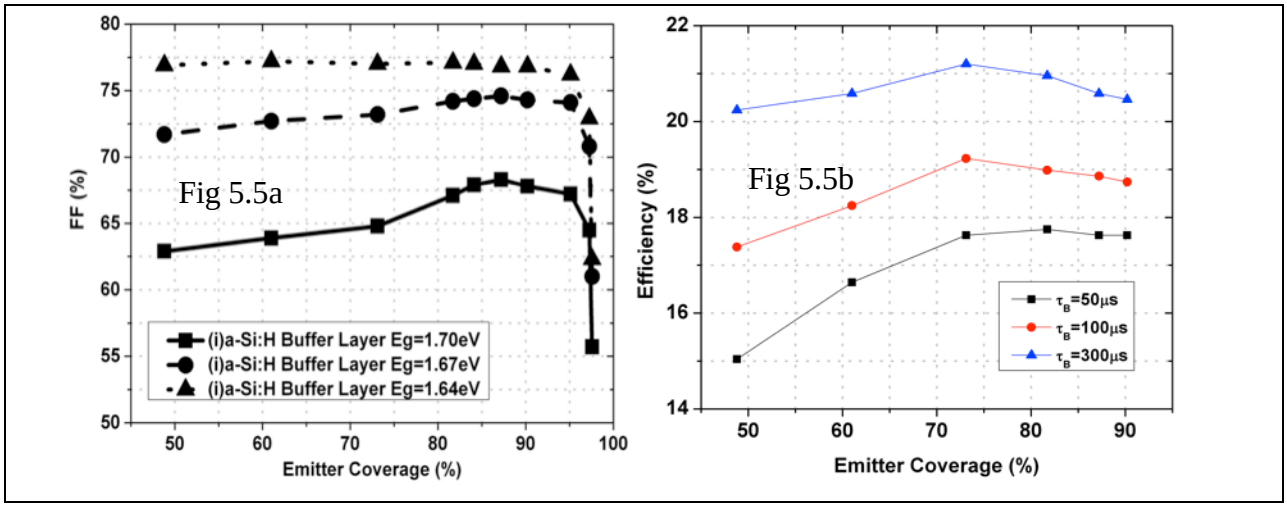


Figure 5.5. Simulated results for IBC-SHJ a) Effect of emitter coverage on IBC-SHJ FF for different buffer bandgaps for with 150 um wafer and 5 msec bulk lifetime using realistic passivation parameters; b) Effect of emitter coverage on efficiency for 50 um wafer with different bulk lifetime using realistic passivation.

Task 6. Optimize a-Si/c-Si heterojunctions

Subtask 6.1 Engineer appropriate emitter / base contacts.

Subtask Goal: Obtain FF>80% on IBC-SHJ cells > 1cm^2 or provide fundamental explanation for FF limit

Results: Simulations using Sentaurus and experimental results from previous work and earlier stages of this contract indicated that both the intrinsic a-Si buffer and p-layer

properties were crucial to obtaining good IBC. We optimized them separately, starting with the buffer layer.

Modeling has shown a lower bandgap (<1.72 eV) and relatively thin (<10 nm) a-Si buffer is needed[38] because of the fundamental a-Si/c-Si valence band offset effects. The buffer layer bandgap can be reduced by increasing the deposition temperature and by increasing the H dilution. However, these methods tend to lead to the formation of nanocrystalline or epitaxial growth with highly defective a-Si bulk quality, which can severely degrade the passivation quality. RF-PECVD films are even more prone to nanocrystallite formation due to reduced ion bombardment. Hence, developing an appropriate and repeatable set of buffer layer conditions, which avoid this nanocrystalline regime, is crucial to the following cell fabrication processes.

A series of symmetric buffer a-Si on c-Si substrate test structures were made to explore a range of options for tuning the bandgap. The underlying logic of why and how we change the conditions was explained in the Task 2. FTIR and VASE were used to characterize the a-Si film's bulk hydrogen bonding, bandgap and thickness. QSSPC was used to evaluate surface passivation quality via effective lifetime. Annealing effects were also investigated. High lifetime (>1000 us as a baseline for good cells) was obtained over a range of conditions, as shown in Table 6.1, and these conditions were later chosen to make into 2.5 cm^2 SHJ cells.

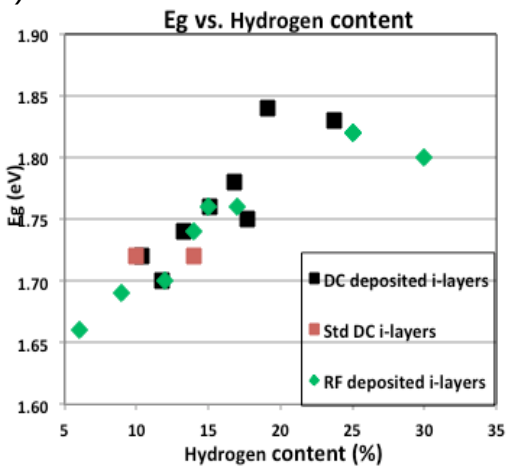
Table 6.1. Combinations of parameters achieving passivated lifetime over 1 ms, all samples were annealed @300°C for 25 mins. Both DC and RF plasma was used.

Power supply (mW/cm2)	Substrate Temp (°C)	H2/SiH4 flow ratio (sccm)	Pressure (torr)	Eg (eV)
50, DC	250	25/10	1.25	1.72
50, DC	200	60/16	1.25	1.75
25, DC	200	40/16	1.25	1.76
50,DC	200	40/16	1.25	1.83
20, RF	225	0/20	0.5	1.69
20, RF	175	80/20	1.25	1.71
20, RF	215	25/10	1.25	1.73
20, RF	175	60/20	1.25	1.75
20, RF	175	20/20	1.25	1.81

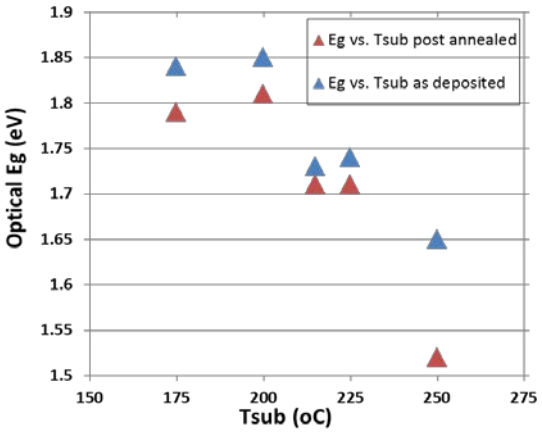
Direct control of buffer layer bandgap through varying the a-Si hydrogen content was demonstrated, as is seen in Figure 6.1a. Similar dependence was obtained for DC and RF films. The decrease in apparent bandgap for hydrogen > 20% is likely due to formation of nanocrystallites in the film. The hydrogen content of thin a-Si films decreases slightly after annealing, hence bandgap was also found to decrease in annealed samples as shown in Figure 6.1b. Figure 6.1(c) shows the changes in effective lifetime after annealing for a series of i.a-Si layers deposited at different temperatures. For the i.a-Si layers grown at >215ºC, the effective lifetime tends to decrease after annealing, suggesting re-crystallization of the film at the a-Si/c-Si interface during annealing. These films were what is widely refered to as 'on the edge'.

Therefore comparing figures 6.1(b) and 6.1(c), it appears that lowest bandgap of i.a-Si layers of ~1.7 eV can be achieved at Tsub~ 215°C without reduction in the passivation quality.

a)



b)



c)

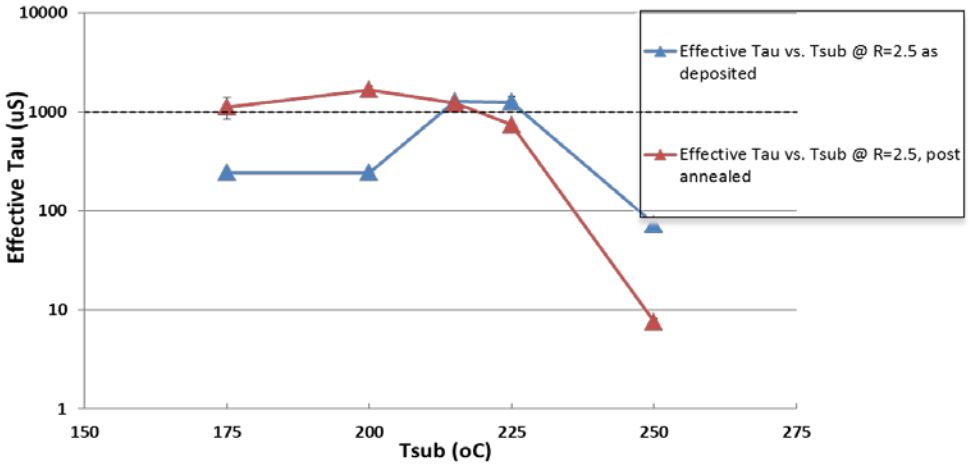


Figure 6.1. (a) Hydrogen content vs. buffer layer bandgap. (b) Decrease in buffer layer bandgap during annealing. (c) Effective lifetime vs. deposition temperature, comparing as-deposited and post-annealed samples. All test structures were prepared with symmetric buffer layer thickness of 9 nm.

A series of front HJ solar cells were fabricated having different i.a-Si layer bandgaps. FF vs the buffer layer bandgap are plotted in figure 6.2. The experimental result shows a large dependence of FF on buffer layer bandgap as suggested from simulation.

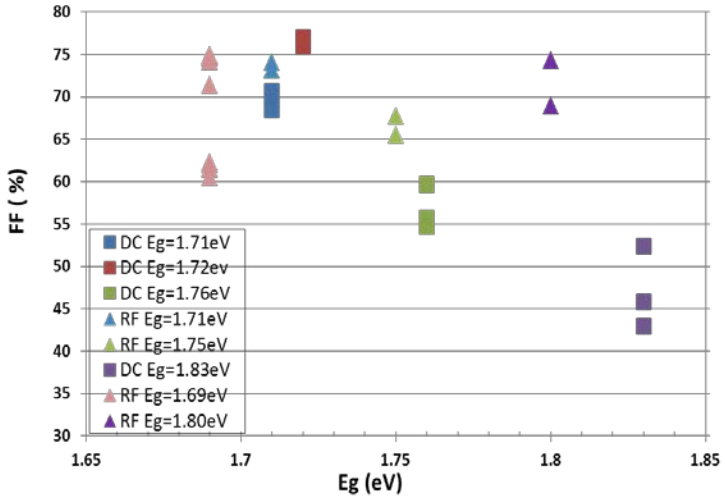


Figure 6.2. FF of FHJ cells with buffer layers deposited by RF (triangles) and DC (squares) power vs. buffer bandgap.

Next, we investigated the effects of p a-Si emitter layer doping and defects by since simulation of interdigitated back contact heterojunction (IBC-HJ) solar cells showed that reducing the p-layer dangling bond density (D_{db}) < 5×10^{18} $cm^{-3}eV^{-1}$ is an effective way to simultaneously increase V_{oc} and FF. Experimentally, the p-layer D_{db} was varied by changing dopant gas flow rate and/or hydrogen dilution during deposition. Then we selected 3 different p-layers for fabrication of FHJ, rear emitter HJ (RHJ) and IBC-HJ devices and analyzed the dark current-voltage (JV) characteristics and suns-V_{oc} curves of IBC-SHJ cells. Results presented here and described in more detail elsewhere[39] show that a low-high doping stack emitter structure is optimum. The lowly doped p-layer provides low surface recombination at the heterojunction, while the higher doped top layer enhances carrier transport and contacting.

The p a-Si:H films were deposited using either DC or RF power with different B_2H_6 to SiH_4 gas phase ratio ($B = B_2H_6/SiH_4$) and hydrogen dilution ($R = H_2/ SiH_4$) on both surfaces of 150 µm n-type FZ c-Si substrates and on one side of Corning glass. The glass samples were used to measure the temperature-dependent dark/light conductivities (σ) from which we obtained the doping level, $N_{a,}$ and activation energies, E_a. FHJ and RHJ solar cells were fabricated on textured wafers with varying p-layer deposition conditions. In standard FHJ cells, ITO contacted the p-layer and Al contacted the n-layer, while it is *vice versa* for the RHJ cells. This difference in contact materials and their properties between FHJ and RHJ has an impact on V_{OC} and FF and leads to an apparent trade-off between them as the p-layer doping decreases and is

presented in more detail elsewhere[39]. IBC-SHJ solar cells with selected deposition condition of p a-Si:H as emitter layers, as shown in Fig.1b, were then fabricated on textured 5ohm.cm CZ n-type c-Si wafers with a-SiNx:H as masking with the 3 step photolithography patterning process.

Figure 6.3 shows the decrease of iV_{OC} as the diborane concentration, B, is increased from 0.1% to 1.5% in the gas phase for both RF and DC deposited films. A simultaneous decrease of E_a was also observed from 0.1% to 1.5%, indicative of both the N_a and the D_{db} changing in a wide range. Those values of N_a and the D_{db} were estimated by simulating temperature dependent conductivity and extended SRH model[39]. These three p a-Si:H conditions were then chosen to fabricate FHJ and RHJ solar cells.

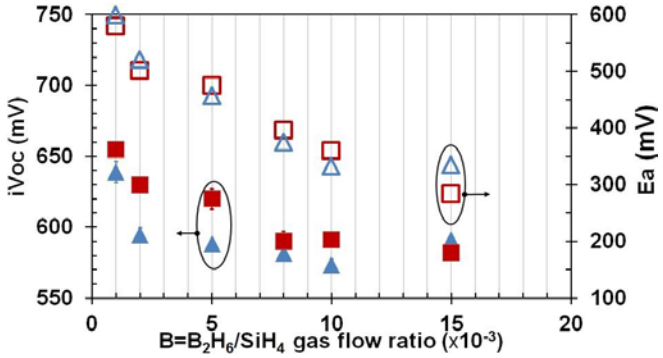


Figure 6.3. a) Schematic of FHJ (left) and RHJ (right) device structures, b) IBC-SHJ device structure, a-Si:H layers correspond to the same colors in all drawings. Light enters through top of all three.

To validate the methodology and parametrization, we simulated a FHJ solar cell with 10 nm thick p-layer using the parameters for dc-B15R6 listed in Table I while keeping all other parameters the same as established in our previous work[35] and compared them with the experimentally measured FHJ cell fabricated with the same p-layer. The inset of Figure 6.4 shows an excellent agreement between experiment and simulation. Subsequently, the FF and V_{OC} were simulated as a function of p a-Si:H D_{db} keeping all other parameters the same. The results indicate a ~20 mV increase in V_{OC} and FF > 80% can be obtained if D_{db} can be reduced from ~10^{19} $cm^{-3}ev^{-1}$ to < 5×10^{18} $cm^{-3}ev^{-1}$. Experimentally, lowering the D_{db} in the p a-Si:H layers should also be accompanied by lower conduction and valence band tail defects, therefore, the simulation underestimates the V_{OC} and FF improvement.

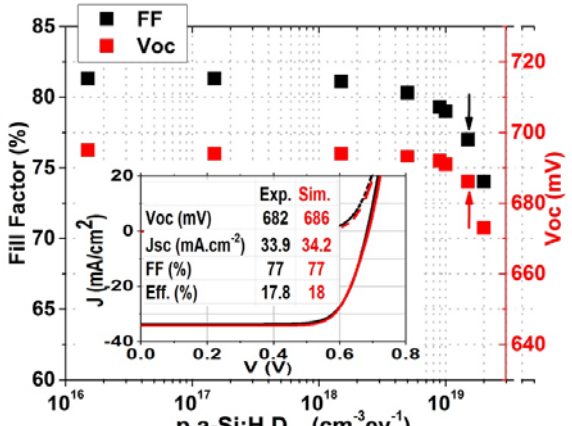


Figure 6.4. FF and V_{OC} as a function of D_{db} of p a-Si:H layer on FHJ cells. The inset shows agreement between simulated (red, with $D_{db} = 1.5\times10^{19}$ $cm^{-3}ev^{-1}$, see arrows) and experimental (black) JV curves for the FHJ cell with 10 nm p-layer dcB15R6.

QSSPC and JV results from FHJ and RHJ cells are shown in Table 6.2. The lowest doped p-layers (rfB2R10) have the highest iVoc as expected due to the lowest D_{db}. The RHJ, which has an Al/p emitter contact, also sustains this high Voc with ΔV_{OC} of only 10 mV while the FHJ, which has a ITO/p emitter contact, has much larger Voc loss with ΔV_{OC} of 38 mV. The FHJ cell with low doping also has a very low FF. We performed suns-V_{OC} measurements with blue (wavelength < 580 nm) and red light (wavelength > 780 nm) band pass filters as described elsewhere[40] to identify the characteristics of front or rear contact blocking barrier / non-ohmic contacts. Details are presented elsewhere[39]. The low-doped p-layer ITO/p contact exhibited a severe opposing diode (suns-V_{OC} bends back at ~ 1 sun intensity) for blue light. This reduces the induced band bending in c-Si ($\psi_{c\text{-}si}$) and hence reduces the minority carrier collection in the FHJ cell leading to both a lower V_{OC} and FF. The absence of bend-back in suns-V_{OC} curve in red light for the RHJ cells suggests that the lower doped p-layer makes an ohmic contact to Al but not to ITO.

Table 6.2 Measured and simulated results from FHJ and RHJ cells using three p-layer conditions. It was found that D_{db} (eV^{-1} cm^{-3}) was nearly identical numerically to the doping Na (cm^{-3})

Cell	p-layer	N_a (cm^{-3}) x1E^{-19}	iV_{OC} (mV)	V_{OC} (mV)	ΔV_{OC} (mV)	J_{SC} (mA. cm^{-2})	FF (%)	Eff. (%)
FHJ	dcB15R6	2.0	687	687	0	30.7	76	16.0
	Sim.	2.0	NA	683	NA	31.3	77	16.5
	rf B10R6	1.8	689	685	4	30.6	76	16.0
	rf B2R10	0.2	700	662	38	30.8	59	12.0
RHJ	dcB15R6	2.0	690	685	5	31.2	69	14.8
	rf B10R6	1.8	687	679	8	31.5	71	15.3
	rf B2R10	0.2	712	702	10	31.9	70	15.7

We then fabricated IBC-SHJ solar cells with three p-layers: low doped 20 nm rf-B2R10, high doped 20 nm rf-B10R6 and stack emitter structure consisting of 5 nm rf-B2R10 with 20 nm rf-B10R6 on top. The low-high doping stack emitter structure was chosen to satisfy the trade-off between good passivation provided by the low doped p-layer with low D_{db} and good contact provided by the high doped p-layer. The device parameters are shown in Table 6.3 The dark JV and suns-V_{OC} curves were analysed using standard two-diode model and the fitted data from both analysis are listed in Table 6.3.

The low doped rf-B2R10 cell has a higher V_{OC} as expected but it also shows lower FF and J_{SC} than the high doped rf-B10R6 cell. The stack emitter cell has the best device performance, having an efficiency of 20%, our highest efficiency IBC cell in the program.

The dark JV curves of the cells were analysed and the extracted parameters were used to correlate with the device parameters. We investigated the dark curves of IBC-SHJ cell with the two-diode model having diode quality factors A = 1 and A = 2.

Table 6.3 Cell data and fitted parameters for IBC-SHJ with 3 different p-layers including a high-low stack. Note that this produced a cell with efficiency = 20%.

p-layer	*V_{OC} (mV)*	*J_{SC} (mA /cm^{-2})*	*FF (%)*	*Eff. (%)*	*V_{OC} @1-sun (mV) from suns-V_{OC}*	*J_{01} (mA /cm^{-2}) suns-V_{OC}*	*J_{02} (mA /cm^{-2}) suns-V_{OC}*	*J_{01} (mA /cm^{-2}) dark JV*	*J_{02} (mA /cm^{-2}) dark JV*
rfB2R10	671	34.5	70	16.1	668	1e-10	4e-5	7e-11	4.5e-5
rfB10R6	648	36.4	73	17.3	649	4e-10	2.5e-5	3e-10	2e-5
Stack	697	38.1	76	20.2	693	6e-11	1.5e-5	3e-11	4e-5

Approximately, V_{OC} is determined by J_{01} while FF is determined by R_S and J_{02}. The stack emitter cell has a comparable low J_{02} as the high doped rf-B10r6 emitter cell indicating the high built-in field across the emitter is maintained with the benefit of better surface passivation provided by thin low doped p-layer with low J_{01}. The stack emitter cell has the lowest J_{01} leading to the highest V_{OC} ~ 700 mV and lowest J_{02} leading to the highest FF = 76%, thus achieving an efficiency of 20.2%. More analysis and comparison of junction behaviour with different p-layer emitters from suns-Voc and JV curves is presented in a conference paper[39].

The subtask goal was to fabricate IBC-SHJ cells with a FF>75% for area >1cm^2. With A=1.6 cm^2, our typical range is FF=65-70% with the highest FF=74%. Using the same wafers, doped layers, and nearly the same contacts, we routinely achieve FF=74-77% with FHJ cells, with the highest FF=78%. Note that figure 2.6 shows that FHJ cells will have a higher FF than IBC cells over a range of buffer layer conditions which is attributed to 2D effects. To investigate this difference, we have conducted extensive JV

measurements and analysis of both IBC-SHJ and FHJ solar cells using filtered light (neutral and spectral filtered) and varying temperature, as well fabricated IBC test structures with very different patterning and rear surface deposited layers. We obtain the diode parameters n, Jo, and Rs using various methods, and calculate several effective FF values (dark FF, Rs corrected FF, iFF from Suns-Voc). We performed EL and LBIC to examine spatial dependence of collection and recombination.

An IBC-HJ and FJ cell having a relatively high FF for that device structure were selected for in-depth analysis. (Subsequent to this analysis from 2014, we fabricated IBC cells with higher FF ~73-74% but MC1431 with 68% was the highest FF at the time.) Parameters are given in Table 6.5. Figure 6.5 shows the FF obtained with different intensity for a FHJ and IBC-SHJ cells with typical FF. They both have an inverse dependence on intensity as expected for Rs-loss. After Rs correction, FF for the FHJ cell is nearly independent of intensity, indicating there are no other current or generation dependent losses. The IBC cell still has some generation level dependence, suggesting additional losses such as current crowding or high level injection. Values of Rs were 1 Ohm-cm^2 for the FHJ cell and 2.5 Ohm-cm^2 for the IBC cell. Both cells extrapolate to a maximum FF~80% without Rs. One expects the Rs losses to be negligible at low intensity. However, iFF from Suns-Voc is ~83-84% on these and many other devices, suggesting there is 3-4 percentage point loss when current flows through the device independent of resistance losses. Using filtered light, we determined that FF is sensitive to the light intensity but not the spectrum, indicating losses are independent of where carriers are generated. Figure 6.6 shows the JV curves in light and dark before and after correction for Rs. Table 6.5 shows the JV performance and the diode parameters ideality (n) and recombination current (Jo) for both devices in light and dark. The IBC-HJ has much higher Rs and a higher recombination, especially in the light. Since the dominant contribution to Rs in FHJ cells is the lateral resistance in the ITO, which does not occur in IBC cells, we need to look elsewhere to find the source of the larger Rs in IBC cells. Table 6.6 shows efficiency and FF recalculated to remove the effect of Rs for IBC and FHJ cells. The dark FF is obtained by shifting the dark curve by Jsc. The FHJ cell has nearly 'ideal' FF as-is and gains little from corrections for Rs. The IBC-SHJ cell (MC1431) shows a large improvement in FF for both corrections. This is consistent with data in Table 6.5, which shows that the dark JV curve for the IBC cell is much closer to the FHJ cell, and especially having low ideality. Note that after removing the effect of Rs, the IBC-SHJ cell has higher 'corrected' efficiency than the FHJ cell due to higher Jsc, validating the potential for high efficiency in our devices.

Table 6.5. Measured cell performance and diode parameters obtained from analysis of the light JV curves for FHJ and IBC-SHJ cells from Figure 6.6.

cell	Device	Voc V	Jsc mA/cm^2	FF %	Eff %	Rs Ωcm^2	Light n Jo	Dark n Jo
FHJ	MC1448	0.661	33.9	77.0	17.3	0.9	1.2, 2E-8	1.2, 1E-8

IBC	MC1431	0.693	35.4	67.6	16.6	2.5	2.2, 2E-4	1.3, 2E-7

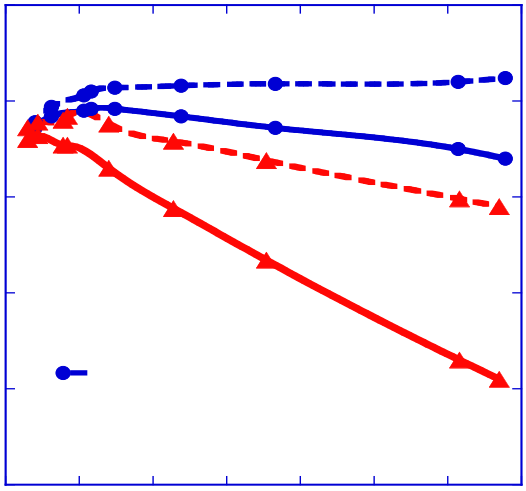


Figure 6.5 FF vs light intensity. Solid: as-measured, dashed: with correction for Rs losses. Cell performance for these FHJ and IBC-SHJ devices is given in Table 6.1

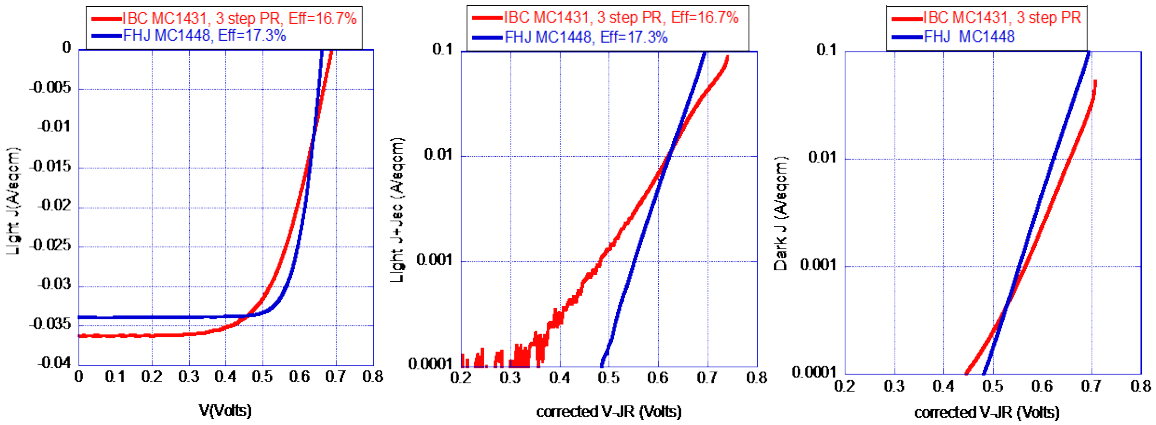


Figure 6.6. JV curves for IBC and FHJ devices having similar efficiency but different FF. Data given in Table 6.1. a) light JV as measured; b) Log JV in light with V corrected for Rs; and c) Log JV in dark with V corrected for Rs.

Table 6.6. FF and Eff for light JV and dark JV (shifted by Jsc) of FHJ and IBC-SHJ cells after removing losses due to Rs from Table 6.1.

cell	Device	Light JV w/o R		Dark JV w/o R	
		FF %	Eff %	FF %	Eff %

FHJ	MC1448	81	18	81	18
IBC	MC1431	77	19	78	20

We also investigated the temperature dependence of the FHJ and IBC cells in order to understand the difference in FF. A complete analysis of the temperature dependence of the JV curves of ~10 cells (FHJ and IBC) is the subject of a Master's thesis[41]. Figure 6.7 shows FF vs temperature for 2 FHJ and 2 IBC cells. In each case there is a normal cell with good passivation (FHJ MC1469-02, IBC MC1492-02) leading to high Voc. There is also one FHJ and IBC cell intentionally made to have poor passivation on the front surface by eliminating the front a-Si i-layer. For the IBC cell, it was replaced with an a-Si n-layer front passivation. Both of these modified cells had much lower Voc, consistent with their lack of a passivating i-layer. Figure 6.7a shows that as T decreases the FF of the 'normal' FHJ and IBC cells each increase then peak and fall off at lower temperatures. The non-standard cells with higher recombination show the increase but significantly less decrease at lower T. Figure 6.7b shows the JV curves for the 4 cells at -55°C. The FHJ with i-layer shows an S-curve, presumably due to hole blocking at the valence band mismatch. We have commonly seen this behavior when measuring FHJ cells at low T. The FHJ device without an i-layer shows no such FF limitation at low temperature, consistent with the above proposal. They both have much higher Rs at -55°C compared to at 25°C where it is ~ 2-3 Ohm-cm^2. Neither of the IBC cells in Figure 6.7b have the S-curve at low T. This is surprising since they both have an 8 nm a-Si i-layer between the p-layer and n-Si wafer just like the FHJ cell.

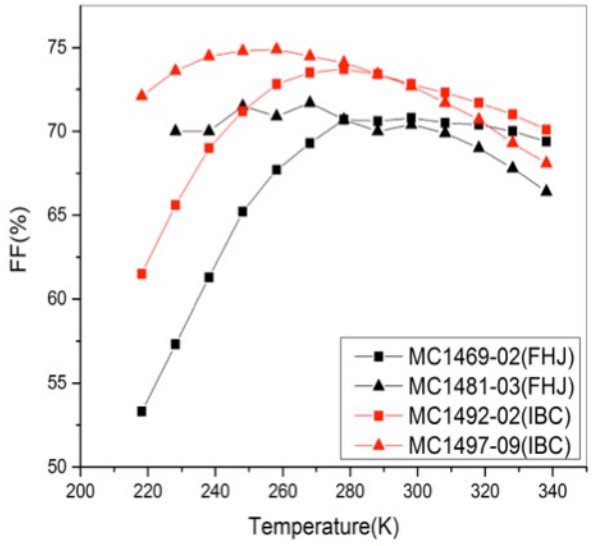


Figure 6.7a) FF vs T for 2 FHJ (black) and 2 IBC (red) cells. MC1469 was standard FHJ, MC1481 had no front i-layer, MC1492 was standard IBC, MC1497 had an a-Si n layer replacing the front a-Si i-layer.

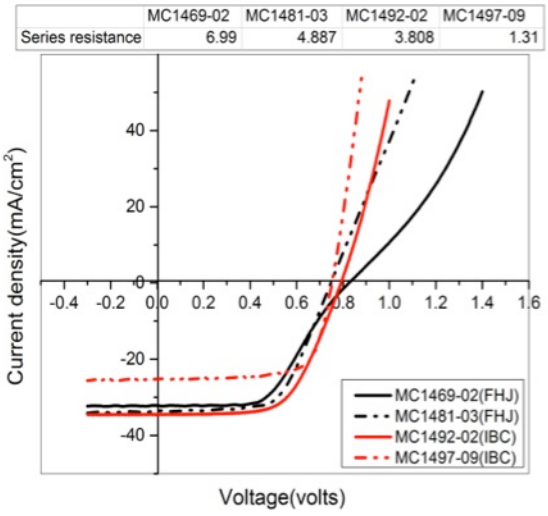
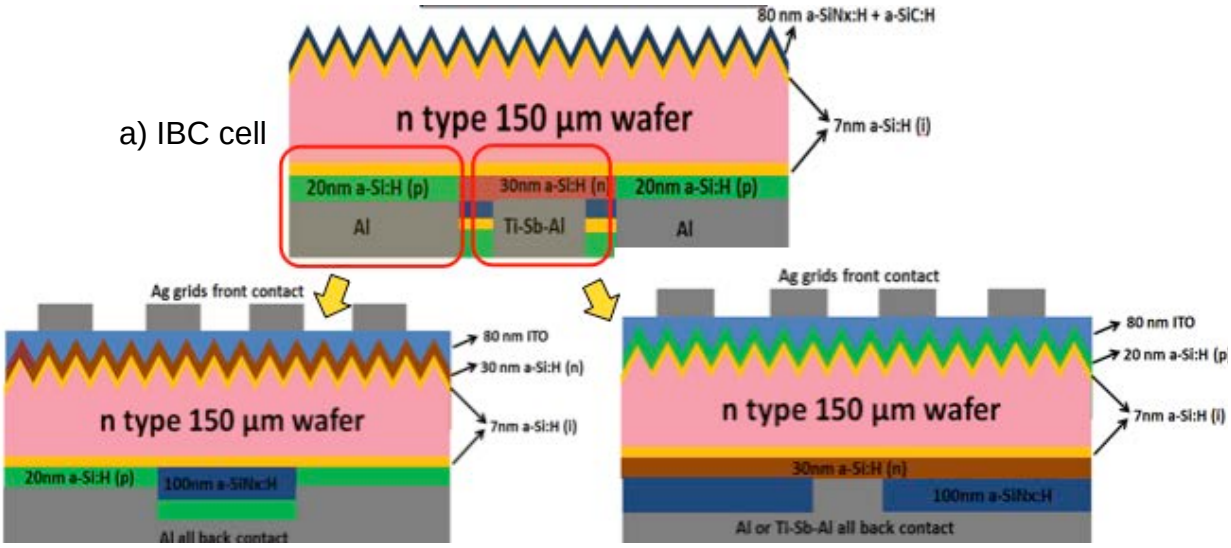


Figure 6.7b) JV curves at -55°C for the same 2 FHJ (black) and IBC (red) cells from Figure 6.7a. Series resistance at -55°C from JV analysis also shown.

Several device structures were fabricated to understand the role of rear heterojunction emitter (RE) and base contact strips in the IBC cell by comparing blanket p and n depositions (100% coverage) and contacts to narrow strip contacts used in the IBC. We are particularly focused on explaining why IBC cells tend to have lower FF. Two versions of these hybrid cells are shown in figure 6.8.



b) rear emitter (RE) SHJ cell c) front emitter (FE) SHJ cell

Figure 6.8 Diagram of a) standard IBC cell; b) RE SHJ with IBC-rear p-strip (83% coverage), front n-blanket; and c) FE SHJ with blanket emitter with IBC-rear n-strip (13% coverage).

Figure 6.9 shows laser beam induced current (LBIC) scans for these two devices with RHJ having 83% coverage of the rear p-strips and FHJ with 13% coverage of the rear n-strips (figures 6.9 b and c, respectively). In 6.9a, there is no loss in collection corresponding to the period of the p-strip fingers even at forward bias. In 6.9b, there is about 5% loss in collection at forward bias corresponding to the period of the n-strip fingers confirming that the n-strip has higher recombination than the adjacent a-Si/a-SiN. This actually corresponds rather well to LBIC on our best IBC cells, confirming that these hybrid structures are relevant to study of IBC structures. Together, these LBIC scans suggest that the lateral current transport does not lead to significant losses in collection especially near maximum power where they might influence FF.

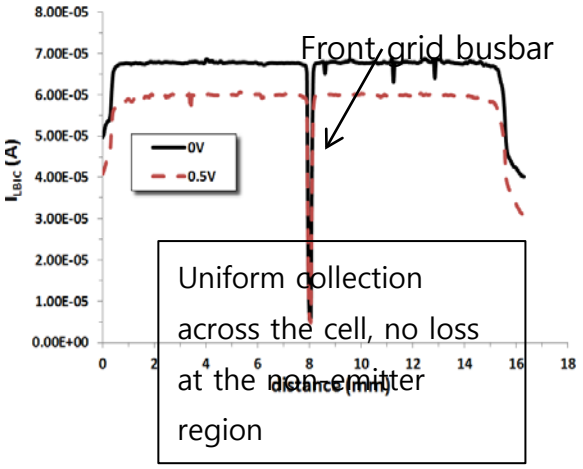


Figure 6.9a) LBIC at 0 and +0.5V for RE cell with 83% p-strip on rear

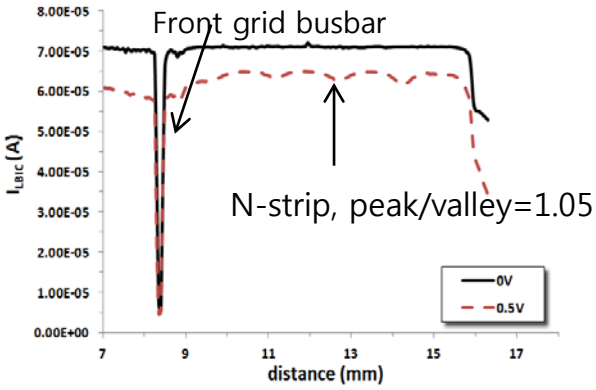


Figure 6.9b) LBIC at 0 and +0.5V for FE cell with 13% n-strip on rear

Subtask 6.2 Evaluate laser front surface texturing and passivation

Goal: SRV<10 sm/s from QSSPC and reflection loss <8% with AR or else abandon laser texture

IPG and IEC had previous experience with laser texturing and removing the highly defective surface layer. From that effort, it was known that obtaining low reflection was not a problem, but achieving good passivation was challenging due to structural defects introduced at the surface. Thus etching and annealing the laser-induced defects and Si slag would be a critical issue.

A large number of polished Si wafer pieces (1x1 inch^2) were laser textured at IPG under conditions likely to provide an appropriately textured surface. The lasing power was varied from 20 to 40 uJ. The reflection of the as-received samples was slightly lower below 500 nm than our standard wet chemical texture using TMAH or our Sunpower textured wafers. There was negligible difference between the different lasing powers.

Although the initial reflection curves looked promising, the minority-carrier lifetimes of the laser-textured samples after solvent-cleaning and Piranha + HF etching were extremely low (< 1 µs) as expected due to the defects caused during laser ablation, as the c-Si on the surface melts and re-solidifies in non-crystalline form. In the second batch of laser textured samples from IPG, a few samples were annealed by excimer laser after texturing, expecting a better surface quality, but their lifetimes were also low (< 1µs). Therefore, we explored defect-etching of the laser-textured samples. HNA, a mixture of nitric acid, hydrofluoric acid and acetic acid, was chosen, as it is the best isotropic etchant in terms of uniformity and reproducibility, and has been studied for other applications in this project. The goal was to develop a defect-etch recipe with HNA, varying concentration and etch time, to achieve a balance between sufficiently etching the surface to give high lifetimes, by removing ablation defects, without removing too much Si so that the beneficial texturing is lost. The reflection curves of samples etched in HNA for different times, between 30-120 sec, are shown in Figure 6.10. After even just 30 sec etching, the reflection increases significantly and is now

higher than that of TMAH-textured samples yet the lifetime remained < 1 usec. Between 60 and 90 sec etching, the lifetime goes from unmeasurably low (<1 µsec) to very high (> 1 msec) with only a slight increase in reflection. This change is very rapid and will be difficult to control. A second brief TMAH (17% at 90^{o}C) defect-etching failed to increase the low lifetimes of wafers. These results suggests that at the present level of investigation, high lifetime and low reflection are mutually exclusive: a high surface quality is only possible after removing nearly all of the texturing with HNA.

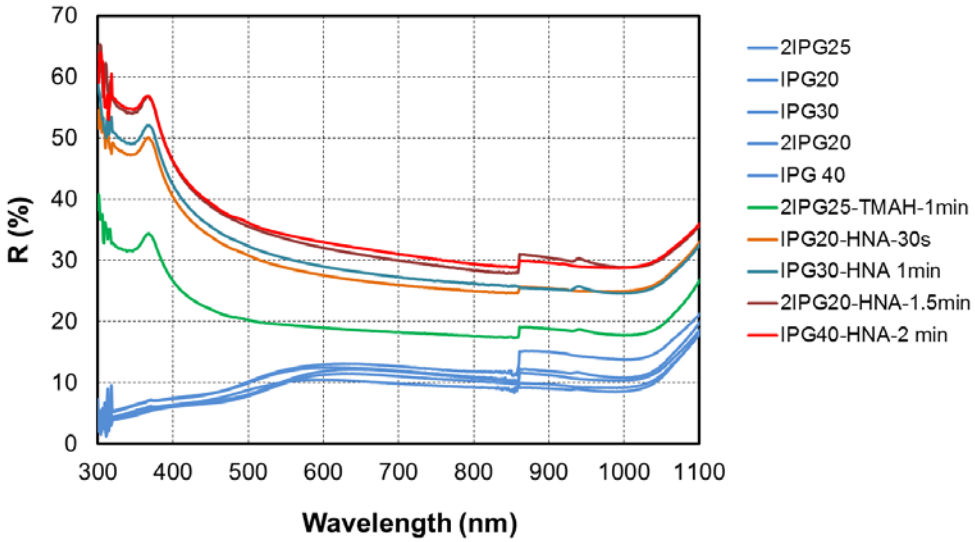


Figure 6.10 : Increase in surface reflection of samples with post-texturing etches

A literature survey found that some laser defect-etching recipes combine both anisotropic and isotropic etchants, such as sodium hydroxide and HNA. Much more work, probably involving varying HNA treatment temperature and more aggressive TMAH etching, would be required to simultaneously achieve high lifetime and low reflection. Compared to texturing by TMAH-etch alone, this would be a more complex process for only a slight decrease in reflection to give, at most, ~ 1 mA/cm^2 gain in photocurrent. For this reason, we abandoned laser-texturing pursuits.

Task 7. Laser processing and patterning and defect annealing/passivation

Subtask Goal: Fabricate IBC-SHJ solar cells >1cm^2 with single layer metallization and laser patterning having Voc>650 mV and FF>75%

Laser Fired Contacts (LFC)

During this period, we focused on evaluating the laser damage to passivation from both LFC and laser isolation using photoluminescence imaging (PLI), scanning electron microscopy (SEM), and electroluminescence (EL). Examination of both LFC and isolation structures with tightly spaced laser shots under a range of lasing conditions finds that once the laser dose is sufficient to melt the Al/Si interface and punch through the SiN, the effective lifetime decreases by about 40% regardless of lasing energy delivered. However, isolated laser spots induce negligible lifetime loss.

Many sets of samples with different metal and insulator stacks were processed during this period towards investigating the impact of sample structure on LFC formation. Since the rear dielectric configuration of the IBC-SHJ cell is not defined at this point, several likely combinations are being investigated for LFC, including a-Sin/p a-Si or a-SiN/n a-Si, or just a-Sin. An IR laser (1064 nm) with pulse duration around 150 ns and a green laser (532 nm) with pulse duration around 7 ns were used at IPG and IEC, respectively. Resistance of LFC structures can be obtained from vertical resistance (R_{LFC} represents the sum of spreading and contact resistance R_C) or lateral transfer length measurements (TLM) as discussed in Subtask 4.1. Vertical measurements are less accurate when Rc is small due to the relatively greater value of the spreading resistance but we can explore more conditions per substrate compared to TLM measurements which are more accurate but restrict the number of lasing conditions that can be investigated. Thus we continue to evaluate both on each substrate.

Our baseline metal stack for LFC is Al(500 nm)-Sb(50 nm)-Ti(5 nm). Sb plays a critical role as the dopant layer, Ti improves adhesion and Al serves as current carrying layer. Ti is known as a deep level defect in silicon and Al is known as a p-type dopant. Therefore, we attempted to 1) remove the Ti layer in stack and 2) replace Al with a non p-type dopant metal.

We successfully made Al-Sb stacks on textured wafer surfaces without adhesion problems. A comparison of Al-Sb stack and Al-Sb-Ti stack is shown in Table 7.1. The morphology and specific contact resistance is very similar. The Al-Sb stack was then applied on a front junction device. MC1433-02 had FF=73%, demonstrating good ohmic contact.

We also made LFC test structures with a Ni-Sb-Ti stack. In this stack Ni replaced Al as the current carrying layer and LFC was performed on these test structures. Although Ni is not a p-type dopant like Al, the calculated specific contact resistance of Ni-Sb-Ti stack is almost 20 $m\Omega cm^2$, which is 3 times higher than Al-Sb-Ti stack (Table 7.1). Due to adhesion problems, the thickest Ni we were able to deposit is 100 nm, which is 1/5 as thick as Al or Ag in the original stack. Also, the resistivity of Ni is $7*10^{-8}$ ohm*m, which is much higher than the resistivity of Al ($2.8*10^{-8}$ ohm*m). Therefore, the sheet resistance on the stack pad is limiting the calculated specific contact resistance. We therefore terminated any further work on alternative metal stacks and stayed with Al-Sb-Ti.

Table 7.1. Comparison of R_C from vertical or horizontal test structures for Al-Sb, Ni-Sb-Ti and Al-Sb-Ti stacks. Wafers were textured in all cases. All structures had n a-Si/Al for a rear Ohmic contact

Structure (metal/dielectric stacks)	Rc from Vertical ($m\Omega cm^2$)	Rc from TLM ($m\Omega cm^2$)
Al-Sb/ p a-Si/ i a-Si/ text n c-Si	<0.7	3.0
Al-Sb-Ti/ p a-Si/ i a-Si/ text n c-Si	<0.3	1.9
Al-Sb/ SiNx/ i a-Si/ text n c-Si	<0.7	9.4

Al-Sb-Ti/ SiNx/i a-Si/ text n c-Si	<0.7	7.1
Ni-Sb-Ti/ SiNx/i a-Si/ text n c-Si	X	20
Al-Sb-Ti/ p a-Si/ i a-Si/ SiNx/ text n a-Si/ i a-Si/ tex n c-Si	<0.1	1.0

New processing and patterning of the rear surface described in Task 10 above creates new passivation stacks under the n-contact strip compared to those previously studied for LFC (a-SiNx and a-Si p). To accommodate the new processing steps for IBC-SHJ cells, LFC through the dielectric stack blocking layers p a-Si/ i a-Si/ SiN_x/ n a-Si/ i a-Si had to be developed. Using either an IR laser (1064 nm) with pulse duration around 150 ns and a green laser (532 nm) with pulse duration around 7 ns, low specific contact resistance Rc <1 $m\Omega cm^2$ was obtained (Table 7.1). This is the lowest resistance we achieved for LFC through p a-Si, SiN_x, or SiN_x/ p a-Si. The ability of firing through stack blocking layers will grant more flexibility in IBC rear side processing.

Processing and results from IBC cells with LFC and complex dielectric stacks are described in Task 10. Figure 7.1 presents the JV curves before and after LFC of two IBC cells having the standard Al-Sb-Ti stack and fired through a stack of a-Si i/p/i/n layers. The cell in Figure 7.1a had the baseline photolithography with 25 um gap while the cell in 7.1b was patterned using the masked PECVD deposition and metal masks were visually aligned leading to a minimum gap of 100 um. The Voc and Jsc are similar. Discussion in Task 10 explains that the difference in FF is likely due to the difference in the gap width and the gap structure. This demonstrates that LFC process developed in this program can have comparable FF to cells without LFC. However, the Voc of the best cell with LFC is about 20-30 mV below comparable cells without LFC.

a)

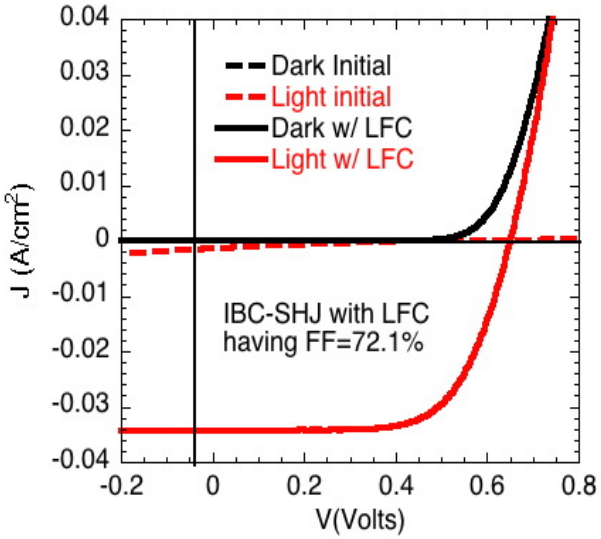


Figure 7.1a) Light and dark JV curve before and after LFC of MC1419-05. Patterning was with baseline 3-step photolithography with 25 µm gap . LFC

b)

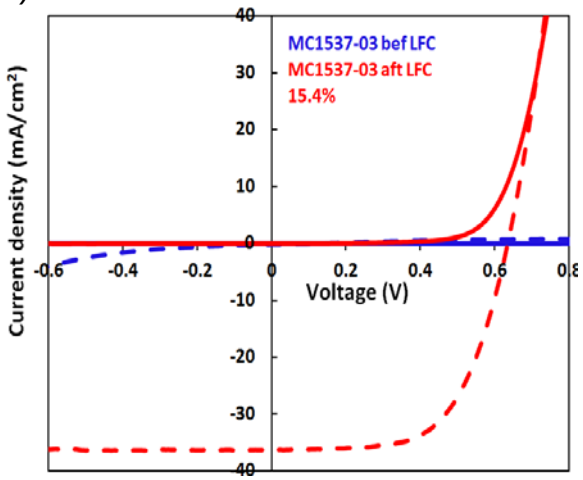


Figure 7.1b) Light and dark JV curve before and after LFC of MC1537-03. Patterning by masked deposition (no photolithograph) with 100 µm gap . LFC

was fired through a dielectric stack of a-Si i/p/i/n. Parameters: Voc=0.645V, Jsc=36.2 mA/cm2, FF=72.1%, Efficiency=16.9%.	was fired through a dielectric stack of a-Si i/p/i/n. Parameters: Voc=0.650V, Jsc=36.5 mA/cm2, FF=64.2%, Efficiency=15.4%.

A paper summarizing IEC's LFC work, especially the innovation of applying the multilayer metal stack with Sb dopant to contact n-Si, has been published[42].

Laser patterning
Laser assisted etching isolation was proposed and first realized at IEC as described in several previous reports. Photoresist (PR) was applied on top of the metal stack and the UV laser was used to remove it. Then the metal in the opening was chemically etched, while the remaining PR was used as an etching resistant layer. Moderately high shunt resistance was obtained.

The transition from laser assisted etching isolation to direct isolation (ablation) has proved to be very challenging. IPG evaluated various lasing conditions using a 10 ps laser at 515 nm. IPG achieved reproducible isolation of metal stack on SiN_x after stepping through a laser process space of over 100 conditions by using a defocused laser beam as shown in Figure 7.2. Typical lasing condition used was listed in Table 7.2.

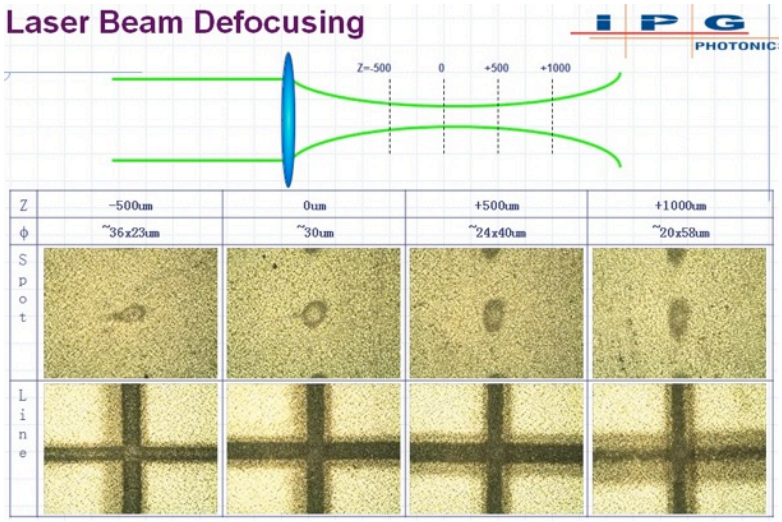


Figure 7.2. Use of a defocused laser, as opposed to an "imaging" technique because of the limited energy density achieved with imaging. This allows for high instantaneous fluence to be tested.

Table 7.6. Lasing condition used for direct laser isolation. Z is deviation from perfect focus as shown in Figure 7.2.

Wave Length	Rep Rate	Z	Power	Inst. Fluence	Scan Speed	PPL

(nm)	(kHz)	(um)	(W)	(J/cm^2)	(mm/s)	(#)
515	200	+/- 500	7.0	4.3	400	12(x/y), 20(y/x)

The results show a successful direct isolation when patterning the metal layers into a SiN_x/i a-Si stack (MC1398), achieving reproducible isolation above 2 kohms. The highest resistance measured was around 8 kohms. The shunt resistance was $6x10^3$ ohm*cm. Figures 7.3 and 7.4 show optical microscopy and SEM/EDS images of bad and good isolation scribes. Additional process development will try to further improve upon these results. Based on our current IBC device interdigitated metal contact pattern, we estimate that we need to achieve >20 kohms for minimal shunt losses.

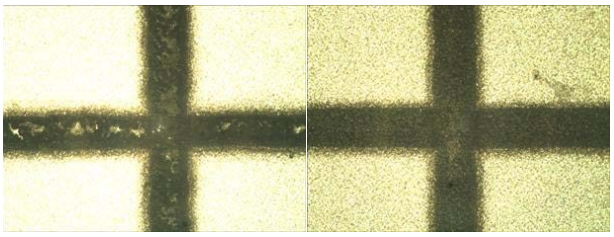


Figure 7.3. Optical image of direct laser isolation with resistance of 75 ohms (left) and 2000 ohms (right). Residuals are visible in low resistance isolation gap while high resistance isolation gap appears to be flat and uniform.

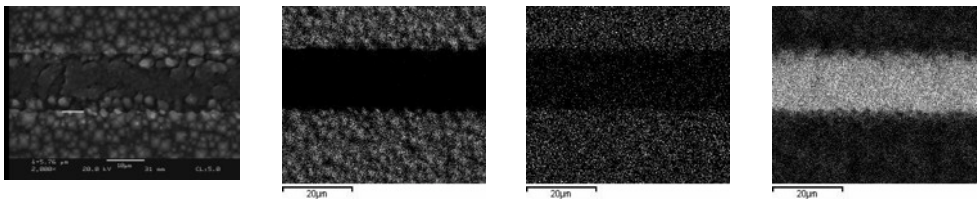


Figure 7.4. From left to right: SEM image and EDS mapping of Al, Sb and Si for a successful direct laser isolation scribe.

Samples and processing were designed to evaluate the damage to the passivation from LFC. The structure of the LFC samples is metal stack (Al-Sb-Ti) / front passivation (SiNx / i a-Si)/ n c-Si/ rear passivation (i a-Si/ SiNx). Double sided SiNx/ i a-Si passivation ensures high initial passivation quality without degradation. Polished wafers are used for better resolution of PL mapping at MIT.

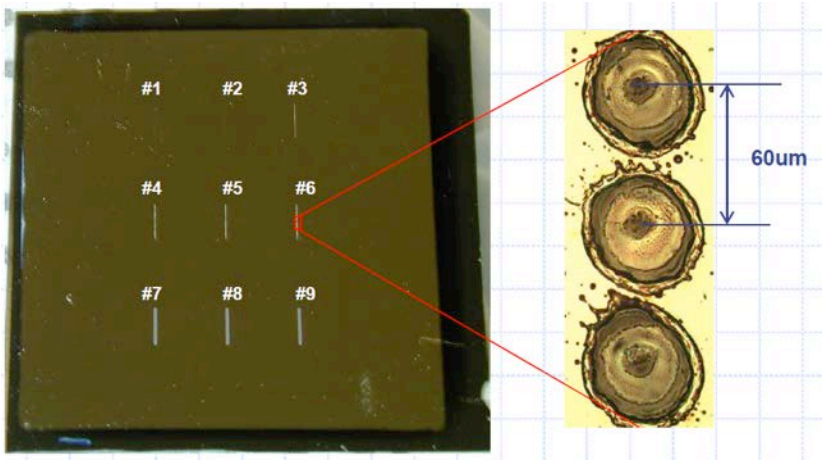


Figure 7.5 LFC laser isolation test structure. Sample is 1x1 inch^2 with 9 lines of LFC with different lasing conditions. Spots were nearly touching. Lines 1 and 2 failed to cause significant visual change. See text for explanation.

Different laser conditions were applied on LFC test structures as shown in Figure 7.5 and Table 7.3. Between each line of LFC spots, the spacing was designed to be > 4mm which is larger than the diffusion length in the wafer. By this way it will prevent or minimize the interference between different LFC lines in PL mapping. However the spots are much closer (60 um on-center) than they would be in a real device (~ 500 um apart).

Table 7.3 Laser condition of LFC lines 1-6 on sample in Figure 7.5

Line#	1	2	3	4	5	6
Type	LFC	LFC	LFC	LFC	LFC	LFC
RR	20kHz	20kHz	20kHz	20kHz	20kHz	20kHz
Power	2.0W	2.2W	2.4W	2.6W	2.8W	3.0W
Size	ϕ 40 um	ϕ 42 um	ϕ 42 um	ϕ 50 um	ϕ 50 um	ϕ 52 um
E Dose	1.0 J/cm^2	1.1 J/cm^2	1.2 J/cm^2	1.3 J/cm^2	1.4 J/cm^2	1.5 J/cm^2

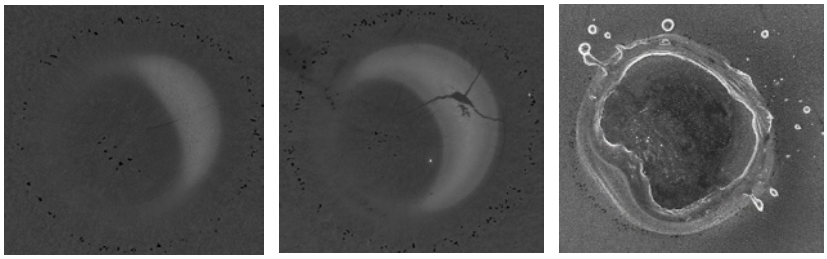


Figure 7.6 SEM of LFC spots: line 1 (left), line 2 (middle) and line 3 (right). These line numbers refer to conditions in Table 7.3 or Figure 7.5.

After LFC lines were fired at IPG, SEM (Figure 7.6) and PL mapping at MIT (Figure 7.7) found that conditions 1 and 2 failed to produce any loss in lifetime, while conditions 3-9 produced essentially identical losses despite a large range in energy. Details about the PL measurements and calibration are found in Section 8.2. As shown in Figure 7.6, when the laser energy is only just enough to remove the metal (line 1) or crack the dielectric layer (line 2), the lifetime does not degrade. When the laser energy is enough to melt the silicon as in line 3, the lifetime degrades significantly, reduced from over 2000 us to below 1000 us. But once the laser melts the Si, the degradation is independent of the lasing power over the range shown. As learnt previously, to achieve good ohmic contact the dielectric layer must be broken down and the silicon/metal must melt. This suggests that depassivation is inevitable for LFC processing. Interestingly when the spacing between each LFC spot is very large (>300 um), as would be found in a device application, neither PL at MIT or EL at IEC could clearly identify any depassivation.

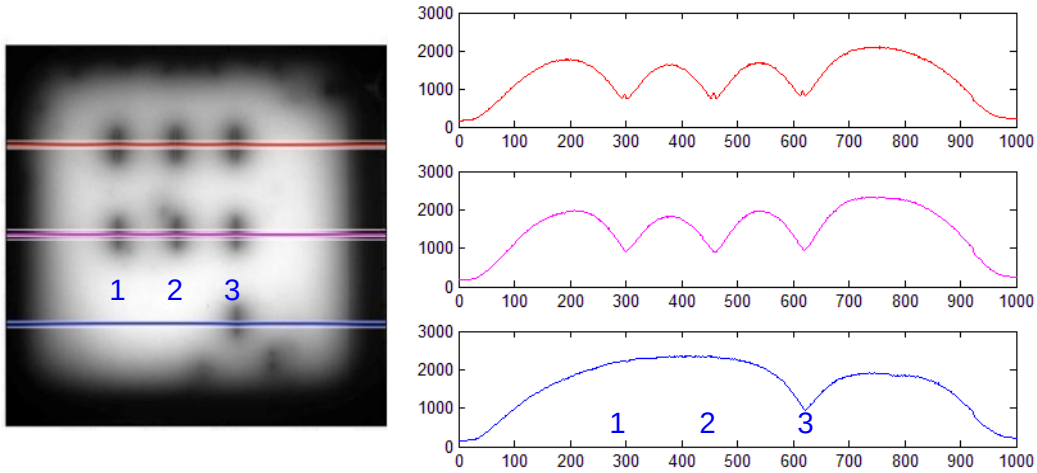


Figure 7.7 PL mapping of LFC test structure (left) and quantitative line scan (right). The PL image is inverted from the photograph in Figure 7.5. Dark regions represent lower lifetime. Line scans on the left show lifetime profile across the 3 rows. Row with cells 1-3 (blue lines) indicate no loss for conditions 1 and 2.

The effect of a very limited number of widely spaced LFC spots was studied by adding them one at time to a completed IBC which was processed with the Al/Sb/Ti metal stack on the n-layer as appropriate for LFC. The random LFC pattern is shown in Figure 7.8a. Fingers had 0,1, 2, 4, or 6 spots. The Voc decreased nearly linearly with the number of LFC spots as in Figure 7.8b. The sample was then measured by EL. No evidence of the LFC's could be found in Figure 7.8c. An EL line scan of finger 6 having a group of 3 and 1 LFC failed to find any decrease in EL associated with the LFC. This is consistent with LBIC measurements which have never identified any loss of photocarrier collection due to a localized LFC slot, but rather the entire contact finger is dark. A study of the impact of LFC spot spacing on depassivation is underway.

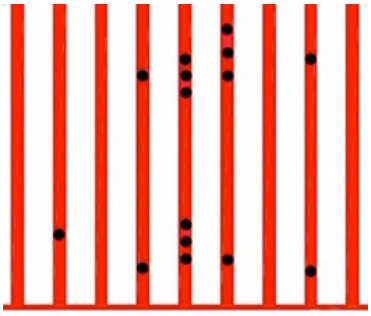


Figure 7.8a n-fingers with 15 random LFC spots.

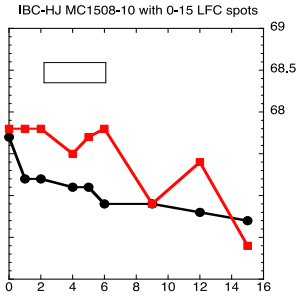


Figure 7.8b Voc and FF vs number of LFC spots

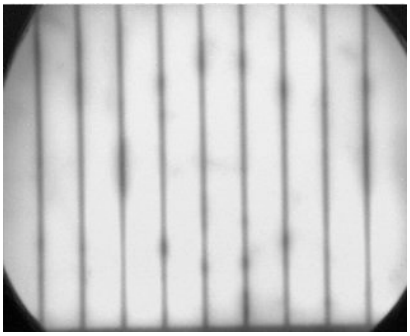


Figure 7.8c EL image. The ring pattern is from the rubber o-ring on vacuum chuck.

Direct laser isolation

The structure of the direct isolation samples is Al / SiNx / i a-Si / n c-Si/ i a-Si/ SiNx. metal. Double sided SiNx/ i a-Si passivation ensures high initial passivation quality. Polished wafers are used for better resolution of PL mapping at MIT. The lasing variables were the fraction of full current (50-90%) and defocussing (1.0, 1.5 mm). For each condition, two squares were scribed to evaluate the isolation resistance and the PL degradation. PL was measured before an after laser isolation.

After direct laser isolation scribe, PL mapping in Figure 7.9 shows almost identical lifetime drop in the laser processed area, despite variations in the laser power (from 50% current to 90% current) or defocussing. Isolation resistance of the 2 mm squares was ~ 10K Ohm-cm2 which is not high enough when translated to the minimum shunt resistance ~ 500 Ohm-cm2 needed for an IBC cell with a much larger perimeter.

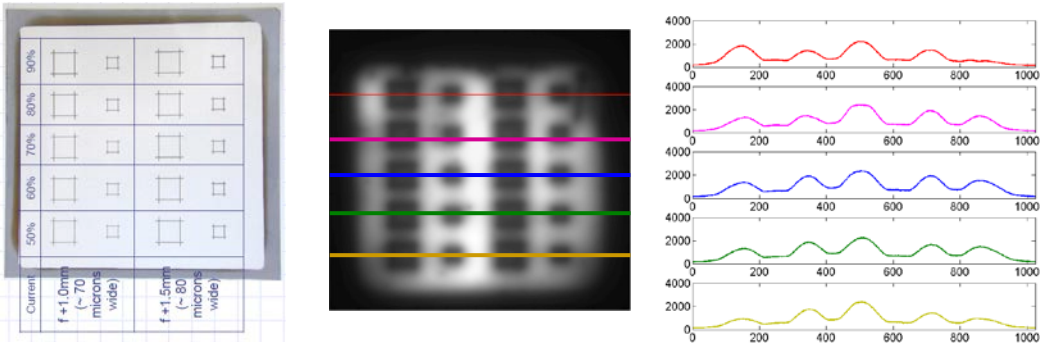


Figure 7.9 Direct isolation samples: Visual image (left), PL mapping (middle) and quantitative PL line scan (right). The line scans cut through two pairs of squares, each at different combination of % current and defocusing.

We have also performed direct isolation with an oxygen jet during processing but we did not see any improvement in passivation. The overall lifetime dropped from over 2100 us down to around 700 us after the direct laser isolation with oxygen jet, comparable to the values in Figure 7.9 . The lifetime could partially be recovered to 800 us after a 200°C anneal for 5 min. PL mapping with and without oxygen jet is shown in Task 8.2.

For both LFC and direct isolation, it seems there is a threshold laser energy dose. Below the threshold, the passivation is not affected by the laser dose. Above the threshold, which is around 1.2 J/cm^2 in this case, the lifetime around the lased feature decreases by around 40% regardless of the energy dose or type of lasing conditions as in Figure. 7.10.

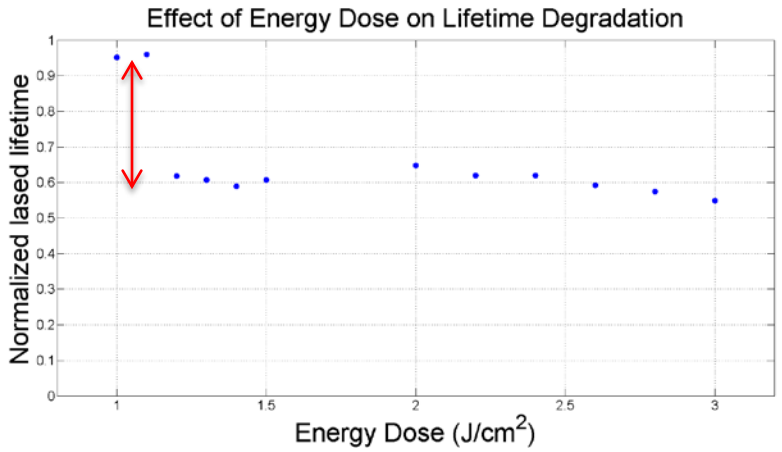


Figure 7.10 Effect of energy dose on lifetime degradation. Note the step at 1.2 J/cm^2. Spots from 1.0-1.5 J/cm2 were LFC conditions from Table 7.1. Spots from 2.0-3.0 J/cm2 are from isolation lasing conditions.

Laser chemical isolation

The laser chemical isolation should not degrade the lifetime by laser processing since the UV psec laser only interacts with the photoresist and perhaps the top of the Al. It does not cause any Al-Si interaction or rupture of the SiN passivation. The test structure of laser chemical isolation is almost identical with direct laser isolation. The only difference is an extra sacrificial photoresist layer on top of the Al.

The PL maps before and after the laser processing and etching processing are shown in Figure 7.11. Negligible degradation was observed at all stages. This is a good demonstration of effectiveness in passivation of the laser chemical isolation strategy.

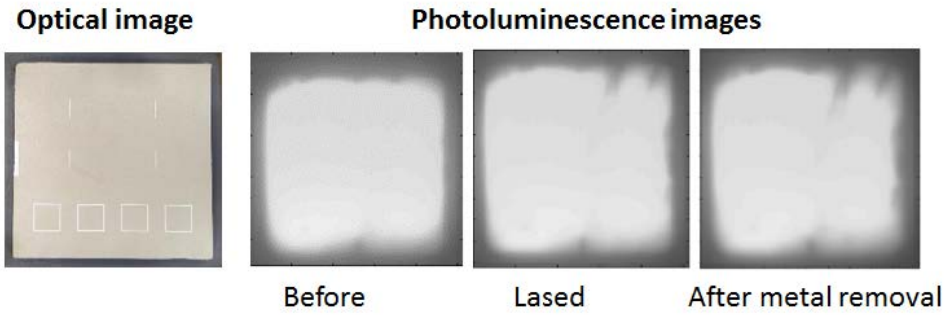
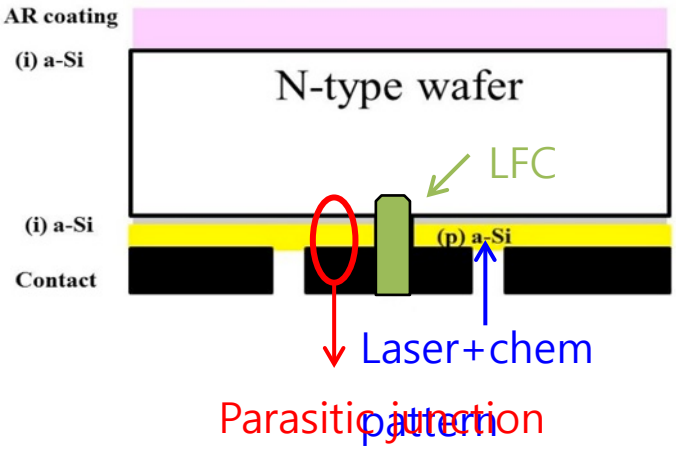


Figure 7.11 Effect of energy dose on lifetime degradation for UV laser patterning of photoresist on passivation Si wafers.

IBC cells were made with laser chemical isolation and laser fired contacts. The rear deposition was only a-Si i/p. This is the simplest IBC device we can envision and was the goal identified in the orginal proposal. Figure 7.12 shows the structure and the cell results. All parameters are quite poor. Other versions of this device were made with different patterning; i.e. a single level masked metallization to give the same structure. It also had the same performance. Based on subsequent IBC device structures and LBIC and EL measurements, we suspect the culprit is a parasitic shunted junction under the non-LFC portion the metal base contact (about 99% of this contact) where the p/i region is shorted by the metal. There is no insulator layer to block the collection of holes from the wafer hence there is a high recombination under this entire contact.

a)



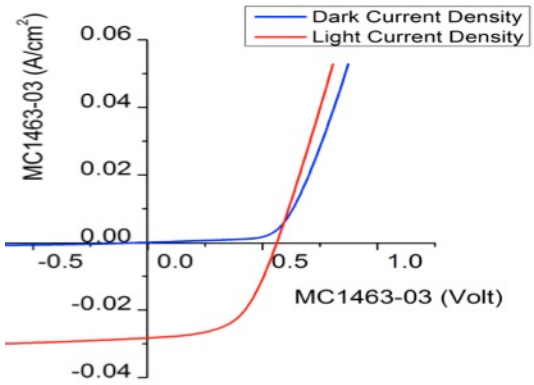


Figure 7.12a IBC structure utilizing LFC and laser+chemical etching with simple rear deposition of a-Si i/p stack.

Figure 7.12b. JV curve after LFC for the simple structure defined by laser+chemical etching. Voc= 570 mV; Jsc=28mA/cm^2; FF=55%; Eff= 8.8%.

Task 8: Defect engineering in thin kerfless Si wafers

Subtask 8.1: Improve J_{SC} and V_{OC} by defect mitigation.
Subtask goal: Improve J_{SC} by >15% and V_{OC} by >5% relative to devices without defect mitigation process on thin kerless Si wafers.
Status: Accomplished.
Highlights:

- From Gen I to Gen II materials, we improved the lifetime from ~30 µs to ~1000 µs, resulting in an increase in the device efficiency potential from ~14% to >20%. This far exceeded our stated J_{SC} and V_{OC} goals.
- Initiated development of a free-carrier-absorption-based temperature- and injection-dependent lifetime spectroscopy apparatus.

To further examine the root cause(s) of lifetime-limiting defects, we developed an experimental setup to perform temperature- and injection-dependent lifetime measurements to identify defects in silicon materials in a non-contact, non-destructive approach. While DLTS is generally limited to impurity concentrations of 10^{11} cm^{-3} for typical doping levels, and typically only probes the majority-carrier half of the bandgap, lifetime spectroscopy can theoretically be used to identify impurities in lower concentrations provided a Shockley-Read-Hall lifetime signature can be identified. This technique can be applied to arbitrary silicon materials given the sample thickness and doping level. The technique we have chosen to adapt for this measurement is free-carrier absorption with a temperature stage, shown schematically in **Figure 8.1**, which has the advantage of not requiring proximity of an inductance coil to measure lifetime (*e.g.*, QSSPC), and could enable mapping when coupled to an XY stage. Initial measurements were conducted on kerfless materials at room temperature; future work beyond the scope of the F-PACE project entails full temperature dependence of the lifetime measurement.

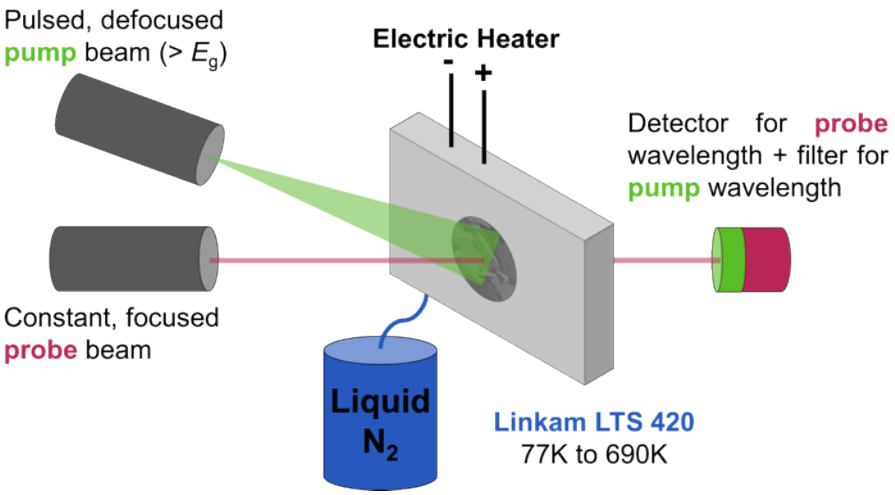


Figure 8.1. Temperature stage with free-carrier absorption lifetime measurement.

Subtask 8.2: Defect minimization and annealing following rear laser processing.
Subtask goal: Micro-Raman and cross-section TEM to determine laser-induced damage. Recover crystallinity to within detection limits, or demonstration that lack of crystallinity does not impact device performance.
Status: Partially accomplished.
Highlights:

- Determined that metal-silicon interface will be recombination active, even when sub-surface laser damage is minimized.
- Determined optimal laser process conditions to minimize surface recombination due to laser-fired contact.

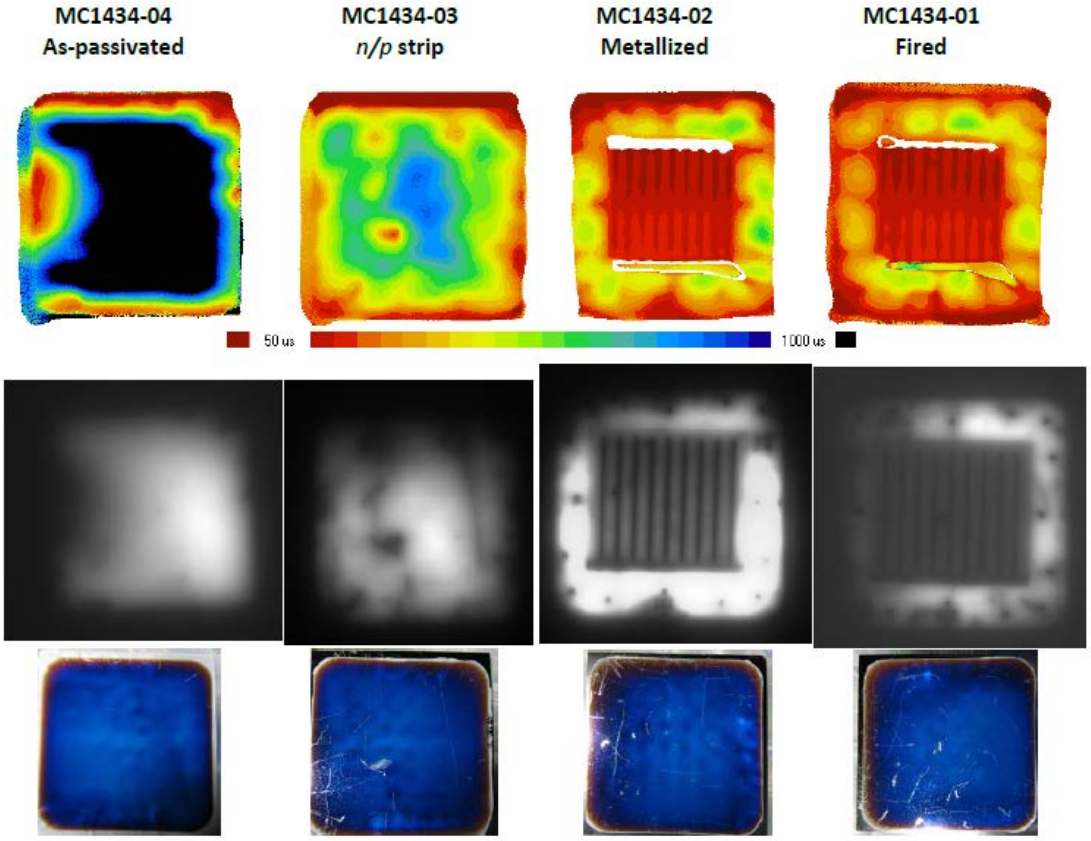


Figure 8.2: PLI and optical microscope images of a wafer at various stages of solar-cell fabrication.

We have established Photoconductance-Calibrated Photoluminscence Imaging (PC-PLI) as quantitative method to evaluate the electrical impact of laser processing. We have determined that 2 mm scribed squares and polished wafers provide optimal for characterization. A standard measurement sequence involves measuring spatially

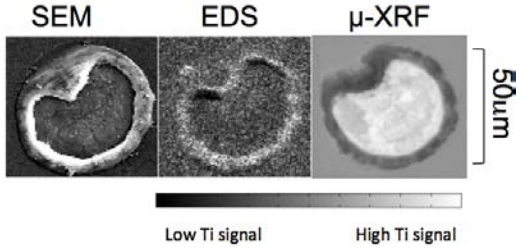


Figure 8.3. (From left to right) A scanning electron micrograph, Ti channel EDS map, and Ti channel μ-XRF map of a LFC spot. Brightness corresponds to detected elemental concentration.

resolved lifetime at various stages of the manufacturing process, as shown in **Figure 8.2**.

We developed a suite of microanalytical tools to examine the electrical and structural properties of LFC's, exemplified by the synchrotron-based µ-XRF flyscan map shown in **Figure 8.3**.

After testing various lasing conditions, the following hypotheses appear to be consistent with the data:

- Metal-silicon contact results in high surface recombination velocity (SRV), an apparent inevitability of laser-fired contacts.
- To minimize SRV at an LFC, the contact area between the metal and the silicon must be minimized. Nevertheless, the contact area must be sufficiently large to achieve targeted contact resistance, lest fill factor decrease.
- A combination of green laser (to form a small incision in the dielectric) and infrared laser (to reflow the metal into the incision, making a small area of metal contact with silicon) may be the optimal combination to enable high lifetime and low SRV (**Figure 8.4**).

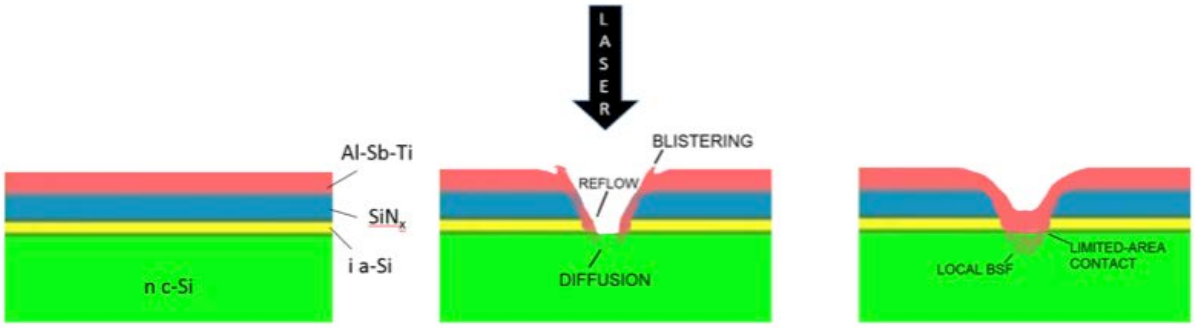


Figure 8.4. Cartoon of our current understanding of laser-matter interactions during the LFC process (middle), as determined by electrical and structural measurements of initial (left) and final (right) conditions. We currently understand optimal LFC formation conditions to be defined by the following characteristics: high lifetime is enabled by (1) limited contact area and (2) limited sub-surface damage, while good contact resistivity is enabled by (3) sufficient SiNx removal, (4) sufficient metal reflow, and possibly (5) sufficient Sb diffusion into the underlying silicon to create a local BSF.

Subtask 8.3: Codify and document, in a review article, principal lifetime-limiting defects in silicon wafers.

Subtask goal: Complete and submit a review article focused on nature, evaluation, and mitigation of most deleterious performance-limiting defects in solar-grade silicon wafers.
Status: Accomplished.
Highlights:

- Paper accepted for publication in Progress in Photovoltaics, reviewing the defect engineering approach for novel absorbers.[43] **Figures 1.1** and **1.2** are key figures in the paper.

We wrote a review paper that distills learnings from this F-PACE project, regarding how to achieve high lifetimes in non-traditional silicon absorbers (including kerfless wafers) by means of defect engineering. The goal of this review article is to discuss the techniques that have been implemented at the growth- and cell-production stage that had led to an outstanding improvement in the electrical performance of the final solar cell devices. This article not only summarizes existing literature, it also defines the material quality targets expected for high efficiency thin kerfless solar cells.

Task 9: Passivation and front surface texturing of thin kerfless Si wafers

MIT trained IEC students and scientists to exfoliate the 60 µm kerfless epi wafers from their substrate. IEC developed procedures for scribing them into 1x1 inch pieces, then cleaning, etching, and handling these substrates in the PECVD, sputtering, and metallization systems. Run MC1422 included standard 1D FJ cells with the emitter on the front (epi side) or rear (substrate side), to evaluate the quality of each surface, as well as with and without texture etching at IEC. The substrate side experiences traumatic cleaving and could have a higher level of defects. Cells had effective lifetimes of 100-200 usec from QSSPC after depositing the front and back a-Si buffer and doped layers. Table 9.1 shows the device results from all pieces from MC1422 processed with front side or back side emitters and smooth or textured surfaces. There was no difference between which side was fabricated with the emitter. Efficiencies of ~16% were obtained and yield was 100%. JV curves are shown in Figure 9.1. Texture increased the short and long wavelength QE as expected as shown in Figure 9.2.

Table 9.1. JV performance of front HJ cells on 60 µm exfoliated wafers.

Piece #	Surface	Emitter	Voc	Jsc	FF	Eff	Avg Eff
MC1422-01	Non-text	Top side	0.648	27.9	76.5	13.8	13.5
MC1422-02			0.663	27.9	75.8	14.0	13.9
MC1422-03	Text		0.654	32.1	75.9	15.9	15.7
MC1422-04			0.657	32.0	76.2	16.0	15.8
MC1422-05	Non-text	Substrate side	0.660	28.0	75.5	14.0	13.7
MC1422-06			0.675	28.6	74.8	14.4	14.1
MC1422-07	Text		0.659	32.0	75.7	16.0	15.9
MC1422-08			0.658	31.8	74.7	15.5	15.5

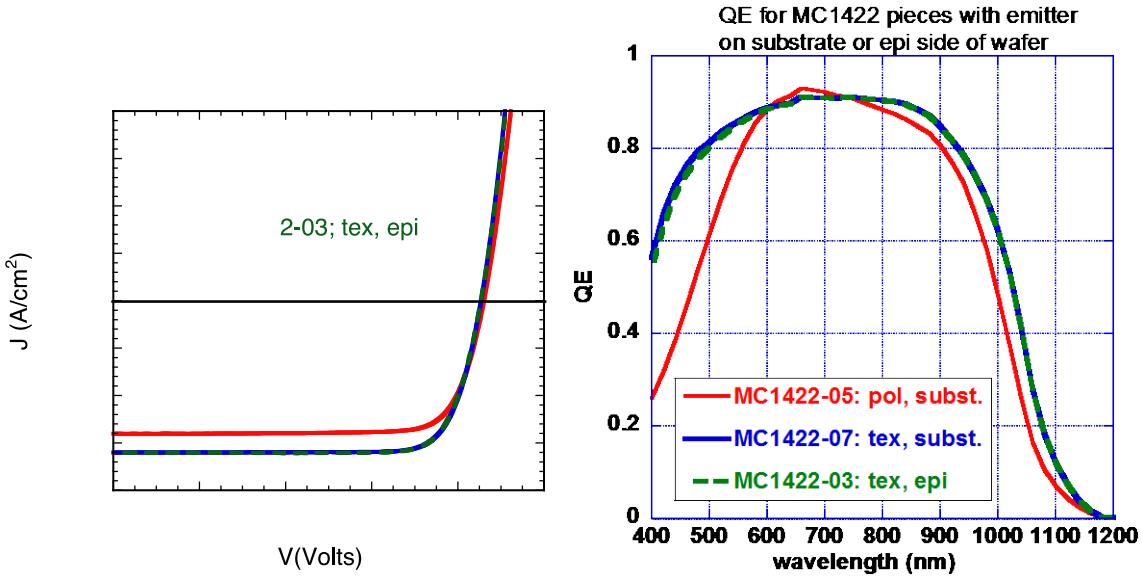


Figure 9.1. (left) JV curves of on kerfless Si wafers with emitter on epi or substrate side with polished or textured surfaces.
Figure 9.2. (right) QE curves of the same devices on kerfless Si.

The next step for this Task was to investigate the front texture and passivation appropriate for an IBC cell. Several runs of kerfless wafers were processed at IEC and obtained very good lifetime and iVoc. However, no devices survived to final JV testing in contrast to FJ device run MC1422 which had yield of 8/8 . Run MC1461 initially started with 5 pieces of kerfless and 3 pieces of standard 300 µm FZ Si. All of the kerfless wafers broke during processing either in the ultrasonic clean, photoresist spin coating (vacuum chuck) or other manual handling. We determined that cutting the 1x1 inch squares along a different orientation from the exfoliated wafer would likely reduce the tendency to break along cleavage planes. Run MC1464 started with 8 wafers. While less wafers broke, the metal adhesion on the n-strip was poor and no devices could be tested. However, the lifetimes and iVoc of these two runs were quite good. Table 9.2 compares the parameters for kerfless wafers from these runs. Clearly we are able to passivate both of the peeled surfaces and obtain good lifetimes prior to metallization. Results in Tables 9.1 and 9.2 verify that we were able to etch and passivate the thin wafers and fabricate them into standard heterojunction cells but also confirm that the IBC process we had developed for 150 µm wafers including multiple photolithography steps needed to be modified for the 60 µm kerfless wafers to reduce breakage. This effort is described in Task 10.

Table 9.2 Lifetime and implied Voc on kerfless 60 µm cells from QSSPC and Voc and efficiency from cell test measurements. QSSPC on the IBC cells was after front surface texture, front and rear passivation, and doped layer deposition and patterning, prior to first metal contact. The IBC cells were unable to be tested as described in the text.

Run #	Type of device	Lifetime (µsec)	iVoc (V)	Eff (%)	Voc (V)
MC1422	FHJ	100	0.670	16.0	0.660
MC1461	IBC	350	0.710	X	X
MC1466	IBC	150	0.690	X	X

We verified that iVoc increased with decreasing thickness as expected due to reduced bulk recombination. Fig.9.3 shows the implied V_{OC} (iV_{OC}) estimated from Sinton QSSPC lifetime measurement as a function of wafer thickness at two different stages of cell fabrication process. The initial stack layer passivation clearly indicates that the iV_{OC} increases with the thinner wafers as predicted by theory due to reduced volume recombination but only with sufficient surface passivation. The formation of interdigitated p-n strip reduces iV_{OC} more on thinner wafers. This is understandable since the thinner wafers are more surface sensitive and p-strip consisting of i/p layers has inferior surface passivation quality than i/n layers.

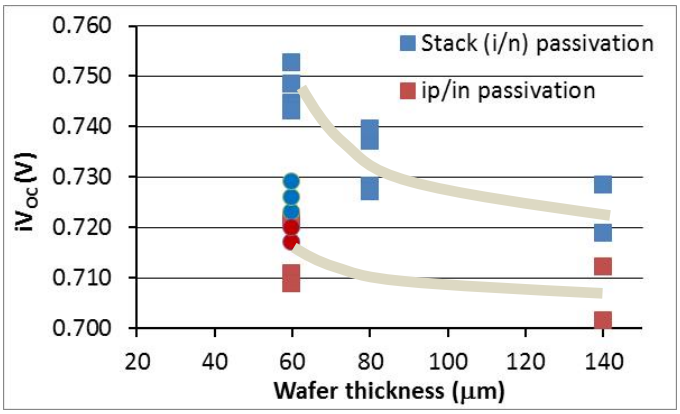


Fig. 9.3: iV_{OC} estimated from Sinton QSSPC lifetime measurement as a function of wafer thickness at two stages of fabrication process. The squares represent chemically thinned Cz wafers. The circles represent as-grown 60 um kerfless wafers.

Front surface texturing is of critical importance to reduce front surface reflection and to increase long wavelength absorption. Jsc values on our best cells have been around 38-39 mA/cm^2 compared to 40-41 mA/cm^2 for record IBC-HJ cells reported by others. We showed that there was little change in Jsc or total integrated reflection with application of a MgF_2 antireflection (AR) layer confirming that our front AR stack and Si texture were optimized for minimal front reflection losses. Thus, we performed a simple analysis of our long wavelength QE losses compared to those of the record IBC-HJ cell from Panasonic.
Figure 9.4a compares the QE on 2 of the better IBC-HJ cells made at IEC with that of the record IBC-HJ Si cell from Panasonic[44]. While the Panasonic cell has slightly higher QE in the region 400-900 nm, it is significantly higher beyond 900 nm. Since both groups use 150 um Cz wafers, the difference not due to increased thickness or starting wafer quality. Figure 9.4b shows the QE again for one of our cells and the absorption plotted as 1-Reflection. The absorption is flat and near 1 from 400-900 nm confirming

good AR layers and front surface texture. The absorption remains high ~ 0.8 even beyond the Si band edge.

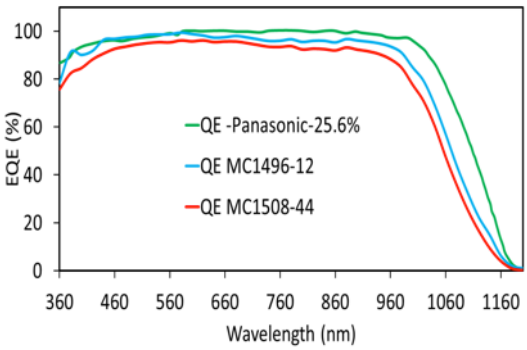


Figure 9.4a QE for IBC cells: Panasonic record and 2 IEC

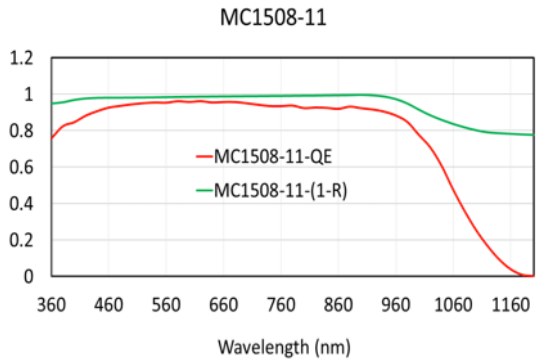


Figure 9.4b QE and Absorption (1-Reflection) for IEC IBC cell

Table 9.1 JV performance of IBC-HJ cells: record from Panasonic and IEC

Cell	V_{oc} (V)	I_{sc} (mA/cm^2)	FF (%)	Eff (%)
Panasonic	0.740	41.80	82.7	25.6
MC1508-11	0.680	38.17	75.2	19.5

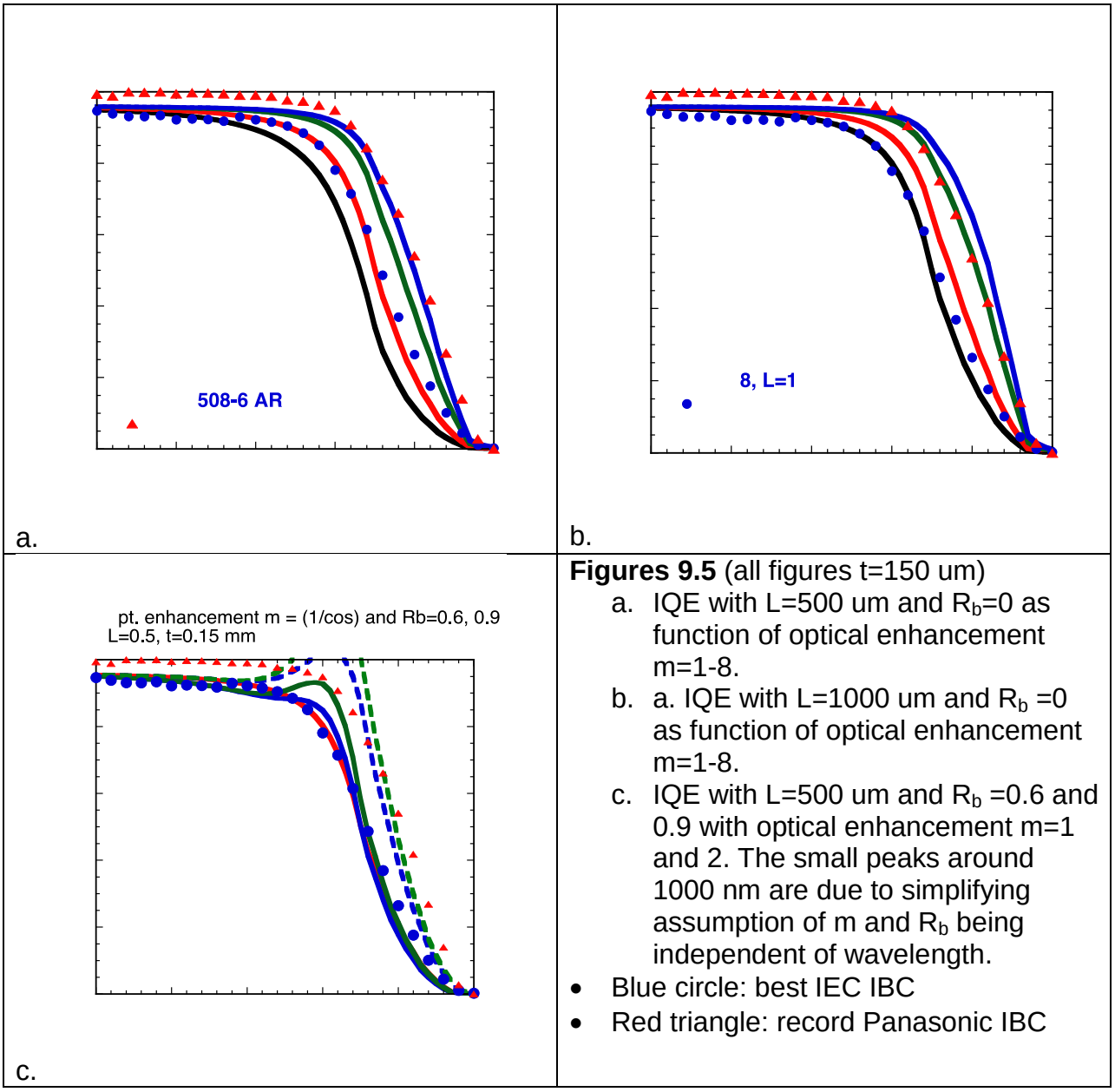
We applied a very simple model of QE containing the 4 critical parameters that can influence the long wavelength QE (LWQE) as lumped parameters (L, m, R_b, and t). The equation for the internal QE (IQE) is

$$IQE=IQE_{max} * [\alpha L/(\alpha L+ (1/m)] * (1+R_b \exp (- \alpha t)) \qquad \text{Eq.9.1}$$

Where •IQE_{max} = 0.96, typical of our cell's peak IQE accounting for front optical losses
- •L= diffusion length 500 µm (baseline) or 1000 µm
- •t=Si wafer thickness, fixed at 150 um
- •m=1/cosθ accounts for increased pathlength due to scattering, m=1-8 with 2-3 typically reported (actually m is function of wavelength but for simplicity kept constant here)
- •R_b=back reflection of metal/a-Si interface also weak f(λ) but constant here With R_b=0.6 for Al/a-Si, = 0.9 for Ag/a-Si based on experience

We investigated the impact of realistic improvement in L, m, and R_b. Calculations (solid lines) and data (symbols) are shown in Figures 9.5 a-c. In general, the optical path enhancement m has the greatest influence. Figures 9.5a and 9.5b show the LWQE for 4 values of optical path enhancement m for diffusion lengths L = 0.5 and 1.0 mm, respectively. The symbols show the measured QE for IBC cells made at IEC and Panasonic. The Panasonic cells are consistent with m=5-8 while the IEC cells are consistent with m=1-2, depending on the diffusion length. It is certainly likely the

Panasonic cell has both higher m and L compared to the IEC cell but this data shows the relative impact of each. Figure 9.5c shows the effect of increasing the R_b from 0 (as in Figures 9.5 a,b) to 0.6 or 0.9 for m=1 or 2. Clearly m has much greater effect than R_b. From this analysis, we conclude that we need to increase both the optical pathlength via better light scattering and the diffusion length via lower back SRV to increase the LWQE in order for our Jsc to approach the record cell. Increasing the back reflection has little benefit at this wafer thickness but will become important as the wafers get thinner.



Figures 9.5 (all figures t=150 um)

a. IQE with L=500 um and R_b=0 as function of optical enhancement m=1-8.
b. a. IQE with L=1000 um and R_b =0 as function of optical enhancement m=1-8.
c. IQE with L=500 um and R_b =0.6 and 0.9 with optical enhancement m=1 and 2. The small peaks around 1000 nm are due to simplifying assumption of m and R_b being independent of wavelength.

- Blue circle: best IEC IBC
- Red triangle: record Panasonic IBC

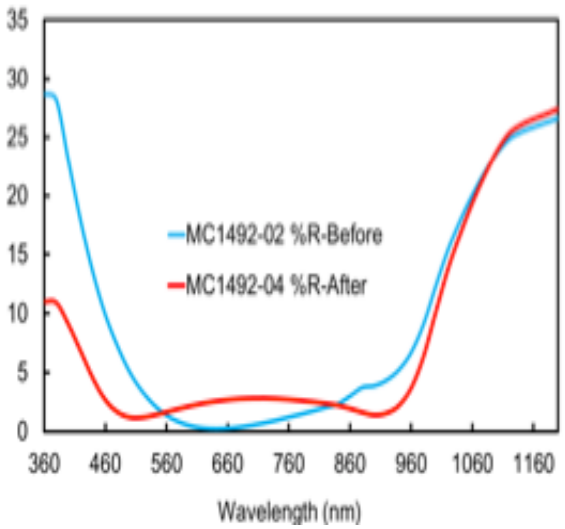
Task 10: IBC-SHJ device architecture

Subtask 10.1: Develop and integrate IBC device architecture

Results: This task focused on: 1. Investigating new front stack passivation methods and optimizing them in terms of antireflection (AR) and electrical passivation properties; 2. Developing new rear contact patterning using masked deposition and structures applicable to thin kerfless wafers; 3. Determining how rear contact processing and patterning influences device performance and stability.

Regarding the front stack, in the first half of the project we had optimized the texture using TMAH etching and passivation and optical antireflection quality with an a-Si/a-SiN/a-SiC triple stack. Here, we investigated additional anti-reflection (AR) layers (MgF_2) and a wide range of front layers including a diffused n+ front surface field (FSF).

Front surface reflection on our cells is typically near zero in the range 500-700 nm (figure 9.4b shows the absorption is ~1 from 500-700 nm) and rises at both shorter and longer wavelengths as seen in Figure 10.1a. We investigated 3 thicknesses of MgF_2 as an AR layer – 90, 120, 150 nm. Note that when the surface is textured, there is less sensitivity to specific AR thickness since light is now not normal incidence but is scattered at different angles. We found little difference in the overall change in reflection with thickness but there were differences where the minimum was and how high the reflection was at lower and higher wavelengths. For all three MgF_2 thicknesses, we found that the blue reflection decreases but a small increase due to a broad peak appears in the mid-range where R was previously near zero. The intensity of the solar spectrum is quite large in this range so small increases in reflection can offset much larger changes in reflection at 350-450 nm. Figure 10.1b shows IQE of two IBC cells having efficiency ~19% where MC1492-02 or -04 had a n+ FSF diffusion and MC1496-11 did not. Table 10.1 lists the Jsc and AM1.5 integrated QE before and after AR layer deposition. The difference in AM1.5 integrated reflection is also given. In general, the AR layer improves the optical generation by 0.5-1 mA/cm^2. This relatively small gain shows that the front surface is already well optimized optically.



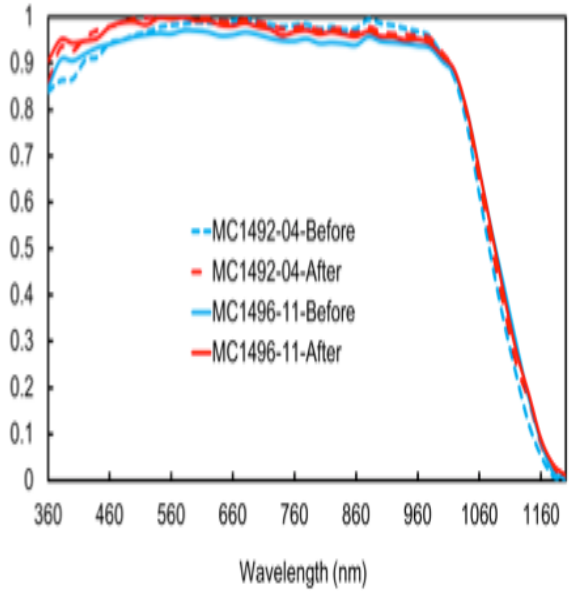


Figure 10.1a) Reflection of IBC cell before and after 120 nm MgF_2 AR layer

Figure 10.1b) IQE of 2 IBC cells before and after MgF_2. IQE in Table 10.1

Table 10.1 Changes in optical photocurrent with MgF_2 AR layer from measured Jsc, and from integration of QE and reflection with AM1.5 spectra. MC1492 pieces had an n+ FSF diffusion and MC1496 did not.

Cell	J_{sc} (mA/cm^2)			IQE (mA/cm^2)			Refl*AM1.5
	Before	After	Δ	Before	After	Δ	Δ
MC1492-02 FSF	37.4	38.0	0.60	37.84	38.69	0.85	0.56
MC1492-04 FSF	37.1	37.8	0.70	37.84	38.85	1.01	0.56
MC1496-11 No FSF	37.8	38.2	0.40	38.02	39.11	1.09	0.72

Regarding the front passivation, while there are reports in the literature of IBC-HJ cells using a-Si i/a-SiN (our baseline), a diffused n+ FSF/a-SiN are also very common. If the role of the front passivation was to repel holes and passivate the Si surface, then perhaps the roles of the diffused n+ FSF/a-Si i-layer could be merged into a single a-Si n-layer with less optical losses and processing. We fabricated devices with a-Si n and a-Si i+n layers capped with our standard a-SiN/a-SiC. We also investigated minor changes to the thickness and bandgap of the standard front a-Si i-layer. Results of the best cells for each are in Table 10.2 and the QE curves are in Figures 10.2a and 10.2b. Deposition of an a-Si n-layer (MC1503-08) directly on the wafer is clearly damaging to the front SRV as evidenced by the low lifetime, iVoc, Voc and blue response (figure 10.2a). Depositing a 10 nm i-layer underneath (MC1503-04) alleviates the negative impact of the defective n-layer but adds additional front absorption losses compared to the standard 8 nm control (MC1510-03). However, reducing the i-layer further to 4 nm or widening the bandgap has no benefit in optical losses within experimental error but does not seem to impact the passivation or SRV.

Table 10.2 Performance of IBC cells with various front surface architecture. All cells received 20 sec HNA etch prior to depositions and had a-SiN/a-SiC stack on top of the

front surface layers. Lifetime and implied Voc measured by QSSPC on devices after all processing and patterning but before metallization.

MC#	Front surface	τ(strip)	iVoc (strip)	Voc(V)	Jsc (mA/sqcm)	F.F (%)	Eff. (%)
1503-04	i/n(20nm)	1314	0.696	0.627	35.4	74.5	16.4
1503-08	n(40nm)	320	0.650	0.623	34.1	72.3	15.4
1510-03	4nm a-Si	846	0.683	0.621	37.9	73.4	17.3
1510-05	8nm a-Si	1425	0.706	0.638	38.5	74.9	18.4
1510-09	1.8 eV a-Si	1649	0.710	0.635	38.0	71.0	17.2

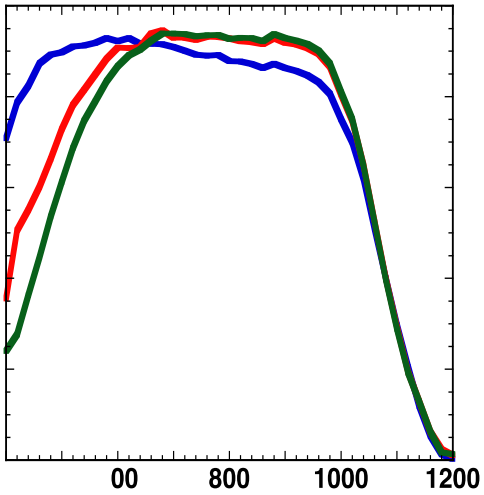


Figure 10.2a) QE of IBC cells from Table 10.2 with different front a-Si layers. MC1510-05 is control also in Figure 10.2b.

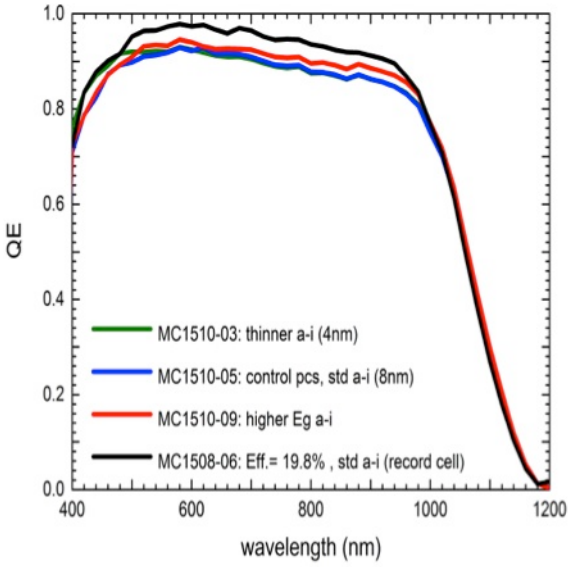


Figure 10.2b) QE of IBC cells from Table 10.2 with different front a-Si i-layer properties.

Using the 20 sec HNA pre-deposition etching and 3 step photolithography, we have obtained 10 cells from 4 different experiments having efficiencies of 19-20%. The diffused FSF had no effect – about half these pieces had a n+ FSF and half did not. Table 10.3 lists the JV performance of one of the best cells tested over ~11 months and after MgF2. A slight decrease in FF is apparent.

Table 10.3 Performance of IBC cell MC1508-11 measured over ~11 months. Masked area = 1.61 cm^2. The negligible gain in Jsc with MgF_2 was due to slight increase in mid-range reflection as shown in figure 10.1.

Date	comment	Voc(V)	Jsc (mA/sqcm)	F.F (%)	Eff. (%)
07/30/14	Initial	0.680	38.2	75.2	19.6
08/13/14	Retest	0.680	38.2	75.0	19.6
08/15/14	MgF2	0.681	38.5	74.6	19.5
09/18/14	Retest	0.680	38.5	74.1	19.2
12/15/14	Retest	0.696	38.1	76.2	19.5
06/17/15	Retest	0.683	38.1	74.5	19.4

However the 3 steps of photolithography are not practical for thin kerfless wafers due to their fragility on the spin coater and aligner as discussed in Task 9. Efforts to combine the LFC with a single metallization step and blanket p-layer without any photolithography were presented above in Task 7. Such cells have low Voc ~ 0.58 V and FF ~ 60% which are attributed to a floating parasitic p/n junction under the n-metal strip where the recombination rate is $>10^5$cm/s, acting as a sink for minority and majority carrier to recombine before getting collected. An alternative simplified process was needed, where the base contact had either a dielectric insulator or n+ layer under the metal to prevent recombination under shorted metal/p/i LFC base contact.

IEC investigated a new approach using masks during PECVD deposition to provide spatially isolated p and n a-Si regions. The device structure is shown in figure 10.4a. A brief description of the process sequence follows. After standard cleaning and etching, the standard front stack (i a-Si / a-SiN / a-SiC) is deposited followed by a blanket deposition of a new back surface passivation (i.a-Si / a-SiN) stack. Next, n a-Si is deposited through an n-strip mask. An HF etch removes a-SiNx from p-strip regions (2%, 60 sec). Then, a blanket p a-Si layer is deposited. The p-strip over the n-strip is not a barrier since it is shorted by the LFC. The p-strip Al is deposited through the p-strip mask and the n-strip is deposited through the n-mask. An LFC is needed to create the base contact. Cells with narrow gap (25 um) tended to be shunted due to the difficulty of visually aligning the metal masks so IPG made laser-cut masks with wider gaps (~100 um).

In figure 10.3a) we show the main processing steps in our standard 3-steps photolithography (PL) IBC-SHJ device fabrication and in figure 10.3 b) the newly

developed non-photolithographic process with masked film and metal deposition. This process needs a LFC to form base contact.

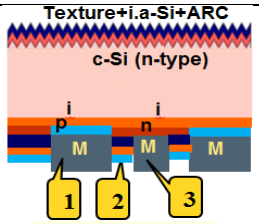
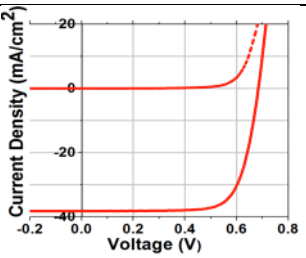
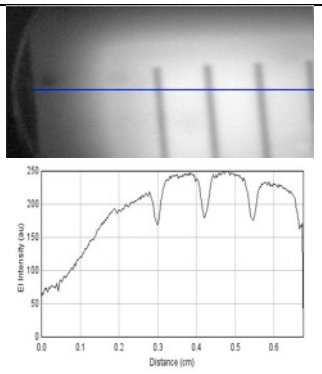
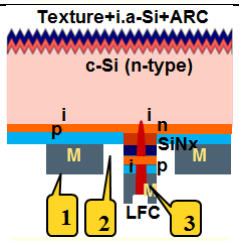
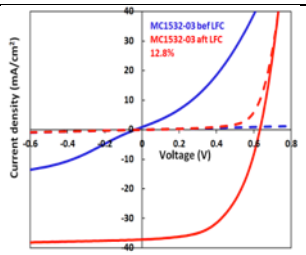
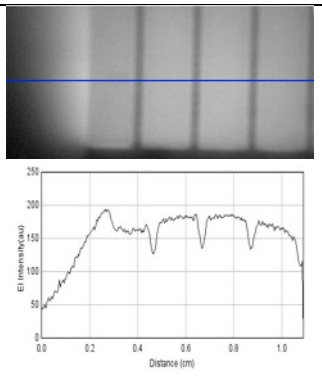
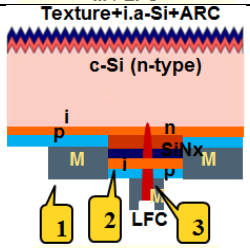
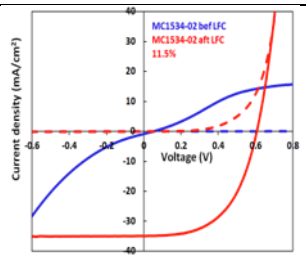
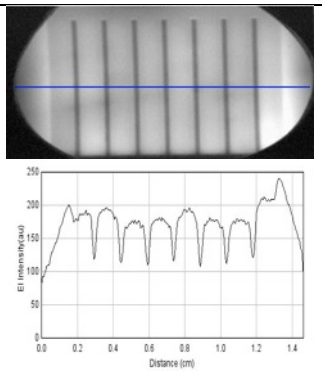
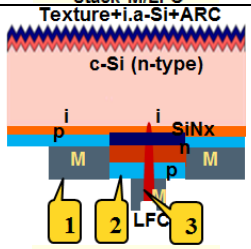
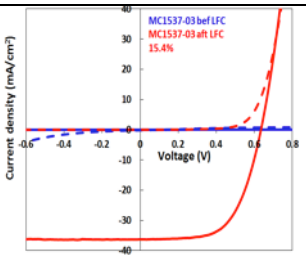
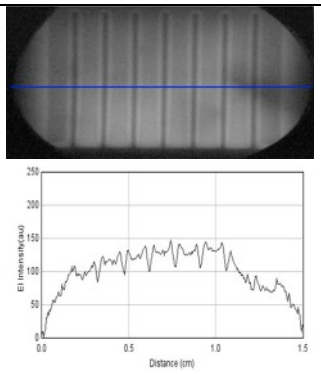
Figure 10.3. Process flow for the 2 different patterning processes: a) 3-step PL; b) masked deposition (MD)

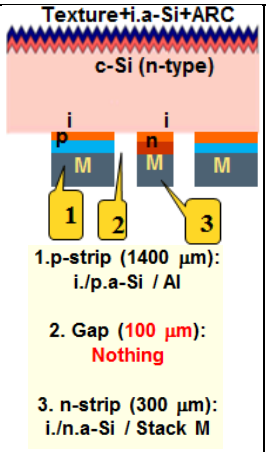
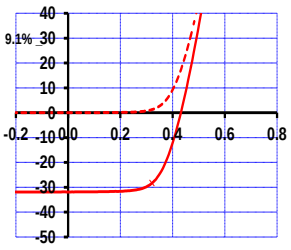
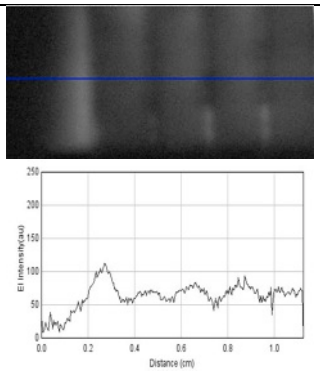
From the process sequences shown above, with masked deposition method we can reduce / eliminate the process induced stress with a more practical handling of thin fragile wafers, thus improve the yields of IBC-SHJ device. Note that during the masked deposition process steps (highlighted with * above) we can modify the emitter-base gap structure and its layer composition by depositing different rear passivation stacks with corresponding etching.

To further understand how the electric field and charge distribution across the path between emitter and base (the gap region) will affect device performance, we utilized masked deposition to fabricate IBC-SHJ device with different gaps as described in table 10.4.

Table 10.4 IBC-SHJ device fabricated with 3-steps photolith. and masked deposition (classified as 4 types) , device structure varies in both gap compositions and geometric dimensions of gap and p , n strips. E.C. is the emitter coverage of the active cell area. Last column shows the EL image and line scan across the p & n strips.

Fabrication	Device structure	Device data	EL images

3-steps photolith. Gap i/n E.C.=82.3%	 1. p-strip (1400 μm) : i./p.a-Si / Al 2. Gap (25 μm) : i./n./SiNx/i./p.a-Si 3. n-strip (250 μm) : i./n.a-Si / Stack M	 Voc=684mV Jsc=38.4mA.cm-2 FF=75% Eff.=19.6%	 Bright: p strips Dark: n strips
Masked depo. Cell type I Gap i/p E.C.=76.2%	 1. p-strip (1300 μm): i./p.a-Si / Al 2. Gap (100um): i./p.a-Si 3. n-strip (400 μm): i./n./SiNx/i./p.a-Si / Stack M / LFC	 Blue: Before LFC Red: After LFC Voc=633mV Jsc=37.2mA.cm-2 FF=54% Eff.=12.8%	 Bright: p strips Dark: n strips Brighter around n strips:Gap
Masked depo. Cell type II Gap i/n E.C.=76.2%	 1. p-strip (1300 μm) : i./p.a-Si / Al 2. Gap (100 μm) : i./n./SiNx/i./p.a-Si 3. n-strip (400 μm) : i./n./SiNx/i./p.a-Si / Stack M/LFC	 Blue: Before LFC Red: After LFC Voc=607mV Jsc=34.3mA.cm-2 FF=54% Eff.=11.5%	 Bright: p strips Dark: n strips
Masked depo. Cell typeIII Gap i/SiNx E.C.=76.2%	 1. p-strip (1300 μm) : i./p.a-Si / Al 2. Gap (100 μm) : i./SiNx/n./p.a-Si 3. n-strip (400 μm) : i./SiNx/n./p.a-Si / Stack M/LFC	 Blue: Before LFC Red: After LFC Voc=656mV Jsc=36.6mA.cm-2 FF=64% Eff.=15.4%	 Bright: p strips Dark: n strips Brighter around n strips:Gap

Masked depo. Cell type IV Gap none E.C.=76.2%		 Voc=432mV Jsc=31.9mA.cm-2 FF=66% Eff.=9.1%	 Bright: p strips Dark: n strips, same as outside active cell area

IBC-SHJ device fabricated with photolithography has overall the best performance, achieving efficiency ~20%. The type I and II mask deposited cells consist of gap structures of i/p and i/n respectively and both have similar JV performances with efficiency of ~12% and with a low FF<60%. The JV curve indicates a voltage-dependent collection with diode ideality factor >2 at MPPT. The voltage dependent carrier transport can be seen as the blue light JV curve before LFC. It is apparent that the band bending and the charge in the gap region, regardless of charge polarity, is affecting the voltage dependent hole collection in cells after LFC. The type III and IV MD cells consist of gap regions that are passivated by i/a-SiNx or nothing respectively which reduces/eliminates the presence of charge in the gap regions. These cells exhibit much higher FF of >64% but are still significantly lower than the PL cell. A wider gap width (25 μm in photolithographic cell vs 100 μm in masked cells) and/or lower emitter coverage in masked deposited cells may limit the achievable FF. The highest efficiency we achieved using i/a-SiNx gap structure in type III mask deposited cells is 15.7%. Type III and IV cells have a similar FF but type III cells have a very low efficiency because they lack passivation in the gap region, which reduces both V_{OC} and J_{SC}. The EL image of type IV cell shows very low luminescence intensity over the entire cell representing a severe surface passivation loss due to unpassivated gap. A striking difference in EL images between PL cell and MD cells appear in the margins outside of the metallized cell area. In photolithographic cells, the regions outside of the cell area are passivated by i/n layers and appear **darker** than the p-strip, whereas, in type I, II and III masked deposited cells, the regions are passivated by i/n layers and appear **brighter**. We know from other passivation studies that the i/n is a slightly better passivation layer but this difference does not explain the large difference in EL intensity. Table 10.5 summarizes the best cell performance with the 2 step photolithography and with the photolithography-free masked patterning.

Table 10.5 Performance of best IBC cells with either photolithography patterning (PL) and masked deposition (MD) photolithography-free patterning. All cells received 20 sec HNA etch prior to depositions and had a-SiN/a-SiC stack on top of the front surface layers without diffused n+ FSF. Lifetime and implied Voc measured by QSSPC on

devices after all processing and patterning but before metallization. Piece 1560-01 had the 2-stage a-Si p-layer with high/low doping, all others had a 1 stage p-layer.

MC#	Wafer 140 um	Patt-ern	Gap (um)	LFC	τ usec (strip)	iVoc V (strip)	V_{OC} V	J_{SC} mA/cm^2	FF %	Eff %
MC1560-04	Cz	PL	25	yes	2010	0.722	0.657	37.8	67.6	16.8
1537-03	Cz	MD	100	yes	502	0.675	0.656	36.6	64.2	15.4
MC1559-05	KFLS	PL	25	yes	456	0.689	0.642	35.9	72.4	16.7
1560-01	Cz	PL	25	no	2560	0.727	0.696	38.08	76.2	20.2

It has been standard practice at IEC to measure each IBC cell with 2 masks having illumination areas of 1.61 and 2.56 cm^2. The total defined metallization area of the cells is 2.56 cm^2. It is always found that as the masked area decreases, Voc decreases as expected because the dark junction area is the same, but Jsc and FF both increase. The increase in Jsc is likely due to excluding the n-strip bus bar which is electrically dead for collecting carriers, and reasons for FF are complex and only partly related to series resistance losses as discussed above in Task 6. In January 2015 one of our IBC cells was tested at NREL using yet a different mask area. The results are below in table 10.6 and in Figure 10.4. Trends in Voc, Jsc and Efficiency are monotonic with illumination area while FF is not. Note that the NREL measurement verifies an efficiency of 19.7% for our program.

Table 10.6. JV parameters of IBC cell MC1508-06 measured at IEC or NREL with different illuminated mask areas.

Masked area cm^2	JV measured	Voc (V)	Jsc (mA/cm^2)	FF	Eff (%)
2.5000	IEC	0.690	36.3	0.705	17.6
1.6100	IEC	0.681	37.9	0.746	19.2
0.99000	NREL	0.667	40.1	0.738	19.7

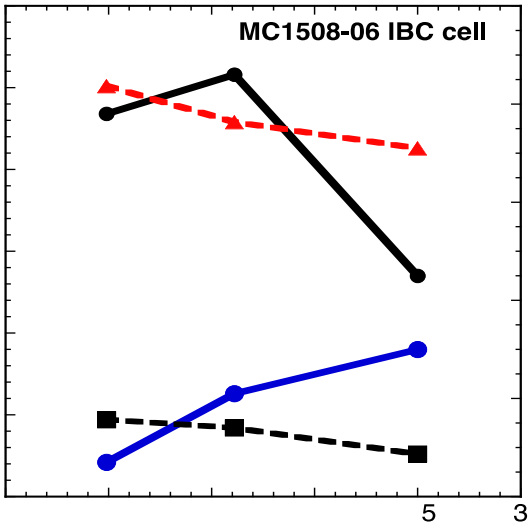


Figure 10.4. JV parameters for MC1508-06 measured with different mask areas. Values listed in Table 10.3. The 1.0 cm^2 area was measured at NREL, the two larger areas at IEC.

We also determined that even for storage in a dessicator, the stability over time of IBC-SHJ solar cells depended on the patterning approach used, in particular, on the gap structure between emitter and base contact. This was presented elsewhere[45] .Previous standard two-step photolithography SHJ-IBC process results in photoresist in the PECVD chamber during doped-layer patterning. This may lead to photoresist outgassing in the PECVD chamber and also limits the deposition temperature to <200°C. Together, these can result in contaminated a-Si:H doped layers, poor repeatability, and low FF. This processing also forms the interdigitated contacts resulting in a gap that is insufficiently passivated, having only a a-Si layer, and susceptible to atmosphere-induced degradation, even with dark storage in a dry environment. We found that cells where the 25 µm gap is passivated primarily with a thin uncapped a-Si layer will have poor stability. The efficiency degrades primarily due to decreases in Voc and FF. Voc degradation results from poor gap passivation on the back and is in accordance with the instability of the single intrinsic a-Si:H layer over time.

The new IBC process flow and device structure resulting from using a-SiN_x:H for patterning forms clean a-Si layers and creates a thicker multi-layer gap structure and yields devices with improved performance that are stable over months[45]. Figure 10.5 shows efficiency for 4 IBC cells with 19-20% efficiency measured over periods of storage from 50-300 days with essentially no degradation. The multi-layer gap passivation by the new patterning approach allows a multilayer passivation stack which could include a-i / a-n / a-SiN_x / a-i / a-p in the gap region instead of only a-i as by the previous two-step photolithography process. Better gap passivation leads to improved cell stability.

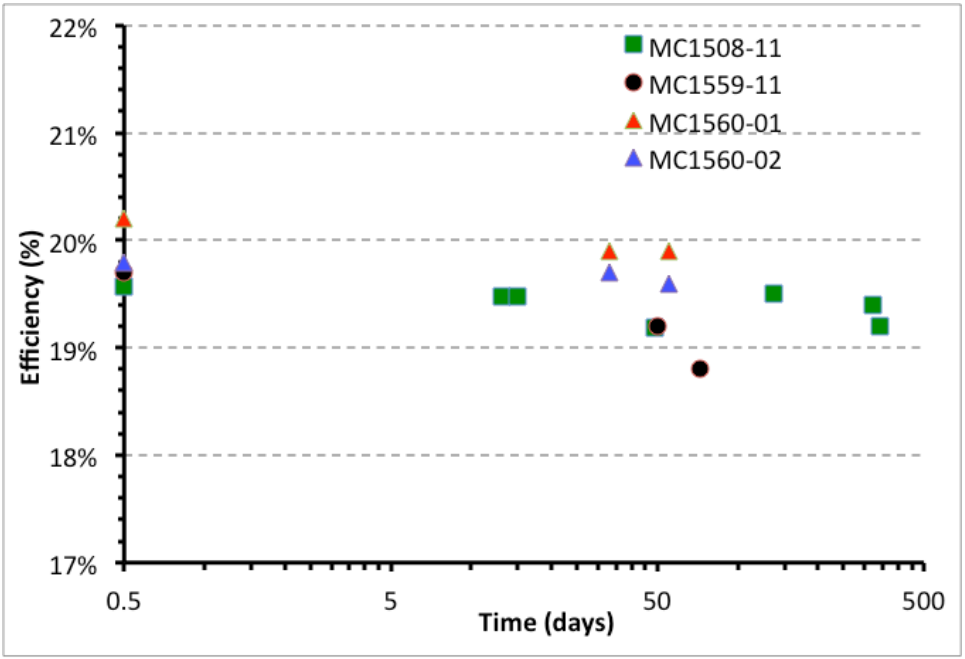


Figure 10.5 Efficiency of 4 IBC cells with multi-layer stacks in the gap, measured repeatedly over 50-300 days.

Subtask 10.2 Fabricate proof-of-concept module
At the beginning of the contract, it was our intention to fabricate encapsulated mini-modules out of ~4-6 series connected IBC cells. However, we ran out of time and did not produce any cells with tabs or electrical surface mounting.

Educational achievements and support

Education and training of post-doctoral researchers, graduate and undergraduate students is an important outcome from this FPACE project. The number of students partially or totally supported by this funding is approximately as follows: 9 PHD (Electrical Engineering, Materials Science, Mechanical Engineering and Physics), 3 Masters degrees (Electrical Engineering, Mechanical Engineering), and 3 undergraduate laboratory assistants. Note that 12 graduate students far exceeds the original commitment to support 2 students each at UD and MIT, demonstrating the commitment to education and training at each of the locations.

The following students received all or some of their support and training funded by this program listed by graduation date.

Name	MS/Ph.D, University	Graduation date
Lulu Zhang	Ph.D Physics, UD	Jun-13

Brent (Zhan) Shu	Ph.D Physics, UD	Jul-13
Hyunjoo Choi	Postdoc, MIT	Aug-13
Christine Simmons	Postdoc, MIT	Jan-14
David Fenning	Ph.D., Mechanical Engineering, MIT	May-14
Joseph Sullivan	Ph.D., Mechanical Engineering, MIT	May-14
Veronica Mest	BS, Electrical and Computer Engineering UD (lab asst)	May-14
Stephanie Scott	S.M., Mechanical Engineering, MIT	Jun-14
Maulid Kivambe	Postdoc, MIT	Aug-14
Judith Hsieh	M.S. Electrical+ Computer Engr, UD	Dec-14
Jasmin Hofstetter	Postdoc, MIT	Feb-15
Douglas M. Powell	Ph.D. Mechanical Engineering, MIT	May-15
Jianbo He	Ph.D Matl Science Engineer UD	Jul-15
Mallory Jensen	S.M., Mechanical Engineering, MIT	June-15
Sergio Castellanos	Ph.D, Mechanical Engineering, MIT	Aug-15
Hank Deaton	BS, Electrical and Computer Engineering UD (lab asst)	May-16
Joe Sutton	BS, Electrical and Computer Engineering UD (lab asst)	Dec-15
Stella Hsieh	Ph.D, Matl Science+Engr, UD	June-16
Lei Zhang	PhD Electrical+ Computer Engr, UD	June-16

Journal Publications

1. D.M. Powell, M.T. Winkler, H.J. Choi, C.B. Simmons, D. Berney Needleman, T. Buonassisi, “Crystalline silicon photovoltaics: a cost analysis framework for determining technology pathways to reach baseload electricity costs,” *Energy & Environmental Science* 5, 5874–5883 (2012); (2012)
2. Douglas M. Powell, Mark T. Winkler, Alan Goodrich, and Tonio Buonassisi, “Modeling the cost and minimum sustainable price of crystalline silicon

photovoltaic manufacturing in the United States," *IEEE Journal of Photovoltaics* 3, 662–668 (2013)
3. H. J. Choi, M. I. Bertoni, J. Hofstetter, D. P. Fenning, D. M. Powell, S. Castellanos, and T. Buonassisi, "Dislocation density reduction during impurity gettering in multicrystalline silicon," *IEEE Journal of Photovoltaics* 3, 189–198 (2013)
4. Augusto, D. Pera, H.J. Choi, P. Bellanger, M. C. Brito, J. Maia Alves, A. M. Vallêra, T. Buonassisi, and J.M. Serra, "Residual stress and dislocations density in silicon ribbons grown via optical zone melting," *Journal of Applied Physics* 113, 083510 (2013)
5. A.C. Goodrich, D.M. Powell, T.L. James, M. Woodhouse, and T. Buonassisi, "Assessing the drivers of regional trends in solar photovoltaic manufacturing," *Energy & Environmental Science* 6, 2811–2821 (2013)
6. J. Hofstetter, D.P. Fenning, D.M. Powell, A.E. Morishige, H. Wagner, and T. Buonassisi, "Sorting metrics for customized phosphorus diffusion gettering," *IEEE Journal of Photovoltaics* 4, 1421 (2014)
7. J. Maser, B. Lai, T. Buonassisi, Z. Cai, S. Chen, L. Finney, S.-C. Gleber, C. Jacobsen, [illegible] generation hard X-ray nanoprobe beamline for in situ studies of energy materials and devices," *Metallurgical and Materials Transactions A* 45, 85–97 (2013
8. K. Nakajima, R. Murai, S. Ono, K. Morishita, M.M. Kivambe, D.M. Powell, T. Buonassisi, "Shape and quality of Si single bulk crystals grown inside Si melts using the noncontact crucible method," *Japanese Journal of Applied Physics* 54, 015504 (2015)
9. D.M. Powell, J. Hofstetter, D.P. Fenning, R. Hao, T.S. Ravi, T. Buonassisi, "Effective lifetimes exceeding 300 µs in gettered *p*-type epitaxial kerfless silicon for photovoltaics," *Applied Physics Letters* 103, 263902 (2013)
10. J. Lindroos, D.P. Fenning, D.J. Backlund, E. Verlage, A. Gorgulla, S.K. Estreicher, H. Savin, T. Buonassisi, "Nickel: A very fast diffuser in silicon," *Journal of Applied Physics* 113, 204906 (2013)
11. S Hegedus "Review of photovoltaic module energy yield (kWhr/kW): comparison of crystalline Si and thin film technologies" *Wiley Review of Energy Environ (WIRE)* 2013 , 2: 218–233 doi: 10.1002/wene.61
12. D. Berney Needleman, H. Choi, D.M. Powell, T. Buonassisi, "Rapid dislocation-density mapping of as-cut crystalline silicon wafers," *Physica Status Solidi Rapid Research Letters* 7, 1041–1044 (2013);
13. Z Shu , U Das, JAllen, R Birkmire, S Hegedus, "Experimental and Simulated Analysis of Front versus All-Back-Contact Silicon Heterojunction Solar Cells: Effect of Interface and Doped a-Si:H Layer Defects", *Progress in Photovoltaics* (2013) DOI: 10.1002/pip.2400.
14. S. Castellanos, M. Kivambe, J. Hofstetter, M. Rinio, B. Lai, T. Buonassisi, "Variation of dislocation etch-pit geometry: An indicator of bulk microstructure and recombination activity in multicrystalline silicon," *Journal of Applied Physics* 115, 183511 (2014)

15. J. He, S. Hegedus, U. Das, Z. Shan, M. Bennett, L.Zhang, R. Birkmire "Laser fired contacts for n-type c-Si solar cells" *Progress in Photovoltaics*, published online: 17 June 2014 DOI: 10.1002/pip.2520
16. M.A. Jensen, J. Hofstetter, A.E. Morishige, G. Coletti, B. Lai, D.P. Fenning, T. Buonassisi, "Synchrotron-based analysis of chromium distributions in multicrystalline silicon for solar cells," *Applied Physics Letters* 106, 202104 (2015)
17. S.C. Siah, M.T. Winkler, D.M. Powell, S.W. Johnston, A. Kanevce, D.H. Levi, T. Buonassisi, "Proof-of-concept framework to separate recombination processes in thin silicon wafers using transient free-carrier absorption spectroscopy," *Journal of Applied Physics* 117, 105701 (2015)
18. J. Hofstetter, C. del Cañizo, H. Wagner, S. Castellanos, T. Buonassisi, "Material requirements for the adoption of unconventional silicon crystal and wafer growth techniques for high-efficiency solar cells," accepted to *Progress in Photovoltaics* (2015)
19. D.M. Powell, V.P. Markevich, J. Hofstetter, M.A. Jensen, A.E. Morishige, S. Castellanos, R. Hao, B. Lai, T.S. Ravi, A.R. Peaker, T. Buonassisi, "Exceptional gettering response of epitaxially grown kerfless silicon," under preparation
20. M.M. Kivambe, D.M. Powell, S. Castellanos, M.A. Jensen, T. Buonassisi, "Characterization of high-quality epitaxial kerfless silicon for solar cells: defect sources and impact on minority-carrier lifetime," under preparation
21. D. Berney Needleman, H. Wagner, P.P. Altermatt, T. Buonassisi, "Assessing grain boundary-limited performance of high-efficiency multicrystalline silicon solar cells via 3-D TCAD device modeling," under preparation

Conference Presentations

1. B Shu, U Das, L Chen, L Zhang, S Hegedus, and R Birkmire, "Design of Anti-Reflection Coating for Surface Textured Interdigitated Back Contact Silicon Hetero-junction Solar Cell" *38th IEEE Photovoltaic Specialist Conference* (Austin) 2012
2. B Shu, U Das, R Birkmire, S Hegedus "Characterization and Modeling of Low Temperature Surface Passivation for Interdigitated Back Contact Silicon Hetero-junction Solar Cell" *38th IEEE Photovoltaic Specialist Conference (Austin)* 2012
3. L Zhang, B Shu , R Birkmire, S Hegedus, U Das "Impact of Back Surface Patterning Process on FF in IBC-SHJ" *38th IEEE Photovoltaic Specialist Conference (Austin)* 2012
4. U Das, J He, Z Shu, L Zhang, C Thompson, R Birkmire, S Hegedus "Sensitivity of surface passivation and interface quality in IBC-SHJ solar cells to patterning process", *39th IEEE Photovoltaic Specialist Conference* (Tampa) 2013
5. D.M. Powell, J. Hofstetter, D.P. Fenning, R. Hao, M.A. Jensen, T.S. Ravi, T. Buonassisi, "High-lifetime kerfless wafers though epitaxy on porous silicon," *Proceedings of the 38th IEEE Photovoltaic Specialists Conference* (Denver) 2014
6. S. Castellanos, T. Buonassisi, "Quantitative residual stress imaging of multicrystalline, quasi-mono, and thin kerfless silicon wafers by infrared

birefringence and sectioning," *Proceedings of the 38th IEEE Photovoltaic Specialists Conference*, (Denver) 2014
7. M.A. Jensen, J. Hofstetter, D.P. Fenning, A.E. Morishige, G. Coletti, B. Lai, T. Buonassisi, "The distribution of chromium in multicrystalline silicon," *Proceedings of the 40th IEEE Photovoltaic Specialists Conference*, (Denver) (2014)
8. M. Ann Jensen, J. Hofstetter, D. P. Fenning, A. E. Morishige, G. Coletti, B. Lai, and T. Buonassisi, "Toward Engineering the Distribution of Chromium in Multicrystalline Silicon." Poster session presented at *40th IEEE Photovoltaic Specialists Conference*; Denver, CO; June 8-13, 2014.
9. M. Kivambe, D. M. Powell, M. Ann Jensen, A. E. Morishige, K. Nakajima, R. Murai, K. Morishita, and T. Buonassisi, ">1.8 Millisecond Effective Lifetime in *n*-type Silicon Grown by the Noncontact Crucible Method." Poster session presented at *40th IEEE Photovoltaic Specialists Conference*; Denver, CO; June 8-13, 2014.
10. D. M. Powell, J. Hofstetter, D. P. Fenning, R. Hao, M. Ann Jensen, T. S. Ravi, and T. Buonassisi, "High-Lifetime Kerfless Wafers through Epitaxy on Porous Silicon." Oral presentation at *40th IEEE Photovoltaic Specialists Conference*; Denver, CO; June 8-13, 2014.
11. M. Ann Jensen, S. C. Siah, J. Hofstetter, M. A. Mahaffey, and T. Buonassisi, "A Free-Carrier-Absorption-Based Technique for Identification of Lifetime-Limiting Defects." Poster session presented at *24th Workshop on Crystalline Silicon Solar Cells & Modules: Materials and Processes*; Breckenridge, CO; July 27-30, 2014.
12. S. Castellanos, M. Kivambe, J. Hofstetter, M. Rinio, B. Lai, T. Buonassisi, "Inferring Dislocation Recombination Strength in Multicrystalline Silicon via Etch Pit Geometry Analysis." Poster session presented at *40th IEEE Photovoltaic Specialists Conference*; Denver, CO; June 8-13, 2014.
13. U. Das, H-Y Liu, J. He, S. Hegedus "The role of back contact patterning on stability and performance of Si IBC heterojunction solar cells" *40th IEEE Photovoltaic Specialists Conference* (Denver), 2014.
14. L Zhang, U. K. Das, Z. Shu, H. Liu, R. W. Birkmire and S. S. Hegedus, "Experimental and simulated analysis of p a-Si:H defects on silicon heterojunction solar cells: trade-offs between Voc and FF" 42th IEEE Photovoltaic Specialists Conference (New Orleans) 2015

Awards (05/01/2014 – 09/30/2014)

- Best poster award, *IEEE PVSC*: S. Castellanos, M. Kivambe, J. Hofstetter, M. Rinio, B. Lai, T. Buonassisi, "Inferring Dislocation Recombination Strength in Multicrystalline Silicon via Etch Pit Geometry Analysis." Poster session presented at *40th IEEE Photovoltaic Specialists Conference*; Denver, CO; June 8-13, 2014.

Budget Period Spending: No input needed.

Patents: None

Training and outreach:

- The IEC and MIT group had strong participation at the DOE/NREL Hands-on PV Experience (HOPE) at NREL (July 16-20, 2012). T Buonassisi made a presentation *"How to "read" an I–V curve to troubleshoot your device"* and U Das made a presentation *"The options and future prospects for amorphous silicon PV products".* MIT graduate students J Sullivan and K Hartman and IEC graduate student L Zhu attended.

- MIT graduate students A Morishege and D Berney Needleman and IEC graduate students Lulu Zhang and Lei Zhang attended the International Workshop on Characterization and Modeling of Si Solar Cells at Arizona State University, Tempe, Arizona (May 29-June 1, 2012)

- IEC hosted 8 high school STEM teachers for 2 weeks (July 2013) and exposed them to concepts and scientific principles behind Si solar cell processing and characterization.

- IEC graduate student J He attended DOE/NREL Hands-on PV Experience (HOPE) at NREL (July 2013)

Next Budget Period Detailed Budget: No input needed.

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