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Fabrication and Characterization of a Single Hole Transistor in p-type GaAs/AlGaAs Heterostructures

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Fabrication and Characterization of a Single Hole Transistor in p-type GaAs/AlGaAs Heterostructures

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Abstract

Most spin qubit research to date has focused on manipulating single electron spins in quantum dots. However, hole spins are predicted to have some advantages over electron spins, such as reduced coupling to host semiconductor nuclear spins and the ability to control hole spins electrically using the large spin-orbit interaction. Building on recent advances in fabricating high-mobility 2D hole systems in GaAs/AlGaAs heterostructures at Sandia, we fabricate and characterize single hole transistors in GaAs. We demonstrate p-type double quantum dot devices with few-hole occupation, which could be used to study the physics of individual hole spins and control over coupling between hole spins, looking towards eventual applications in quantum computing.

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CONTENTS

INTRODUCTION

To date, experiments looking at the possibility of using spins in semiconductors as quantum bits have primarily focused on electron spins. It was only recently suggested that hole spins in GaAs might provide better decoherence times. One of the main reasons that there are relatively few experiments on holes in GaAs, as compared to electrons, is the difficulty of fabricating stable hole nanostructures (such as a quantum dot) [1-3]. The origin of the electrical instability was not known, but the heterostructure modulation doping layer was a possible candidate [2]. Therefore, building on recent advances in undoped high-mobility two dimensional hole gasses [4], we fabricated p-type quantum dots starting with undoped GaAs/AlGaAs heterostructures. The low temperature mean free path in these structures can be longer than 1 μm, which is larger than typical nanostructure dimensions. This should aid in the formation of low-disorder few hole nanostructures, where hole transport and control over the confining potential is not impeded by defects.

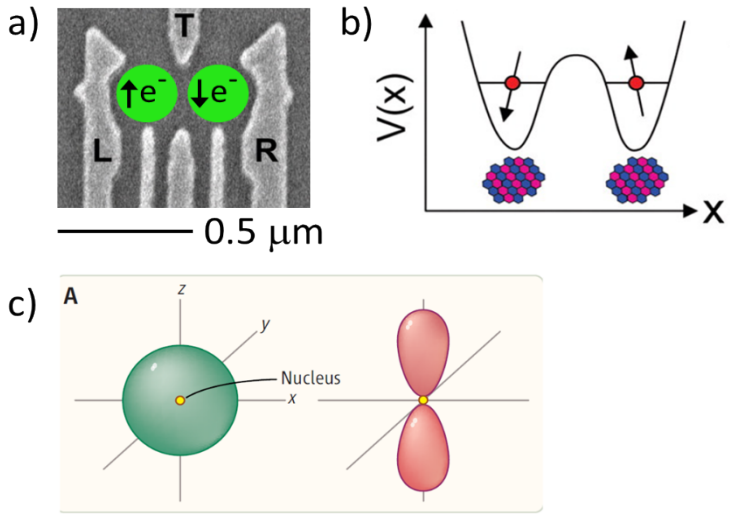

Figure 1. a) SEM image of metallic gates on the surface of GaAs/AlGaAs heterostructure, defining a double quantum dot structure in the 2D electron gas below (adapted from Ref [2]). b) Sketch of two electrons confined in the double dot potential, showing host semiconductor nuclei. c) Cartoon of electron (left) vs. hole (right) wavefunction, illustrating the difference in the overlap of the wavefunction with the nucleus, which strongly affects the coupling of electron vs. hole spins to the nuclear spins.

One of the motivations for investigating single hole transistors in GaAs is the potential improvement in spin coherence time for holes vs. electrons. Figure 1a shows a GaAs double quantum dot device formed by surface gates and Fig. 1b shows a cartoon of the two electrons confined in the double quantum dot potential and presence of background nuclear spins [5]. In electron quantum dots in GaAs, interaction of electron and nuclear spins in the host semiconductor is a major source of electron spin decoherence [5]. Figure 1c illustrates the difference between the electron and hole wavefunctions in GaAs. The lack of overlap of the hole wavefunction with the nucleus leads to a much weaker interaction between the nuclear and hole

spin, as compared to the electron spin, which makes hole spins a promising candidate for spin-based quantum bits [6,7].

In this project, we demonstrated electrically stable single and double quantum dots in GaAs. Using charge sensing, we showed the ability to completely empty the dot and control the occupation at the few-hole level. The double quantum dot interdot coupling is tunable over a wide range, from formation of a large single dot to two well-isolated individual dots. These devices should provide a path for controlling and coupling individual hole spins in GaAs.

ACCOMPLISHMENTS

Shallow, High Mobility Undoped 2DHS

Initial experiments focused on basic characterization of the two dimensional hole system (2DHS) that would be used to create the single hole transistor, looking at carrier density and low-temperature mobility. To form nanostructures with sharp electrostatic confinement in the 2D layer, it is necessary to use a relatively shallow 2D layer. The distance between the Schottky gate and the 2D layer should be on the order of or less than the width of the desired confinement potential in the 2D layer. Using shallow 2D layers will help to form ballistic quantum point contacts and create small quantum dots with few hole occupation. We aimed for a hole mobility $\geq 10^5$ cm^2/Vs, corresponding to a mean free path of at least ~ 1 μm at typical hole densities, which should be long enough to allow for the fabrication of nanostructures (e.g., quantum dots) that are not dominated by impurities or defects.

Figure 2a shows a sketch of the device structure used to create the 2DHS, consisting of a GaAs/AlGaAs heterostructure, ALD Al_2O_3 dielectric layer, and global accumulation gate. The upper Al gate is used to accumulate holes at the GaAs/AlGaAs interface, 100 nm below the heterostructures surface. The heterostructure consists of a 300 nm GaAs buffer layer, a superlattice of 300 repeats of 3 nm of GaAs=10 nm of AlGaAs, 1000 nm of GaAs, 100 nm AlGaAs, and a 10 nm GaAs cap. The entire structure is grown at a temperature T = 630 C.

In Fig. 2b and 2c we show Hall measurements for a bulk 2D device at T = 4 K. For this device, the Al_2O_3 layer thickness is 244 nm. Figure 2b shows density p versus Al upper gate voltage V_{TG}, determined via low B-field Hall resistivity measurements. A linear fit to the data yields a slope of -1.30 10^{11} cm^2/V. This capacitance can be explained by assuming a relative permitivity of 11.5 for the AlGaAs barrier and 7.2 for the Al2O3 layer. Figure 2c shows Hall mobility versus density p, where the resistivity is determined from van der Pauw measurements. We note that the mobilities at T = 4 K may be limited by phonon scattering and are likely to increase as the temperature is lowered.

Fabrication of Single Hole Transistor Device

After demonstrating the high mobility 2DHS and ability to control the 2D hole density with a global surface gate, we added lower nano-patterned electrostatic gates to the device to form nanostructures. Figure 3a-b shows images of the actual device, where Fig. 3b shows a scanning electron micrograph of the Ti/Au (10 nm Ti, 40 nm Au) depletion gates on the surface of a GaAs/AlGaAs heterostructure (VA0582) for a partially processed device, fabricated via electron beam lithography and lift-off. These lower Ti/Au gates are used to locally deplete the 2DHS to define the nanostructure. Ohmic contacts to the hole layer are formed via AuBe evaporation and anneal. A 110 nm thick layer of Al_2O_3 grown via atomic layer deposition electrically isolates the upper gate from AuBe Ohmic contacts and lower Ti/Au gates; a mesa etch step is not required.

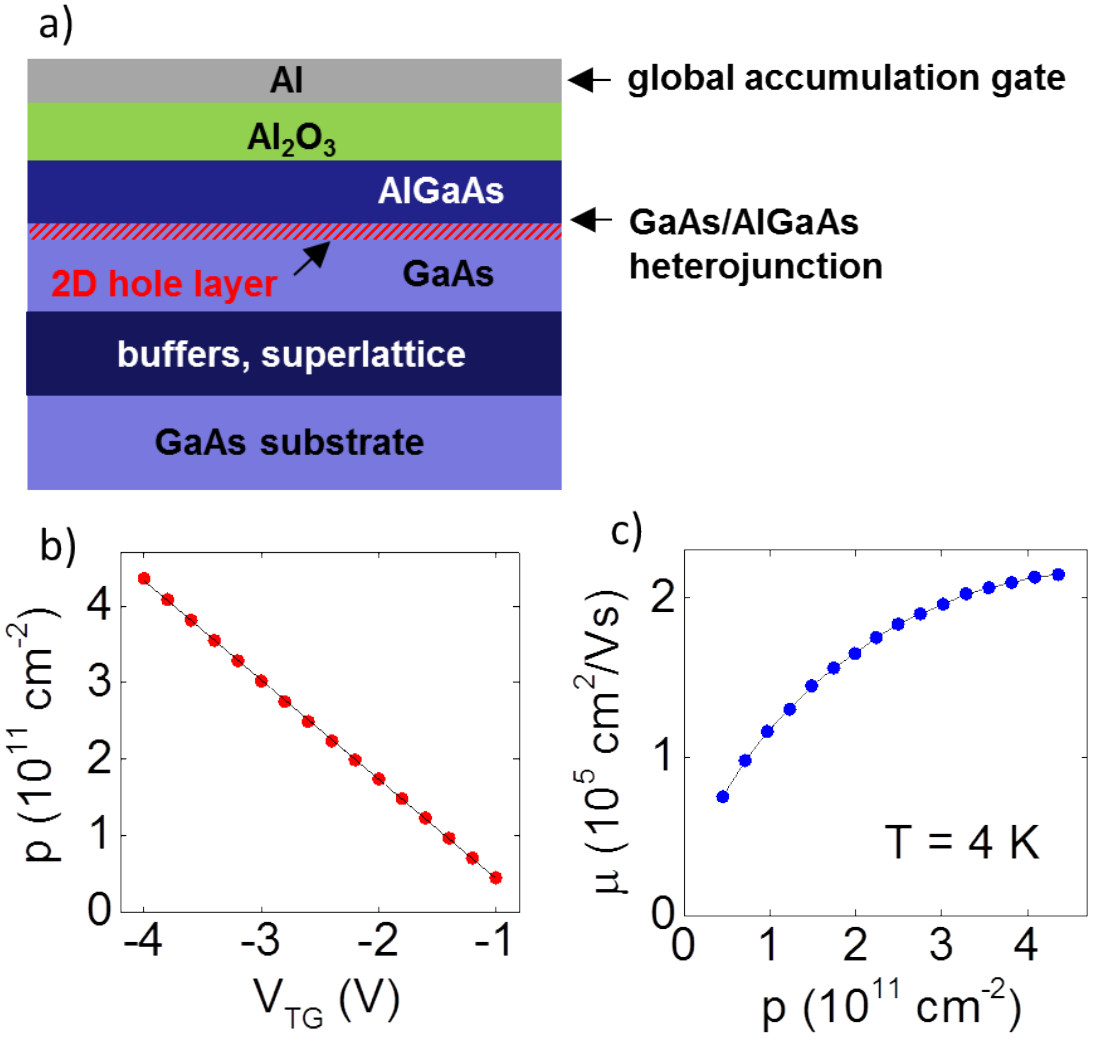

Figure 2. a) Sketch of undoped 2DHS device structure, showing GaAs/AlGaAs heterostructure, Al_2O_3 dielectric, and global accumulator gate. b) Measured 2D Hall effect density vs. global accumulation gate voltage at T = 4 K. c) Mobility vs. 2D density

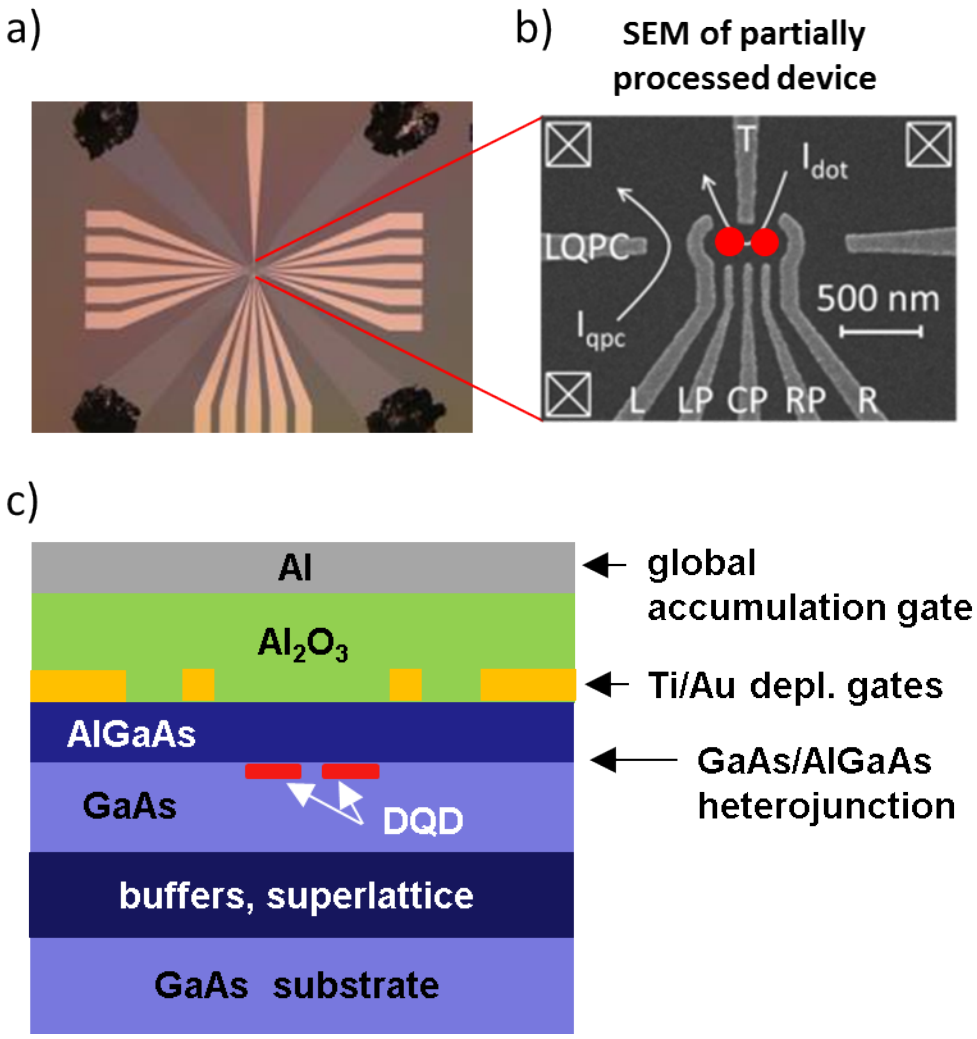

Figure 3. a) Photo of entire GaAs chip (~ 3 x 3 mm) and b) SEM image of the depletion gates on the surface of the GaAs/AlGaAs heterostructure. c) Sketch of device structure showing addition of nano-patterened Ti/Au depletion gates for formation of DQD.

First Generation Double Quantum Dots

Single Dot Transport

Figure 4 shows transport in one of our first double quantum dot devices. The nanostructure gate pattern for this device is shown in Fig. 3b. This gate design was chosen as it is known to form few electron single quantum dots in GaAs with a high degree of tunability [8]. Although the device is designed primarily to form a double quantum dot, we are also able to operate this device as a single quantum dot. We are able locally deplete the 2D hole density in this device with the Ti/Au surface gates with no noticeable leakage current between the gates and 2D hole layer. The device conductance is experimentally determined via standard low-frequency lock-in measurements with an rms ac source-drain bias of 50 - 100 μV. For all measurements shown, the

Al upper gate voltage is held constant at -6 V. The device was measured in a 3He refrigerator with a temperature of $T = 380$ mK.

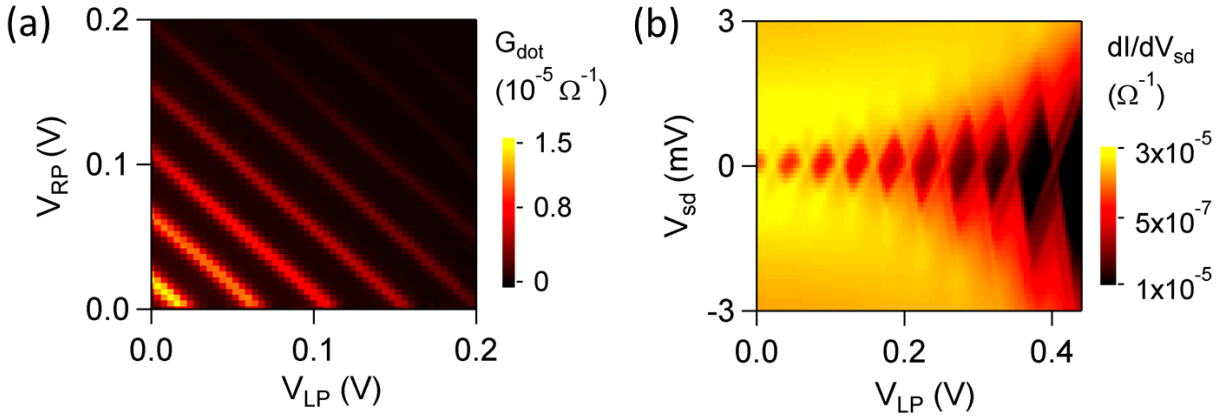

Figure 4. a) Dot conductance G_{dot} vs. V_{LP} and V_{RP} . b) dI_{dot}/dV_{sd} versus V_{sd} and V_{LP} showing Coulomb diamonds.

Figure 4a shows quantum dot conductance versus left and right plunger gate voltages V_{LP} and V_{RP} with $V_{CP} = 0$ V. In this regime, the device behaves like a large single dot, with roughly equal capacitance between the dot and gates LP and RP, where $C_{dot\text{-}LP} = 3.5$ aF and $C_{dot\text{-}RP} = 3.6$ aF. The data of Fig. 4a show no evidence of hysteresis or electrical instability, in contrast to mesoscopic devices fabricated in p-doped GaAs/AlGaAs heterostructures [1-3]. In Fig. 4b we show a stability diagram with Coulomb diamonds for this dot. The last visible diamond indicates a dot charging energy of ~ 1.6 meV, and shows excited states with a spacing of roughly $E_{orb} \sim$ 0.5 meV. Using $E_{orb} \sim \pi\hbar^2/m^*l^2$, we obtain a rough estimate of the dot size [9] $l \sim 100$ nm. Although the effective hole mass will depend on the details of the dot confinement potential [10], here we use the effective mass for heavy holes in 2D systems in GaAs/AlGaAs single-interface heterostructures, $m_{HH} \sim 0.5m_e$ [11].

Double Dot Transport

Figure 5a shows quantum dot conductance versus V_{LP} and V_{RP} after increasing the center plunger voltage to $V_{CP} = 0.2$ V. Transport gradually evolves from single dot to double dot-like as the confinement is increased. At the upper right corner of Fig. 5a the dot tunnel barriers become too opaque to measure conduction directly through the dot. Figure 5b shows conductance through the left quantum point contact (QPC) versus V_{LQPC}. As expected for a QPC, the data show plateaux in the conductance, with the second-to-last plateau occurring near $2e^2/h$. The last plateau occurring below $2e^2/h$ may be the so-called "0.7 structure", which has been previously observed in electron [12] and hole QPCs [13-14]. The precise conductance values, especially for the higher conductance plateaux, are likely affected by lead resistance since we use a two-terminal measurement. In Fig. 5c we show the QPC transconductance dG_{qpc}/dV_T versus V_{LP} and V_{RP} in the region of gate voltage indicated by the yellow box in Fig. 5a. In order to use the QPC to charge sense the occupation of the dot, we tune V_{LQPC} in order to sit on the steep portion of the

G_{qpc} versus V_{LQPC} curve below the last conductance plateau. The data clearly show sensing of both left and right dot charge occupation, where single hole changes in the left dot occupation produce a larger change in dG_{qpc}/dV_T than for the right dot due to the closer physical proximity between the left dot and QPC.

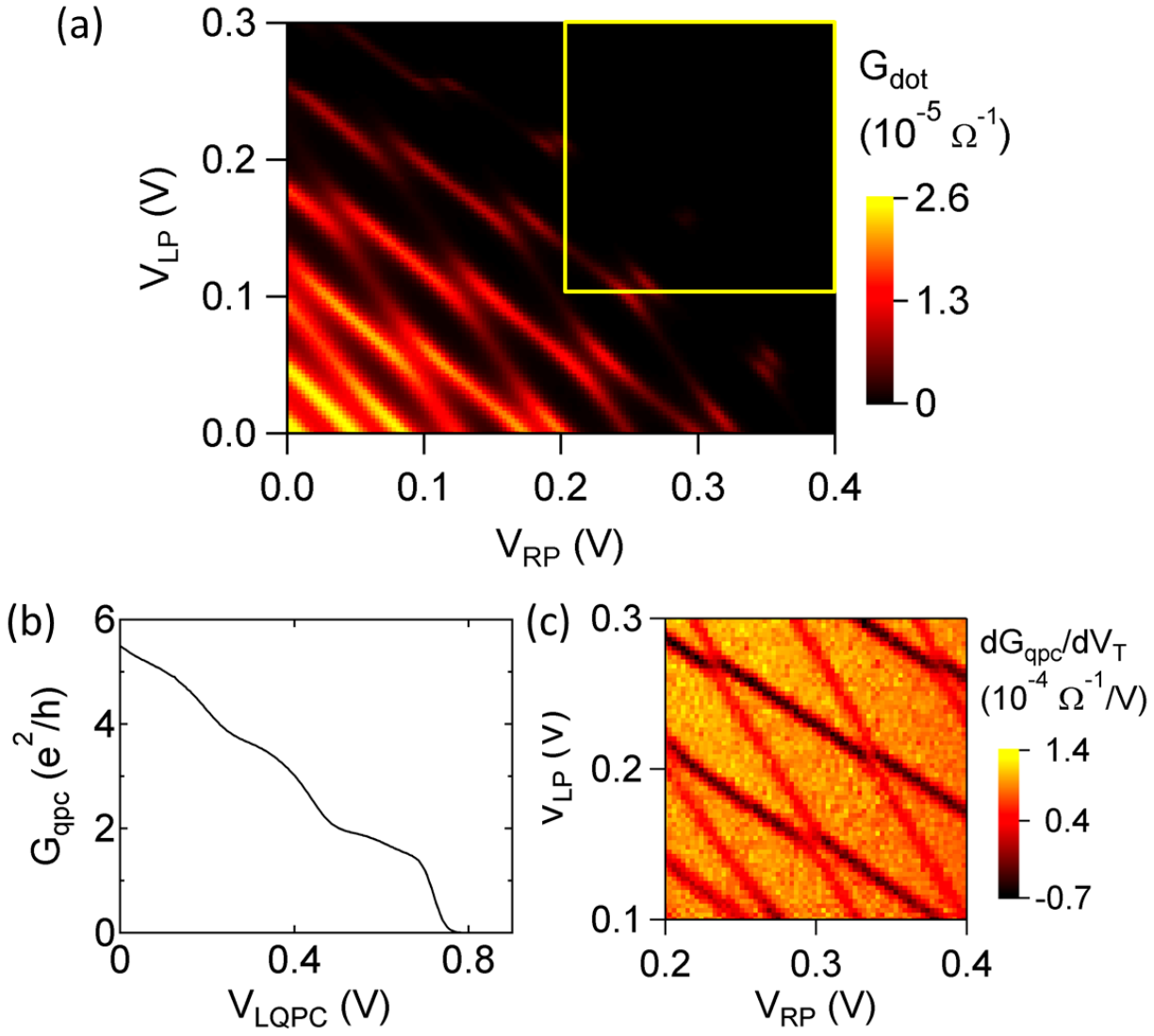

Figure 5. a) Dot conductance G_{dot} vs. V_{LP} and V_{RP} for fixed gate voltages V_{CP} = 0.2 V, V_{LQPC} = V_L = 0 V, and V_{CP} = 0.5 V. The yellow box outlines the gate voltage region spanned in c). b) Left QPC conductance vs. V_{LQPC} for V_L = 0 V. c) QPC transconductance dG_{qpc}/dV_T vs. V_{LP} and V_{RP} with V_{CP} = 0.2 V. V_{LQPC} is varied from 0.43 to 0.4 V in order to maintain constant sensitivity.

In Fig. 6a-c we show QPC transconductance versus left and right plunger gate voltages V_{LP} and V_{RP} at three different center plunger gate voltages V_{CP} = 0, 0.2, and 0.4 V. The data demonstrate the ability to use the CP gate to tune the DQD from a highly-coupled regime, where the transport

is reminiscent of that expected for a large, single dot, to a weakly-coupled regime where the charge sensing signal shows two well-isolated dots.

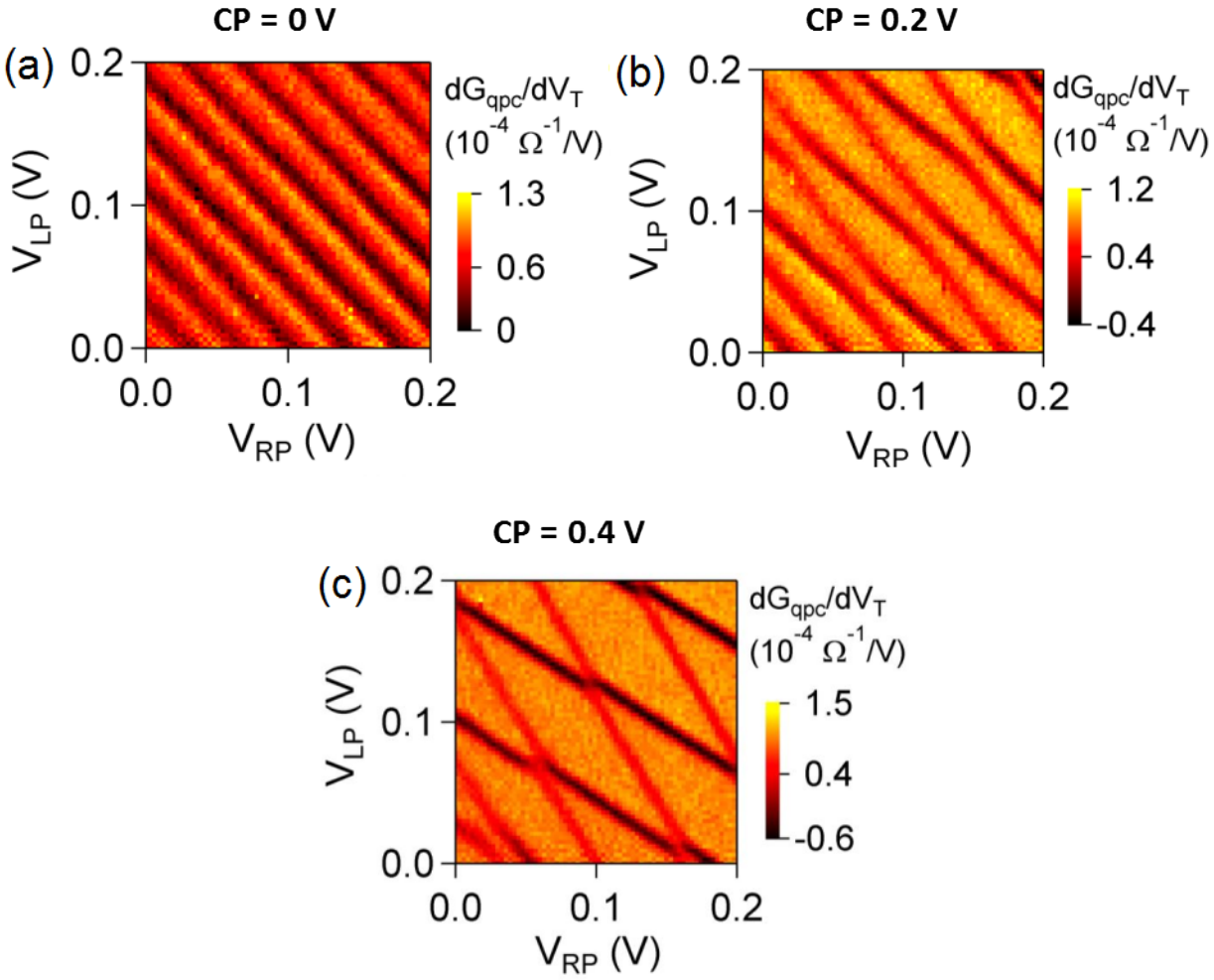

Figure 6. a) Left QPC transconductance dG_{qpc}/dV_T vs. V_{LP} and V_{RP} for a) V_{CP} = 0 V, b) V_{CP} = 0.2 V, c) V_{CP} = 0.4 V,

Figure 7 shows a continuation of the charge sensing data to larger V_{LP} and V_{RP} voltages, for V_{CP} = 0.7 V. The absence of transitions in the charge sensing signal in the upper right region of the plot, for both the left and right dot, over a wide voltage range, indicat that the DQD is empty. This allows us to label the various regions between charge transitions with DQD hole occupation (N,M), as shown in Fig. 7, where N (M) indicates the number of holes in the left (right) dot, respectively. We note that the interdot tunnel coupling in Fig. 7 appears to be nearly pinched off. Although the interdot coupling is easily tuned for many-hole occupation, tuning becomes more challenging as the dot occupation approaches (0,0). Modification of the gate design may be necessary to increase tunability of the interdot coupling in the few-hole regime.

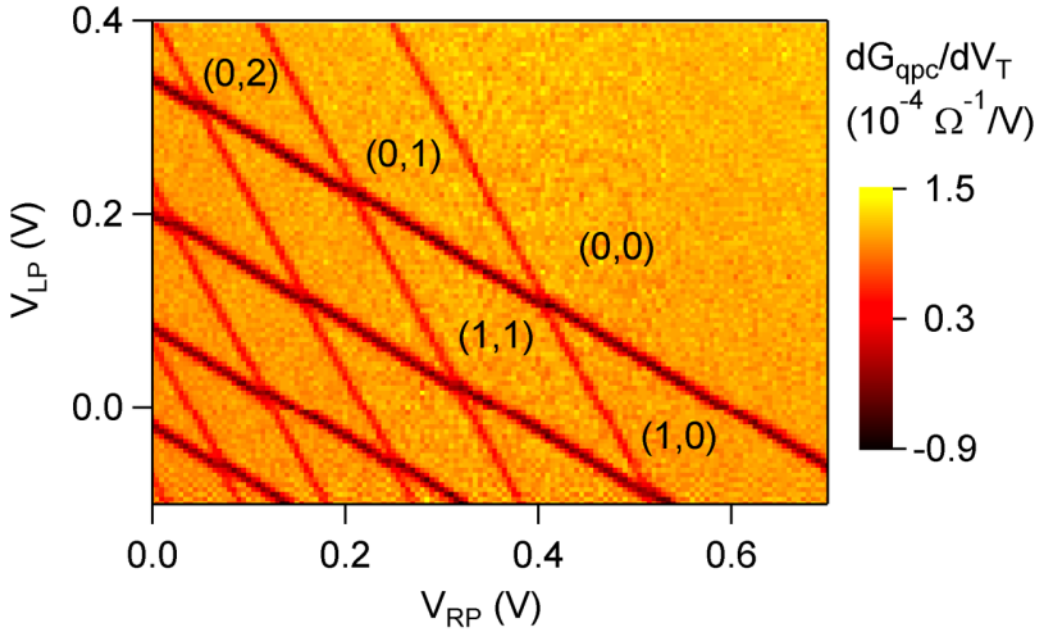

Figure 7. Left QPC transconductance dG_{qpc}/dV_T vs. V_{LP} and V_{LP} for V_{CP} = 0.7 V, showing ability to completely empty the dot and operate the device in the few hole regime.

Second Generation Double Quantum Dots

In first generation DQD devices, the interdot coupling was tunable for several hole occupation, but as the occupation drops to one or two holes per dot, tuning this coupling becomes difficult, as this tunnel barrier is nearly pinched off. To improve the tunability, it is of interest to utilize heterostructures with shallow 2D hole layers (< 100 nm depth) [15]. This should help to reduce the length of tunnel barriers and also to decrease the size of the electrostatic confinement potential, which may be required in order to achieve similar orbital level spacings to those obtained in electron quantum dots, since the heavy hole effective mass is larger than the electron effective mass in GaAs ($m_{HH} \sim 0.2m_e$ - $05m_e > m_e = 0.07m_e$).

In Figure 8a we show mobility versus hole density for a 2DHS with 50 nm depth. Somewhat surprisingly, the impact to mobility due to moving from a 100 nm to 50 nm depth heterojunction is minimal. The high quality of these 2DHS is indicated by the performance of a QPC fabricated in this material. Figure 8b shows an SEM of the surface of a partially processed DQD device, where the gate layout allows formation of a QPC on either the right or left side of the DQD. We focus on transport through the left QPC, which is intentionally designed to have a larger width, which allows for observation of more transport channels through the QPC. In Fig. 8c we show conductance through the left QPC as a function of the LQPC gate. As the QPC channel is gradually depleted, the conductance drops in discrete steps, quantized at multiples of $2e^2/h$, as expected for ballistic transport through a channel, indicating that the motion of holes in this device is not impeded by defects.

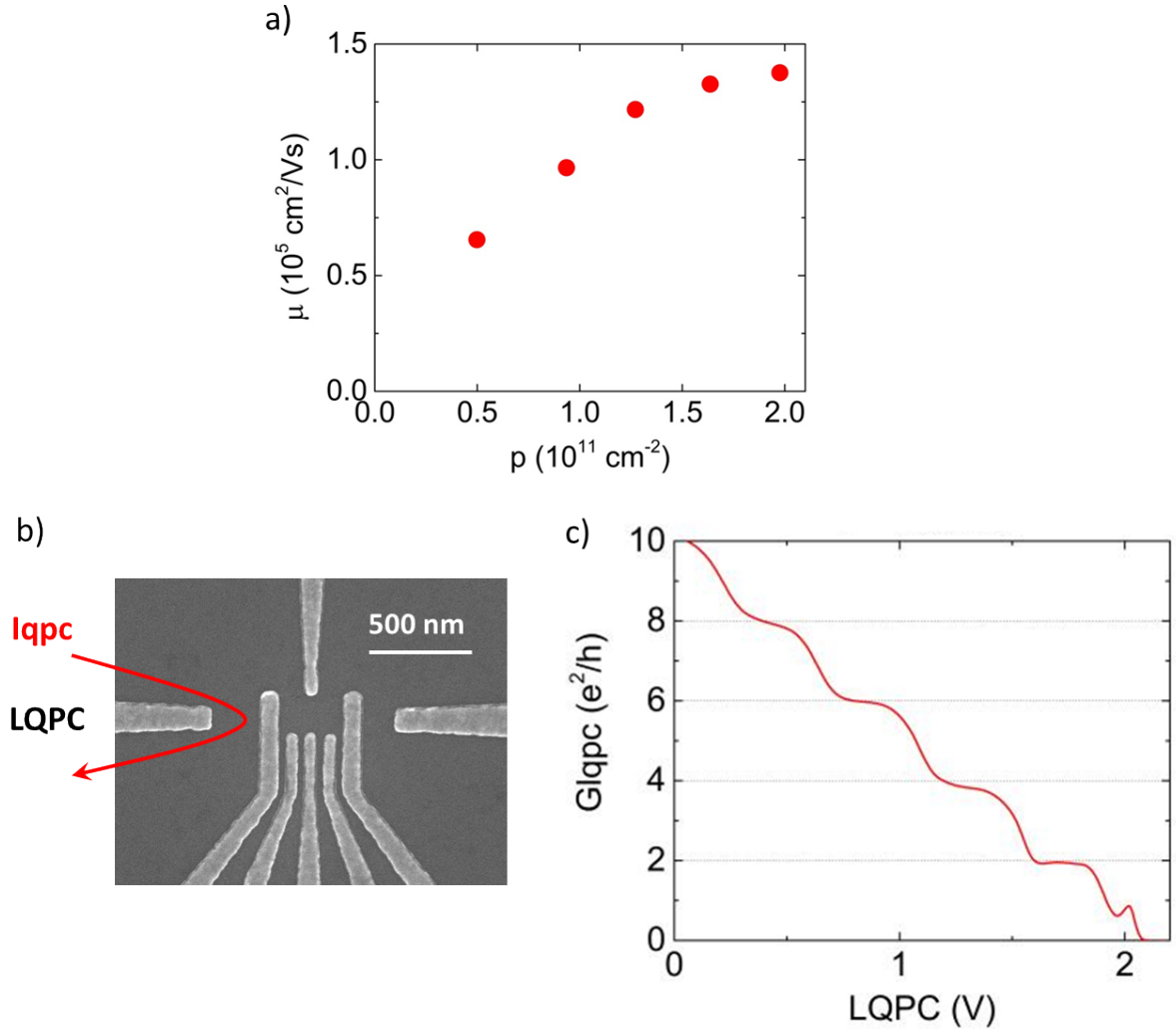

Figure 8. a) Mobility of undoped 2DHS with 50 nm depth vs. hole density. b) Scanning electron micrograph of surface of partially processed DQD device showing depletion gate layout. c) Conductance of QPC versus LQPC gate voltage, where quantized steps in conductance show ballistic transport.

The depletion gate design for our second generation DQD is shown in Fig. 9a, which shows an SEM of the Ti/Au depletion gates and a sketch indicating the location of the path for transport through the DQD ("Idot") and through the adjacent charge sensing dot ("Ics"). This gate design is known to produce a tunable electron DQD in Si/SiGe heterostructures [16]. Figure 9b shows the charge sensor transconductance as a function of LL and LR depletion gates, demonstrating the ability to completely empty the DQD and operate in the few hole regime. The visible splitting at the charge transition triple points indicates a significant interdot coupling. As desired, this interdot coupling is now much larger than for the first generation DQD at 100 nm depth, as can be seen by comparing the triple point splitting shown in Fig. 9b versus that shown in Fig. 7. The tunnel couplings are now large enough that one can measure transport directly through the DQD at the (1,1) – (0,2) charge transition, as shown in Fig. 9c. Figure 9c also shows the DQD excited state structure. The first excited state transition energy of ~ 0.7 meV is slightly

larger than the 0.5 meV orbital level spacing obtained in the first generation dot, suggesting that not only are the tunnel barriers more transparent in the shallow DQD, but also that the dots are of smaller size.

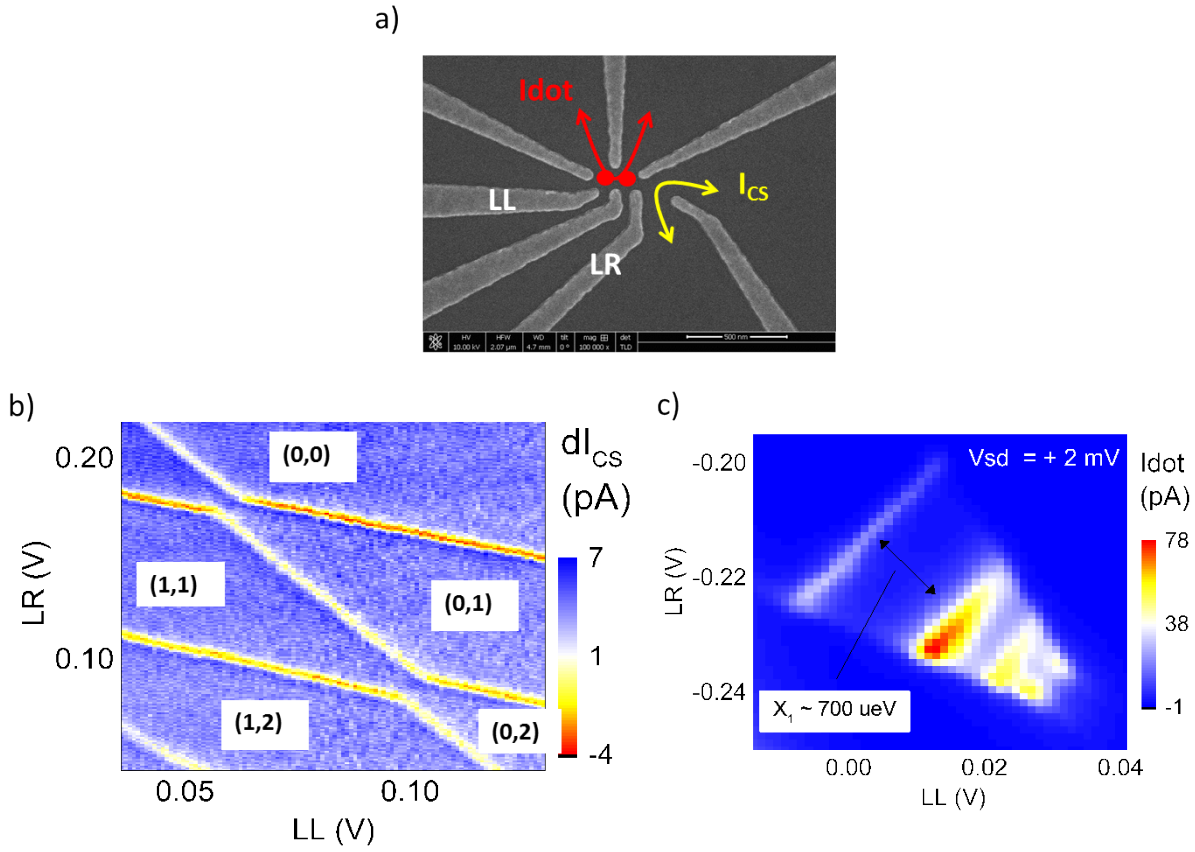

Figure 9. a) Scanning electron micrograph of surface of partially processed device showing Ti/Au depletion gate layout. b) Charge sensor transconductance vs. LL and LR depletion gates. Labels indicate DQD hole occupation. c) Direct transport through DQD at large source-drain bias (2 mV) at the (1,1) – (0,2) charge transition, showing excited state structure.

Charge Noise

A past hurdle facing hole nanostructures in GaAs was the ability to form devices with surface depletion gates that are stable [1-3]. In both electron [17] and hole [1-3] nanostructures in GaAs, the conductance can drift over time or exhibit telegraph noise, depending on the device design and GaAs/AlGaAs heterostructure. The mechanism behind the conductance drift and/or noise is not well understood. By using undoped devices we have achieved a very high level of device electrical stability. Figure 10a shows a single Coulomb blockade peak in transport vs. depletion gate LP through a one of our p-type quantum dots. The noise in the conductance measured at a fixed gate voltage such that the transport is on the edge of the Coulomb blockade (as indicated

by the red dot in Fig. 10a) peak is shown in Fig. 10b. The noise is close to that expected due to the voltage sources used to control the dot depletion gates.

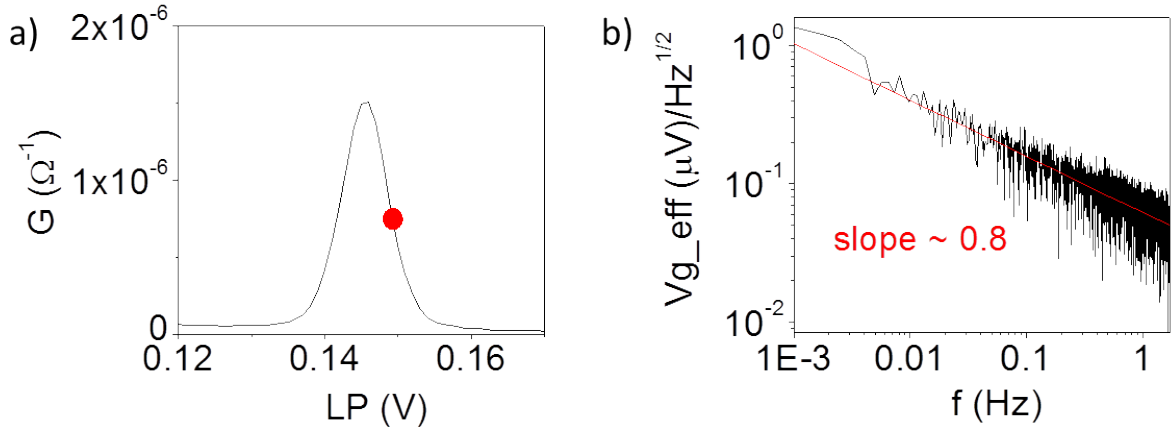

Figure 10. a) Dot conductance versus LP depletion gate voltage showing a single Coulomb blockade peak. b) Noise versus frequency in conductance through dot while at fixed gate voltage such that the device is operating on the edge the Coulomb blockade peak shown in a) (location indicated by red dot). The noise is converted to an effective total gate voltage noise using all of the capacitances from the various gates to the dot (measured via Coulomb blockade transport).

CONCLUSIONS

In conclusion, we have demonstrated few-hole DQDs in undoped (100) oriented GaAs/AlGaAs heterostructures. The devices show excellent charge stability and negligible hysteresis with respect to gate voltage. The mobilities are high enough such that the mean free path of the holes is ~ 1 μm, which is larger than typical nanostructure dimensions The interdot coupling can be tuned over a wide range, controlling the transition from a large single dot to two well-isolated quantum dots. Using charge sensing we show that the dots can be completely emptied of holes and operated in the few-hole regime. These devices may provide a means for future experiments focusing on manipulation of single hole spins in GaAs quantum dots.

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