U.S. Department of Energy
Energy Efficiency and Renewable Energy
Bringing you a prosperous future where energy is clean, abundant, reliable, and affordable

Solar Energy Technologies Program

National Solar Technology Roadmap:

Wafer-Silicon PV

Facilitator: *Bhushan Sopori*

Participants included:
National Renewable Energy Laboratory
Sandia National Laboratories
U.S. Department of Energy
University and private-industry experts

DRAFT

Management Report
NREL/MP-520-41733
June 2007

National Solar Technology Roadmap: Wafer-Silicon PV

Scope

Silicon photovoltaic (PV) technologies are addressed in two different technology roadmaps: Wafer-Silicon PV and Film-Silicon PV. This Wafer-Silicon PV roadmap applies to all bulk-silicon-based PV technologies—including those based on Czochralski, multicrystalline, float-zone wafers, and melt-grown crystals that are 100 μm or thicker, such as ribbons, sheet, or spheral silicon. Silicon feedstock issues and low-optical-concentration approaches are also addressed.

Thinner silicon-based films are addressed in the Film-Silicon PV roadmap, which focuses on silicon films on supporting substrates such as glass, polymer, aluminum, stainless steel, or metallurgical-grade silicon. Such devices typically use amorphous, nanocrystalline, fine-grained polycrystalline, or epitaxial silicon layers that are 1–20 μm thick.

Technology development stage: Commercial volume production.

Target applications: Residential, commercial, and utility.

Background

Wafer-silicon PV technologies are currently the dominant commercial PV technology by a huge margin, and they are likely to remain dominant for at least 10 more years (2017). Wafer-silicon PV offers one of the lowest costs in $/W and levelized cost of energy (LCOE) $/kWh for every application and has the best proven reliability. Moreover, there is considerable momentum behind wafer-silicon PV because it has the largest installed base and largest annual manufacturing capacity; as a result, the performance and cost are expected to continue to improve along the historic 81% learning curve. The current purified polysilicon feedstock shortage has recently driven up prices of the silicon substrate, which was already a major portion of the cell cost. But substrate prices are likely to recover in 2008 as additional feedstock manufacturing capacity comes on line. The increased cost of silicon has driven innovation in cell efficiencies, yield, and wafer thickness that will accelerate the move to a new, lower-cost baseline when the silicon feedstock price comes back down.

Roadmap Overview

Wafer-silicon PV R&D is currently focused on achieving reduced cost in $/W or $/kWh through the following:

- Reduced materials cost, particularly the silicon substrate
- Increased conversion efficiency
- Improved manufacturing processes and higher throughput
- Improved reliability (reduced wafer breakage, tighter performance distributions)

Specific tasks include the following:

- Absorber
    - Research improved impurity and defect engineering.

  - Use thinner, larger-area wafers with more-efficient silicon utilization.
  - Develop new surface and bulk passivation techniques.
- Cells and Contacts
  - Develop lower-cost, high-throughput cell processes that result in higher-efficiency devices.
  - Develop novel cell-contacting schemes.
  - Develop novel devices structures such as heterojunction cells.
  - Improve light-trapping and antireflection.
- Interconnects
  - Pursue innovations to improve manufacturability of cells and interconnects.
- Packaging
  - Pursue innovations to reduce optical losses.
  - Develop encapsulation materials that reduce module cost and maintain reliability.
  - Continue to refine accelerated life testing that predictably replicates failures seen in the field.
  - Develop low-concentration optics and associated changes to module design.
- Manufacturing
  - Accelerate the implementation of R&D progress into commercially available products.
  - Develop and implement in-line diagnostics.

Metrics

Parameter	Present Status (2007)	Future Goal (2015)
Polysilicon	$45–60/kg	$20/kg
Wire sawing	$0.25/W	$0.15/W
Wafer size	~250 cm^2	~400 cm^2
Wafer thickness	200–250μm	120 μm
Volume manufacturing	100–200 MW/yr plants	500 MW/yr plants
Automation	Partial	Complete
Efficiency, best lab cells	25%	27%
Efficiency, commercial modules	12%–18%	15%–21%
Module manufacturing cost	$2/W (at $30/kg)	$1/W

Identified Needs

This roadmap is organized to show separately the priorities for High-Efficiency Single-Crystal and Low-Cost Multicrystalline Solar Cells. Some of the identified needs related to module manufacturing are common.

			Nat'l Lab			Industry		
		University	NREL	Sandia	Other	TPP	Incubator	Other
High-Efficiency Single-Crystal Cells								
Need	**Significance**							
1. Thinner wafers and processes	Silicon material represents the largest fraction of module cost. Thinner wafers can lower material cost and have potential to yield higher efficiency.	x	x			x	x	
2. Surface passivation	Lower surface recombination is needed to yield cell efficiencies > 25%.	x	x					
3. Light management for thin cells	Thinner cells need very effective light-trapping and reduced metallization shadowing.	x	x			x	x	
4. Low recombination contacts	High efficiencies require metallization schemes for low recombination contacts.	x	x			x	x	
5. Feedstock cost	Develop less-expensive methods to produce feedstock suitable for PV.					x	x	
Low-Cost Multi-Crystal Cells								
Need	**Significance**							
1. Bulk defect engineering & passivation	Identify performance-limiting mechanisms in cells made from current c-Si feedstock materials. It will provide a pathway to using lower-cost feedstock and higher efficiency on lower-cost cells.	x	x			x	x	
2. Thinner wafers & processing	Thinner wafers can lower material cost and have potential to yield higher efficiency. However, because wafer breakage increases steeply as the wafers become thinner, advanced techniques for wafer handling and "gentler processes" are needed.	x	x			x	x	
3. Solar-quality feedstock	Reduce cost of Si materials in cell without hurting efficiency.		x			x	x	
4. Light management – antireflective coating	Light management of the entire module is needed.	x	x			x	x	

5. Low-cost contacts	Pathway to reducing metallization cost. Demonstrate low-cost metallization processes: - Lower shadowing and lower % Si-M contact-area - Maskless metallization - Newer metal schemes - Simultaneous front- and back-contact Formation							
Common Aspects of High-Efficiency Single-Crystal and Low-Cost Multi-Crystal Modules/Systems								
Need	**Significance**							
1. Interconnects, packaging, reliability	Reduce cost of Si modules, BOS, and installation. The non-cell parts of the system are typically about half the total cost.			x		x	x	
2. Manufacturing diagnostics & process modeling	The optimization of efficiency and yield requires isolation and complete understanding of each process step. This can be achieved through diagnostics and process modeling.	x	x			x	x	
3. Reduced Si waste	Identify practical pathways for reducing the amount of Si needed per watt. Silicon material represents the largest fraction of module cost (~25%).	x	x			x	x	