GaN Initiative for Grid Applications (GIGA)

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1. Executive Summary

For nearly 4 ½ years, MIT Lincoln Laboratory (MIT/LL) led a very successful, DoE-funded team effort to develop GaN-on-Si materials and devices, targeting high-voltage (>1 kV), high-power, cost-effective electronics for grid applications. This effort, called the GaN Initiative for Grid Applications (GIGA) program, was initially made up of MIT/LL, the MIT campus group of Prof. Tomas Palacios (MIT), and the industrial partner M/A Com Technology Solutions (MTS). Later in the program a 4th team member was added (IQE MA) to provide commercial-scale GaN-on-Si epitaxial materials.

A basic premise of the GIGA program was that power electronics, for ubiquitous utilization - even for grid applications - should be closer in cost structure to more conventional Si-based power electronics. For a number of reasons, more established GaN-on-SiC or even SiC-based power electronics are not likely to reach theses cost structures, even in higher manufacturing volumes. An additional premise of the GIGA program was that the technical focus would be on materials and devices suitable for operating at voltages > 1 kV, even though there is also significant commercial interest in developing lower voltage (< 1 kV), cost effective GaN-on-Si devices for higher volume applications, like consumer products.

Remarkable technical progress was made during the course of this program. Advances in materials included the growth of high-quality, crack-free epitaxial GaN layers on large-diameter Si substrates with thicknesses up to ~5 μm, overcoming significant challenges in lattice mismatch and thermal expansion differences between Si and GaN in the actual epitaxial growth process. Such thick epilayers are crucial for high voltage operation of lateral geometry devices such as Schottky barrier (SB) diodes and high electron mobility transistors (HEMTs). New “Normally-Off” device architectures were demonstrated – for safe operation of power electronics circuits. The trade-offs between lateral and vertical devices were explored, with the conclusion that lateral devices are superior for fundamental thermal reasons, as well as for the demonstration of future generations of monolithic power circuits. As part of the materials and device investigations breakdown mechanisms in GaN-on-Si structures were fully characterized and effective electric field engineering was recognized as critical for achieving even higher voltage operation. Improved device contact technology was demonstrated, including the first gold-free metallizations (to enable processing in CMOS foundries) while maintaining low specific contact resistance needed for high-power operation and 5-order-of magnitude improvement in device leakage currents (essential for high power operation). In addition, initial GaN-on-Si epitaxial growth was performed on 8”/200 mm Si starting substrates.

2. Program Timeline

- In mid 2009, MIT/LL (FFRDC) was approached by DOE/OE (M. Soboroff) to explore possibility of leading a team to advance GaN-on-Si materials and device technology for cost-effective, grid power electronics and eventual commercialization for grid applications.
- First funding received via Interagency Agreement in August of 2010; initial team formed (via competitive R&D research subcontracts) with MIT Campus (Prof. Palacios' group) and M/A-Com Technology Solutions (MTS).
- Based on continuing technical successes, 4-phases of funding (through September of 2012); PoP Oct. 2009 through Dec. 2014.
- Domestic commercial epitaxial materials supplier identified by competitive solicitation and R&D subcontract issued to Kopin in December 2012 (4^{th} full member of GIGA team).
- 1 Jan 2013, M. Soboroff retired; G. Bindewald assumed DOE/OE PM role for GIGA program. No additional FY13 and FY14 program funding available.
- 10 Jan 2013 IQE agrees to purchase III-V assets of Kopin, becomes IQE MA (IQE).
- Continuing technical progress in FY13 and partial FY14. R&D subcontracts terminated in Jan-Mar 2014 due to lack of additional funding.
- Briefing to DoE AS Pat Hoffman on 27 March 2014. Additional input on interest level of major system integrators on GIGA technology requested. 5kV "notional" datasheet developed.
- Apr-June 2014 remaining GIGA technical work at Lincoln wound down; submission of last QPR.
- Mid 2014, K. Cheung replaced G. Bindewald as Program Manager.
- June 2014 -present (post GIGA) Lincoln shifted focus on GaN-on-Si for RF and other applications; growth and device fabrication on 200 mm GaN-on-Si wafers; CMOS compatible (gold free) processing in the Lincoln MEL; continuing independent technical development work at MIT, MTS and IQE on GaN-on-Si materials and devices for a variety of applications, with the ability to reconstitute a coordinated GIGA-team-like power electronics program if future funding were available.

3. Review of Technical Highlights

The following table summarizes the technical highlights of accomplishments under the GIGA program, described in each of the 18 quarterly reports submitted to EERE:

QPR	Quarter	Technical Highlights Each Quarter
1	Y1Q1	• Established Interagency Agreement between DOE and MIT Lincoln Laboratory (MIT/LL), with major R&D subcontracts issued to MIT campus (MIT) and M/A-COM Technology Solutions (MTS) • Developed high-temperature rapid thermal annealing (HT-RTA) for implant annealing studies – <MIT/LL> • Addressed impurity issues in hydride vapor phase epitaxy (HVPE) GaN process – <MIT/LL> • Deposited HVPE-GaN for overgrowth /improved yield – <MIT/LL> • Developed a new dual-gate GaN transistor structure to combine high threshold voltage (2.9 V), low on-resistance (5 m and high breakdown voltage (640 V)- <MIT> • Developed a substrate-removal technology to increase the breakdown voltage of GaN-on-Si transistors beyond 1,500 V -<MIT> • Mask Designed for Buffer Leakage / Isolation Experiments – <MTS> • Buffer Leakage / Isolation Wafer Runs initiated – <MTS>
2	Y1Q2	• Performed major reworking of gas purification system for HVPE substrate growth <MIT/LL> • Investigated the establishment of a 200mm GaN-on-Si OMVPE epitaxial growth capability at Lincoln Laboratory <MIT/LL> • Studied of the breakdown mechanism of GaN-on-Si transistors <MIT> • Developed an ion implantation technology for engineering the contact and sheet resistance in GaN-based power transistors. <MIT & MIT/LL > • New mask set with 116 three terminal design/process variants submitted to CAD layout <MTS>
3	Y1Q3	• Delivered four initial semi-insulating HVPE GaN templates for device overgrowth <MIT/LL> • Identified, procured and initiated facilitization of new MOCVD reactor <MIT/LL> • Studied of the breakdown mechanism of GaN-on-Si transistors <MIT> • New mask set with 116 three terminal design/process variants submitted to CAD layout.<MTS>
4	Y1Q4	• Corrected safety issue with H2 in HVPE reactor <MIT/LL> • Progress made towards the startup of new III-N MOCVD reactor <MIT/LL> • Studied the design-space for high voltage GaN transistors <MIT> • Additional device characterizations results were obtained <MTS> • Design work on V_{br} >1200 Schottky diodes was begun <MTS>
5	Y	Vbr≥*1800*V Device <MIT>

	2Q1	• Design procedure for High Breakdown Voltage Device <MIT> • Additional device characterizations results were obtained <MTS> • Design work on V_{br} >1200V Schottky diodes was begun <MTS>
6	Y2Q2	• Completed facilitization/installation of MOCVD reactor <MIT/LL> • Successful growth and characterization of initial III-N MOCVD films <MIT/LL> • Specified & ordered *in situ* growth monitoring tool for III-N growth on Si <MIT/LL> Vbr≥*1800*□Device <MIT> • Design procedure for High Breakdown Voltage Device <MIT> • Initial characterization of pulsed-IV performance of GaN power devices. <MIT> • Additional device characterizations results were obtained <MTS> • Design work on V_{br} >1200V Schottky diodes was begun <MTS>
7	Y2Q3	• Successfully grew AlGaN HEMT epilayers on 2-in sapphire <MIT/LL> • Grew initial III-N epilayers on 4-in (111) Si <MIT/LL> • Installed *in situ* growth monitoring tool for III-N growth on Si <MIT/LL> Vbr≥*2500*□device from MIT-LL GaN-on sapphire <MIT> • Investigated phase-change materials for enhanced device cooling <MIT> • Improved breakdown field with triple-N2 implant isolation <MTS> • Completed design work on V_{br}>1200V Schottky diodes <MTS>
8	Y2Q4	• Improved AlGaN HEMT epilayers on 2-in sapphire <MIT/LL> • Optimizing *in situ* growth monitoring tool for III-N growth on Si <MIT/LL> • Fabrication a high breakdown voltage GaN-on-Si (~2300V) transistor using substrate removal technology <MIT> • Lateral GaN-on-Si Schottky diode with high breakdown voltage (~ 800V) demonstrated <MTS>
9	Y3Q1	• Upgraded/repaired in-situ diagnostics setup/system wiring on growth reactor <MIT/LL> • Grew five advanced device structures requested by MIT Campus <MIT/LL> • Fabrication of a ~3000V breakdown voltage HEMT using substrate removal technology <MIT> • Simulation of design space for 5000 V lateral and vertical devices <MIT> • Breakdown voltage of 1500 V was achieved on a lateral ACFP GaN Schottky diodes <MTS>
10	Y3Q2	• Performed initial epitaxial growths on ammonothermal bulk GaN substrates <MIT/LL> • Seven advanced device structures grown as requested by MIT Campus <MIT/LL> • Initial optimization performed on growth of GaN on 4-in silicon wafers <MIT/LL> • Build/Setup offline susceptor annealing furnace for susceptor cleanings <MIT/LL> • High breakdown voltage HEMT fabricated using substrate removal technology <MIT> • Design space explored for development of 5000 V lateral and vertical devices <MIT> • Epitaxial variants designed and large order for materials placed with supplier <MTS> • Further investigations conducted as to the limits of breakdown voltage in

		present 2- and 3-terminal devices <MTS>
11	Y3Q3	• Developed uniform growth on 4-in sapphire substrates <MIT/LL> • Improved growth uniformity/stability on Si (111) <MIT/LL> • Developed a new surface cleaning procedure (ozone + UV) which helps to significantly reduce the interface traps in MIS-HEMTs to prevent frequency dispersion. <MIT> • Demonstrated GaN-on-Si diodes with blocking voltages in excess of 3kV. <MIT> • Achieved >1500 V three terminal reverse breakdown on a GaN on Si HEMT structure by passivating the GaN Surface. <MTS> • Reduced gate leakage current by >100x by forming a Ga_2O_3 layer directly under the gate metallization creating a depletion mode MISFET. <MTS> • Completed field plate modeling using a 2D structure simulator and have used the results to design and initiate a test matrix of double ACFP Schottky Diodes. <MTS> • Applying field plate modeling results to add a GCFP to the HEMT designs. Designs in layout. <MTS>
12	Y3Q4	• Installed/optimized improved in-situ diagnostic head <MIT/LL> • Improved stress control on Si (111) overgrowths <MIT/LL> • Evaluated Hall mobility in initial crack-free HEMT-on-Si material<MIT/LL> • Developed a barrier etch stop structure in which the gate recess etch could be precisely controlled. <MIT> • Demonstrated an E-mode GaN HEMTs with a record effective channel mobility and very low interface density of states. <MIT> • Demonstrated a peak I_{max} current in a three terminal HEMT structure having 10 mm of gate periphery of 5.5 A. <MTS> • Demonstrated a normalized peak I_{max} current handling in a three terminal HEMT structure of 740 mA/mm. <MTS> • Demonstrated a peak forward current in a ACFP lateral GaN Schottky diode of 10 A. <MTS> • Applying field plate modeling results to add a GCFP to the HEMT designs. Designs in layout. <MTS> • Growth and calibration of AlN/GaN super-lattice buffer layers for stress management in GaN-on-Si HEMT structures (IQE)
13	Y4Q1	• Grew and delivered advanced device layers to MIT Campus <MIT/LL> • Investigated the effect of wafer crystal orientation miscut on Si (111) overgrowths <MIT/LL> • Achieved AlGaN/GaN HEMT on (111) Si with virtually no post-growth wafer bow. <IQE > • Evaluated material properties and on-wafer uniformity of AlGaN/GaN HEMT on (111) Si. <IQE> • Demonstrated high 2DEG mobility of 1660 cm^2/V s and on-wafer sheet resistance non-uniformity of about 3.6 %. <IQE > • Developed an Au-free Ohmic contact with low annealing temperature on the barrier etch stop structure. <MIT> • Effectively modulated the device threshold voltage by Fluorine treating the device active region surface. <MIT> • Analyzed Lots 1761020, 1761022, 1761024 for trapping behavior <MTS> • Applied a Plasma O2 treatment to create a G2O3 MISHEMT <MTS>

		• Measured a 0.2 to 0.4 V increase in the barrier height <MTS> • Demonstrated 100x reduction in reverse leakage by application of a Ga_2O_3 barrier <MTS> • Demonstrated a peak forward current in a ACFP lateral GaN Schottky diode of 8 A for an epitaxial variant with lower 2DEG sheet charge <MTS> • Demonstrated the integrity of the Ga_2O_3 barrier under high forward current stress <MTS> • Completed new mask layout to add a GCFP and dual GFCP/SCFP structures to the HEMT designs <MTS>
14	Y4Q2	• AlN nucleation layer optimization study <MIT/LL> • GaN-on Si wafer stress optimization <MIT/LL> • Mg and C doping studies in GaN <MIT/LL> • Growth of very low dislocation HEMT epilayers on ammonothermal substrates <MIT/LL> • N+ GaN sputter target growth for MIT Campus <MIT/LL> • Developed up to ~ 5 µm thick crack-free, low wafer bow AlGaN/GaN HEMT structures on (111) Si <IQE> • Demonstrated high electron mobility of >1750 $cm^2/V{\cdot}s$ for the sheet charge density of about $8{\times}10^{12}$ cm^{-2}. <IQE > • Demonstrated the HEMT DC characteristics comparable to those for devices on sapphire. <IQE> • Demonstrated two-terminal breakdown voltage of about 1000 V for 5µm isolating space. <IQE > • Developed an Au-free Ohmic contact with low annealing temperature on AlGaN/GaN structure. <MIT> • Process on making GaN-on-diamond structure by layer transfer and wafer bonding technology. <MIT> • Measured 15 A of I_{max} current handling on a 30 mm HEMT design on lot1761020 <MTS> • Applied a Plasma O_2 treatment to create a G_2O_3 MISHEMT <MTS> • Measured 1640 volt breakdown on a dual ACFP design <MTS> • Demonstrated 10,000x reduction in reverse leakage by application of a Ga_2O_3 barrier and a dual ACFP <MTS> • Initiated lots utilizing the new mask layout (1864) to add a GCFP and dual GFCP/SCFP structures to the HEMT designs <MTS> • Initiated Experiments to investigate HfO_2 passivation on HEMT devices <MTS> • Evaluated initial IQE epitaxy through the isolation implant process <MTS>
15	Y4Q3	• Improved 2DEG mobilities on 4-in Al_2O_3 <MIT/LL> with record mobilities of >2200 cm^2/V-s at a sheet charge density of ~1e13 cm^{-2} • Lower HEMT access resistance development using modified epitaxial structure/selective etching <MIT/LL> • Demonstrated AlGaN/GaN HEMT structures with three-terminal breakdown voltage of >1000 V. <IQE> • Developed 7 µm thick crack-free AlGaN/GaN HEMT structures on (111) Si. <IQE> • Improved crystalline quality of AlGaN/GaN HEMT structures achieving (002) and (102) x-ray rocking curve FWHM of about 600 arcsec and 1000 arcsec, respectively. <IQE>

		• Developed a new room-temperature SiN passivation technology. <MIT> • Measured the equivalent of 20 A of I_{max} current handling for 30 mm HEMT design on a packaged multi-field plate HEMT from lot 1864001 <MTS> • Measured >2000 volt breakdown on a dual ACFP design <MTS> • Demonstrated 10,000x reduction in reverse leakage by application of a Ga_2O_3 barrier and a multiple field plates on both HEMT and lateral Schottky diode devices <MTS> • Indentified the most likely sources of tunneling based leakage in Ni/Au electrodes and validated that these tunneling mechanisms can be modulated by field plate design <MTS> • Completed the initial lot of the 1864 HEMT design which included a GCFP and dual GFCP/SCFP structures in the test matrix<MTS> • Initiated an 1813 lateral Schottky diode lot which included a 3rd ACFP to further reduce leakage and improve reverse breakdown voltage • Continuing Experiments to investigate HfO_2 passivation on HEMT devices <MTS> • Continuing to evaluate IQE epitaxy on both HEMT and lateral Schottky diode structures <MTS>
16	Y4Q4	• Optimized and characterized selective GaN etch <MIT/LL> • Demonstrated performance impact of optimized etch on HEMTs, showing device improvement resulting from decreased plasma damage <MIT/LL> • Commenced evaluation IQE material for studying dynamic transistor characteristics <MIT/LL> • Developed up to 5 µm thick crack-free AlGaN/GaN structures on Si substrate with < 50 µm post-growth bow and warp. <IQE> • Achieved 7 µm thick crack-free AlGaN/GaN structures on Si substrate. <IQE> • Achieved (002) and (102) x-ray rocking curve FWHM of about 400 arcsec and 640 arcsec, respectively. <IQE> • Demonstrated AlGaN/GaN HEMT structures with high electron mobility of about 1800 $cm^2/V\ s$ and associated sheet charge density of ~ $7\times10^{12}\ cm^{-2}$. <IQE> • Demonstrated AlGaN/GaN HEMT structures on Si substrate having DC characteristics comparable to those for devices on sapphire. <IQE> • Demonstrated AlGaN/GaN HEMT structures with low leakage currents and breakdown voltages of >1000 V. <IQE>
17	Y5Q1	• The R&D subcontracts to the 3 GIGA partners (MTS, MIT Campus and IQE MA) were not been renewed in FY14 due to lack of new funding and thus this QPR presented only remaining work by MIT Lincoln Laboratory <MIT/LL> • Evaluated IQE MA material with improved channel structures <MIT/LL> • Fabricated and tested transistors using modified IQE MA material structure and tested dynamic transistor characteristics <MIT/LL>
18	Y5Q2	• Final QPR presented only very limited work by MIT Lincoln Laboratory <MIT/LL>

4. Detailed Accomplishments

In the following sections, additional technical details will be provided in the selected areas of (1) materials/wafer development (2) diode development and (3) transistor development.

4.1 Materials/Wafer Development

From the start of the GIGA program, having a reliable domestic source of epitaxial materials was considered critical for the ultimate success of the program. Having the ability to customize parameters, such as epitaxial layer thickness, barrier composition and thickness and wafer bow beyond standard "commercial" metrics would be necessary to achieve the higher breakdown voltages and higher currents required for grid applications. While early best device results were obtained from only one non-domestic supplier, this clearly was not a viable path forward.

The development of materials followed two major pathways, based upon the choice of starting substrate. The primary focus of GIGA was to develop GaN power devices on low-cost (111) Si substrates to allow for the significant advantages of scaling and cost reduction over competing approaches such as GaN-on-SiC. The challenges associated with growth on Si substrates were addressed under this program. A second, much smaller effort was to develop the homoepitaxial growth on recently commercialized ammonothermal substrates, to afford significant reductions in the number of structural defects to study their impact on device high voltage device performance.

4.1.1 GaN on Si (111)

Stress Control

Generally, limitations on wafer bow are based on processing requirements, such as acceptable limits in various lithography tools. Additionally, non-stress-engineered epilayers on silicon are generally tensile stressed due to GaN's higher thermal expansion coefficient vs. silicon, leading to film cracking. Early in the program it was shown that optimization of the buffer layer structure, specifically the short-period superlattice (SPSL), is important for minimization of the resultant wafer bow. This is due to the buildup of compressive stress in the epilayer during the growth of the superlattice that counterbalances the tensile stress buildup on cool down in the film due to its higher thermal expansion coefficient, as compared with the silicon substrate. Generally, higher voltage operation requires either a thicker GaN buffer layer or removal of the silicon substrate due to intrinsic limitations on the resistivity and critical field in high purity silicon. Thicker epilayers are more technically challenging due to commensurate requirements on stress evolution, electrical properties and dislocation densities. As demonstrated in this program, ultimately removal of the substrate and bonding to an electrically insulating heat spreader would optimize performance if it could be done economically.

Most of the materials development for GIGA was done on 100mm diameter Si (111) starting substrates. This was based on the fabrication requirements of MTS, as well as the desire to push the performance limits on the device layers without the requirement to do this over larger areas. Scaling to 200mm diameter substrates was always considered to be our long term target to: a.) significantly reduce materials cost b.) benefit from the more advanced, supported lithography tool set generally designed at the 200mm wafer size and c.) make wafers that could be processed in Lincoln Laboratory's silicon process facility that was recently retooled to 200mm. Additionally, MTS had processed a number of 200mm GaN-on Si wafers at the Intel Hudson facility.

In optimizing the layer structure, it was found that the deposition parameters of the AlN layer (particularly thickness) also play a significant role in the evolution of the curvature of the wafers. For example, a series of HEMT layers were grown where the thickness of the AlN nucleation layer was varied from 185 to 300 nm. The overall structure is shown in Figure 1.

GaN	~2nm
$Al_{0.27}Ga_{0.73}N$	26nm
AlN	~1nm
GaN	430nm
AlN/GaN SL	7nm/40nm x50
GaN	60nm
AlN	185-300nm
Si (111)	625 μm

Figure 1 - HEMT structure used to optimize AlN nucleation layer thickness.(MIT/LL)

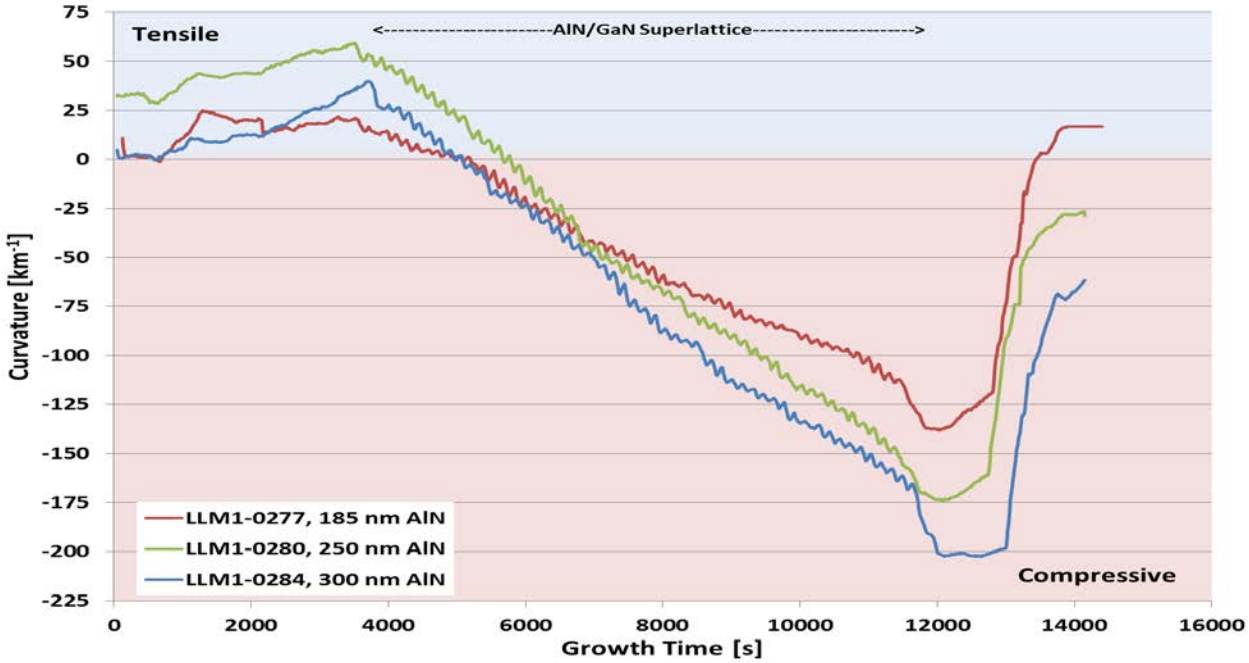


Figure 2 - Stress evolution in AlGaN HEMT structure grown on silicon with varying AlN nucleation layer thickness. Note: negative values correspond to compressive stress (convex curvature).(MIT/LL)

The stress state of the wafer during growth was monitored by measuring the curvature of the wafer during the growth, using an *in-situ* curvature sensor from Lay-tec. The results of three AlGaN HEMT layer growths, with the thickness of the AlN nucleation layer varied, are shown in Figure 2. **Figure** The total epilayer thickness of these samples were >3μm. As can be seen in this chart, the evolution of compressive strain during the growth of the SPSL does seem to proceed more quickly for thicker AlN nucleation layers. This change in stress during the SPSL ends up being the predominant factor in determining the final strain state of the wafer, with the sample with the thickest AlN nucleation layer giving the highest level of compressive stress at the end of the run. As can be seen, during cool down, this compressive stress is compensated by the TCE mismatch strain.

The curvatures of GaN-on-Si wafers were measured, at room temperature, *ex situ* of the reactor. Linear traces of the wafer shape, through the center of the wafer, are shown in Figure 3. It is important to note that none of these samples had any cracks except very close (<1 mm) to the edge. As can be seen, the sample with the thinnest (185 nm) AlN nucleation layer shows about 44 μm of concave bow. The two samples with thicker AlN buffers are both convex, indicative of net compressive stress in the epilayer at room temperature.

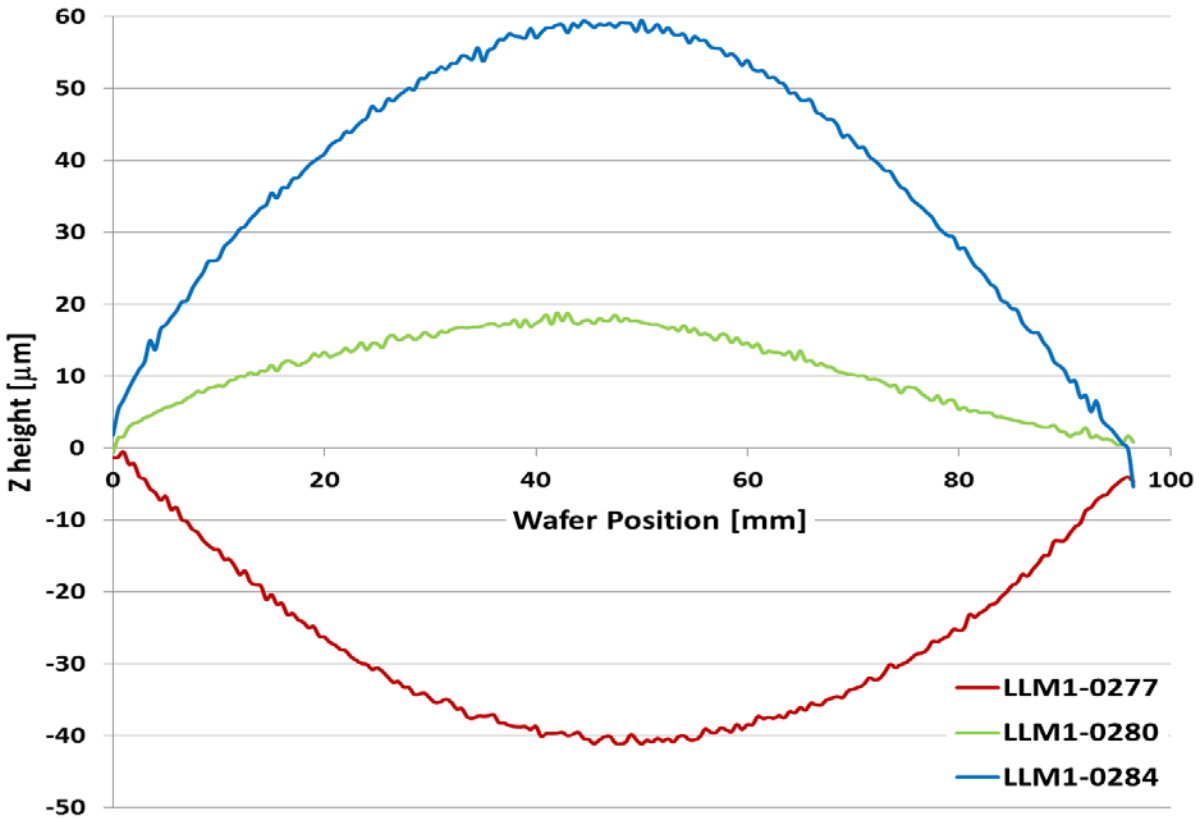


Figure 3 - Room temperature scans across centers of 100 mm AlGaN HEMT-on-Si epiwafers.(MIT/LL)

Conductivity Control

Having the ability to precisely control the conductivity in various device and buffer layers is critical for achieving high-voltage operation in GaN-on-Si power devices. Leakage paths in a device structure serve to dissipate power and generate heat that can cause the premature breakdown of the device and/or limit reliability. Iron (Fe) and Carbon (C) are two common compensating impurities used in GaN devices and both were utilized to control breakdown behavior in the device layers grown for this program.

Iron (Fe) Doping

A set of samples was grown at IQE under the same growth conditions using various ferrocene fluxes in order to assess the vapor phase to solid phase (vapor-solid) distribution coefficient of Fe and a controllability range of the Fe doping. The ferrocene flux used during the SL growth was the same for both the GaN and AlN layers. Samples were analyzed by SIMS depth profiling. Figure 4 reports the Fe concentration in the bulk GaN and GaN/AlN SL as a function of the ferrocene flux into reactor. The Fe concentration in the GaN/AlN SL is the "average" Fe concentration yielded by SIMS over the entire set of GaN/AlN pairs. The actual Fe concentration can be different in each layer constituting SL and different from the "average" Fe concentration.

One can see in Figure 4 that the Fe concentration is controlled by varying ferrocene flux in the range of 1×10^{18} – 1×10^{20} cm^{-3}. It can be also seen that the Fe concentration in GaN increases almost linearly with increasing ferrocene flux. The vapor-solid distribution coefficient is approximately 1. The Fe concentration in the GaN/AlN SL is about one order of magnitude higher than that in GaN and the dependence of the Fe concentration on the ferrocene flux is somewhat sublinear. It should be noted that the GaN layers in the SL were grown under the same conditions with that for the bulk GaN. The high Fe concentration in the SL can be due to the high Fe concentration in AlN which in turn can be explained by low growth rate of the AlN layers in SL. High Fe concentration in AlN can be also due to the Fe segregation on the surface of GaN. The SIMS studies of the uncapped SL structures confirm high Fe concentration in AlN

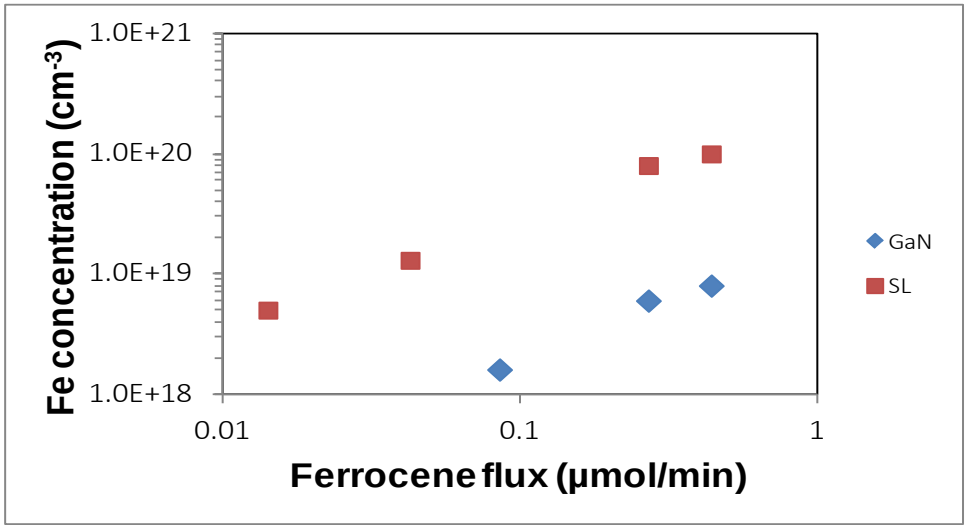


Figure 4**.** Fe concentration in GaN (blue diamonds) and GaN/AlN/SL (red squares) grown on Si substrate as a function of ferrocene flux into MOCVD reactor. (IQE)

layers of the SL. Figure 5 illustrates the SIMS analysis of the Fe depth profile in the 35 pair SL where a few uppermost GaN/AlN pairs exhibit clear oscillations of the Fe concentration. Based on the analysis of the uppermost layers of the SL, the Fe concentration in the AlN layers of the SL is approximately 4 times higher than that in the GaN. The Fe concentration oscillations deep inside the SL fade during SIMS profiling due to increasing roughness of the analyzed surface with increasing sputtering depth.

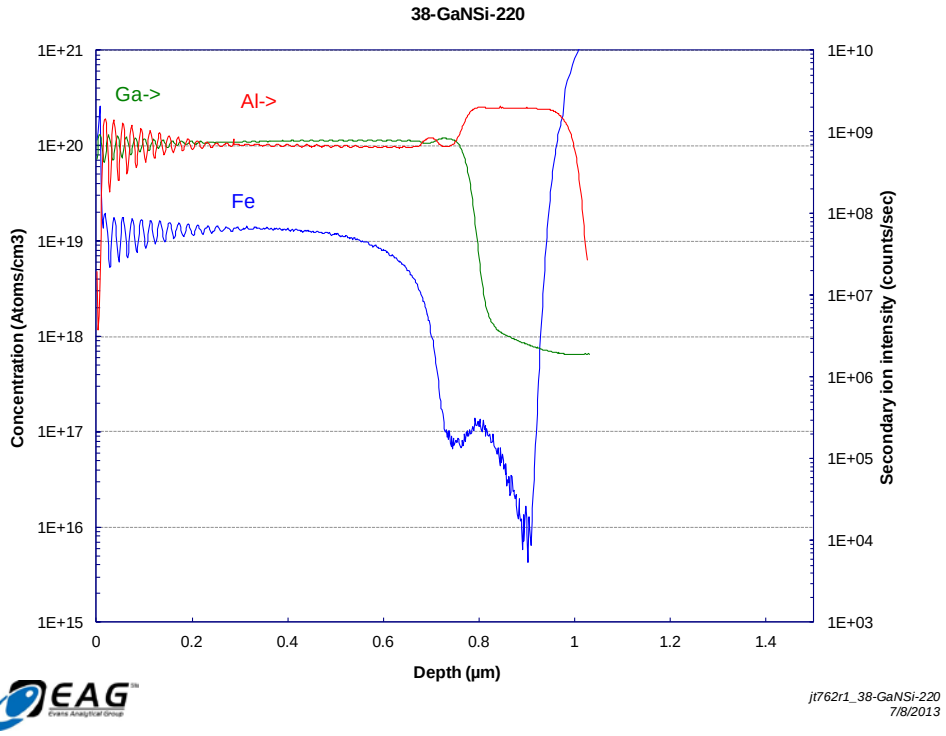


Figure 5. SIMS Fe concentration (blue line) depth profile overlaid with the matrix elements markers in GaN/AlN SL structure. The Fe concentration in the uppermost AlN and GaN layers of the SL is approximately 2×10^{19} and 5×10^{18} cm^{-3}, respectively. (IQE)

Carbon (C) Doping

The incorporation of carbon (from the prevalent organic molecules that exist in the reactor due to the cracking of the metalorganic sources materials) is well known to depend on a number of growth parameters, including growth temperature, pressure and growth rate. In order to study this behavior, MIT/LL grew a series of GaN samples where different growth conditions were established and the resultant incorporation of carbon was determined, post-growth, by secondary ion mass spectroscopy (SIMS) analysis. For each sample, grown at a specific temperature, twelve different pressure/growth rate conditions were determined. The results are shown in Figure 6.

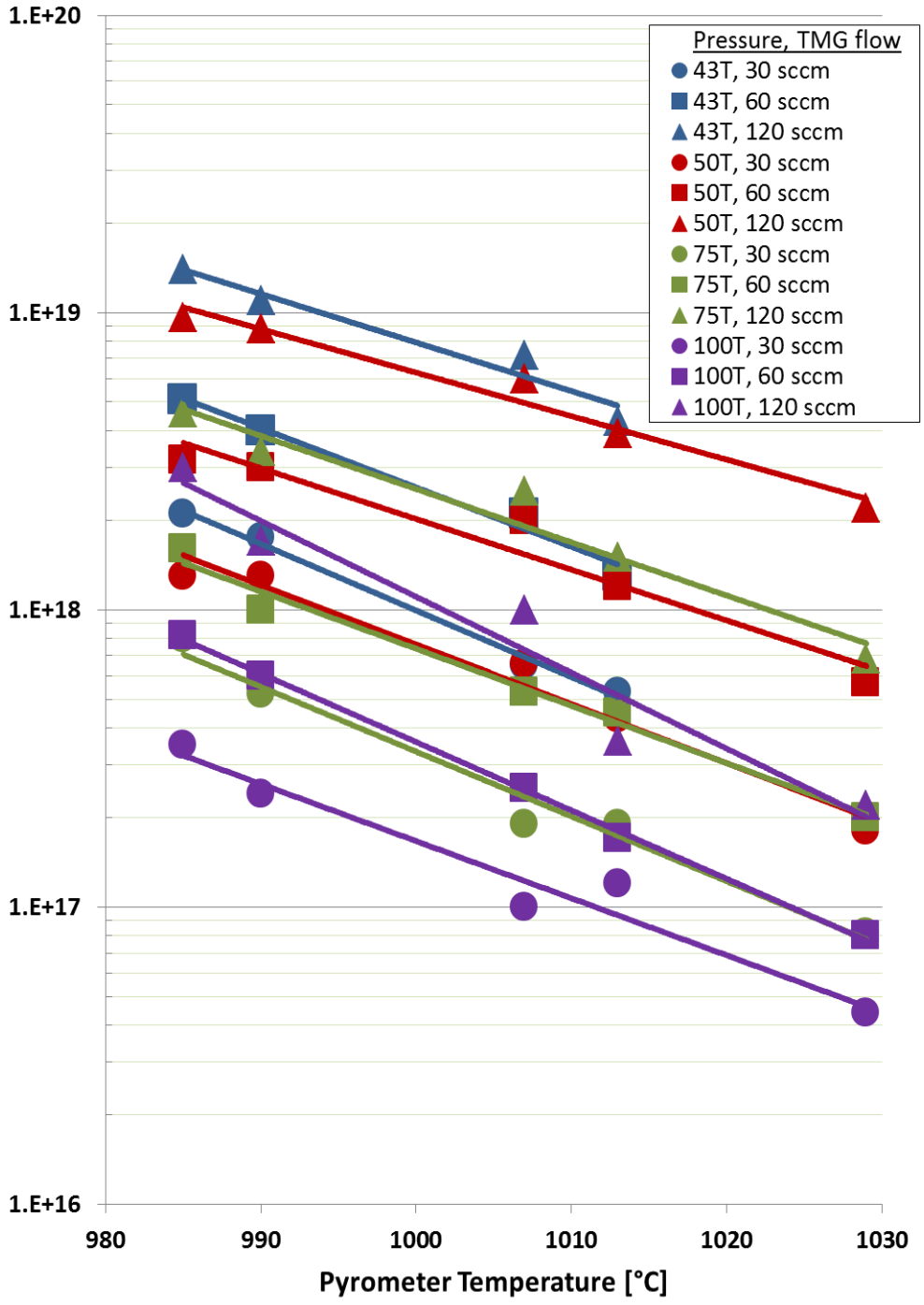


Figure 6 - Carbon concentration measured by SIMS in GaN layers grown with varying temperature, pressure and TMGa flow (growth) rate. (MIT/LL)

GaN-on-Si Wafer Uniformity

Figure 7 reports the thickness maps for the 2.5 µm, 3.5 µm and 5 µm thick GaN HEMT structures on 4-inch (111) Si substrates. The actual average thicknesses are 2.4, 3.5 and 4.9 µm, respectively. The standard thickness deviation across the wafers with 4 mm edge exclusion is in the range of 1.6 – 2.0 %. The 3.5 and 4.9 µm thick structures as well as the standard one exhibit

a crack-free surface morphology across the entire wafer with the exclusion of very narrow (about 1 mm) wafer rim.

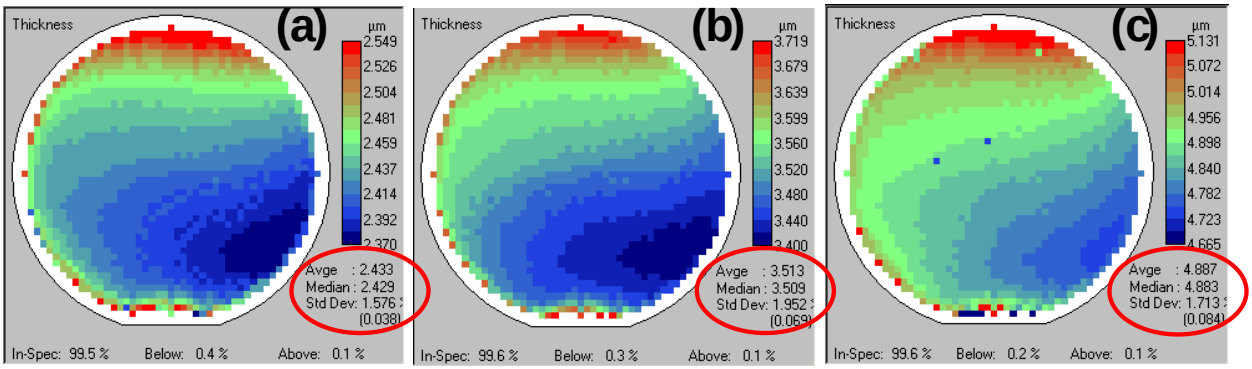


Figure 7**.** Thickness maps of 2.5 µm (a), 3.5 µm (b) and 5 µm (c) thick GaN HEMT on (111) Si. (IQE)

The post-growth wafer bow was measured using MTI Instrument thickness measurement tool described in previous reports. Figure 8 shows the plots of the median wafer surface for the 3.5 and 4.9 µm thick HEMT structures as well as the 2.4 µm thick structure. The 3 point wafer bow calculated by MTI Instrument software is 6 (convex shape), -17 (concave shape) and -2 (concave shape) µm for 2.4, 3.5 and 4.9 µm thick structure, respectively. This result demonstrates that a virtually flat GaN HEMT structure up to 5 µm in thickness can be successfully grown on Si substrate using GaN/AlN SL.

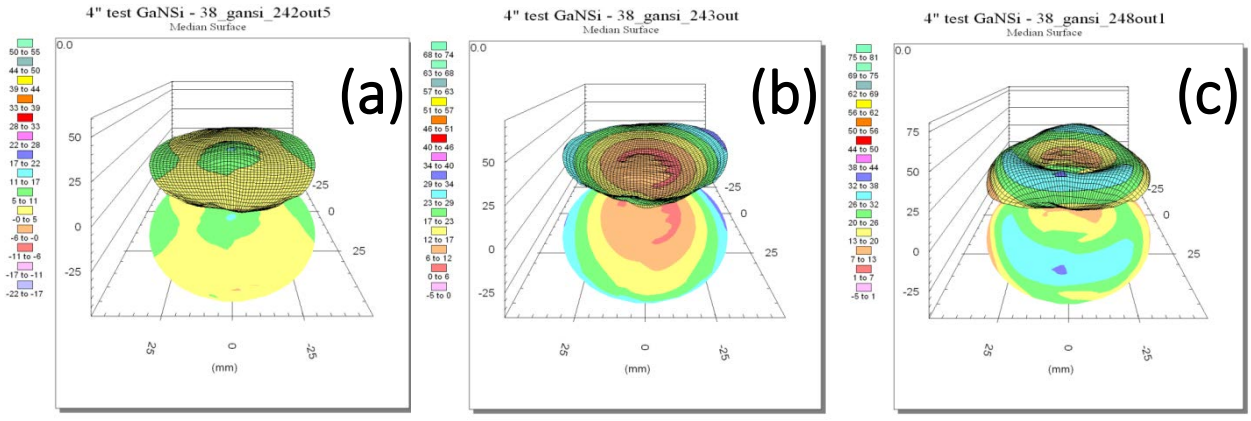


Figure 8. Post-growth median wafer surface plots of 2.4 µm (a), 3.5 µm (b) and 4.9 µm (c) thick GaN HEMT on (111) Si. The wafer bow is 6 (convex), -17 (concave) and -2 (concave) µm for 2.4, 3.5 and 4.9 µm thick structure, respectively. (IQE)

The crystalline quality of the HEMT structures with different thicknesses was analyzed using a Philips MRD X'pert high resolution x-ray diffractometer. The full width at half maximum (FWHM) of the x-ray rocking curves were measured and analyzed in (002) symmetric and (102) asymmetric reflections. The room temperature Hall effect measurements were carried out on the Accent HL5500 Hall system to assess the electron transport properties of the GaN-based HEMT

structures with different thicknesses. The Ti/Al/Ni/Au ohmic contacts were formed using Van der Pauw geometry on the as-grown wafers. Table 1 summarizes the crystalline and electron transport properties of the 2.4 µm, 3.5 µm and 4.9 µm thick GaN HEMT structures on (111) Si substrate.

thickness, µm	2.4	3.5	4.9
(002) FWHM, arcsec	795	759	693
(102) FWHM, arcsec	1300	1189	1164
2DEG density, cm^{-2}	8×10^{12}	7×10^{12}	8×10^{12}
2DEG mobiliry, cm^2/Vs	1630	1790	1770

Table 1. Summary of x-ray and Hall effect data obtained from 2.4, 3.5 and 4.9 µm thick HEMT structures grown on Si substrate. (IQE)

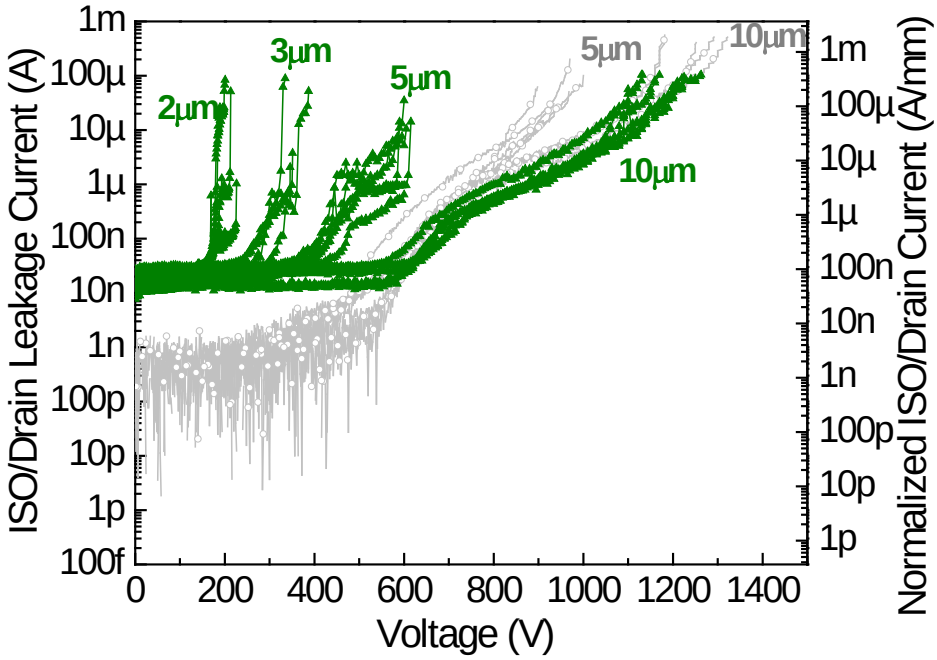


Figure 9 - 3-terminal punch-through (green) and 2-terminal isolation (grey) characteristics for 3.5 µm thick HEMT structure. The gate to drain distance varies from 2 to 10 µm for the 3-terminal device structure. The 2-terminal characteristics are shown for 5 and 10 µm wide gaps.

IQE measured the three-terminal punch-through characteristics of the 2.5, 3.5 and 5 µm thick structures, as shown in Figure 9. HEMT patterns with the gate to drain distance varying from 2 to 10 µm were characterized and compared to the two-terminal isolation characteristics for 5 and 10 µm wide gaps. The three-terminal punch-through voltage scales well with increasing gate to drain distance up to 10 µm. For a 10 µm gate to drain distance, the three-terminal leakage current follows the curve of the two-terminal isolation current for a 10 µm gap. It suggests that a device leakage occurred mostly through the buffer layer for this type of HEMT. For shorter gate to drain distances (2 – 5 µm), the punch-through may occur in the active region of the device.

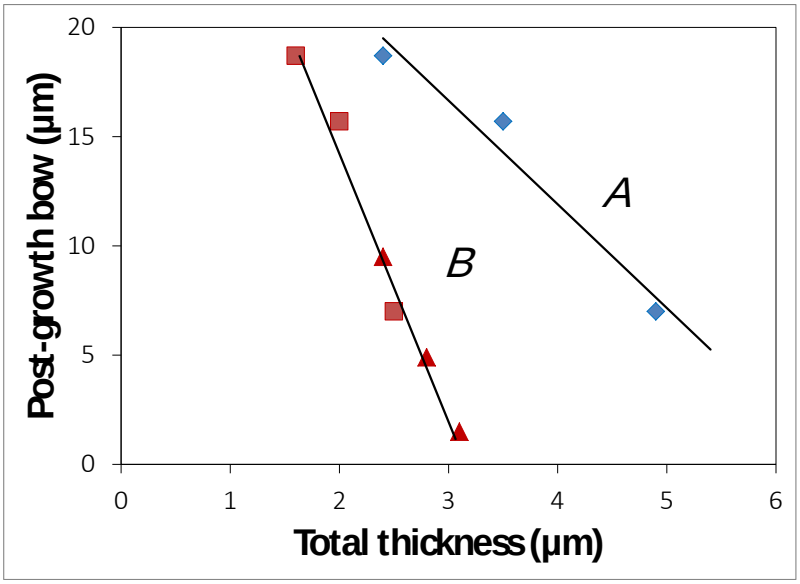


Figure 10. Post-growth wafer bow as a function of total thickness of GaN-based structure for series A and B. Red square and red triangle symbols correspond to the structures based on 35 and 76 pairs SL, respectively.(IQE)

In early studies, in order to increase the total thickness of GaN-based HEMT structure, IQE simultaneously increased both the number of pairs in SL and the thickness of the GaN buffer layer grown over the SL. In particular, the number of pairs increased from 76 to 180 and GaN buffer thickness from 0.7 to 1.5 µm to increase the total thickness of GaN-based HEMT from about 2.5 to about 5 µm. This set of structures will be referred to as series A.

In more recent work, IQE synthesized a set of structures with the number of pairs in SL fixed at either 35 or 76 and the thickness of GaN buffer layer varying in the range of 0.7 – 1.9 µm. The total thickness of GaN-based HEMT structures thus achieved was in the range of 1.6 – 3.2 µm. As before, the conductive and high-resistivity 4 inch (111) Si substrates were used for the growth of structures. This set of samples is referred to below as series B.

The in-situ observations for series A and B were confirmed by the post-growth wafer bow measurements on a MTI Instrument thickness measurement tool. The post-growth wafer bow measurements are summarized in Figure 10, where the post-growth wafer bow is plotted as a function of total thickness of GaN-based structure for series A and B. All the wafers from both series had slight convex shape with the wafer bow ranging between 0 and 20 µm. However, the wafer bow trends negative faster for series B compared to series A. It implies that a flat GaN-on-Si wafer can be more easily synthesized using approach employed in series A, i.e. proportionally increasing thickness of both SL and GaN buffer layer grown over the SL.

If two structures from series A and B, having the same total thickness, are compared with respect to their x-ray properties, the structures from series B exhibit narrower (002) and (102) x-ray peaks. This finding is illustrated in Figure 11. The 2.5 µm thick structures were chosen for given example. The x-ray FWHM in both reflections is 20 – 25 % narrower for series B sample. The narrower x-ray rocking curve indicates lower dislocation density and better crystal quality of GaN-based films grown in this series.

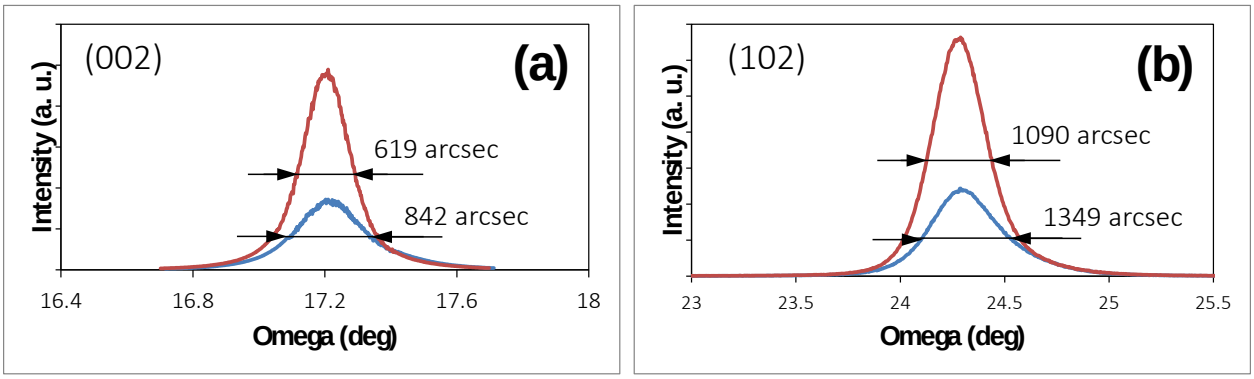


Figure 11 - The x-ray rocking curves in (002) (a) and (102) (b) reflections for 2.5 μm thick structures from series A (blue line) and series B (red line).(IQE)

Selected HEMT structures were sent to MTS for a device process evaluation. Structures had a post-growth wafer bow in the range of -10 to +20 μm (nearly flat wafers). During the wafer processing at MTS, it was revealed that most of the wafers could not be handled by the photo-stepper robot arm. In order to study the effect of the wafer shape on the handling issue, a set of the wafers with different shape was grown. The post-growth wafer shape was adjusted using thicknesses of the AlGaN layer grown over the AlN NL and of the GaN layers in the AlN/GaN SL. During our stress management studies, we found that an increase in thickness of both the AlGaN layer and GaN layer in the SL lead to more compressive stress in the structure and subsequently to more convex shape of the post-growth wafer. For this set of wafers, the AlGaN and GaN thicknesses were varied in 30 – 150 and 12 – 15 nm range, respectively.

Figure 12 illustrates the median wafer surface for a set of wafers with varied thickness of the GaN layers in the SL (Figure (a – c)) and varied AlGaN thickness (Figure (d – f)). One can see that the wafer shape was gradually changed from a convex, wafer bow of about 15 μm (Figure (a)), to a concave, wafer bow of about -30 μm (Figure (f)). This set of wafers was sent to MTS for the wafer handling evaluation.

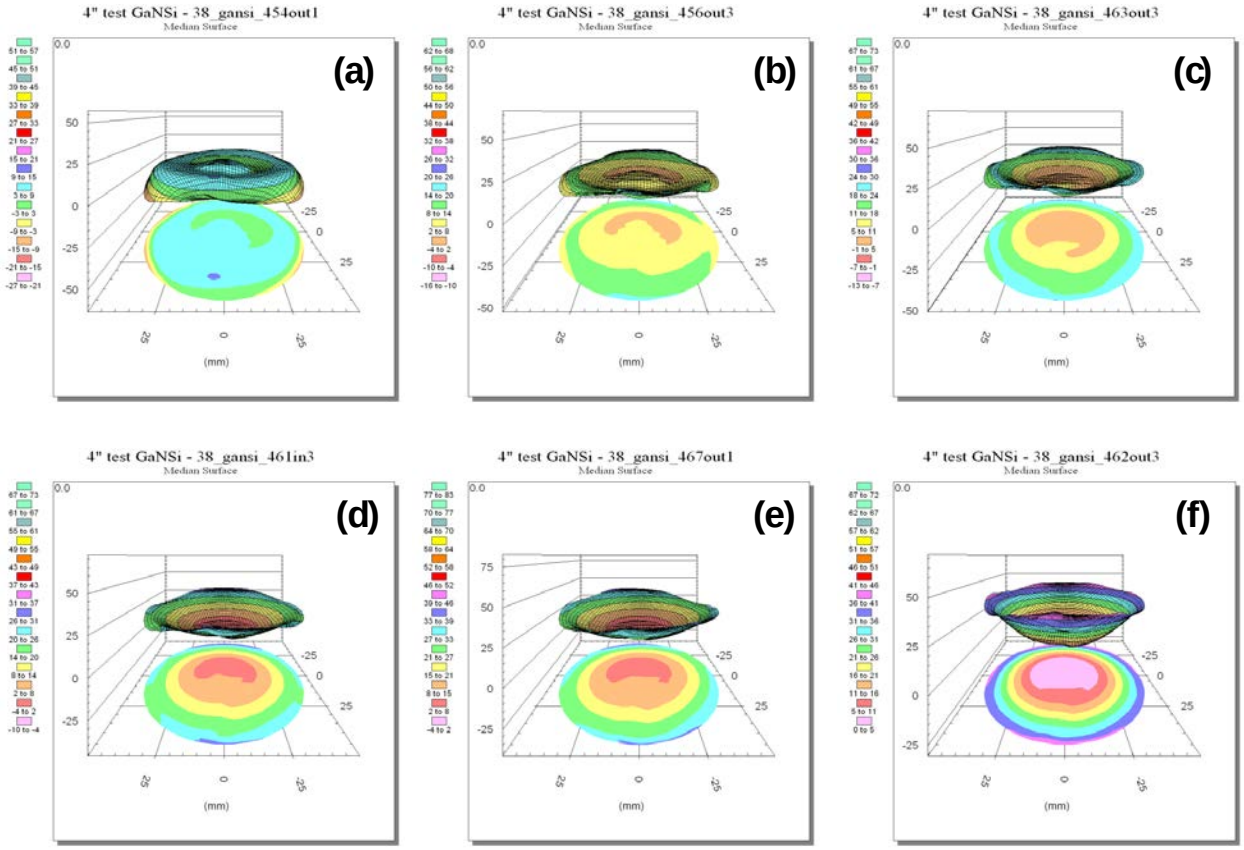


Figure 12 - Median wafer surface taken by MTI instrument for series of HEMT structures with adjusted thickness of GaN in AlN/GaN SL (a – c) and adjusted thickness of AlGaN layer (d – f).(IQE)

In order to assess the 2DEG transport properties of the HEMT, the sheet resistance of entire wafers was mapped using Lehighton contactless Eddy-current-based measurements. The typical Lehighton sheet resistance map is reported in Figure 13. The 2.5 μm thick AlGaN/GaN HEMT structures grown on the intrinsic Si substrates were used for this study. The AlGaN carrier supplying layer thickness and composition were 21 nm and 27 atomic % of Al. As shown in Figure 13, the average sheet resistance is 416 Ohm/sq. The excellent sheet resistance uniformity was obtained over 4 inch wafer with the sheet resistance standard deviation of 1.4 %. Using the Lehighton sheet resistance statistics and the following equation:

NON-UNIFORMITY = {(MAX – MIN)/(MAX + MIN)} × 100,

the sheet resistance non-uniformity was calculated to be 3.6 % which meets the critical program target for sheet resistance non-uniformity of < 5%. Further optimization of the GaN channel layer adjacent to the AlGaN carrier supplying layer (two-dimensional electron gas (2DEG) region) is necessary to reduce the HEMT sheet resistance to < 400 Ohm/sq.

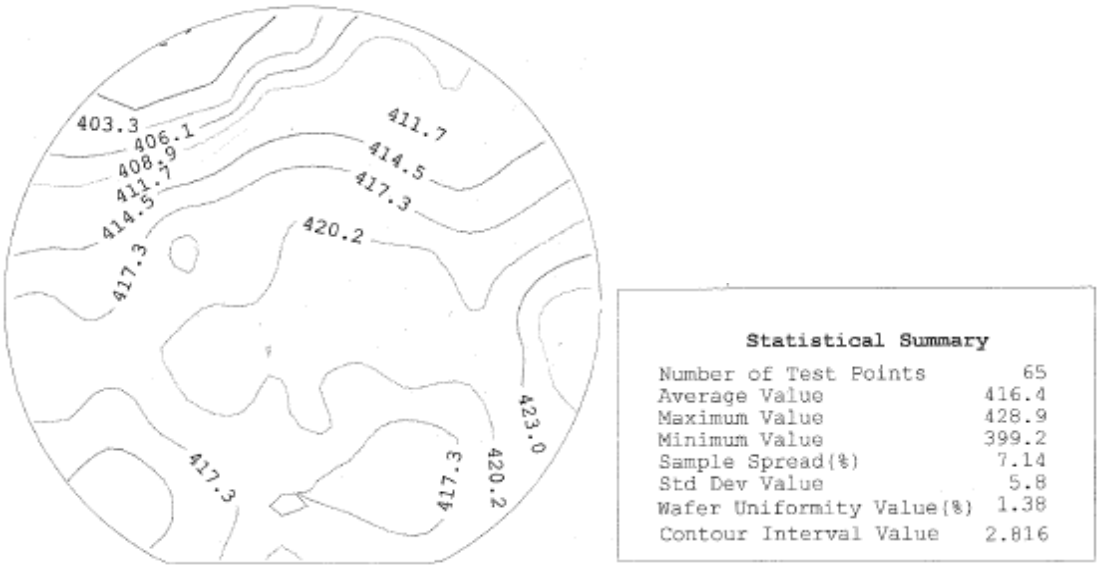


Figure 13 - Lehighton sheet resistance map of the AlGaN/GaN HEMT on 4 inch (111) Si substrate.

4.1.2 GaN Epitaxial Growth on Lattice-Matched Ammonothermal Bulk GaN

MIT/LL initially found that homoepitaxial growth on commercial ammonothermal GaN substrates was more difficult than expected, due to an observed epilayer roughening during the course of the run. Initially, it was speculated that this was the result of either insufficient surface polishing or residual surface contamination. Strategies employed to improve the cleaning and/or "etch-back" surface damage did not improve the experimental results. The growth strategy developed to achieve high quality growth was to eliminate thermal pretreatment of the GaN substrate prior to growth and initiating the epilayer growth at a reduced temperature. Because of the small substrate size (1-in diameter), MIT/LL fabricated a substrate holder from 4-in silicon substrates with a 1-in diameter laser-cut hole, positioned such that the 1-in wafer would pass under the optical port of *in-situ* diagnostic tool. This allowed the monitoring of the surface roughness during the growth. Growth was initiated immediately upon reaching the growth temperature, which was significantly lower (50-80°C) than is typically used for bulk GaN growth. Fairly quickly a slow reduction in the reflectance was seen which provided an indication that the sample was roughening. A small increase in growth temperature slowed this process and eventually, a slow recovery in the reflectance signal was seen when the growth temperature was restored to normal levels. The growth was allowed to continue for sufficient time to enable the growth of about 8 μm of material to allow the surface to replanarize and to spatially isolate the top HEMT layer from the highly conductive substrate.

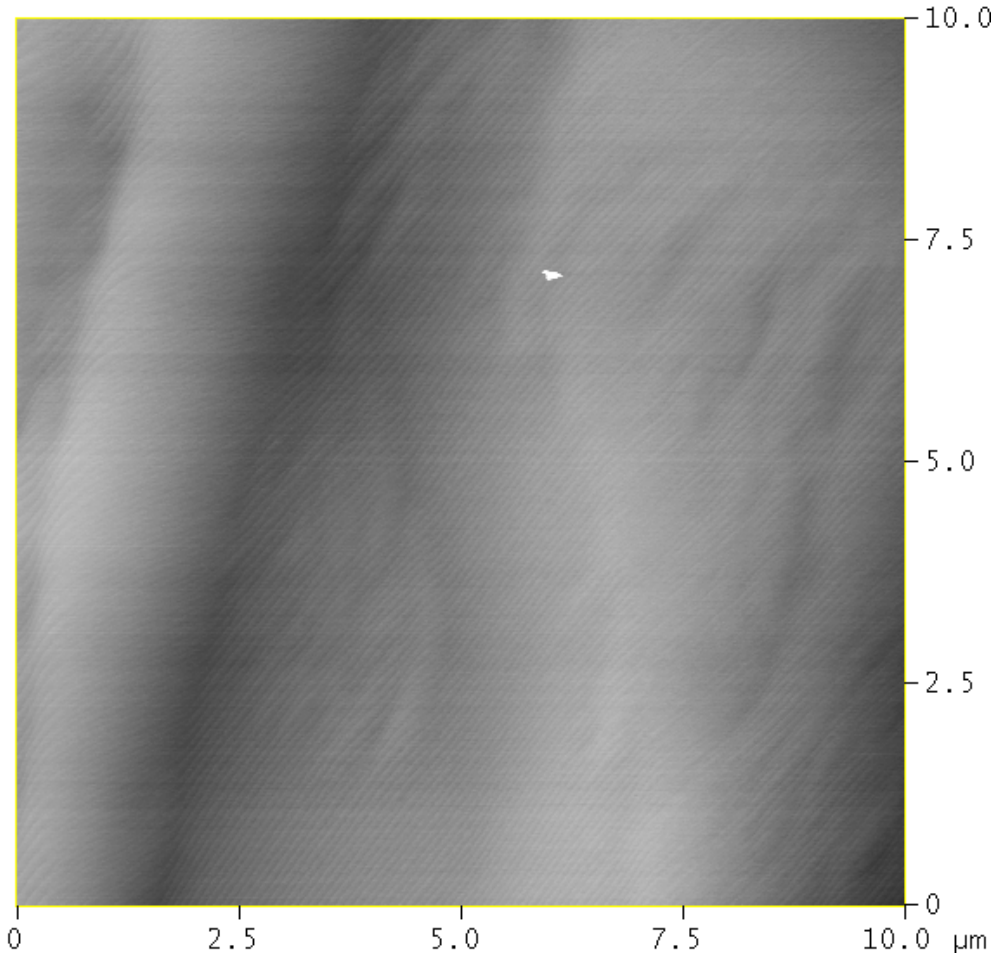


Figure 14 - 10x10 mm AFM scan of AlGaN HEMT structure grown on ammonothermal GaN substrate. RMS roughness is 0.908 nm, which is substantially improved over previous growths.(LL)

An AFM scan of the resultant surface is shown in Figure 14, showing smooth, parallel atomic terraces, with no observable "pinning" of these steps at dislocations. This suggests that these films have extremely low dislocation densities. The large scale features are consistent with the observed roughening of the surface early in the growth. The large scale of these features explains why the subsequent smoothing proceeded relatively slowly. It is believed that these features are the result of the structural transformation of the bulk material, as was seen previously. Hg-probe capacitance-voltage measurements of the structure are shown in Figure 15. As can be seem, accumulation of charge, typical for a 2DEG, is seem near the surface with very rapid (~1V) depletion of the 8 μm buffer layer. The increase in electron concentration at 8 μm is due to the high n-type doping of the GaN substrate.

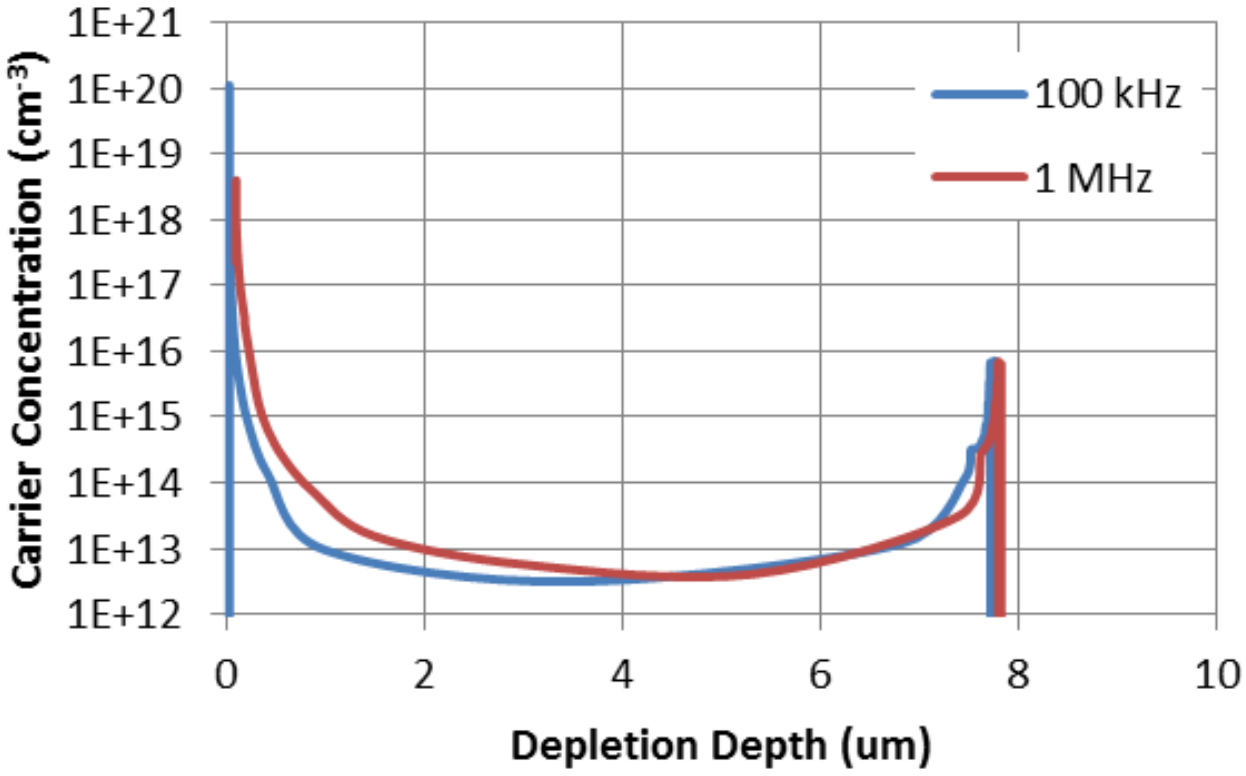


Figure 15 - Hg-probe C-V measurements of AlGaN HEMT structure grown on bulk ammonothermal GaN substrate (LL)

4.2 Diode Development

In the early stages of the GIGA program, it was realized that choosing lateral device geometries would lead to great synergism between simultaneously demonstrating high voltage 2-terminal Schottky barrier (SB) diodes and 3-terminal high electron mobility transistors (HEMTs) in the same fabrication process. In addition to shared fundamental device fabrication issues such as making good ohmic contacts, making good rectifying contact (SB and transistor gate), thermal management, controlled isolation and buffer leakage, etc., there was a recognition that incorporating SB diodes and transistors in very close proximity on the same layer would facilitate compact, manufacturable IC-like concepts for power circuits such as shown in Figure 16 below.

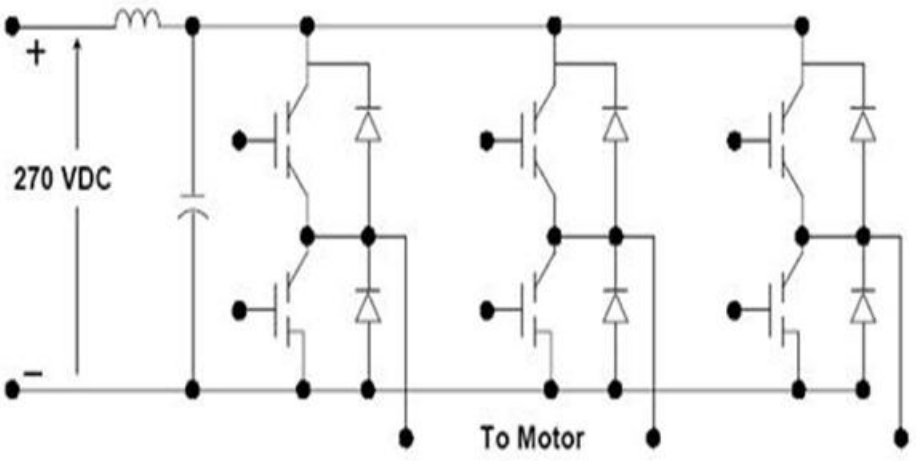


Figure 16 Typical DC-to-3 phase inverter (MTS)

Before the GIGA program was started , there was an original widely-held outside misconception that both the lattice mismatch defects and CTE induced stresses in GaN-on-Si wafers would limit their useful operating voltages to less than 600V – as opposed to devices produced from the much more highly developed GaN-on-SiC wafers. In the 2nd QPR, MTS reported and encouraging isolation study that showed that with proper ion implantation (as opposed to mesa etching) 2-terminal, variable-spacing test devices demonstrated an equipment-limited breakdown voltage of >1360V between the ohmic contacts. These early results were achieved with unpassivated structures and required the use of Fluorinert liquid on the top of the device to prevent arc flash over in air. Later in the program (QPR 9) MTS achieved a ~1500V breakdown Schottky barrier diode with an Anode-connected field plate (for improved electric field control) and a passivated surface (to prevent arc flash-over in air), as shown in Figure 17.

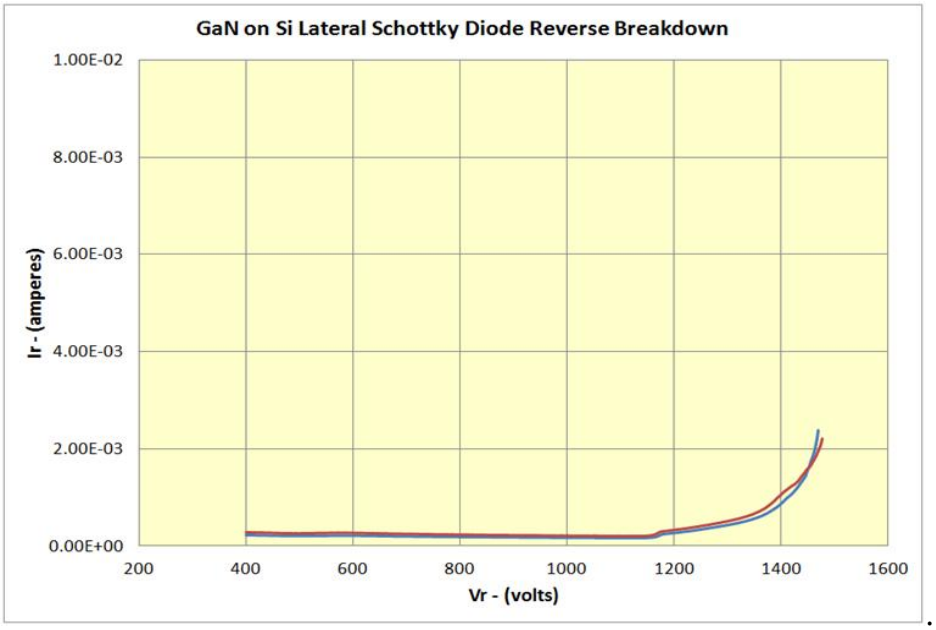


Figure 17 - Single Point reverse breakdown Measurements of GaN-on-Si Schottky Diode (MTS)

For even further increases in reverse breakdown voltage in the SB diodes, MIT Campus developed a selective area Si substrate removal/transfer processes (details to be described in the Transistor section below), in order to minimize parasitic leakage currents through the conductive Si substrate . By utilizing this substrate removal technique SB diode breakdown voltages >3000 V (equipment limited) were observed, as shown in Figure 18.

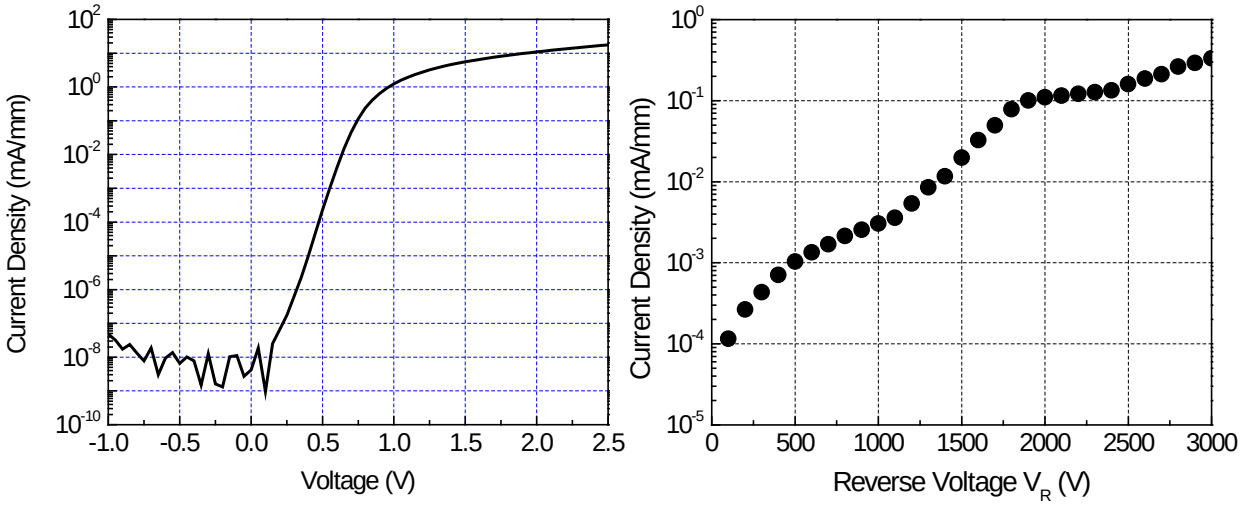


Figure 18- Forward and Reverse Characteristics for a Schottky diode with a spacing of 40µm (MIT)

While the substrate removal technique was shown to be effective at increasing breakdown voltage in SB diodes (and HEMTs as will be discussed below), there was on-going development of more standard device processing with more complicated dual- and triple-anode connected field plates at MTS for proper electric field control, as there was a concern expressed about the ease of manufacture and scale-up of the substrate removal process. As shown in Figure 19, excellent wafer-level results (breakdown voltages >2000V) were obtained from dual anode field plate SB diodes in prototype fabrication lots run through the standard fabrication facility at MTS. In addition, triple anode field plates designs were established (model results showed breakdown voltages > 3000V) although actual device measurements were not completed before the end of the GIGA program at MTS.

LOT	WAFER	SCRIBE	DEVICE	VR(V)	IR(uA)	TESTER
1813008	2	AK050000DW	12	>2000	<5	curve Tracer
1813008	2	AK050000DW	12	>2000	<5	curve Tracer
1813008	2	AK050000DW	12	>2000	<5	curve Tracer
1813008	2	AK050000DW	30	>2000	<5	curve Tracer
1813008	2	AK050000DW	30	>2000	<15	curve Tracer
1813008	2	AK050000DW	30	>2000	<5	curve Tracer
1813008	2	AK050000DW	42	>2000	<5	curve Tracer
1813008	2	AK050000DW	42	>2000	<5	curve Tracer
1813008	2	AK050000DW	42	>2000	<5	curve Tracer
1813008	4	AI051000DW	12	>2000	<5	curve Tracer
1813008	4	AI051000DW	12	>2000	<5	curve Tracer
1813008	4	AI051000DW	12	>2000	<5	curve Tracer
1813008	4	AI051000DW	30	>2000	<5	curve Tracer
1813008	4	AI051000DW	30	>2000	<5	curve Tracer
1813008	4	AI051000DW	30	>2000	<5	curve Tracer
1813008	4	AI051000DW	42	>2000	<5	curve Tracer
1813008	4	AI051000DW	42	>2000	<5	curve Tracer
1813008	4	AI051000DW	42	>2000	<5	curve Tracer

Figure 19 - On Wafer Manual Probe test Results from Dual Anode Connected Field Plate SB Diodes. (MTS)

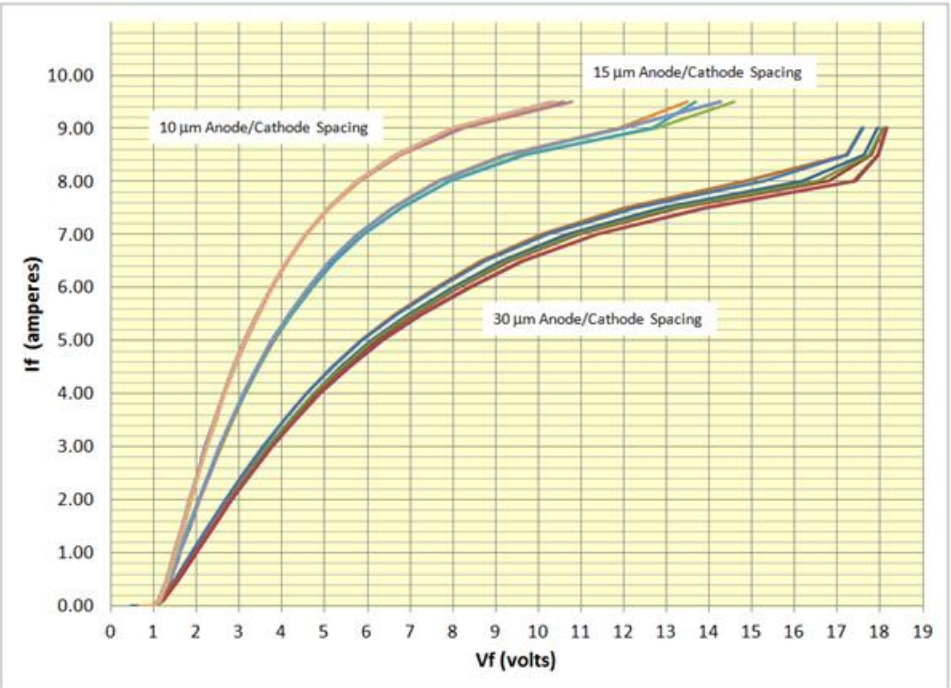


Figure 20 - Linear Plot of the Forward Characteristic of 20 Anode Lateral GaN on Silicon Schottky Diodes having a Total Anode Periphery of 20.0 mm and 10 µm to 30 µm Anode-to-Cathode Spacings

In addition to high breakdown voltages, high forward current handling capability of the SB diodes is also a key metric. Figure 20 shows a plot of the maximum forward current in anode connected field plate SB diodes measured by MTS on unpackaged devices. Not only is the forward current capability of ~10A remarkable, but the fact that these measurements were taken for devices not on a soldered heat sink is a good indication of the survivability and ruggedness of the GaN-on-Si materials and device technology.

4.3 Transistor Development

Much of the device development effort in the GIGA program focused on the demonstration of high-voltage 3-terminal lateral-geometry HEMT devices. While there was a lot of synergy with the parallel development of later SB diodes, the transistor fabrication and testing was more complex and required somewhat different technology development paths.

4.3.1 Comparison of Lateral vs. Vertical Transistors

An important part of the GIGA program was to explore the various trade-offs between high-voltage, high-current lateral and vertical transistor devices in GaN-on-Si materials. While lateral devices have advantages in relative ease of epitaxial growth and device fabrication of SB diodes and HEMT structures, vertical devices have been extensively utilized in other materials systems at the highest breakdown voltages and currents. To better understand these trade-offs, MIT conducted a theoretical study of the device physics and performance in each geometry. While initial calculations indicated a slight performance advantage in the vertical geometry, it was subsequently recognized that the key limiting factor is power dissipation/thermal management and this then gave the advantage to lateral devices, with the relatively thin epitaxial stack. One plot summarizing this is shown in Figure 21.

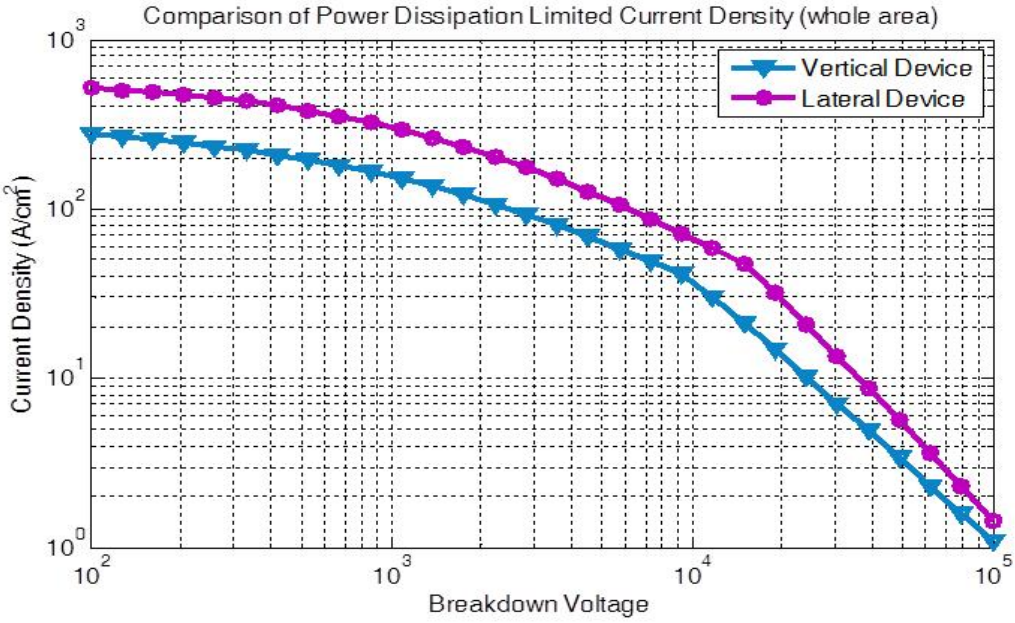


Figure 21 - Current Density with Breakdown Voltage after Considering the Power Dissipation (MIT)

4.3.2 High Voltage HEMTs

As discussed in the SB diode section above, an early investigation into substrate removal techniques at MIT showed encouraging results and greatly improved breakdown voltages. The substrate removal process shown in Figure 22, resulted in record HEMT performance of breakdown voltages > 1500V and a specific on resistance of 5.3 $m\Omega*cm^2$.

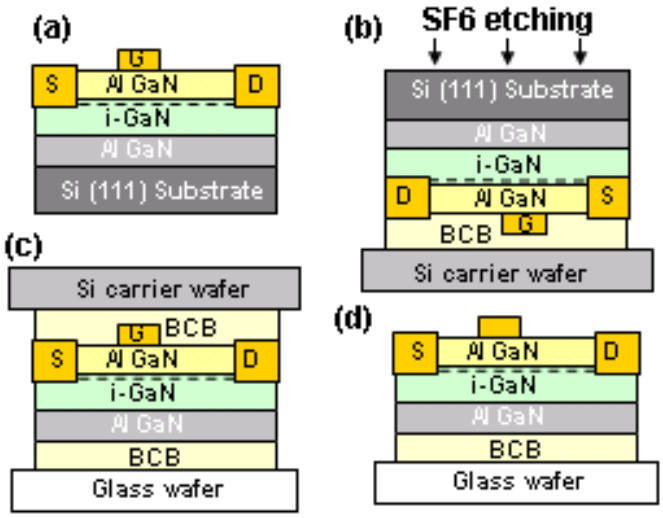
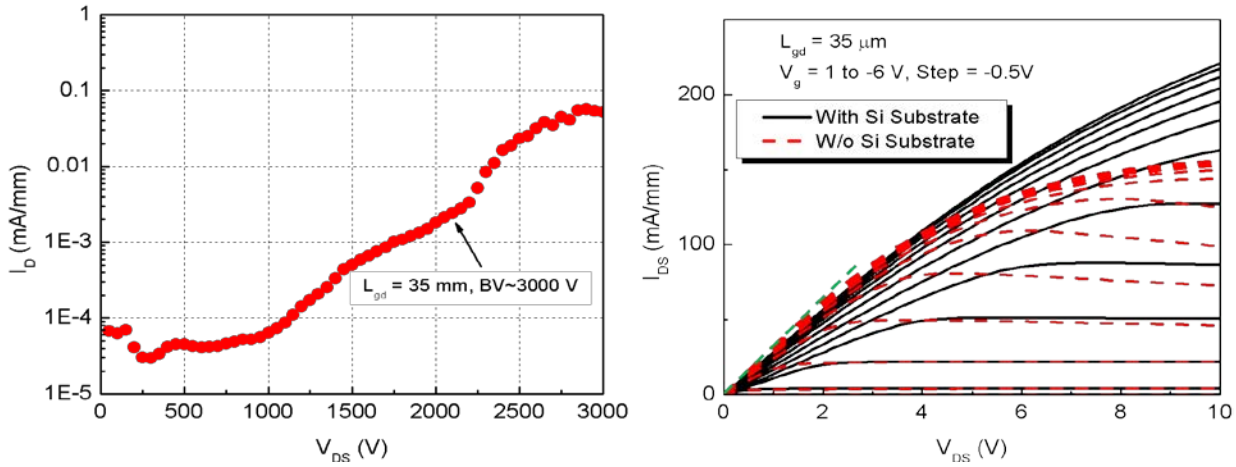


Figure 22 - Process flow of the substrate transfer technology. (a) Standard AlGaN/GaN HEMT on Si substrate; (b) bonding to a Si carrier wafer and Si (111) substrate removal; (c) GaN/AlGaN buffer bonded to a glass wafer; (d) Final device, after releasing the carrier wafer.

Very soon after this initial demonstration, MIT made improved GaN-on-Si HEMTs with breakdown voltages of ~1800V and specific on resistances of 2.4 $m\Omega*cm^2$. These tests required immersion in Fluorinert to avoid surface flashover in air since these devices didn't utilize adequate surface passivation. Later in the program (QPR 7), using GaN HEMTs grown on sapphire substrates by MIT/LL, MIT demonstrated ~2500V breakdown voltage was possible in such HEMTs. With further development of the selective Si substrate removal process, MIT was able to demonstrate ~3000V HEMT devices (QPR 9), as shown in Figure 23.



□□□ =□ □ □ □ after removing the substrate.

While the results from MIT with substrate removal technology were very encouraging, MTS continued to work on more conventional device fabrication processes that might be more readily scaled up to production quantities. In particular, MTS focused on the design and fabrication of multi-level field plates to properly control the high electrical fields that were present in high breakdown voltage devices.

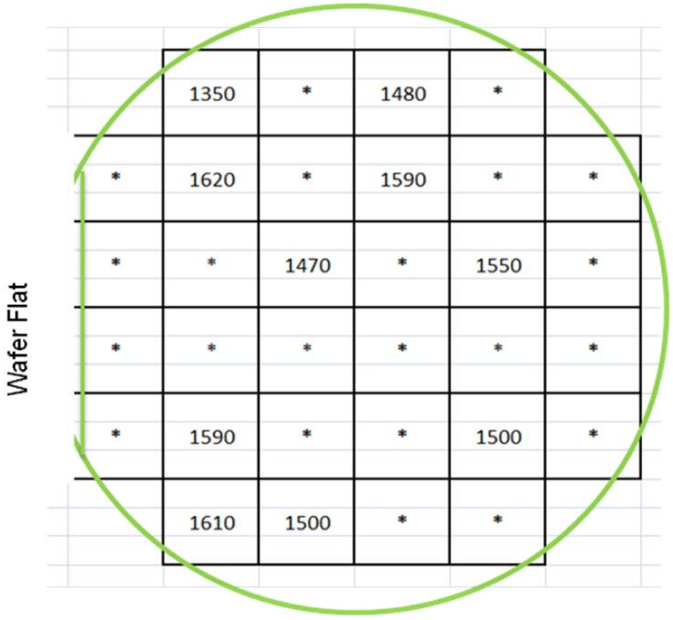


Figure 24 – Distribution Plot of V_{ds} for a 15 μm Gate-to-Drain Spacing, Free Standing, Trapezoidal Gate, GaN on Silicon HEMT

Initial prototype device results from MTS, for HEMTs even without advanced field plate structures was encouraging. Figure 24 shows a full 4-in wafer map of breakdown voltages for a trapezoidal gate HEMT design, with a measured peak breakdown voltage of ~1620V.

For further increasing the breakdown voltage in lateral HEMTs, MTS investigated more advanced field plate structures, both from models and experimental measurements. Figure 25 shows a conceptual cross section of a HEMT structure with multiple field plates.

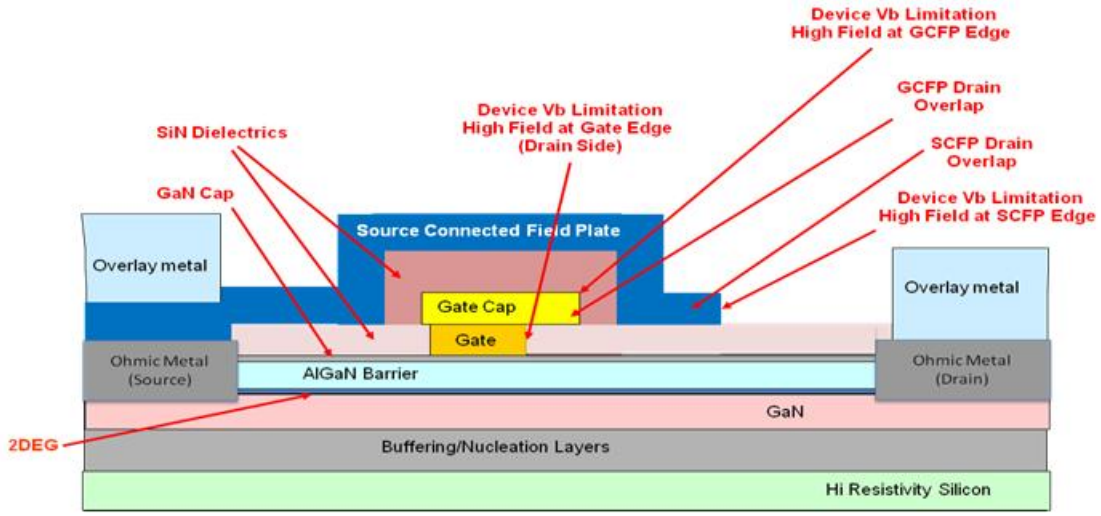


Figure 25 – Conceptual Cross section of HEMT Structure with Gate Connected and Source Connected Field Plates (MTS)

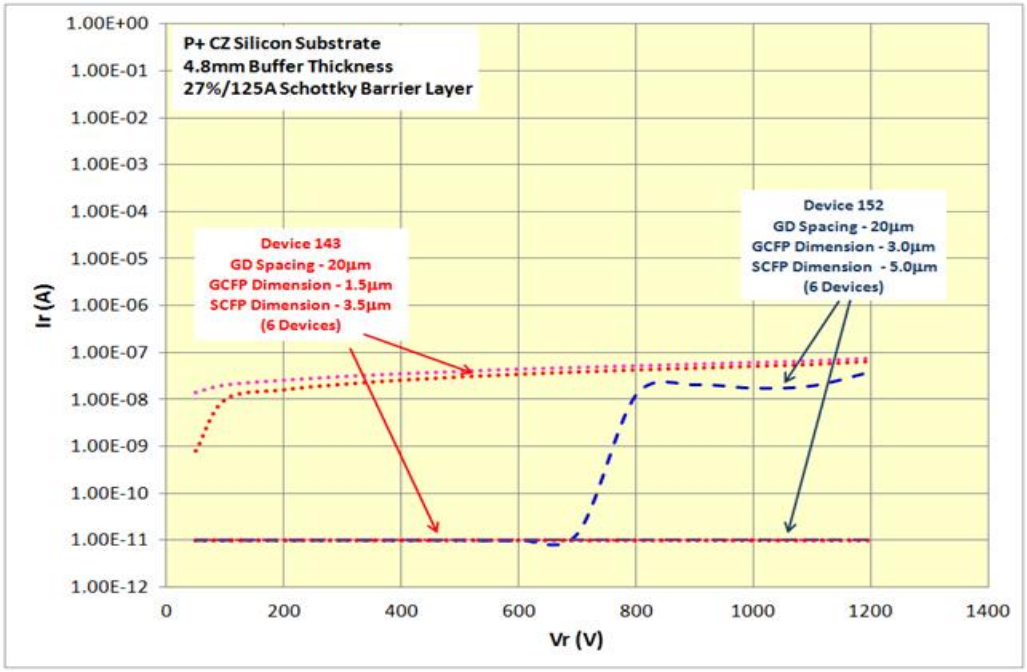


Figure 26 – Initial Reverse HEMT Leakage/Breakdown Test Results (MTS)

By utilizing more advanced field plate structure, MTS observed breakdown voltages in HEMTs of ~2000V. Another important attribute of the advanced field plate structures is the observation that the gate-to-drain leakage currents could be suppressed by 10,000X, as shown in Figure 26. In addition, as in the case for SB diodes, maximum current handling capability of HEMTs is an important consideration for grid applications. Figure 27 shows a photomicrograph of a multiple field plate HEMT device soldered into a standard RF power FET package (as there is a lack of a suitable DC power FET package at this time). Using this device a normalized maximum current of ~0.7 A/mm was observed (a >40% improvement over the unpackaged device) . If this device

were to be produced in a longer gate periphery of 30mm, >20A of current handling capability could be achieved.

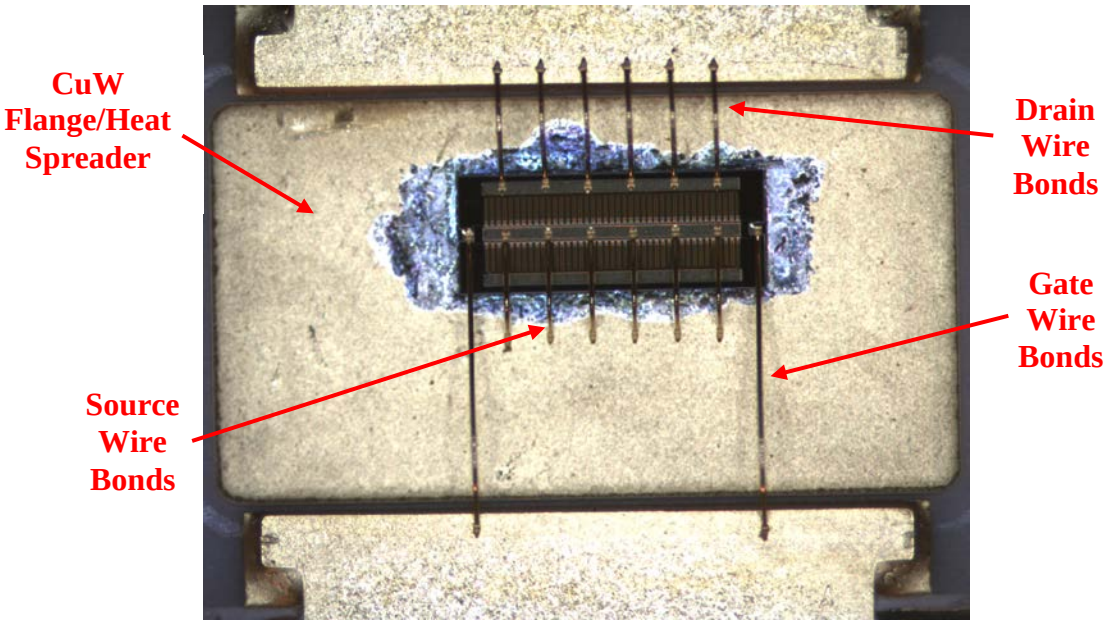


Figure 27 – Completed Assembly of the Multiple Field Plate HEMT Device Showing Die Attachment to the CuW Heat Spreader and the Wire Bonding Configuration. (MTS)

4.3.3 Advanced, Low-damage Etching

Most AlGaN HEMT structures (such as shown in Figure 2) employ a very thin (1-2nm) n-type GaN cap layer to facilitate the formation of Ohmic contacts to the device. A device with this surface GaN extending between contacts would be expected to exhibit significant leakage resulting from conduction across the doped cap. Additionally, this doped cap would result in a reduction in a transistor's gate Schottky barrier height that would reduce the gate diode turn-on voltage and increase gate leakage. In order to suppress these negative effects that might be expected through the addition of such a doped cap layer, a highly selective plasma etch was developed which allowed for complete removal of the n+ cap layer without etching into the AlGaN barrier. This particular etch was also optimized to cause minimal plasma damage, as the channel of GaN HEMT devices is sensitive to plasma damage on the top surface. An AFM scan of the test of this etch is shown below in Figure 28.

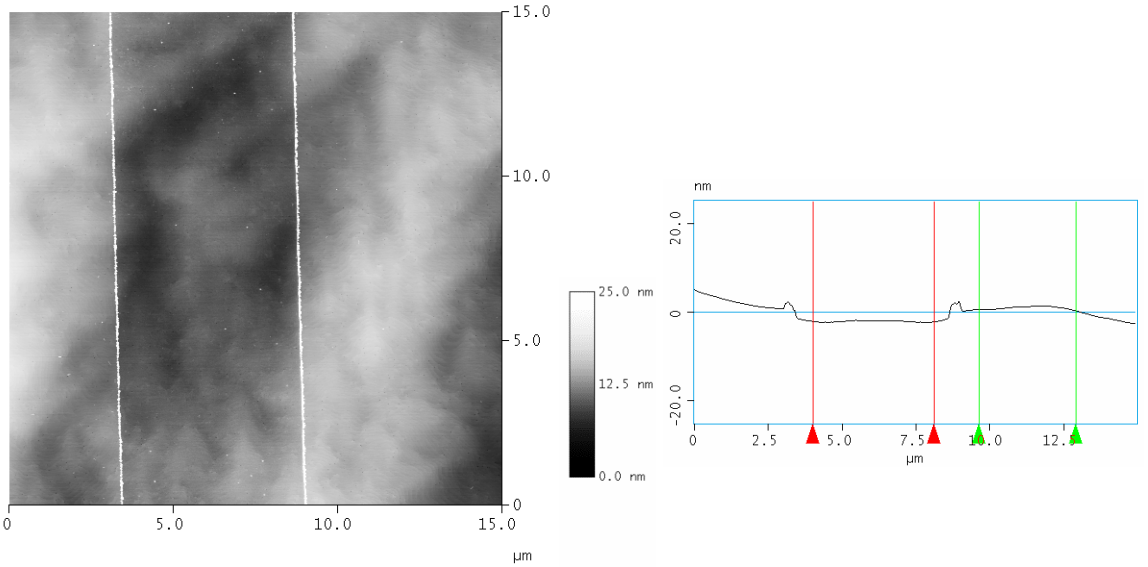


Figure 28 - AFM scan of etched region with cross-section to show step height (MIT/LL)

Subsequent transistor fabrication was performed on this modified n+ cap wafer, with comparisons to the standard HEMT epitaxial structure using both the standard process flow and the cap-removal process flow. These wafers were grown sequentially in the reactor, with the only change being the addition of n+ doping to the GaN cap layer. The three types of device samples used in this experiment are detailed below in **Table** .

Sample Name	**Standard**	**u-GaN Etched**	**n+ GaN Etched**
Cap Doping	UID	UID	n+
Process Flow	Standard	Cap Etch	Cap Etch

Table 2- Table of device samples tested

The incorporation of the n+ GaN cap layer resulted in an $I_{d,max}$ increase of approximately 8% when compared to the standard sample with the undoped cap. A plot of this comparison is shown below in Figure **Figure** 29, with gate voltages ranging from +2V to -4V in 1V steps.

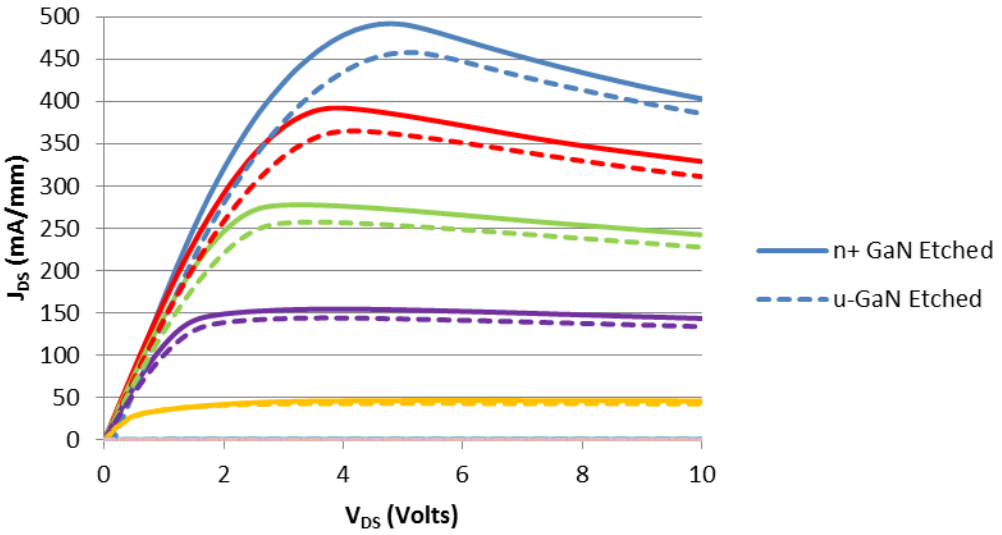


Figure 29 - Etched HEMT results comparing n+ cap (solid) and undoped cap (dashed) (MIT/LL)

Comparison between the cap etch process flow and the standard process flow on the undoped structure shows a decrease in both G_m and $I_{d,max}$ as shown below in Figure 30. This effect is expected to some degree and is most likely due to plasma damage caused by the cap etching process. The etching process should be minimized in order to reduce this effect on the channel.

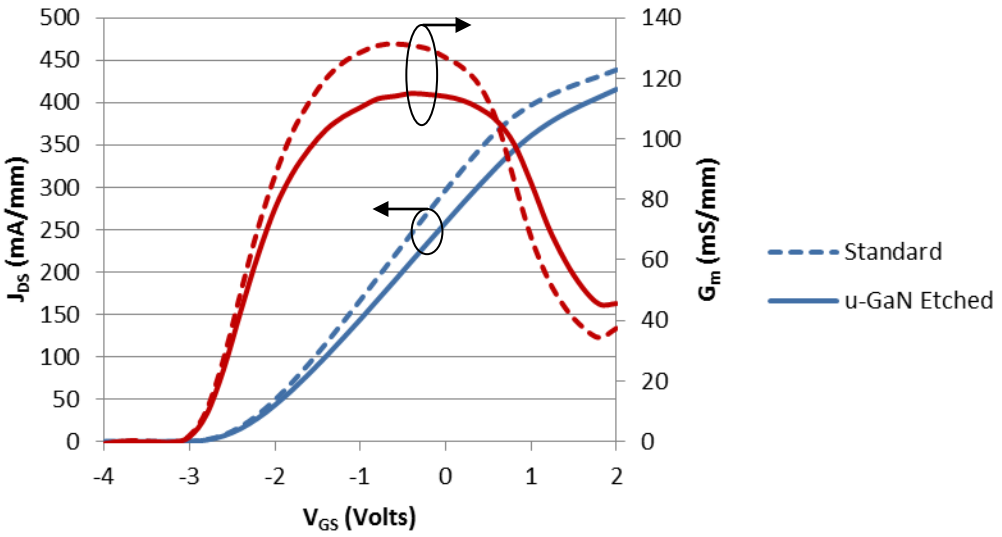


Figure 30- Gate comparison between u-GaN etched structures (solid) and control (dashed) (MIT/LL)

5. Program Reviews

In addition to numerous internal GIGA team meetings, conference calls, etc., there were a number of more formal GIGA program reviews and meeting conducted during the course of the program. At these review meetings, representatives from DoE, ARPA-E, DoE National Laboratories and other DoE contractors were usually present. The dates and locations of these formal reviews are summarized below:

	Location	Date
1	MIT Lincoln	8/18/2010
2	M/A Com Technology Solutions	10/26/2011
3	MIT campus	8/23/2012
4	IQE MA	5/20/2013
5	DoE Headquarters	3/27/2014
6	M/A Com Technology Solutions	11/18/2014

6. Milestone Status

The following table presents a high-level summary of the GIGA program milestones.

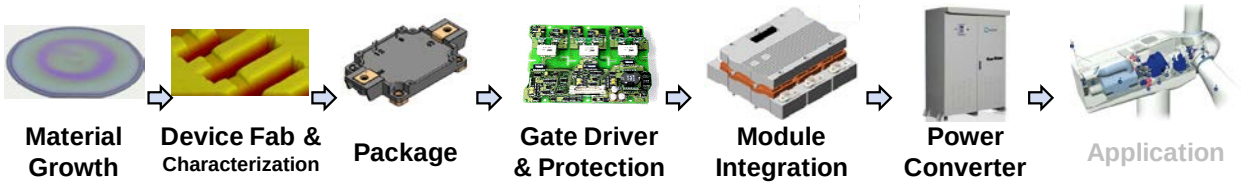
Device Type	Blocking Voltage (kV)	Current (A)	Frequency (kHz)	Milestone Schedule* (month: Q/ CY)	Milestone Schedule* (date)	
2-terminal,	1.5	2	-	3: Q1/2012	2-Apr-12	√
2-terminal,	3	>=2	-	9: Q3/2012	1-Oct-12	√
3-terminal,	2	>10	>5	12: Q4/2012	31-Dec-12	√
2-terminal,	3	>=5	-	18: Q2/2013	1-Apr-13	√
3-terminal,	5	>=15	>5	24: Q4/2013	31-Dec-13	√
2-terminal,	5	>= 10	-	27: Q1/2014	31-Mar-14	√
3-terminal,	7.5	5	>5	30: Q2/2014	30-Jun-14	
2-terminal,	>7.5	>=15	-	36: Q4/2014	31-Dec-14	
3-terminal,	>7.5	>=15	>5	36: Q4/2014	31-Dec-14	
				* assuming 1 Jan 2012 start		

The shaded region (30 Jun 14 and beyond) indicates activities beyond the effective end date of the program, since the major R&D subcontracts were not renewed due to the lack of any additional funding since FY12 (even though IQE MA was added as an additional major GIGA team member in FY13). This premature program termination (before the projected end of the period-of-performance) resulted in the abandonment of any work toward higher voltage devices

(7.5 kV and beyond). In addition the last two 5 kV device milestones were partially met as the combination of high voltage operation at high current was hindered by the ability of the team to effective package these devices. However, independently, high voltage operation and high current operation were achieved with similar device structures.

7. Proposed Follow-on Efforts

As described in previous reports and program reviews, the GIGA program reached important milestones and enabled the completion of most of the efforts involved in the first 2 steps in the 6-step development process (shown below) needed to insert GaN-on-Si technology into high-power applications such as the grid. It was clear toward the end of the program that the next sequential step required – packaging – was the key to further advancing the more widespread testing and ultimate adoption of this technology for grid applications (at least at the 5 kV operating voltages), but additional resources were required to address this task. In addition, toward the end of the program, the GIGA team produced a "notional" datasheet (Appendix II) of a 5kV, 50A module that has attracted a significant amount of interest from outside system integrators.



With this strategy in mind, the GIGA team proposed a 2-year follow-on effort, to leverage the core technology development already funded by the DoE. This proposed follow-on effort would be comprised of the following high-level tasks:

- Task 1: Develop manufacturing technology for 5kV/50A switches
- Task 2: Develop materials technology to support device production
- Task 3: Develop high voltage/ high current packaging as an industry standard
- Task 4: System demonstrations

Appendix I . Publications

[1] B. Lu, E. L. Piner, and T. Palacios, “Breakdown mechanism in AlGaN/GaN HEMTs on Si substrate,” Proc. Of the 68th Device Research Conference, Notre Dame, IN, June 21-23, 2010.

[2] Timothy Boles, Costas Varmazis, Douglas Carlson, Tomas Palacios, “Effect of Isolation Techniques on GaN on Silicon Breakdown Voltage”, International Workshop on Nitrides, September, 2010

[3] B. Lu, E. L. Piner, and T. Palacios, “High Performance Dual-Gate AlGaN/GaN Enhancement-Mode Transistor,” Proc. Of the International Symposium on Compound Semiconductors (ISCS-2010), Takamatsu, Japan, May 31st-June 4th, 2010.

[4] B. Lu and T. Palacios, “High Performance Dual-Gate AlGaN/GaN Enhancement-Mode Transistor”, IEEE Elec. Dev. Lett., vol. 31, no. 9, p. 990, September 2010.

[5] B. Lu and T. Palacios, “High Breakdown (>1500 V) AlGaN/GaN HEMTs by Substrate Transfer Technology”, IEEE Elec. Dev. Lett., vol. 31, no. 9, p. 951, September 2010

[6] Lu, B., E. L. Piner, and T. Palacios, “Schottky Drain Technology for High Voltage AlGaN/GaN HEMTs on Si Substrates,” IEEE Electron Dev. Letts., vol. 31, 302-304, 2010.

[7] B. Lu, D. Piedra, and T. Palacios, "GaN power electronics," in 18th International Conference on Advanced Semiconductor Devices and Microsystems, ASDAM 2010, October 25, 2010 - October 27, 2010, Smolenice, Slovakia, 2010, pp. 105-110.

[8] M. Sun, H.S. Lee, B. Lu, D. Piedra, E. Matioli, and T. Palacios, “1.8kV-breakdown AlGaN/GaN HEMT on Si substrate with Ron=2.4mΩcm2”, in the 9th International Conference on Nitride Semiconductors (ICNS-9), July, 2011, Glasgow, UK, 2011.

[9] H.-S. Lee, D. Lee, and T. Palacios, “AlGaN/GaN High-Electron-Mobility Transistors Fabricated Through a Au-free Technology,” IEEE Electron Device Letters, v 32, 623-625, May 2011

[10] M. Sun, H.S. Lee, B. Lu, D. Piedra, and T. Palacios, “1.8 kV-Breakdown AlGaN/GaN HEMT on Si Substrate with Ion Implantation Isolation”, submitted to IEEE Electron Device Letters.

[11] D. Piedra, T. G. Desai, R. Bonner, J. Pascaul-Guiterrez, M. Sun, and T. Palacios, “Integration of a Phase Change Material for Junction Level Cooling in GaN Devices”, submitted to the 28th Annual Thermal Measurement, Modeling and Management Symposium (SEMI-THERM 28), 2012.

[12] H. S. Lee, D. Piedra, M. Sun, X. Gao, S. P. Guo, T. Palacios, "3000 V 4.3 Ωcm2 InAlN/GaN MOSHEMTs with AlGaN Back Barrier," *IEEE Electron Dev. Letts.*, vol. 33, pp. 982-984, 2012.

[13] S. Atcitty, R. Kaplar, S. Das Gupta, M. Marinella, A. Armstrong, L. Biederman, M. Sun, T. Palacios, and M. Smith, "GaN-Based Wide-Bandgap Power Switching Devices: From Atoms to the Grid" ECS Transactions, 50, (3) , 2012

[14] D. Piedra, T. G. Desai, R. Bonner, J. Pascaul-Guiterrez, M. Sun, and T. Palacios, "Integration of a Phase Change Material for Junction Level Cooling in GaN Devices", to be published in the 28th Annual Thermal Measurement, Modeling and Management Symposium (SEMI-THERM 28)

[15] T. Boles, C. Varmazis, D. Carlson, T. Palacios, G. Turner, and R. Molnar, "High Voltage GaN on Silicon HEMT", accepted as a poster presentation at ISCS 2012.

[16] T. Boles, C. Varmazis, D. Carlson, T. Palacios, G. Turner, and R. Molnar,">1200 volt GaN on Silicon Schottky Diode", accepted as an oral presentation at ISCS 2012..

[17] B. Lu, E. Matioli and T. Palacios, "Tri-gate Normally-Off Power MISHEMT," IEEE Electron Dev. Letts., vol. 33, 360-362, 2012.

[18] H.-S. Lee, D. Piedra, M. Sun, X. Gao, S. Guo, T. Palacios, "3000-V 4.3-mΩ•cm2 InAlN/GaN MOSHEMTs With AlGaN Back Barrier," IEEE Electron Device Letters, v 33, 982-984, July 2012.

[19] M. Sun, H.S. Lee, B. Lu, D. Piedra, and T. Palacios, "Comparative breakdown study of mesa- and ion-implantation-isolated AlGaN/GaN high-electron-mobility transistors on Si substrate", Appl. Phys. Express, vol.7, 074202, 2012.

[20] S. Atcitty, R. Kaplar, S. Das Gupta, M. Marinella, A. Armstrong, L. Biederman, M. Sun, T. Palacios, and M. Smith, "GaN-Based Wide-Bandgap Power Switching Devices: From Atoms to the Grid" ECS Transactions, 50, (3) , 2012

[21] T. Boles, C. Varmazis, D. Carlson, T. Palacios, G. W. Turner, R. J. Molnar, ">1200 volt GaN-on-Silicon Schottky Diode", International Symposium on Compound Semiconductors 2012, August, 2012

[22] T. Boles, C. Varmazis, D. Carlson, T. Palacios, G. W. Turner, R. J. Molnar, "High Voltage GaN-on-Silicon HEMT", International Symposium on Compound Semiconductors 2012, August, 2012

[23] T. Boles, C. Varmazis, D. Carlson, T. Palacios, G. W. Turner, R.J. Molnar, "High Voltage GaN-on-Silicon HEMT, Physica Status Solidi, January, 2013

[24] T. Boles, C. Varmazis, D. Carlson, T. Palacios, G. W. Turner, R.J. Molnar, "GaN-on-Silicon High Voltage Schottky Diode", Physica Status Solidi, April, 2013

[25] T. Boles, D. Carlson, T. Palacios, M. Soboroff, “Cost Effective, High Performance GaN Technology”, Compound Semiconductor Magazine, April, 2013

[26] T. Boles, C. Varmazis, D. Carlson, T. Palacios, G. W. Turner, R.J. Molnar, “GaN-on-Silicon High Voltage Schottky Diode”, Physica Status Solidi, April, 2013

[27] T. Boles, C. Varmazis, D. Carlson, L. Xia, D. Jin, T. Palacios, G. W. Turner, R. J. Molnar, “High-Voltage GaN-on-Silicon Schottky Diodes”, CSMANTECH, May, 2013

[28] T. Boles, C. Varmazis, D. Carlson, L. Xia, D. Jin, T. Palacios, G. W. Turner, R. J. Molnar, “High Voltage GaN-on-Silicon HEMT’s”, CSMANTECH, May, 2013

[29] Y. Zhang, M. Sun, T. Fujishima, Z. Liu, K. Bagnall, D. Piedra, E. Wang, and T. Palacios, “Electro-thermal Modeling and Thermal Performance Study of GaN Vertical and Lateral Power Transistors,” IEEE Trans. Electron Dev., vol. 63, 2224-2230, July 2013

[30]S. DasGupta, R.J. Kaplar, M. Sun, M.J. Marinella, S. Atcitty, and T. Palacios “Effect of Interaction of Deep Level Defects with Quantum Well States on Detrapping Transients in High-Voltage AlGaN/GaN HEMTs” Abstract #1943 224th ECS Meeting , 2013.

[31] T. Boles, D. Carlson, L. Xia, A. Kaleta, C. McLean, D. Jin, T. Palacios, G. W. Turner and R. J. Molnar, “Effect of Multi-Field Plates on GaN-on-Silicon HEMTs “,CSMANTECH 2014.

Appendix II . Notional Datasheet

GaN5KV200A

GaN HEMT Notional Data Sheet

Gallium Nitride on Silicon Lateral Transistor V_{CES} = 5000V, I_{Fmax} = 200A, I_{Fav}=50A

Features:

- 5000V GaN High Mobility Electron Transistor, Normally off,
- Included anti-parallel high speed GaN diode
- High speed switching, self commutating, fast turn off and on
- 150 ° C operating temperature
- Robust packaging options: Single Switch Presspack, or Dual Switch Half Bridge Module
- Multichip packaging with internal parallel connections
- High isolation voltage
- Lowest in-class switching energy

Applications:

- Utility medium voltage solid state transformers
- Series connected utility DC-AC link converters
- Medical MIR gradient amplifiers
- Pulsed energy applications
- Electromagnetic launchers

Maximum ratings

Parameter	Symbol	Conditions	Values	Unit
Repetitive peak forward voltage	V_{CES}	Tj=25C, Vg=0	5000	V
Maximum peak drain current	I_{CM}	Tj=150C, pulse	200	A
DC drain current	I_{CD}	Tj=150C, RMS or DC	50	A
Diode forward current surge	I_{FM}	Tj=150C, pulse	200	A
Diode forward current	I_F	Tj=150C, RMS or DC	50	A
I^2t for diode	I^2t	T=10 ms	100	A
Gate- source voltage	V_{GES}	V_{CE}=0	+-20	V
Isolation voltage	V_{iso}	Dual pack to plate	9000	VAC 60hz
Junction temperature	T_j	operating	-40 to 150	° C
Storage temperature	T_{stg}	storage	-40 to 150	° C
Maximum collector dissipation	P_c	Tc=25C, Tj<150C	1000	W

Electrical Characteristics, T_J=25°C unless otherwise specified:

Characteristics	Symbol	Test conditions	Min	Typ	Max	Unit
Drain cutoff current	I_{CES}	V_{GE}=0, V_{CE}=V_{CES}	-	-	5	mA
Gate leakage current	I_{GES}	V_{GE}=V_{GES}, V_{CE}=0	-	-	0.5	uA
Gate-Source threshold V	$V_{GE(th)}$	I_C=10mA, V_{CE}=10V	4.0	5.0	7.0	V

D-S Saturation V	$V_{CE(sat)}$	$I_C=I_{CD}$, V_{GE}=15V	-	3.5	4.0	V
Input Capacitance	C_{ies}	V_{GE}=0, V_{CE}=10V	-	20	-	pF
Output Capacitance	C_{oes}	V_{GE}=0	-	300	-	pF
Reverse transfer capacitance	C_{res}	V_{GE}=0	-	100	-	pF
Inductive turn on delay	$T_{d(on)}$	V_{CC}=2500V,	-	-	100	nS
Inductive rise time	T_r	$I_C=I_{CD}$,	-	-	30	nS
Inductive turn off delay	$T_{d(off)}$	V_{GE}=0-15V,	-	-	100	nS
Inductive fall time	T_f	R_G=30Ω,	-	-	30	nS
Turn on energy	E_{on}	L_s=200nH,	-	1875	-	uJ/P
Turn off energy	E_{off}	Inductive load	-	2000	-	uJ/P
Diode reverse recovery t	t_{rr}		-	-	100	nS
Diode reverse recovery Q	Q_{rr}		-	1000	-	nC
Diode reverse recovery E	E_{rr}		-	2500	-	uJ/P
Recommended switching f	f_{SW}	Hard switching	-	50	-	kHz
Stray inductance (D1-S2)	L_{SCE}	terminal-chip	-	60	-	nH
Lead resistance	R_{CE}	terminal-chip	-	0.8	-	m Ω

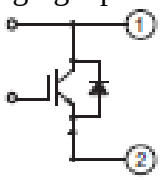
Thermal and Mechanical Characteristics, T_J=25°C unless specified

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Thermal resistance	$R_{th(J-C)}Q$	Per HEMT(4)	-	-	0.2	° C/W
Thermal resistance	$R_{th(J-C)}D$	PerDiode(4)	-	-	0.4	° C/W
Contact resistance, case to sink	$R_{th(C-HS)}$	Per module, thermal grease applied	-	0.020		° C/W
Clearance distance in air	$d_{a(t-b)}$	Terminal to base	35	-	-	mm
Clearance distance along surface	$d_{s(t-b)}$	Terminal to base	64	-	-	mm
Clearance distance in air	$d_{a(t-t)}$	Terminal to terminal	19	-	-	mm
Clearance distance along surface	$d_{s(t-t)}$	Terminal to terminal	54	-	-	mm
Comparative tracking index	CTI		600	-	-	

***Tc measurement point is just under the chips

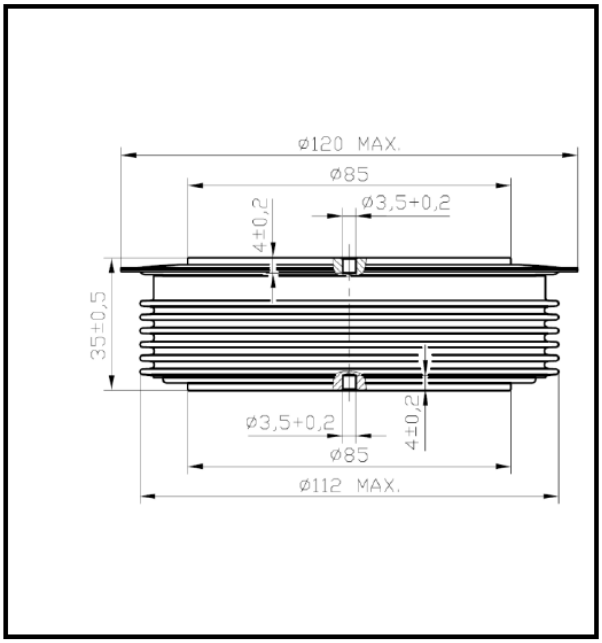
Packaging Option A: Presspack, Dual sided cooling, Creepage and Clearance meet IEC 60077-1

③

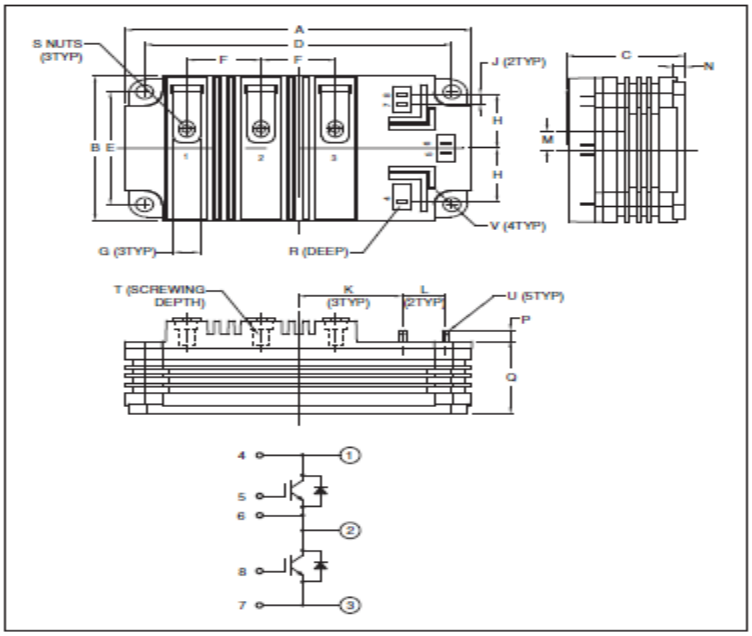


Mechanical Data

F_m	Mounting force	70 ± 7	kN
m	Weight	2.0	kg
D_S	Surface creepage distance	56	mm
D_a	Air strike distance	28	mm



Packaging Option B: Dual HV Module, Isolated Base, Creepage and Clearance meet IEC 60077-1



Outline Drawing and Circuit Diagram

Dimensions	Inches	Millimeters
A	5.51	140.0
B	2.87	73.0
C	1.89	48.0
D	4.88±0.01	124.0±0.25
E	2.24±0.01	57.0±0.25
F	1.18	30.0
G	0.43	11.0
H	1.07	27.15
J	0.20	5.0
K	1.65	42.0

Dimensions	Inches	Millimeters
L	0.69±0.01	17.5±0.25
M	0.38	9.75
N	0.20	5.0
P	0.22	5.5
Q	1.44	36.5
R	0.16	4.0
S	M6 Metric	M6
T	0.63 Min.	16.0 Min.
U	0.11 x 0.02	2.8 x 0.5
V	0.28 Dia.	7.0 Dia.