An Integrated Gate Driver in 4H-SiC for Power Converter Applications

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***Abstract*—A gate driver fabricated in a 2-µm 4H silicon carbide (SiC) process is presented. This process was optimized for vertical power MOSFET fabrication but accommodated integration of a few low-voltage device types including N-channel MOSFETs, resistors, and capacitors. The gate driver topology employed incorporates an input level translator, variable power connections, and separate power supply connectivity allowing selection of the output signal drive amplitude. The output stage utilizes a source follower pull-up device that is both overdriven and body source connected to improve rise time behavior. Full characterization of this design driving a SiC power MOSFET is presented including rise and fall times, propagation delays, and power consumption. All parameters were measured to elevated temperatures exceeding 300˚C. Details of the custom test system hardware and software utilized for gate driver testing are also provided.**

Keywords—Gate Driver, SiC, Silicon Carbide, Wide Bandgap, Power Electronics

I. INTRODUCTION

The recent commercialization of wide bandgap (WBG) power devices fabricated in silicon carbide (SiC) and Gallium Nitride (GaN) has provided new opportunities for electronic applications to operate at higher frequencies, voltages, and temperatures exceeding the inherent capabilities of silicon. When integrated into power conversion modules and traction drives, these WBG-based devices provide the potential for higher efficiency operation, lower system mass and size, and higher power density over silicon-based circuits due to the inherent properties of the WBG materials [1]. Industry is now commercializing limited WBG devices, namely power switches and diodes. However, recent literature has reported on the ability to fabricate WBG support electronics, including gate drivers and other low-voltage monitoring circuits in SiC, establishing the benefits of higher degrees of WBG electronics systems integration [2,3]. This work presents the furthering of these efforts by producing a second generation gate driver based on a previously published design [4].

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II. SIC INTEGRATED GATE DRIVER

A. Gate Driver Design

The gate driver topology described in this paper is shown in Figure 1. Improvements of this design over a previously published version include the addition of an input level translator, multiple power connectivity options, a substrate isolated output pull-up device, and general device resizing to improve the gate driver performance for moderate levels of gate overdrive. Referring to Fig. 1, the input level translator is composed of 4 inverters (X_1-X_4) each having a source follower output stage which ensures that the output feeding the following stage has a sufficiently low logic level to correctly drive following stages. One risk with having multiple cascaded, resistor-transistor-logic (RTL) – based inverter stages is that the pull-up resistor value and associated pull-down device must be sized appropriately to minimize the associated RC-controlled rise time while ensuring a suitable logic '0' is obtained at each inverter output. Failure to reach this condition satisfactorily may result in inverter output logic low levels moving closer to undefined levels as signals propagate resulting in the eventual inability to produce valid logic levels late in the inverter or logic chain. Use of this inverter topology mitigated this risk at the cost of reduced logic '1' output levels. Note that high output levels are limited to VDD – V_{GS} for a source follower output stage. Buffer stages X_5 and X_6 were built as RTL inverters and provide the gain necessary to translate the logic '1' output to full positive rail values. Connectivity options to VDD-OD provide the means to 'program' the amount of current available for charging the capacitive gate of the output stage pull-up device (M_{PU}). These

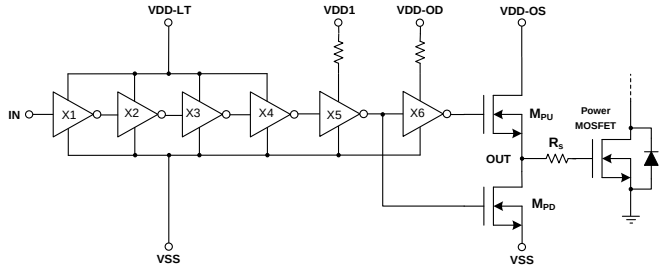

Fig. 1. Simplified gate driver architecture and connection to power MOSFET.

connections are best optimized during testing and are made at the packaging level. The combination of connections allows the selection of pull-up resistor values ranging from 94 Ω – 210 Ω.

The process used for fabricating the design utilized a p-substrate and did not have an n-well option. This prevented the output pull-up device (M_{PU}) from having a source-body connection, resulting in a significant increase in rise time due to the body effect. To mitigate this undesired effect, the M_{PU} device was fabricated as a second die and packaged such that the isolated substrate could be source connected to minimize the body effect.

The final significant design change from the original gate driver involved complete resizing of the circuit to maximize the dynamic performance (limited by the output rise time) at low to moderate levels of gate overdrive (VDD-OD). The target overdrive level was selected as 32V rather than the 40-V overdrive used in the initial design, as lower overdrive levels provide improved reliability, and HSPICE simulations indicated 32V was sufficient.. To resize the design for improved performance, the circuit was first simulated with the expected output device capacitance (power MOSFET gate model) and the upper and lower output device sizes were determined for the case where ideal output stage drive sources were used. The sizing of the lower and upper output stage drive inverters, X_5 and X_6 respectively, were estimated by calculating the associated RC time constant desired, determining the associated pull-up resistor R, and then solving for the size of the pull-down device. This ratio of pull-up resistor to pull-down MOSFET size was set to produce a 'low' voltage output level of <1V. Note that with CMOS design the ratio of N-type to P-type device width/length is generally approximated by the ratio of the device's transconductance parameters (KP) provided in the SPICE model. The KP of a device is commonly defined as $\mu_0 C_{ox}$, where μ_0 is the carrier mobility and C_{ox} is the oxide capacitance per unit area which often produces a ratio of ~2.5 for standard CMOS processes. However, this design does not have PMOS devices, so the alternate pull-up resistor to pull-down MOSFET W/L ratio was calculated and then validated via HSPICE simulation using a custom model generated specifically for use with the devices available in this process [5].

B. Layout Considerations

The SiC process used for fabrication of the design was a P-Epi, 2-µm, single metal, NMOS-only process, optimized for fabrication of vertical SiC powerMOS switching devices. Having only one metal layer for signal and power routing required the occasional use of polysilicon as a routing layer. Efforts were made to only use polysilicon routing for traces having very low current requirements. A goal of limiting current densities to ≤ 1mA/µm^2 for all conductive traces was followed during layout. In addition, diffusion resistors were used rather than polysilicon resistors to improve thermal coupling to the SiC substrate, and resistors were separated where possible to minimize concentrated areas of heating. Following layout and extraction, the circuit was simulated using HSPICE.

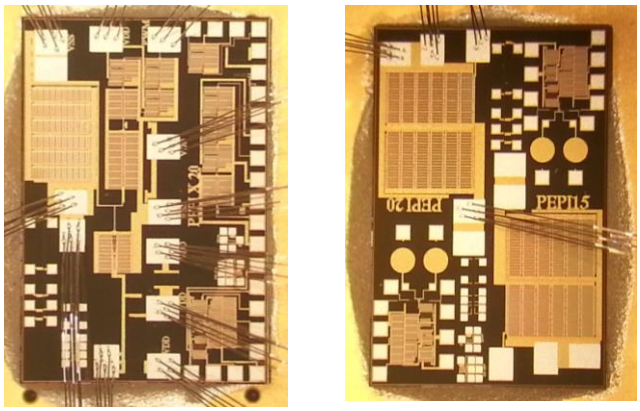

Fig. 2. SiC gate driver die (left) and separately fabricated pull-up device die (right).

III. EXPERIMENTAL RESULTS

A. Gate Driver Test System

The gate driver was fabricated as a chip set along with a number of other test cells and circuits. The chip set (gate driver die and pull-up device die) are shown in Fig. 2. A test setup was also designed to facilitate the evaluation and characterization of the SiC gate buffer. The die were bonded to a daughterboard carrier PCB (Fig. 3) which was mounted on a motherboard having the SiC powerMOS load device, supply filtering, input control signal isolation, and power supply connections. A mechanical stand was designed and constructed to fixture the motherboard and provide temperature control of a cold finger that thermally contacted the backside of the daughterboard. The opposite side of the cold finger was heated using a commercial hotplate and a thermocouple was placed between the daughterboard and the cold finger for monitoring the temperature. Initially, an IR imaging camera was used to determine the temperature difference between the thermocouple and the gate driver chip as a function of the gate driver power consumption. These tests indicated that the gate driver die temperature was approximately equal to the measured thermocouple temperature plus 7.7˚C/Watt of gate driver power consumption. A custom LabVIEW-based software program was developed to enable automated testing of gate driver units. The program included the capability to

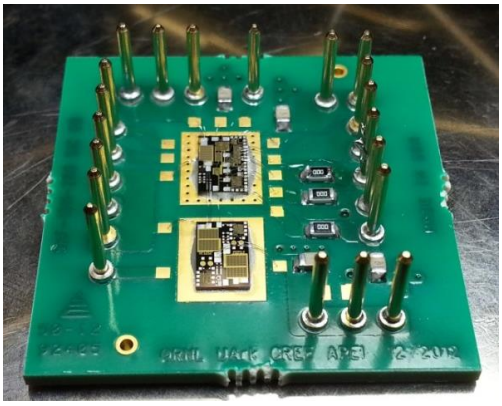

Fig. 3. Daughterboard with bonded SiC gate driver die set for testing.

perform voltage sweeps as well as data collection, display, and storage.

B. *Measurement Results*

Following fabrication of the SiC gate driver die, 27 gate buffer modules were assembled using the daughterboard PCBs as shown in Fig. 3, and were tested using the developed test system. Initial tests were performed at room temperature to verify basic functionality and to investigate the effect of using different supply voltage configurations. These tests showed that increasing VDD-LT beyond 20V had no significant effect on the overall dynamic performance of the gate driver except that larger supply voltages tended to increase the delay through the unit. Similarly, increasing VDD1 beyond the nominal 20V level did not significantly improve the output fall time, which was within expectations. The output voltage drive level (VDD-OS) was not a significant factor in performance optimization as the voltage is fixed by the drive requirements for the switching device used. However, increasing VDD-OS does increase the measured rise time since there is a slew limit imposed on the output drive signal due to limited source and sink currents in the output stage.

Tests were performed on all 27 of the assembled gate buffer modules to determine the approximate yield and room temperature performance. For these tests the rise time, fall time, delays, and power consumption were measured for VDD-OD swept from 20V-40V, with all power supply voltages at 20V, and with a single powerMOS load. These tests indicated an approximate yield of 70% for the gate driver die pair.

The measured rise and fall times are plotted for 10 SiC gate driver units as a function of VDD-OD (see Fig. 4). As expected, the VDD-OD had a very significant impact on the rise time of the gate driver output as the affected buffer stage directly drives the source follower output stage pull-up device (M_{PU}). However, the measured fall times are inversely proportional to the value of VDD-OD. This behavior is due to a voltage division between the pull-up resistor tied to VDD-OD and the X_6 output NMOS on-resistance which acts to keep M_{PU} slightly on during M_{PD} pull-down. Thus, a matching rise and fall time of ~50ns can be observed for VDD-OD ~30V-31V.

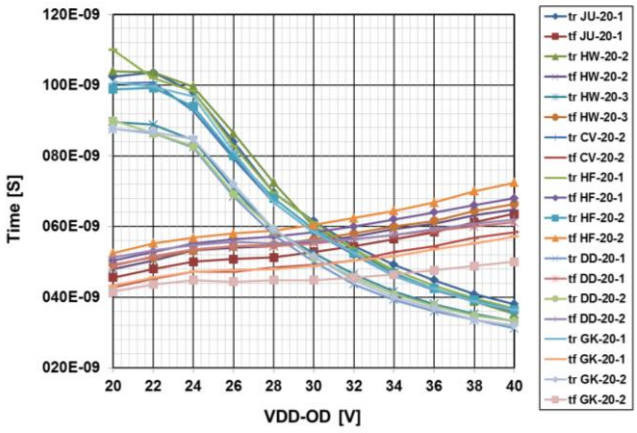

Fig. 4. Measured rise and fall times vs. VDD-OD for 10 SiC gate driver units (other supply voltages = 20V, single powerMOS load).

Subsequent tests were performed on two of the units over a die temperature range of approximately 90˚C to 340˚C. The rise times, fall times, propagation delays, and power dissipations were measured for each of the test conditions. This data is plotted in Figures 5-9. In these figures each of the curves represents the measured parameter (rise time, fall time, delay1, delay2, power) at a different VDD-OD value, plotted as a function of the calculated die temperature. Note that the first data point of each curve is the die temperature with the hot plate at room temperature. Here the die temperature is well above room temperature due to self-heating of the die. Consequently, for matched rise and fall times of ~45ns, VDD-OD=31V is the preferred case. Under this condition the rise time and fall time variation over the measured temperature range was 6.3% and 2.7%, respectively. The propagation delays of Figures 7 and 8 are very similar for all VDD-OD values, and match well over the temperature range tested. Both show a similar temperature dependence with a ~22% variation over the measured temperature range. The measured power consumption is shown in Fig. 9 and varied from 8.2W - 6.8W over the temperature range tested for VDD-OD=31V. The power

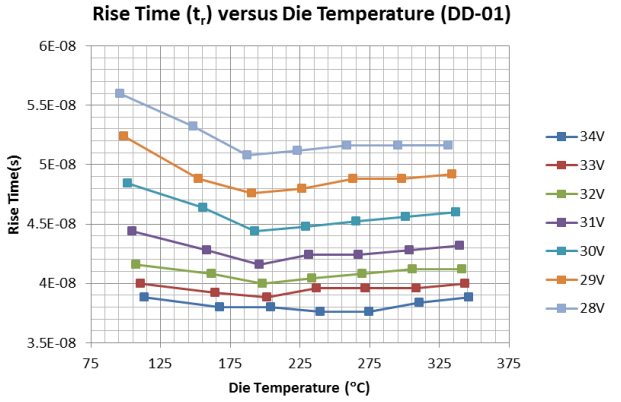

Fig. 5. Measured rise time over temperature (VDD-OD = 28V-34V, other supplies voltages = 20V, single powerMOS load).

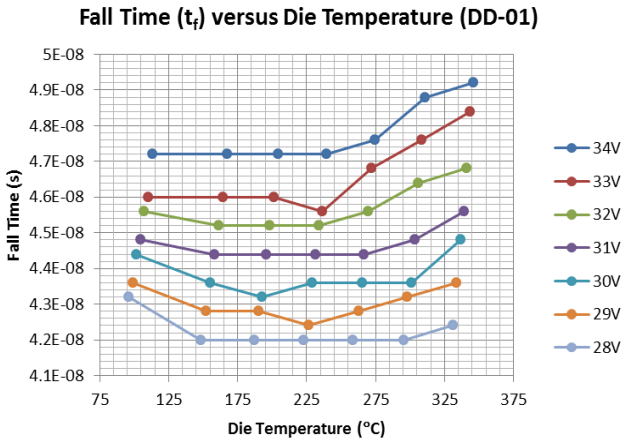

Fig. 6. Measured fall time over temperature (VDD-OD = 28V-34V, other supplies voltages = 20V, single powerMOS load).

decrease with temperature is due to the positive temperature coefficient of the n-diffusion resistors used in the design. This data shows that the gate buffer operates very well over the temperature range tested.

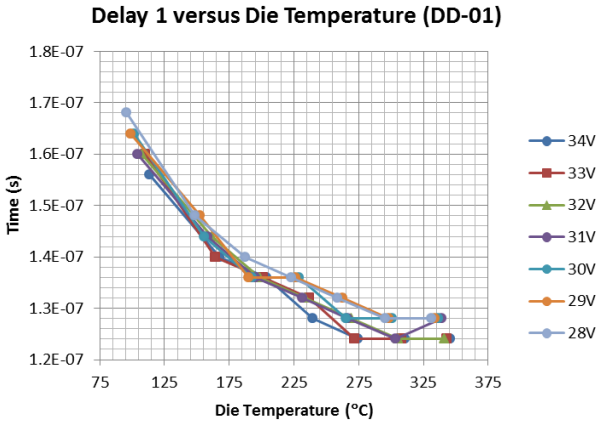

Fig. 7. Measured delay1 (low to high transition) over temperature (VDD-OD = 28V-34V, all other supplies voltages = 20V, single powerMOS load).

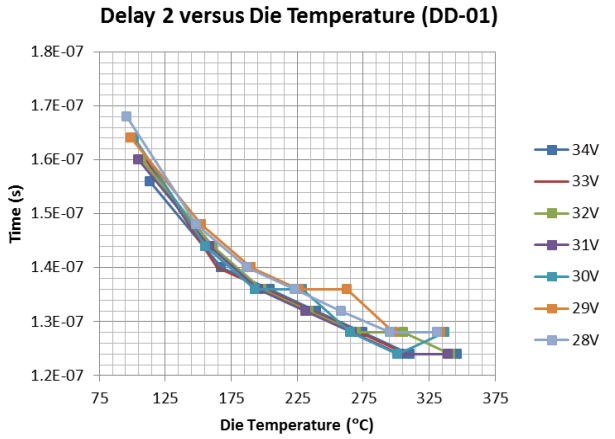

Fig. 8. Measured delay2 (high to low transition) over temperature (VDD-OD = 28V-34V, other supplies voltages = 20V, single powerMOS load).

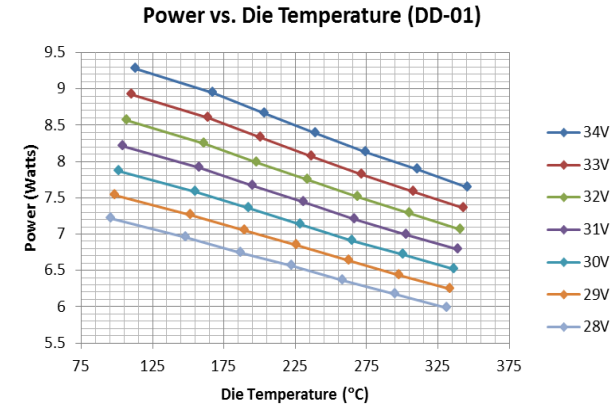

Fig. 9. Measured power consumption over temperature (VDD-OD = 28V-34V, all other supplies voltages = 20V, single powerMOS load).

IV. Conclusions

In this work an integrated SiC gate driver designed to operate at moderate overdrive voltages was presented. Specifics of the design, layout, and testing were summarized both at room temperature and over a die temperature range of 90˚C to 340˚C. An automated test system was developed and implemented allowing for voltage sweeps to be performed to evaluate the effect of supply voltages on dynamic performance. Overdriving of the output stage pull-up device through the use of higher VDD-OD values produced a significant decrease in rise time, as expected. Conversely, overdriving was shown to produce an undesired increase in the fall time due to reduced turn-off ability of the output stage pull-up device at high levels of overdrive. At room temperature, a VDD-OD of ~31V produced similar rise and fall times of ~50ns and nearly matched propagation delays of ~165ns, while consuming ~8.2W.

Two gate driver units were fully characterized over a die temperature range of 90˚C to 340˚C while driving a powerMOS load. With VDD-OD=31V, the units produced rise and fall times of ~45ns, delays ranging from ~165ns to ~125ns, and power consumption of ~8.2W to ~6.8W. The associated variation in the rise times, fall times, and delays were 6.3%, 2.7%, and 22%, respectively.

This design performed significantly better than its predecessor due to improvements in the overall topology, improved device sizing, and separate packaging of the output stage pull-up device enabling elimination of the body effect. The results of this work support the feasibility of a single die-integrated gate driver and powerMOS device.

Acknowledgments

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References

[1] J. B. Casady, R. W. Johnson, “Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review,” *Solid-State Electronics*, vol. 39, issue 10, pp. 1409-1422, October 1996.

[2] J. A. Valle-Mayorga, A. Rahman, and H. A. Mantooth, “A SiC NMOS Linear Voltage Regulator for High-Temperature Applications,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2321–2328, 2014.

[3] M. Glover, P. Shepherd, M. Francis, M. Mudholkar, H. A. Mantooth, M. Ericson, S. Frank, C. Britton, L. Marlino, T. McNutt, A. Barkley, B. Whitaker, and A. Lostetter, “A UVLO circuit in SiC compatible with power MOSFET integration,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 425–433, Sep. 2014.

[4] Ericson, N.; Frank, S.; Britton, C.; Marlino, L.; Sei-Hyung Ryu; Grider, D.; Mantooth, A.; Francis, M.; Lamichhane, R.; Mudholkar, M.; Shepherd, P.; Glover, M.; Valle-Mayorga, J.; McNutt, T.; Barkley, A.; Whitaker, B.; Cole, Z.; Passmore, B.; Lostetter, A., "A 4H silicon carbide gate buffer for integrated power systems," *IEEE Trans. Power Electron.*, vol. 29, no. 2, p. 539–542, Feb. 2014.

[5] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, and H. A. Mantooth, “Datasheet Driven Silicon Carbide Power MOSFET Model,” *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2228, 2014.