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Design and Evaluation of a Clock Multiplexing Circuit for the SSRL Booster Accelerator Timing System

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Office of Science, Community College Internships Program (CCI) Program

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U.S. DEPARTMENT OF ENERGY
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SLAC NATIONAL ACCELERATOR LABORATORY

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SPEAR3 is a 234 m circular storage ring at SLAC's synchrotron radiation facility (SSRL) in which a 3 GeV electron beam is stored for user access. Typically the electron beam decays with a time constant of approximately 10hr due to electron lose. In order to replenish the lost electrons, a booster synchrotron is used to accelerate fresh electrons up to 3GeV for injection into SPEAR3. In order to maintain a constant electron beam current of 500mA, the injection process occurs at 5 minute intervals. At these times the booster synchrotron accelerates electrons for injection at a 10Hz rate. A 10Hz 'injection ready' clock pulse train is generated when the booster synchrotron is operating. Between injection intervals-where the booster is not running and hence the 10 Hz 'injection ready' signal is not present-a 10Hz clock is derived from the power line supplied by Pacific Gas and Electric (PG&E) to keep track of the injection timing. For this project I constructed a multiplexing circuit to 'switch' between the booster synchrotron 'injection ready' clock signal and PG&E based clock signal. The circuit uses digital IC components and is capable of making glitch-free transitions between the two clocks. This report details construction of a prototype multiplexing circuit including test results and suggests improvement opportunities for the final design.

†Work supported by the U.S. Department of Energy, Office of Science, Office of Workforce Development for Teachers and Scientists (WDTS) under the Community College Internships Program (CCI).

Introduction:

- My birthplace is Eritrea, North East Africa
- Now studying at Seattle Central Community College
- Planning for Electrical Engineering degree
- CCI intern at SLAC, SSRL directorate,
  Diagnostics & Instrumentation
- Joined the CCI program through student mentoring at SCCC

System Overview :

- Beam current at SPEAR3 needs to be maintained at 500mA
  - New electron bunches injected into the accelerator every 5 minutes
  - These bunches are directed towards predetermined relative spaces
  - Task needs high timing coordination
  - Timing circuit uses two sources of 10Hz clock signal (PG&E and peaking strip)
- Present timing circuit has glitches
  - Some injection cycles are lost

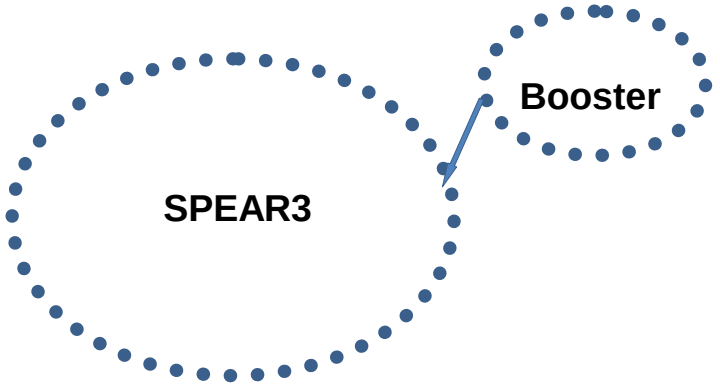

Fig. 1: SPEAR and Booster rings

Project Objective:

- To see if existing timing circuit can be modified…

Methodology:

- Design and build an alternative 10Hz clock multiplexing circuit
- Test for glitches on multiplexer output
- Compare output waveform with that of the existing system
- Demonstrate that the existing timing circuit is suitable for better performance (with upgrades)

How I prepared for the task:

Before I started working on the project, I was given:

- General picture of how the whole system works
- Detail explanation on injection system and timing circuit
- Training on how to use test equipment (Oscilloscopes, signal generators...etc.)
- Safety trainings (radiation, electrical and cyber)

Tasks Accomplished - 1 :

- Multiple discussions and meetings:
  - Circuit analysis (rough schematic of timing circuit)
  - Input/output ports and signals
  - Test glitch-free switching circuit
  - Install in chassis

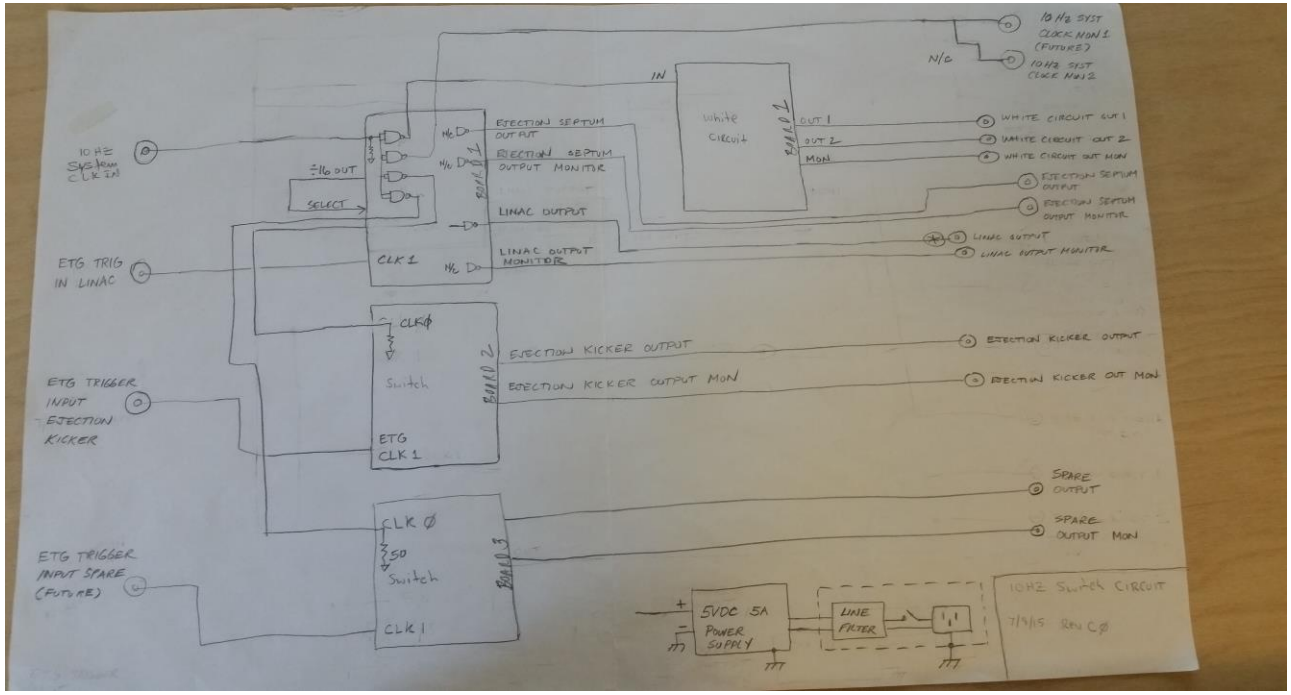

Fig. 2
New timing Circuit block diagram

Tasks Accomplished - 2 :

- Circuit synthesis:
  - First breadboard (test proposed switching circuit)
  - Then circuit board prototype (for machine testing)

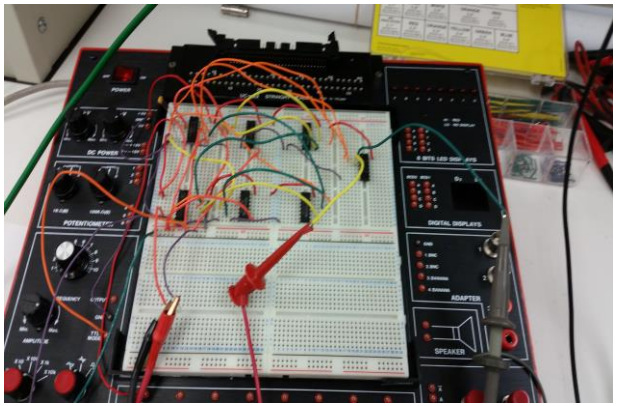

Fig. 3
Switching circuit built on breadboard

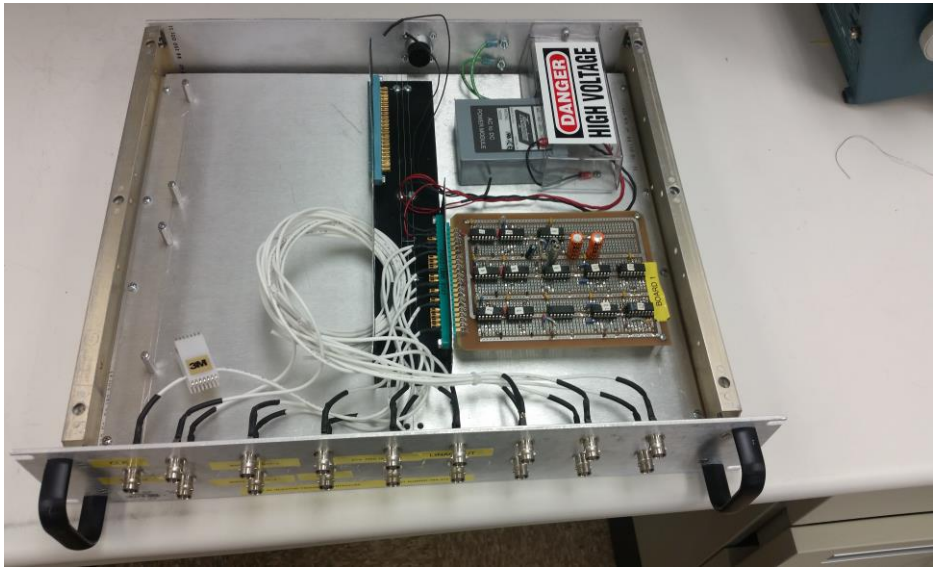

Fig. 4 switching circuit prototype in chassis

Tasks Accomplished - 3:

- Testing:
  - Bench/Lab test using test equipment:
    - ✓ Circuit switches cleanly between clock input signals
    - ✓ No glitches
    - ✓ However, misses one pulse during switching

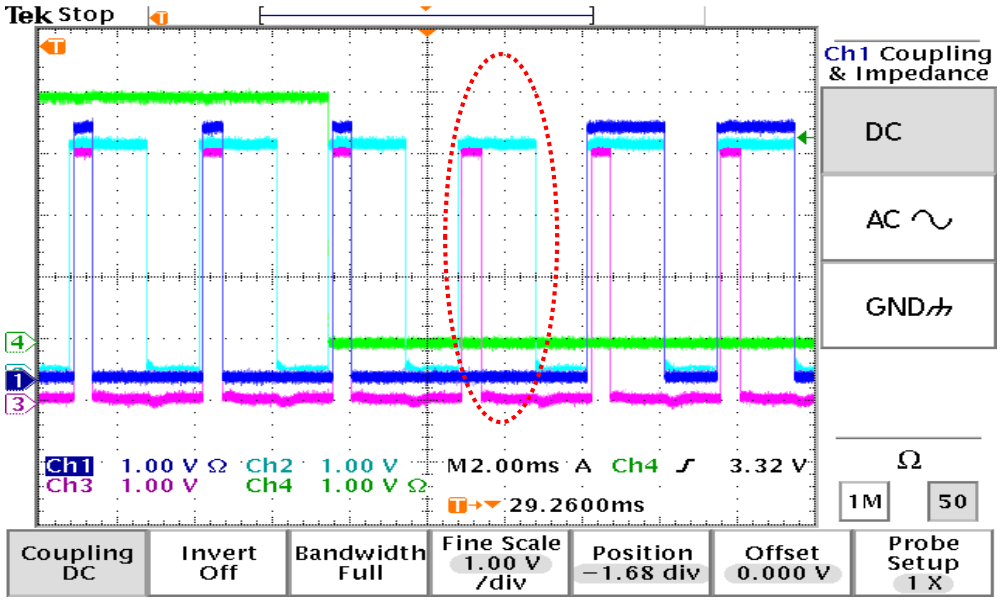

Fig. 5 Input/output waveforms of switching circuit (bench test)

- **Select Input**
- **Clock input1**
- **Clock input2**
- **Output**

Tasks Accomplished - 4:

- Test on machine:
  - ✓ Initial system test (LINAC to ring injection timing)
  - ✓ Circuit connected in Parallel to machine:
    - switches correctly between input clock signals
    - However, does not incorporate necessary signal delays (Note: Design excluded certain parts due to time limit)

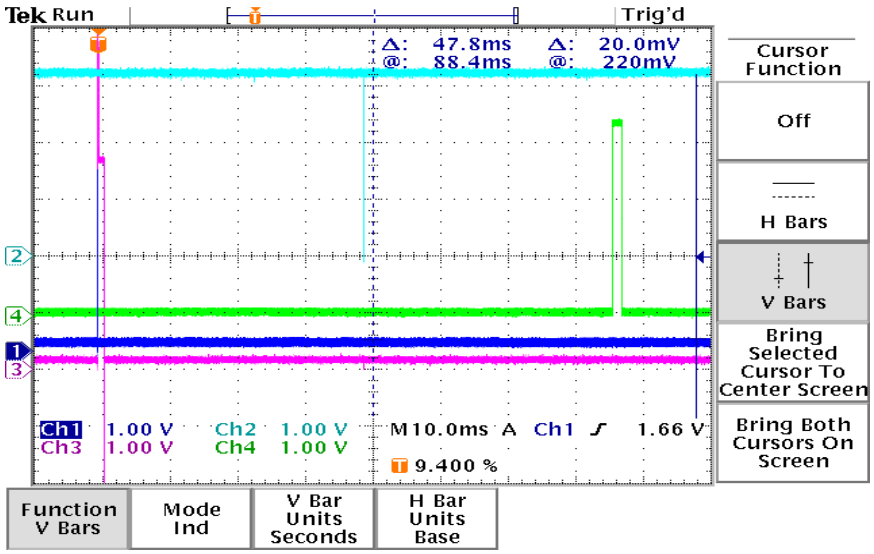

Fig. 5. Prototype Circuit board test 8/10/15

- **Clock input from power company**
- **Clock input from Peaking strip**
- **Output from switching circuit (prototype)**
- **Extraction Trigger Gate output**

Summary and Conclusion:

- The new 10Hz switching circuit does not glitch
- Circuit will be incorporated into the existing timing system
- Needs further development to include more features
  - self switching giving priority to the peaking strip
  - 40 ms delay when driven by PG&E
- Circuit also needs to be studied further to predict the effect of the missing pulse (if any).

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