UCRL-ID-122209

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1994 LDRD Final Report
93-SR-089

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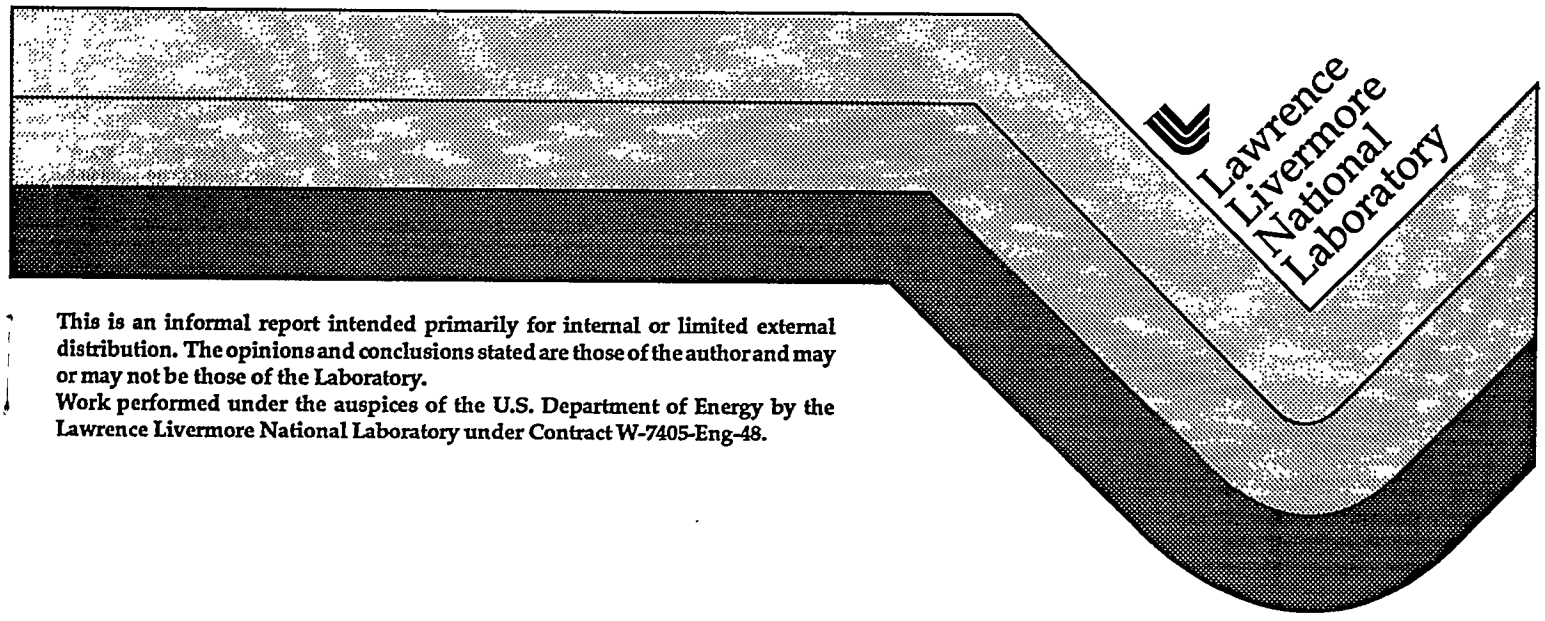
September 1995



Laser Tabbed Die: A Repairable High-Speed Electrical Interconnection Technology

by

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Abstract:

A unique technology for multichip module production is presented. The technology, called Laser Tabbed Die (L-TAB), consists of a method for forming surface-mount-type "gull wing" interconnects on bare dice. The dice are temporarily bonded to a sacrificial substrate which has a polymer thin film coated onto it. The gull wings are formed on the side of the die with a direct-write laser patterning process which allows vertical as well as horizontal image formation. Using the laser patterning system, trenches are formed in a positive electrodeposited photoresist (EDPR) which is plated onto a metal seed layer, allowing copper to be electroplated through the resultant mask. After stripping the resist and the metal seed layer, the polymer film on the substrate is dissolved, releasing the chip with the "gull wings" intact. The chips are then bonded onto a circuit board or permanent substrate with solder or conductive adhesive.

Introduction:

The performance of complex integrated circuit-based electronic systems is ultimately limited by the interconnection of IC chips to the next level of packaging. As chip speed increases, the effect of package induced delays becomes more significant. Single chip packaging using wirebonding to interconnect the chip to a lead frame, followed by surface mount soldering or pin-through-hole attachment is incapable of functioning at frequencies in excess of 200 MHz [1]. One approach to solving the packaging delay problem is to use a set of technologies generally referred to as multichip module (MCM) packaging [2], in which bare dice are bonded directly to a substrate, allowing for much shorter, lower resistance interconnects between chips. There are a large

number of different MCM processes which are generally grouped into three categories: MCM-D ("D" represents deposited films), MCM-C ("C" refers to ceramic) and MCM-L ("L" means laminate substrates such as FR-4 printed circuit boards). The highest performance technology is the MCM-D version, which uses thin film deposition and lithographic techniques to pattern fine line interconnections between chips. MCM-D produces the densest packaging of chips on a substrate, because of the reduced interconnect dimensions (i.e., reduced line widths and spacing).

Two related difficulties [3, 4] with MCM-D technology are the "known good die" (KGD) problem, and the module reparability problem. Bare chips are generally tested for functionality while still in wafer form, but they are not characterized at their top performance speed, nor are they burned-in, until after they are packaged. When such chips are used for MCM-D applications, the probability for failure of the module is very high. The problem can be solved by fully testing the die before bonding, so that only "known good die" are used. This KGD solution can be difficult and expensive to implement. This paper presents a method for producing die on sacrificial, testable substrates. After testing, the die can be excised easily, and reattached to a permanent substrate which has been pre-tested for functionality, producing a high yield module from known good die and known good substrates.

Even with the use of KGD, module reparability is still an important requirement for the production of an economically viable product. Modules with 10 - 100 die cannot be thrown away if a single die fails. An MCM-D technology must have the capability of removing individual die from failed modules, or replacing failed die with KGD. In practice, both KGD and reparability are essential for producing MCM-D products in acceptable yields. The L-TAB method presented here produces KGD, and is as repairable as surface mount packaging (an important single chip packaging technology), but with greatly reduced pitch requirements.

The L-TAB process [5] is based on the use of a sacrificial polymer film which is coated onto a temporary substrate. A laser patterning technique [6, 7], often referred to as Laser Pantography (LP), is used to "draw" patterns on an electrodeposited photoresist (EDPR) layer, and copper is electroplated into the mask formed by the development of the resist. The pattern is drawn on the vertical sidewalls of the die as well as on the top of the die and the substrate surface, creating a thin film copper interconnection from the die to the substrate. The capability of patterning in three dimensions (3D) is one of the unique features of LLNL's LP system [8], and provides a short, reliable, high performance electrical

connection. The die are tested and burned-in on the temporary substrate, and removed by dissolving the sacrificial layer from under both the leads on the substrate (forming gull wings on the side of the die) and the chip itself. Reattachment to a permanent substrate is a straightforward process of connecting the gull wings to bond pads on the substrate using patterned solder or a Z-axis conductive adhesive. If enhanced mechanical stability is required, the chip can be held down with a thermoplastic adhesive, which will flow at elevated temperature, facilitating removal for rework purposes.

Experimental:

Laser direct write apparatus

The laser exposure tool is shown schematically in Fig. 1. An argon-ion laser operating in the multiline UV range from 338 to 364 nm is used as the light source. The laser can be diverted along either of two beam paths, one normal to the surface, and the other at an angle to the surface. Angles of from 30 to 60 degrees with respect to the normal can be used. An acousto-optic modulator is used both to change the laser power, and as a fast electronic shutter. The laser beam is fixed during laser patterning; the x, y, and z stages are moved to obtain a pattern. The x and y stages are generally scanned at 10 mm/s, and the incident laser power is 20 mW, with a beam size of 6 μm x 35 μm (a cylindrical lens is used to focus the beam to a line, and an aperture is employed which allows the long dimension of the beam to be varied from 5 to 65 μm in size). Microscope objectives coated for use in the UV are used to focus the laser beam after the cylindrical lens. These objectives are fixed, and a z-axis translation stage is used to move the sample vertically with respect to the objectives. A mirror mounted on a computer-controlled stepper motor is moved into the beam path to direct the beam through the angled objective. A monitoring lamp directed through the normal objective by means of a beam splitter onto both the substrate surface and into a camera allows the operator to both register the die with respect to the substrate, and to watch the laser rastering on the surface.

Materials

The polymer of choice for the sacrificial layer is phenoxy resin PKHC made by Phenoxy Associates. A 25% solids solution of the phenoxy resin in n-methyl pyrolidone (NMP) or cyclohexanone was

generally used. Other polymer systems were also investigated. OCG's Probimide 411 pre-imidized polyimide was used as received. The cyanoacrylate adhesive was a "Krazy Glue" product, and the phenolic resin solution was AJ-1400 photoresist from Shipley Co. A one-part epoxy, A-702, came from Resin Technology Group, Inc. The electrodeposited photoresist (EDPR) was obtained from Shipley Co., under the name PEPR-2400.

Results:

Process overview

Figure 2 shows an outline of the process for forming gull wings on bare chips. A temporary substrate is coated with a uniform sacrificial release layer to which chips are directly bonded. A metal seed layer is deposited on the module. This layer completely covers both the horizontal and vertical surfaces (i.e., the sidewalls of the die). Photoresist (EDPR) is electroplated unto the metal seed layer, and is exposed with the laser direct write apparatus. After developing the resist, copper is electroplated through the photoresist mask, which is then etched away to reveal the metal seed layer. Finally, the seed layer is removed, allowing testing and burn-in to be performed. The die are then released by dissolving the sacrificial layer in an appropriate solvent. The process of reattachment to a permanent substrate can be accomplished with solder, electrical interposer, or Z-axis adhesives.

Release layer and die attach:

The release layer is formed on a temporary substrate (e.g. a silicon wafer) by spinning-on a solution of the phenoxy resin. After drying at 120° C for 30 min in a nitrogen ambient to remove all the residual solvent, the wafer is placed on a hot plate and brought to a temperature of 180°-200° C, which is well above the T_g (110° C) of the phenoxy resin. The die are then placed on the softened resin, to which they easily adhere with minimal pressure. A pick and place should be used both to accurately position the die with respect to each other, and to apply a consistent amount of pressure during bonding. The pressure used to bond the chips, together with the thickness of the release layer, determine the extent of fillet formation at the base of the die. A small fillet (extending 100-200 μm up the sidewall from the base) is essential for obtaining mechanically sound gull wings in high yield.

The use of a thermoplastic adhesive such as phenoxy resin is the key to the process. Removing the solvent by evaporation before bonding means that under the die there will be no trapped solvent to cause gaps and edge lifting. An alternate method of adhering the die to the release layer involves pushing the die into a polymer film still containing solvent (a typical adhesive process) with the result that gaps at the interface between the die sidewall and the substrate surface form. This was particularly true for the preimidized polyimide which was tried in this study, which also tended to shrink substantially when cured. To be an effective die attach procedure for L-TAB, the polymer system should be a 100% solids process at the time of bonding, which the phenoxy resin film is after evaporation of the solvent. Other possible adhesive systems include cyanoacrylates and epoxies, both of which are 100% solids. However, both materials suffer from problems in other parts of the process, and will be discussed below.

Deposition of the copper seed layer

A metal multilayer is sputtered onto the temporary substrate with the attached chips. The purpose of the metal layer is to provide a conductive surface over the entire module for electroplating both EDPR and Cu. A titanium (500 Å) adhesion layer is deposited in RF diode mode, followed by a copper (2000 Å) layer sputtered on top of the Ti in RF magnetron mode. Deposition conditions are chosen to maximize adhesion while minimizing film blistering. The cyanoacrylate and the phenolic resin films both blistered badly in the sputtering chamber, while polyimide, phenoxy resin, and the epoxy held up well.

Electroplating of EDPR

Instead of using a standard spin-on resist to form the photoactive coating on the module, a positive electrodeposited photoresist is used. The reason for using EDPR is that spin-on films will not conformally cover the chip sidewalls, and will be very non-uniform on the flat surfaces as well when large topographical features are involved. EDPR films, on the other hand, deposit uniformly over conductive surfaces regardless of the topography, and are, therefore, uniquely suited for patterning vertical as well as horizontal surfaces. The thickness of the EDPR film ranges from 5 to 10 μm, and is dependent upon plating voltage and temperature, but is only marginally dependent upon plating time. The plating is self-limiting, so that plating times from 20 sec to 2 min produce identical films (the excellent uniformity of the EDPR film results

from the self-limiting nature of the process). The temperature is an important variable with regard to film thickness. Typical plating temperatures range from 25° to 30° C, with thickness variations of 3 - 4 μm over that range. The best metallization results were obtained with 7 μm films, from which 5 μm copper lines could easily be produced. After EDPR plating, the surface of the module is rinsed with water, air dried, and baked at 90° C for 10 min to allow the resist to coalesce. After soft baking, the module is ready for exposure.

EDPR exposure, and development

The resist is exposed with the laser apparatus described above. The interconnects on the sidewall are not written by scanning each individual line as the z-position is varied. Such a procedure is very time consuming, particularly since many VLSI die have in excess of 50 I/O per sidewall. A much faster, more manufacturable process is used instead: starting at the base of the die, the x stage is moved in the direction of the sidewall to be patterned, and the laser is turned on and off, creating a series of small boxes (typically 20 μm x 40 μm, where 20 μm is the linewdith) along the entire length of the sidewall. At the end of the sidewall the z stage is moved up ~35 μm, and the x stage is scanned in the negative direction, forming another series of boxes connected to the first. This process is repeated ~10 times until the connected boxes form lines running from the bottom of the sidewall to the top (i.e., the individual I/O lines have been "stitched" together). Additional rasters are performed on the top of the chip and on the substrate to bring the lines to the desired location on the flat surfaces. For chips with I/O on more than one side, the theta stage is used to rotate the module into the correct orientation with respect to the angled beam.

Convenient testing and burn-in of the die require that the I/O from each die be routed (fanned out) to the outer perimeter of the temporary module for electrical connection to the test equipment. This routing can be done with the normal beam of the laser patterning apparatus, or can be done with a projection aligner and a standard chrome mask. The result is that the gull wings are not separate from the fan-out metallization. Later in the process, the gull wings will have to be excised from the temporary metallization before release from the temporary substrate (see below)

The resist is developed in 1% aqueous sodium carbonate at 35° C for 2 - 3 min. Since the color of the resist contrasts sharply with the color of the Cu seed layer, an optical determination of

development completion is straightforward. After development, the module is ashed in an oxygen plasma at 150 W for 3 min. This procedure reduces the field EDPR by ~0.4 μm, but cleans up any residual organics on the exposed Cu.

Interconnect metallization

Copper plating is performed in a high flow plating tank which contains an aqueous acidic copper sulfate solution. A pulsed waveform is used to plate the Cu. A 1 ms over-voltage pulse is used to enhance nucleation on the surface of the exposed Cu seed, followed by a 9 ms lower voltage pulse. This procedure assures good uniformity across a 4" substrate (≤ 6%). A plating rate of ~3500 Å is typical, and the surface morphology is ~ 0.5 μm. Final metallization layers on top of the copper can be applied at this point by electroplating Ni and Au.

EDPR and seed layer removal

The EDPR film is removed after metallization by immersion in a 65° C, 2% sodium hydroxide solution for several minutes. This procedure cannot be used if there is any exposed bond pad aluminum which has not completed covered by the Cu metallization. An alternate method is to dissolve the resist in a polar, aprotic solvent such as NMP or acetonitrile at elevated temperature. Following resist removal, the Cu seed layer is stripped at room temperature in a 10% ammonium persulfate solution in an APT spin-spray etcher. Typically, rates of 1000 Å/min are achieved, and a 100% overetch is used to assure the clearing of the sidewalls. The Ti adhesion layer is etched in an SF_6 plasma.

Testing, excising, die removal, and reattachment

As mentioned previously, ease of testing requires that the die I/O (gull wings) be fanned out from the die periphery to the edges of the temporary module, forming test pads for probing. The test pads can be considerably larger than standard die bond pads, and can be attached to probe stations either with traditional probe tips (or cards), or with semi-permanent connections like wire bonds or beta connectors, which are conducive to high speed testing.

After testing is complete, the fan-out lines are cut near the die edge to form the ends of the gull wings (YAG lasers are available for cutting copper lines). For mechanical strength, the gull wings should not extend more than 500 μm past the base of the die (an ideal distance is 250 μm for linewidths of 50 μm).

The final step in the gull wing formation process is the removal of the die from the temporary substrate. The die are removed by dissolving the sacrificial phenoxy release layer in hot NMP - the die float off the substrate with gull wings intact (experiments with an epoxy release layer failed at this stage of the process. No solvent could be found to dissolve the epoxy sufficiently to release the die). Figure 3 is a photograph of gull wings after the die has been removed from the substrate (the die is a blank piece of Si). The gull wings are 75 μm wide on 200 μm centers. Another die is shown in Figure 4, which is a set of four photographs showing different magnifications of the same die. The dimensions (30 μm lines on 100 μm centers) are considerable smaller than those in Figure 3.

The solder reattachment process is straightforward: solder is deposited (either evaporated or electroplated) on the permanent substrate in the appropriate places (techniques for doing this are well established in the flip-chip solder-bump interconnect business). A pick and place is used to position the chips onto the bond pads of the substrate, and flux is used to temporarily hold the die in place. The solder is then reflowed in an oven at the appropriate temperature. An alternative to oven reflow is to use a laser soldering apparatus to reflow the solder lead by lead.

It should be noted that the testing, excising and reattachment procedures were not developed as part of this project. The gull wings were formed (laser patterned) to their final length (500 μm from the base of the die in Figs. 3 and 4). Descriptions of the anticipated processes have been included for clarity and consistency, and to show the future direction of this work.

Discussion:

The success of the EDPR process for patterning vertical as well as horizontal surfaces was an important factor in the development of the L-TAB process. Since the resist exposure and development is a photolytic process, a fairly low power UV beam can be used (0.1 - 0.5 $mW/\mu m^2$). Earlier 3D laser patterning technologies developed at LLNL relied on pyrolytic processes carried out with a high power visible laser beam (5 - 15 $mW/\mu m^2$). The drawback to these pyrolytic processes is that a lot of heat is deposited in the release layer, causing it to blister, and making the process unworkable.

The development of the thermoplastic release layer process was the most important factor in making the L-TAB process

successful. As mentioned in the Results section (see above), other methods for forming an adhesive/release layer were unsuccessful, either because of trapped solvent in the film (e.g., polyimide, phenolic resin), because the release layer (cyanoacrylate) is not resistance to heat, plasma, and solvents, or because the release layer (epoxy) does not dissolve completely in any solvent. The thermoplastic phenoxy resin solved these problems because it retains no solvent during bonding, and is fairly heat resistant, while being sufficiently soluble in polar aprotic solvents to dissolve completely in hot NMP. The thermoplastic method allows the temporary substrates to be prepared in advance and stored for later use. It also simplifies the bonding process, and results in very uniform fillet formation, which greatly improves the gull wing yield.

A major advantage of the L-TAB process is the high density of interconnects that can be fabricated. None of the current interconnect technologies can handle a peripheral array of bond pads with a pitch smaller than 4 mil. This means that for a 1 cm^2 die, the maximum number of I/O is 400 (using 4 sides). In the near future, complicated logic chips will have a significantly larger number of I/O, and will be forced to used flip-chip bonding with area-array bond pads, a technology which is not right for every application. The L-TAB process offers an alternative to flip-chip, because the pitch can easily be pushed from 4 mil to 2 mil, doubling the I/O capacity. Further reductions in pitch dimension should also be possible, suggesting that L-TAB may be the advanced packaging process of the future.

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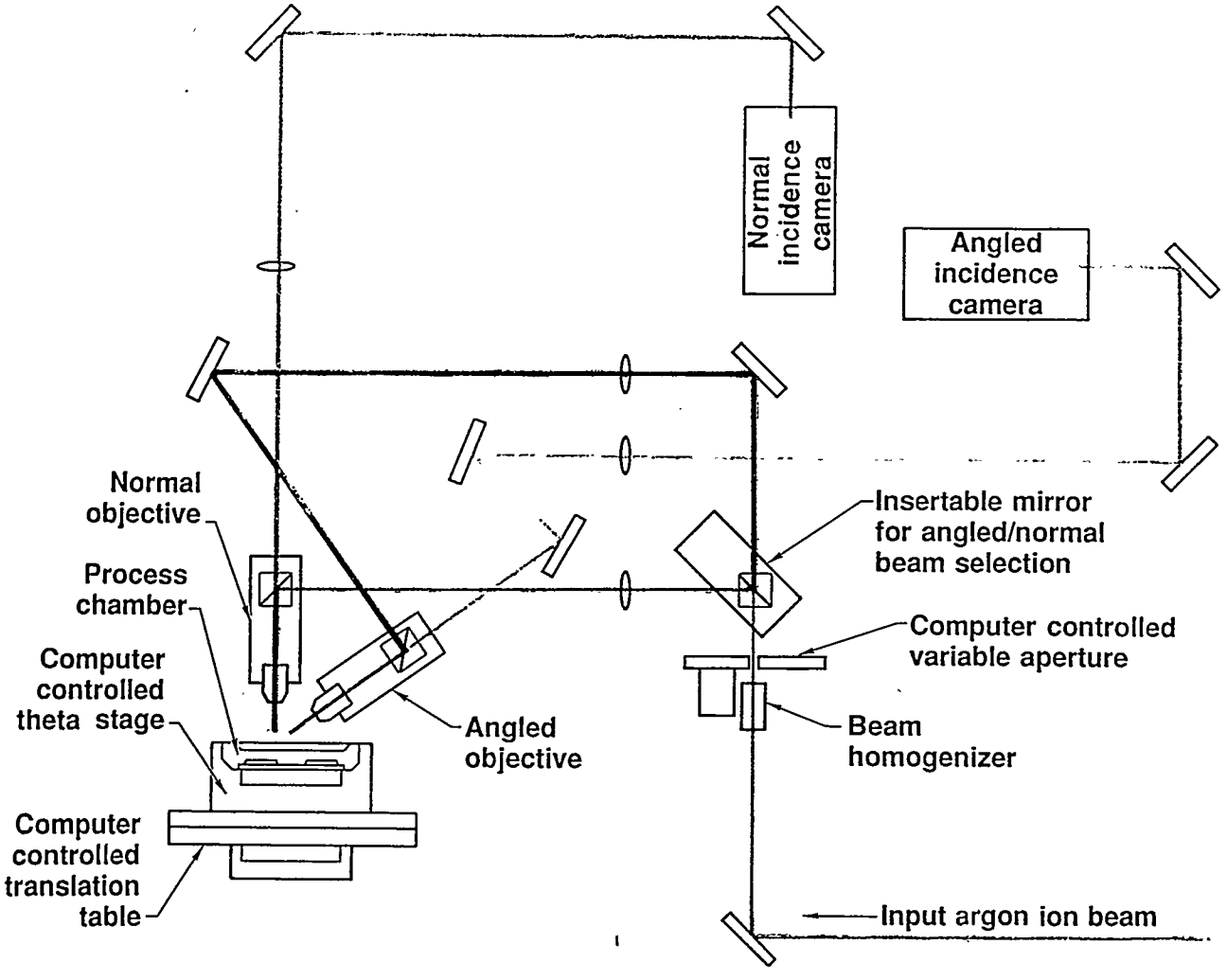
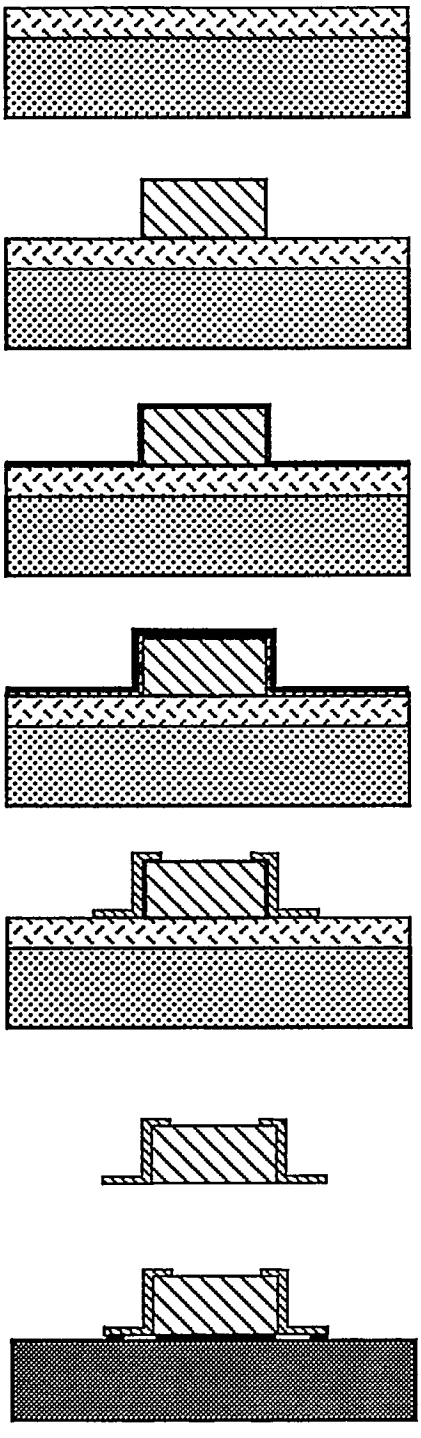


Figure 1. The laser pantograph apparatus



A. Release layer on temporary substrate

B. Die bonded to release layer

C. Metal seed layer deposited

D. EDPR plated onto seed

E. Cu plated, EDPR and seed removed

F. Release layer dissolved

G. Die reattached to permanent substrate

Figure 2. L-TAB Process Flow

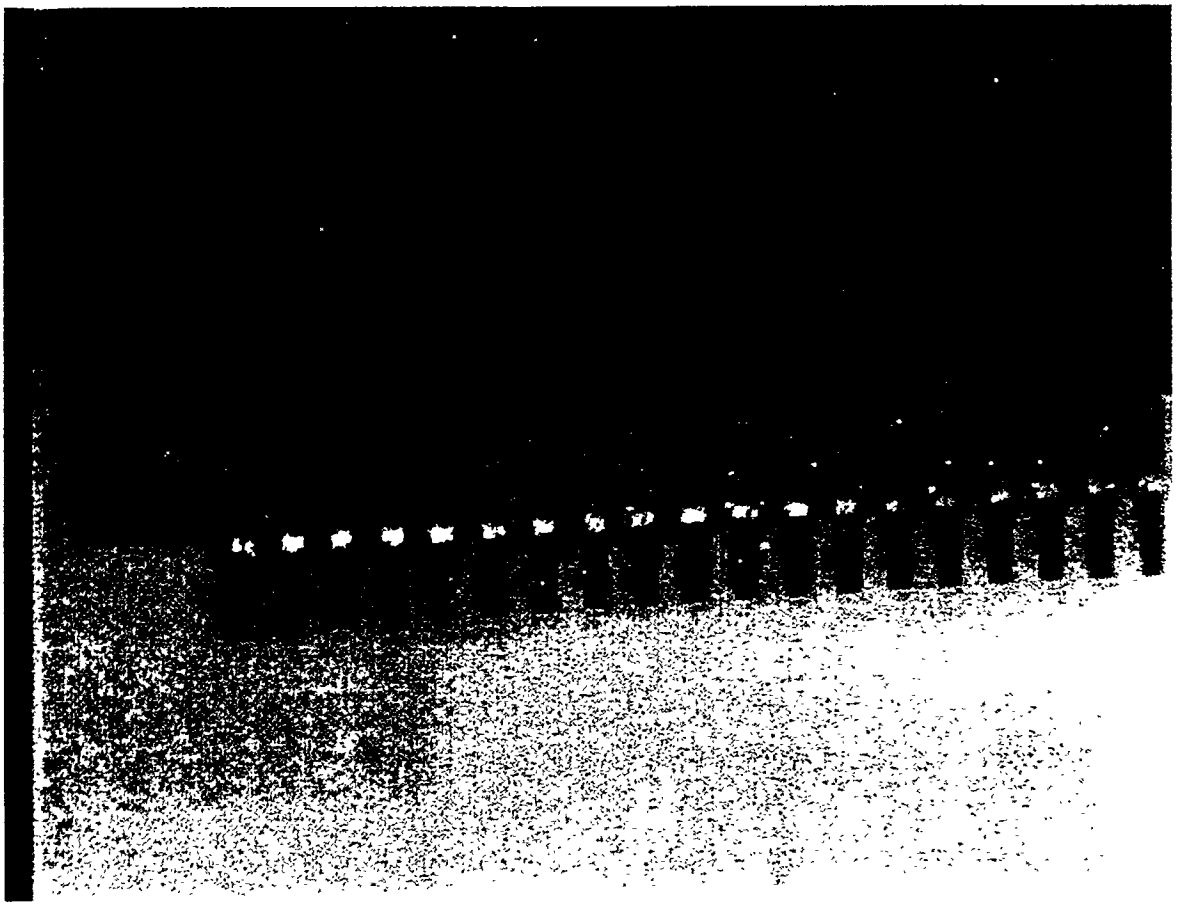


Figure 3. Photograph of gull wings on a blank silicon die. The lines are 75 μm wide and the pitch is 200 μm.

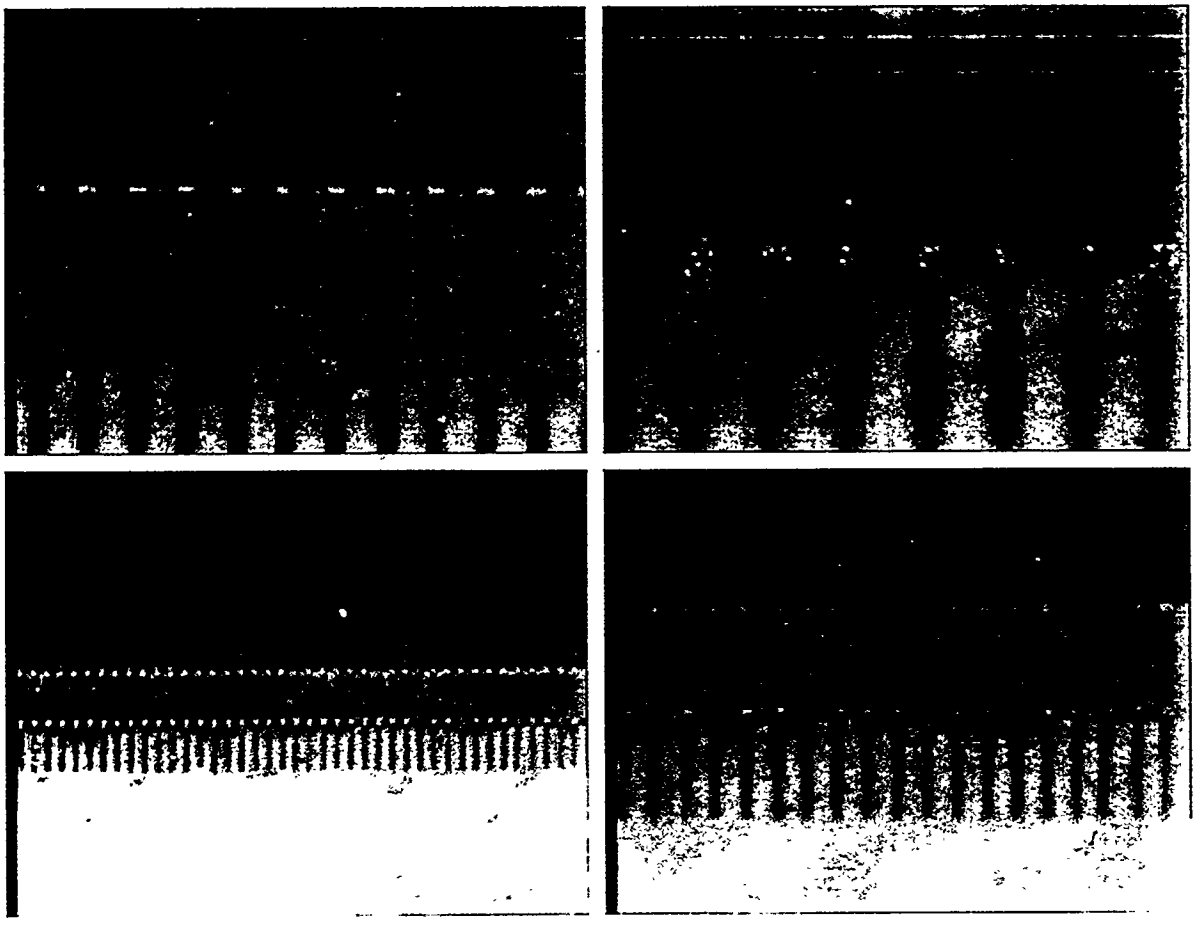


Figure 4. 30 μm gull wings with 100 μm pitch. All 4 photographs are of the same die, with different magnifications

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