Design of a High Efficiency 30 kW Boost Composite Converter

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***Abstract*—An experimental 30 kW boost composite converter is described in this paper. The composite converter architecture, which consists of a buck module, a boost module, and a dual active bridge module that operates as a DC transformer (DCX), leads to substantial reductions in losses at partial power points, and to significant improvements in weighted efficiency in applications that require wide variations in power and conversion ratio. A comprehensive loss model is developed, accounting for semiconductor conduction and switching losses, capacitor losses, as well as dc and ac losses in magnetic components. Based on the developed loss model, the module and system designs are optimized to maximize efficiency at a 50% power point. Experimental results for the 30 kW prototype demonstrate 98.5% peak efficiency, very high efficiency over wide ranges of power and voltage conversion ratios, as well as excellent agreements between model predictions and measured efficiency curves.**

I. Introduction

Dc-dc converters in applications such as maximum power point tracking in photovoltaic power systems, or drive trains in electric or hybrid vehicles (EV, HEV), are required to operate efficiently over wide ranges of power and voltage conversion ratios. System performance depends on improvements in weighted converter efficiency. In EV or HEV applications, such system efficiency improvements translate directly into increased equivalent miles-per-gallon (MPGe) performance [1]. Even more importantly, loss reductions translate into reduced size and cost of the cooling system.

The traditional boost converter employed in EVs or HEVs [2] has low efficiency at light load power. Also, power density is low due to the low switching frequency and high power losses. To increase average efficiency and power density, a modified dual active bridge has been proposed [3], [4], with the number of switching devices reduced by half compared to the conventional dual active bridge(DAB). However, the switch voltage stresses are equal to the output voltage or the input voltage. For the case when the voltage rating is higher than 600 V, silicon IGBTs are commonly employed, as high voltage silicon MOSFETs are not competitive, while emerging wide bandgap devices are more expensive. The switching frequency with silicon IGBTs is limited to around 10 kHz. Also, switching loss with conventional DAB control (phase shift between primary and secondary) increases under light load conditions. Several previous studies have been focused on reducing voltage stresses over switching devices while maintaining high peak efficiency. In [5], a soft-switched continuous current mode(CCM) boost converter was introduced to achieve a higher voltage conversion ratio and to extend zero-voltage switching(ZVS) range by auxiliary circuits. Also, voltage stresses and current stresses imposed on the discrete components are reduced. However, low efficiency is observed under light load conditions and accurate control is necessary to regulate the output voltage. In [6], a multiphase bidirectional flyback converter was introduced to reduce number of discrete components and capacitor RMS current. However, this flyback topology has large voltage stress over switching devices and is not suitable for wide voltage conversion range. In [7], a four level flying-capacitor dc-dc converter (3X dc-dc converter) was described. This topology greatly improves efficiency over wide power range and also reduces voltage stresses over switching devices. However, the flying capacitors of this topology have not only large RMS current but also large energy rating ($0.5CV^2_{rating}$) due to the required capacitance and voltage ratings. Also the output voltage regulation is restricted to discrete values, $V_{IN}, 2V_{IN}$, and $3V_{IN}$.

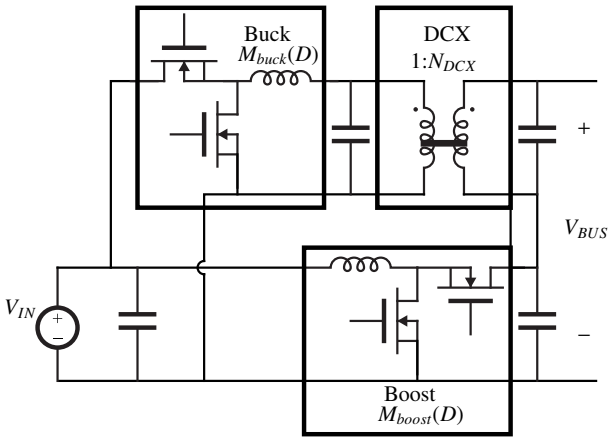

Fig. 1. Composite converter architecture consisting of buck, boost, and DCX (DC transformer) modules [8]

To reduce the voltage stresses over switching devices, maintain high efficiency over wide operating range and reduce the energy rating of capacitors, a *composite converter architecture* has been proposed [8], as shown in Fig. 1 with

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experimental verification on a 10 kW prototype. In the composite architecture, dissimilar partial-power converter modules are combined to address the dominant loss mechanisms and to achieve superior efficiency performance. This approach is briefly reviewed in Section II. The objectives of this paper are to address module and system-level design optimization of the composite dc-dc converter based on a comprehensive loss model, and to demonstrate the results on a scaled-up 30 kW prototype operating from 140-280 V input and capable of generating up to 800 V output. The loss model is summarized in Section III, and the design optimization is presented in Section IV. Section V presents experimental results for the scaled-up 30 kW composite converter prototype, which demonstrates 98.5% peak efficiency.

II. Boost Composite Converter Architecture

The composite converter architecture shown in Fig. 1 has been proposed for boost dc-dc applications to achieve high weighted efficiency over a wide range of input and output voltages. The composite architecture consists of a boost module, a buck module, and a dual active bridge (DAB) converter operated as a DC transformer (DCX).

The voltage conversion ratio of the composite converter is

$$M = \frac{V_{BUS}}{V_{IN}} = M_{buck} N_{DCX} + M_{boost} \tag{1}$$

where M_{buck} and M_{boost} are the buck and the boost module conversion ratios, respectively, and N_{DCX} is the fixed conversion ratio of the DCX module. Operating modes of the composite converter are illustrated in Fig. 2, for the case when the input dc voltage is between 140 V and 280 V, the maximum output voltage is 800 V, and the required dc conversion ratio is $1 \leq M \leq 3.8$. At bus voltages below 400 V, the composite converter is in the boost-only mode, with the buck and the DCX modules shut down. For $M = N_{DCX} + 1$, both the boost and the buck modules operate in pass-through mode (not switching with $M_{buck} = M_{boost} = 1$), while the DCX processes a fraction of the output power. This results in exceptionally high efficiency. One may also note that the modules are arranged and operated so that device voltage stresses are limited to 400 V in the 800 V application, allowing the use of 600V power semiconductor devices with improved figure of merit such as superjunction MOSFETs. As demonstrated in [8], the composite converter can achieve very high efficiencies over wide ranges of power and input and output voltages.

III. Comprehensive Loss Model

To facilitate composite converter module and system optimization, a comprehensive loss model is developed. The model includes semiconductor switching and conduction losses, as well as dc, ac winding copper losses and core losses in magnetic components.

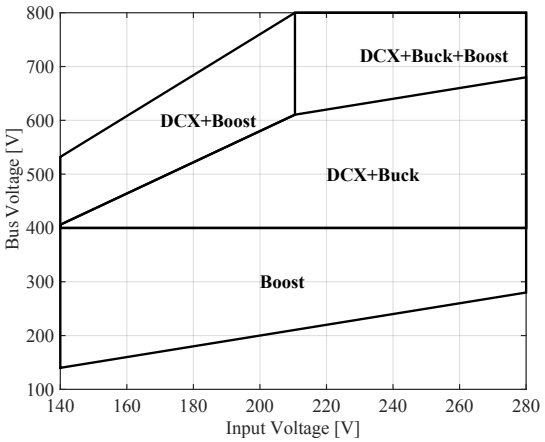

Fig. 2. Operating modes of the composite converter in the bus voltage versus input voltage plane, for $N_{DCX} = 2$

A. Semiconductor switching loss

Piecewise linear (PWL) functions as described in [9] are employed for switching loss calculation. The advantage of the developed PWL loss model is that it allows use of parameters imported from device datasheets, so that available MOSFETs can be easily compared. The developed PWL switching loss model is based on several assumptions:

- Parasitic circuit inductances and capacitances, and any ringing during switching transitions, are neglected.
- The MOSFET gate-to-source capacitance is considered constant.
- When a power switch is implemented using multiple MOSFETs in parallel, the total switch current is evenly distributed among the paralleled devices.
- The switching losses are included only for hard-switching operation. At operating points where zero-voltage switching (ZVS) is achieved, the switching losses are neglected.

With these assumptions, the switching loss is calculated for each subinterval of a switching period. Fig. 3 shows the approximated piecewise linear waveforms of gate-source and drain-source voltages, and drain-source current, and the power loss as a function of time during hard-switching turn-on transition. Each switching loss, P_1, P_2, and P_3, represents the switching loss in each interval. The diode reverse recovery loss is represented by P_{QRR}. The reverse recovery time can be determined by computing minority-carrier lifetime of p-n junction body diode [10]. Also, the stored energy of MOSFET dissipated during hard-switching turn-on transition can be calculated with effective output capacitance ($C_{O(er)}$) imported from datasheet. The total switching loss during hard-switching turn-on transition is

$$P_{SW} = P_1 + P_2 + P_3 + P_{Qrr} + 0.5 C_{O(er)} V_{DS}^2 \times f_s \tag{2}$$

while f_s is the switching frequency of converter.

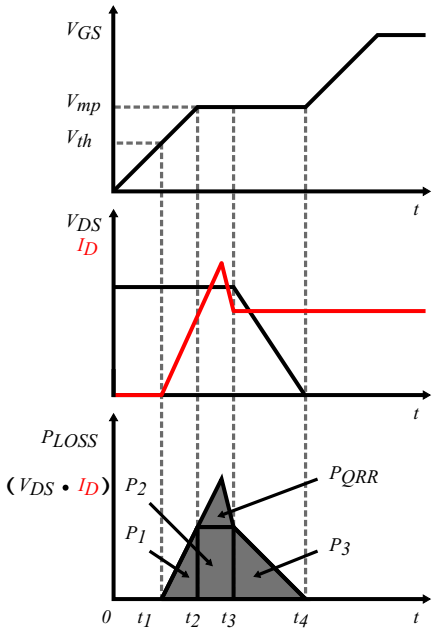

Fig. 3. Piecewise linear waveforms approximating MOSFET hard switching during turn-on transition: gate-source and drain-source voltages, drain-source current, and the power loss.

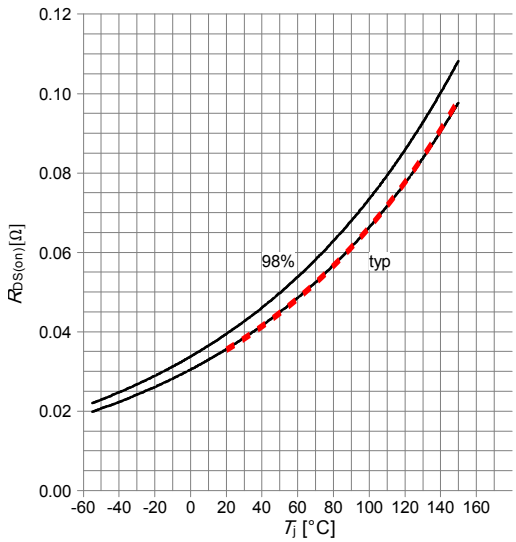

Fig. 4. IPW65R041CFD drain-source on-state resistance as a function of junction temperature (black) and a curve-fitted function (red)

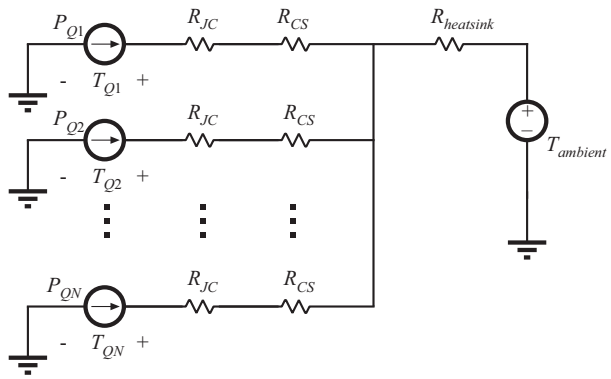

Fig. 5. Simplified thermal model for the MOSFET junction temperature, R_{JC} : 0.25Ω, R_{CS} : 0.6Ω, $R_{heatsink}$: 0.02Ω, $T_{ambient}$: 25°C

B. Semiconductor conduction loss

The MOSFET on-state drain-source resistance depends on the junction temperature, as shown in Fig. 4 for the Infineon IPW65R041CFD MOSFET. The black curves show the typical on-state resistance, while the red dashed curve represents a function obtained by curve fitting. The MOSFET on-state resistance is modeled based on the curve-fit function shown in Fig. 4. The on-state resistance can be represented as

$$R_{DS}(T_{junction}) = R_{DS(25°C)} \times \left(1 + \frac{\alpha}{100}\right)^{T_{junction}-25} \quad (3)$$

where α is a coefficient in the curve fitted function, equal to 0.8 in this case. To predict the MOSFET junction temperature, a simplified thermal circuit model shown in Fig. 5 is employed. P_{Qx} is loss of each MOSFET in parallel, R_{JC} is the thermal resistance of MOSFET junction-to-case, R_{CS} is the thermal resistance of case-to-heatsink, $R_{heatsink}$ is the heat sink thermal resistance, and $T_{ambient}$ is the ambient temperature.

First, switching losses and conduction losses with on-state resistance at 25°C are preliminarily calculated. Then this loss is applied to the thermal circuit of Fig. 5. As a result, the junction temperature of MOSFET can be predicted. With this MOSFET junction temperature, on-state resistance is calculated and conduction loss is updated with re-calculated on-state resistance. Taking the junction temperature into account is an improvement in the conduction loss model compared to the loss model with constant on-state resistance.

C. Magnetic loss

Magnetic loss consists of core loss and winding loss including DC and AC winding copper losses. DC winding copper loss is proportional to the square of the DC winding current, while AC winding copper loss represents the loss due to the skin and proximity effects and fringing loss. Dowell's method [11] is used for AC winding copper loss. Core loss is calculated according to the iGSE method [12] for both inductors and transformers.

IV. Design Optimization of the Composite Converter

The required input and output voltages and the conversion ratio for the composite converter application considered in this paper are illustrated in Fig. 2. The maximum output power is 30 kW. The specific design optimization objective is to minimize the losses at a particular operating point: V_{IN} = 210 V, V_{BUS} = 650 V, at 15 kW (50%) output power.

A system-level decision involves a choice of the DCX conversion ratio N_{DCX}. The power processed by the DCX (and buck) and the boost modules is determined by N_{DCX}. With a smaller N_{DCX}, the power processed by the boost module is larger, and vice versa. Fig. 6 shows the power processed by the boost or the DCX (and buck) modules as functions of N_{DCX} at the 210 V input, 650 V bus voltage operating point with 15 kW output power.

Taking into account that the device voltage stress should be limited to 400 V, the maximum output voltage of the boost module is set to 400 V. Since the maximum required

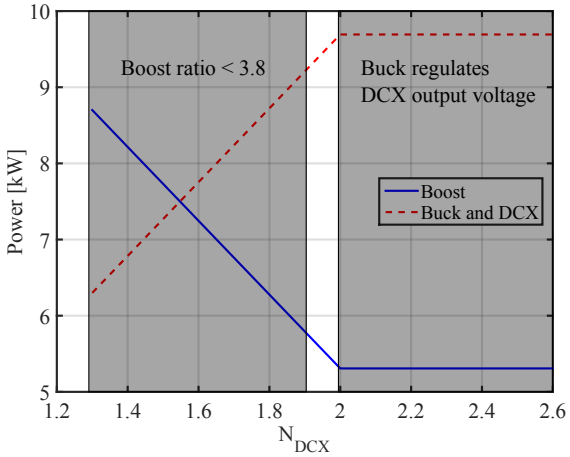

Fig. 6. Power processed by boost and DCX (and buck) as a function of N_{DCX}, for V_{IN} = 210 V, V_{BUS} = 650 V, P = 15 kW (50%) system output power

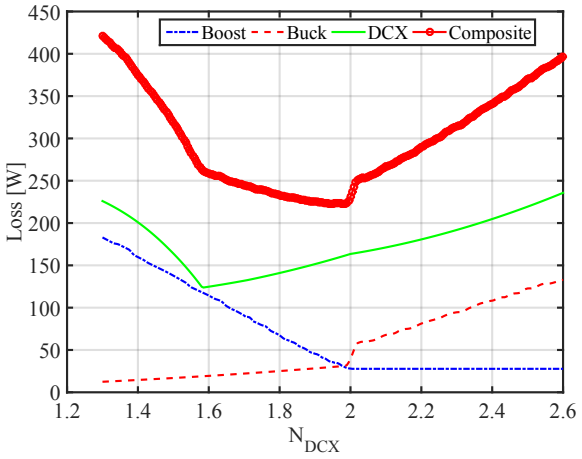

Fig. 7. Predicted module and composite converter losses as function of N_{DCX}, for V_{IN} = 210 V, V_{BUS} = 650 V, P = 15 kW (50%) system output power

conversion ratio is M = 3.8, it must be possible to produce the maximum output (800 V) for input voltages greater than or equal to 800/3.8 = 210 V. Hence, N_{DCX} must be greater than or equal to (800 – 400)/210 = 1.9. With $N_{DCX} \geq 2$, the buck module step-down ratio is adjusted to regulate the output voltage. Hence, the power processed by each module becomes constant for $N_{DCX} \geq 2$, but losses and efficiencies in the buck and DCX modules increase with increasing N_{DCX}. Based on the above considerations, it is clear that an optimum N_{DCX} is expected to be approximately 1.9. The loss model is used to evaluate the module and the overall composite converter losses as functions of N_{DCX}, and the results are shown in Fig. 7.

Even though the DCX loss is the lowest for N_{DCX} = 1.6, the loss of the composite converter is found to be the lowest at N_{DCX} = 2, which also meets the voltage conversion requirement $N_{DCX} \geq 1.9$. Hence, N_{DCX} = 2 is selected for the system implementation.

Given N_{DCX} = 2, the power processed by the boost module is

$$P_{boost} = \frac{P_{BUS}}{V_{BUS}} V_{out-boost} \tag{4}$$

while the output voltage of boost module for 210 V input, and 650 V bus voltage is

$$V_{out-boost} = (V_{BUS} - V_{IN} N_{DCX}) \tag{5}$$

A. Boost and Buck module

The boost module design is performed to achieve the lowest losses at the power levels and the conversion ratio given by (4) and (5), respectively. For N_{DCX} = 2, the power processed by DCX and boost module at 15 kW (50%) system output power are found to be 9.7 kW and 5.3 kW, respectively. Based on the comprehensive loss model presented in chapter section III, magnetics optimization is performed based on the flow chart shown in 8. The final goal of this optimization process is to achieve the highest efficiency at given operating condition, while making sure the core does not saturate under worst-case high-power conditions and the windings fit into the core window area. The resulting inductance from the optimization process for the boost module is 17 µH. As a check of magnetics optimization, Fig. 9 shows the model-predicted efficiency of the boost module for three different boost inductances: 8 µH, 17 µH, and 32 µH. At the optimization point of 210 V input, 230 V output, and 5.3 kW power for the boost module, 17 µH of inductance achieves the highest efficiency.

One may note that the buck module operates in pass-through mode under the given operating condition of 210 V input/ 650 V_{BUS} output. The buck module allows designers to choose the sub-critical operating conditions. In this paper, 220 V input/ 405 V_{BUS} output is chosen for the sub-critical operating point. At this operating point, the buck module is switching while the boost module operates under pass-through mode. The resulting optimized inductance for the buck module is 32 µH.

B. DCX module

The dual active bridge (DAB) module is operated as a DC transformer (DCX). One major difference between DAB and DCX is in how the converter controlled. The DCX is operated always under open-loop control and the phase shift between primary and secondary is entirely determined by body-diode reverse recovery of secondary MOSFET and non-linear output capacitance of MOSFET (C_{OSS}). Under these conditions, we observe higher efficiency. Accurate modeling of DCX steady state operation is required for design and optimization. In this section, a simplified DCX steady state model is introduced and then optimization of the DCX module is explained.

Fig. 10 shows the DCX tank inductor current waveforms at different load conditions. The ideal trapezoidal waveform shown in Fig. 10(b) is obtained for a particular load power such that $V_{OUT} = N_{DCX} V_{IN}$. The output voltage is higher than $N_{DCX} V_{IN}$ under light load and lower than $N_{DCX} V_{IN}$ under

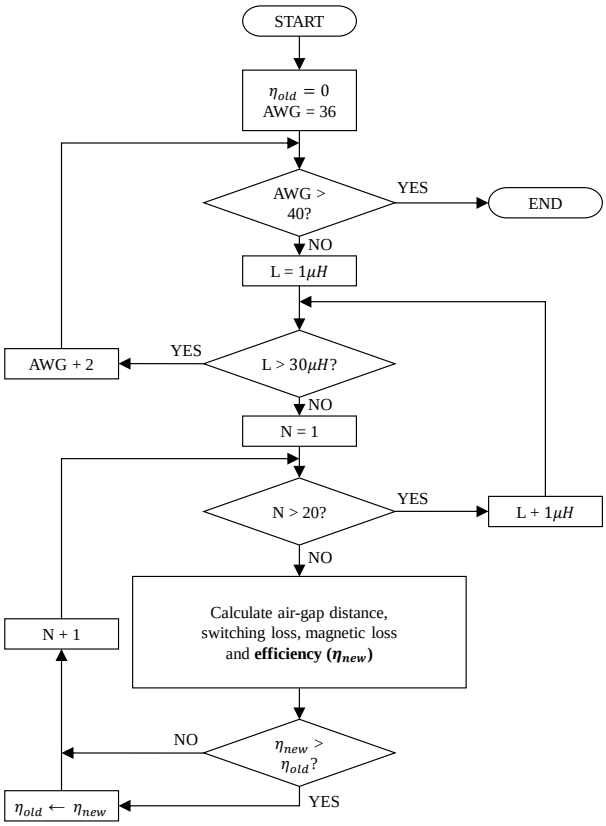

Fig. 8. Flowchart of magnetics optimization

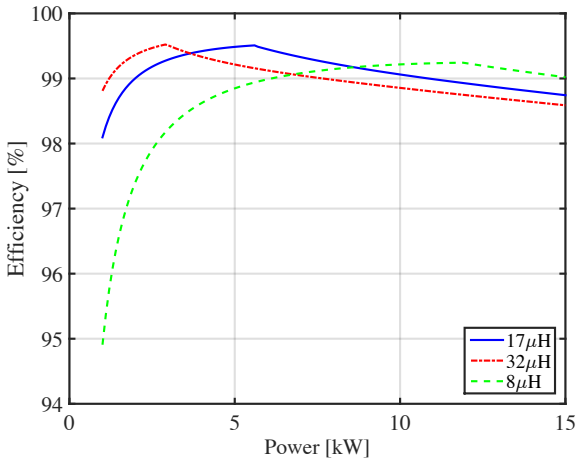

Fig. 9. Predicted boost module efficiency with 8 µH, 17 µH, and 32 µH, as a function of power processed by the boost module

heavy load, with corresponding current waveforms are shown in 10(a) and (c), respectively.

The simplified steady state DCX model is based on transformer current waveform shown in Fig. 11 and several assumptions:

- Dead-time between low-side and high-side MOSFET gate signal is zero.
- Resonant transitions of tank inductor and MOSFET output capacitance (C_{OSS}) are neglected.

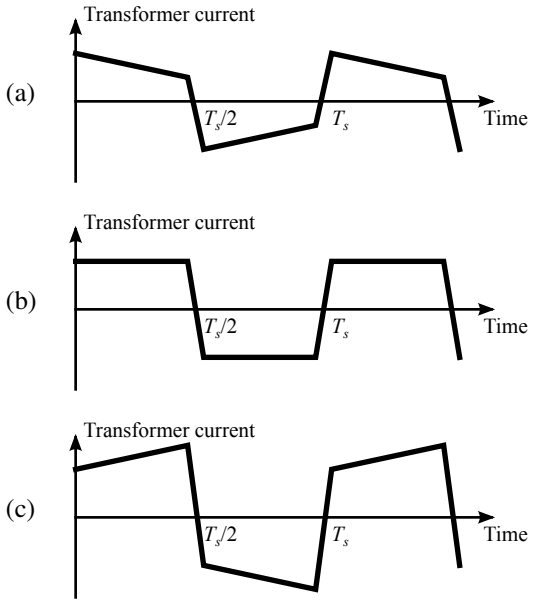

Fig. 10. DCX transformer current under: (a) light load condition; (b) optimized load condition; (c) heavy load condition

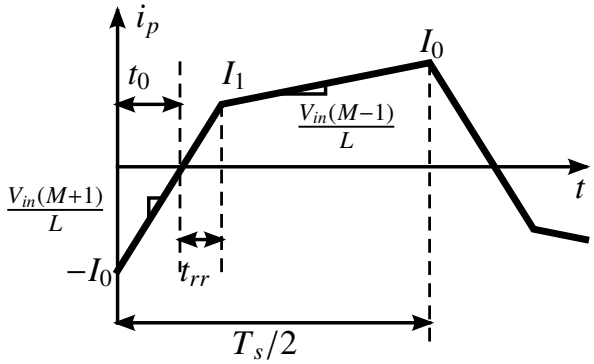

Fig. 11. Detailed DCX transformer current waveform, which is used in the simplified DCX model

- Output capacitance is fairly large so that output capacitor voltage can be considered constant.
- Average transformer current is zero.
- Magnetizing current of transformer is neglected.

The DCX voltage ratio M in Fig. 11 is defined as:

$$M = \frac{V_{out}}{N_{DCX} V_{in}} \tag{6}$$

As shown in [13], a simplified model to calculate the accurate reverse recovery time t_{rr} is:

$$t_{rr} = \tau \cdot \left(1 - e^{-\frac{t_0 + t_{rr}}{\tau}}\right) \tag{7}$$

where τ is the body diode minority-carrier life-time. The relationship between I_0 and I_1 with t_0 and t_1 can be expressed as:

$$I_0 = t_0 \cdot \frac{V_{in}\,(M+1)}{L_{tank}} \tag{8}$$

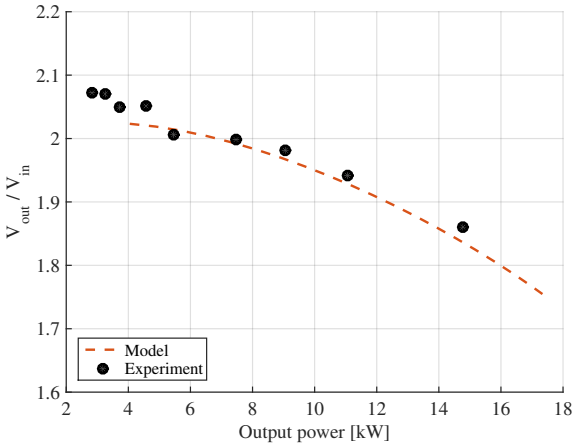

Fig. 12. Measured DCX voltage conversion ratio vs. simplified model at fixed 200 V input

and

$$I_1 = t_{rr} \cdot \frac{V_{in}\,(M+1)}{L_{tank}} \tag{9}$$

To guarantee that the transformer current waveform is continuous, it is required that

$$I_0 - I_1 = \frac{V_{in}\,(1-M)}{L_{tank}} \cdot \left(\frac{T_s}{2} - t_0 - t_{rr}\right) \tag{10}$$

The average transformer current should be equal to the output current reflected to the primary side:

$$Q = \frac{1}{2}t_0 I_0 - \frac{1}{2}t_{rr} I_1 + \frac{1}{2}\,(I_0 + I_1) \cdot \left(\frac{T_s}{2} - t_0 - t_{rr}\right) = N_{DCX} I_{out} \frac{T_s}{2} \tag{11}$$

Solution of equations (7) to (11) allows M to be found, and the DCX voltage conversion ratio is then obtained from (6).

Fig. 12 shows the calculated voltage conversion ratio compared to the experimental results. Notice that the measurements deviate from the model more significantly only at very light loads. This is because (7) is a simplified model, which is no longer valid at light loads. An accurate solution valid across all loads can be found in [13]. Nevertheless, from Fig. 12, it can be observed that the simplified model is very accurate for $P_{out} \geq 20\%P_{max}$. Once t_0, t_{rr}, I_0, and I_1 are solved, the actual transformer current waveform is known, and various loss components can be calculated.

Based on the simplified steady state model for DCX, the optimized tank inductance can be found at the given operating point. At the 210 V input / 650 Vbus output with 15 kW system power, DCX processes 9.7 kW of system power. The DCX exhibits the best efficiency when the tank inductor current has trapezoidal shape, because the transformer rms current and inductor core loss are then minimized. Based on Eqs. (7) to (11), the optimized tank inductance is 2.7 µH.

V. Experimental Results

Based on the design summarized in Section IV, a 30 kW composite converter prototype has been built with the module specifications listed in Table I. Fig. 13 shows measured

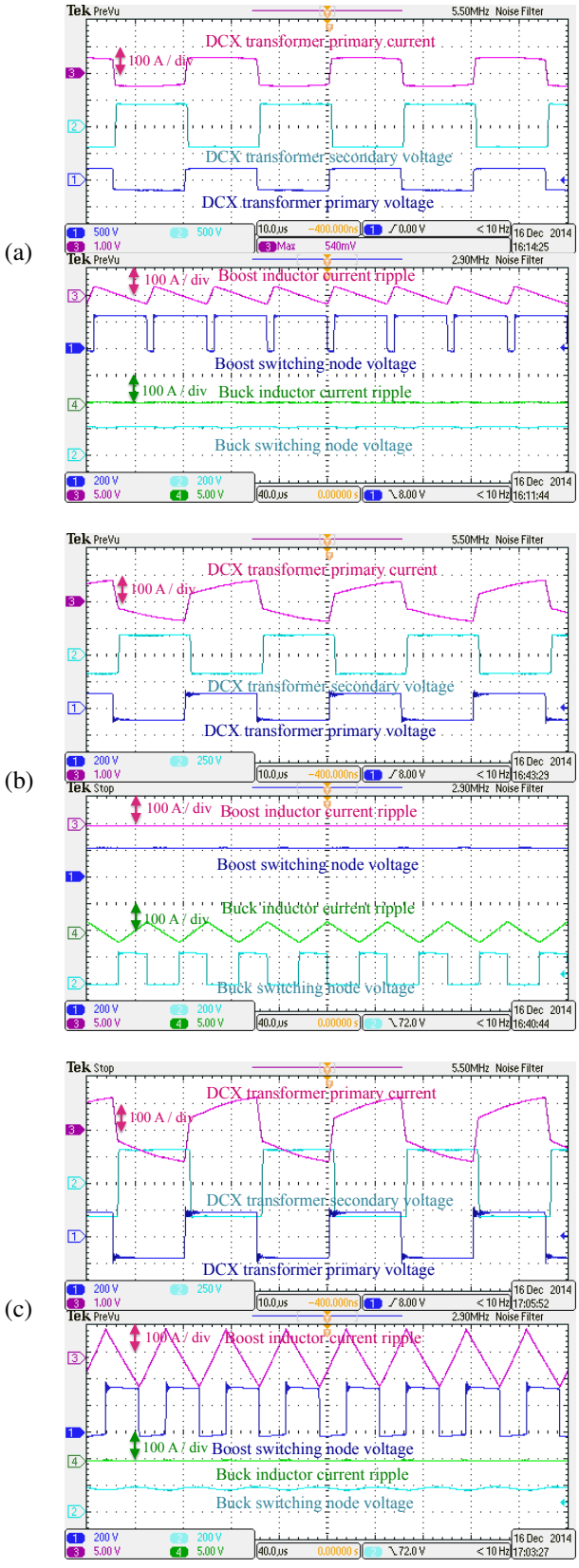

Fig. 13. Composite converter operating waveforms at three different power points. (a) DCX+Boost mode under 210 V input and 650 V bus voltage with 15 kW system power , (b) DCX+Buck mode under 220 V input and 400 V bus voltage with 10 kW system power (c) DCX+Boost mode under 170 V input and 650 V bus voltage with 30 kW system power

TABLE I
COMPOSITE CONVERTER DESIGN SUMMARY

Buck / Boost	
Number of MOSFET die	10
MOSFET	IPW65R041CFD2
Switching frequency	20 kHz
Inductance	17 µH for Boost, 32 µH for Buck
Inductor core material	Amorphous alloy
DCX	
Number of MOSFET die	28
MOSFET	IPW65R041CFD2
Switching frequency	33 kHz
Tank inductance	2.7 µH
Transformer turns ratio	6:12
Transformer core material	Ferrite

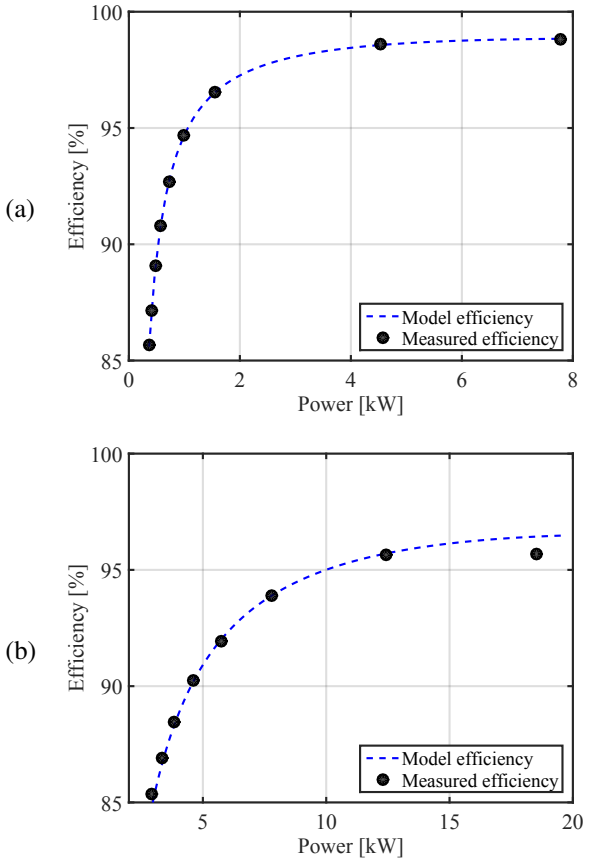

Fig. 14. Comparison of the boost module model-predicted and measured efficiency. (a) 150 V input and 200 V output voltage , (b) 200 V input and 400 V output voltage

waveforms of DCX tank inductor current and switching node voltages, and inductor currents and switching node voltages of the boost and buck modules, respectively, at three different operating points. At the operating point where the optimization objective is specified (Fig. 13(a)), the DCX operates with minimum RMS currents (trapezoidal current waveshape) and with zero-voltage switching of both bridges. The buck module is in pass through mode (not switching at all), while the boost module step-up ratio is small, and inductor current ripple is

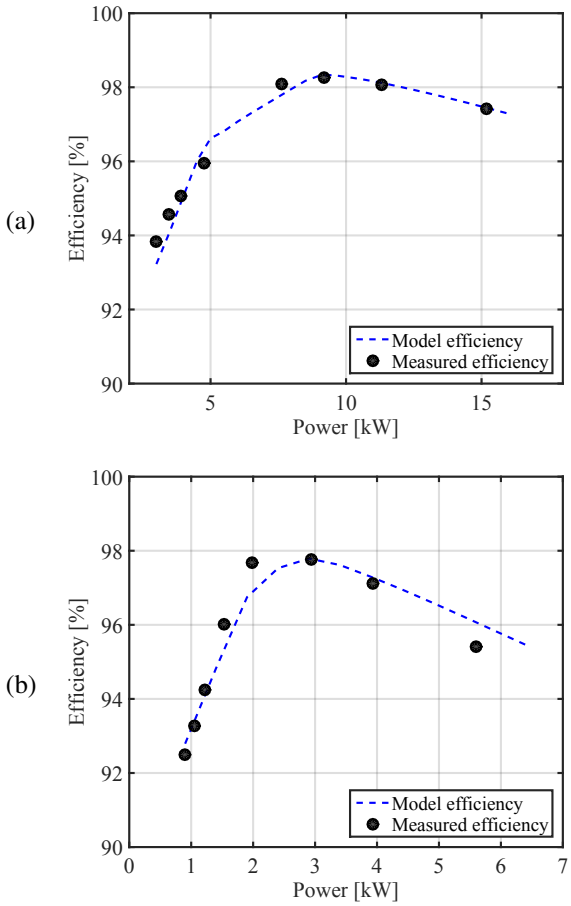

Fig. 15. Comparison of the DCX model-predicted and measured efficiency. (a) 200 V input, (b) 100 V input

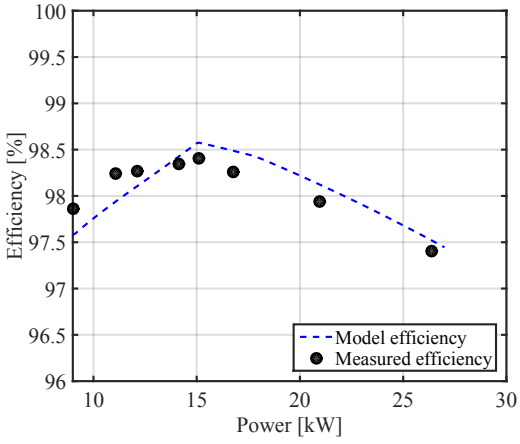

Fig. 16. Comparison of the complete composite converter model-predicted and measured efficiency at 210 V input and 650 V bus voltage.

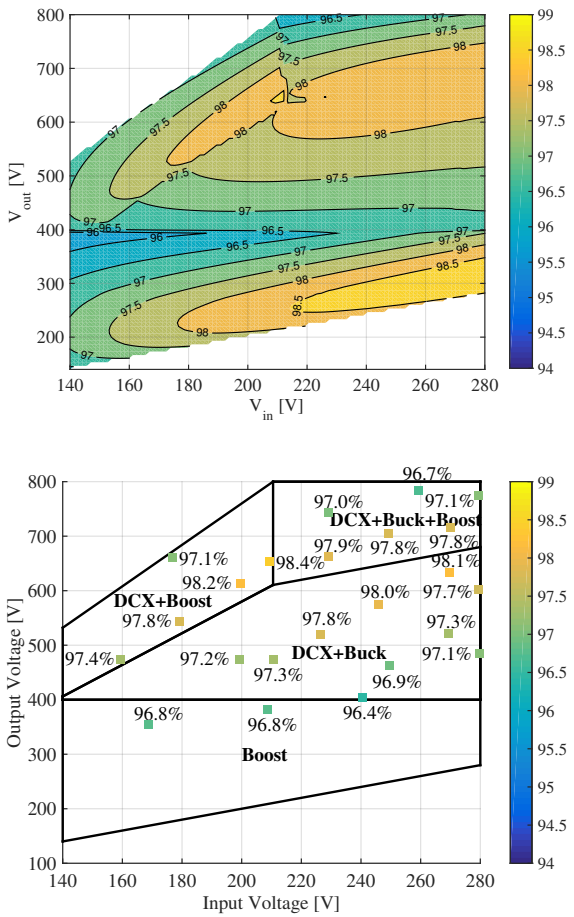

Fig. 17. Complete composite converter model-predicted and measured efficiency at different input / output voltages in different mode under 15 kW fixed power. (a) Comprehensive loss model efficiency , (b) Measured efficiency

such that zero-voltage switching is achieved, resulting in very high module and overall composite converter efficiencies.

Based on the comprehensive loss model, losses and efficiency of the composite converter are calculated over a wide operating range. Fig. 14 shows a comparison of the model-predicted efficiency and measured efficiency for the boost module at 150 V input, 200 V output, and for 200 V input, 400 V output, respectively. Also, a comparison of the model-predicted DCX efficiency and measured DCX efficiency under 200 V input and 100 V input are shown in Fig. 15. Since the duty cycle of the DCX is always 50%, the DCX output voltage is higher than the input voltage by N_{DCX}. One may note excellent matching between model predictions and measured efficiency results for the modules. The loss model of the composite converter combines the module loss models. The resulting model-predicted and measured efficiencies under 210 V input and 650 V bus voltage are shown in Fig. 16. At this operating point, the buck module operates in pass-through mode, while the boost module and the DCX are switching. It can again be observed that the model predictions match the measured results very well, and that a peak efficiency of 98.5 % is indeed achieved at 50% power level, as desired. Fig. 17 shows the comprehensive loss model efficiency and the measured efficiency under fixed 15 kW system power in the output voltage versus input voltage plane, demonstrating high efficiency performance in different operating modes. The measured efficiency shows an excellent agreement with obtained efficiency using the loss model.

VI. Conclusions

In this paper, design optimization of a 30 kW boost composite dc-dc converter is described based on a comprehensive loss model. The loss model is verified by experiments. Based on the optimal design, the laboratory prototype of the 30 kW composite converter demonstrates 98.5% peak efficiency at 50% power and maintains high efficiency over a wide operating range.

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