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Executive Summary

The objective of this project is to investigate a new surface passivation technique, valence-mending passivation, for its applications in crystalline-Si solar cells to achieve significant efficiency improvement and cost reduction. As the enabling technique, the project includes the development of chemical vapor deposition recipes to passivate textured Si(100) and multicrystalline-Si surfaces by sulfur and the characterization of the passivated Si surfaces, including thermal stability, Schottky barrier height, contact resistance and surface recombination. One important application is to replace the Ag finger electrode in Si cells with Al to reduce cost, by ~\$0.1/W_p, and allow terawatt-scale deployment of crystalline-Si solar cells. These all-Al Si cells require a low-temperature metallization process for the Al electrode, to be compatible with valence-mending passivation and to prevent Al diffusion into n-type Si. Another application is to explore valence-mending passivation of grain boundaries in multicrystalline Si by diffusing sulfur into grain boundaries, to reduce the efficiency gas between monocrystalline-Si solar cells and multicrystalline-Si cells.

The major accomplishments of this project include:

1) Demonstration of chemical vapor deposition processes for valence-mending passivation of both monocrystalline Si(100) and multicrystalline Si surfaces. Record Schottky barriers have been demonstrated, with the new record-low barrier of less than 0.08 eV between Al and sulfur-passivated n-type Si(100) and the new record-high barrier of 1.14 eV between Al and sulfur-passivated p-type Si(100). On the textured p-type monocrystalline Si(100) surface, the highest barrier with Al is 0.85 eV by valence-mending passivation.
2) Demonstration of a low-temperature metallization process for Al in crystalline-Si solar cells. The new metallization process is based on electroplating of Al in a room-temperature ionic liquid. The resistivity of the electroplated Al is ~7×10^{-6} Ω-cm, similar to that of screen-printed Ag.
3) Demonstration of two all-Al, Ag-free Si solar cells, with an electroplated Al front electrode and a screen-printed Al back electrode. One cell is an industrial p-type front-emitter cell, and the other is an n-type back-emitter cell. The efficiency of the p-type cell is close to 15%. This is an industrial cell and its efficiency is capped at ~18%.
4) Demonstration of grain boundary passivation by both hydrogen and sulfur using hydrogen sulfide (H_2S). When the new grain boundary passivation is combined with Al_2O_3 surface passivation and post-annealing, the minority carrier lifetime in the p-type multicrystalline Si samples shows a significant improvement up to 68 fold.
5) In a side project, a simple green process is developed which is capable of recycling over 90% of the Si material in end-of-life crystalline-Si solar cells. The recycled Si meets the specifications for solar-grade Si and can be used as a new poly-Si feedstock for ingot growth.

Comparison of Proposed versus Actual Project Goals

The following table summarizes the project's proposed goals versus actual progress for each task. Deviations between an Initial negotiated deliverables / milestones and an actual deliverable / milestone are discussed in the "Deliverable / Milestone Deviations" section of the Technical Narrative.

Task #	Task description	Initial Negotiated Deliverable / Milestone	Actual Deliverable / Milestone
1	Passivation of mono-Si(100)	Schottky barrier <0.1 eV; thermal stability >300°C	Schottky barrier <0.08 eV; thermal stability >500°C
2	Baseline n-type crystalline-Si cell	Boron diffusion 0.5–1 μm depth; 10^{19} cm^{-3} surface concentration	0.5 μm junction depth; 10^{19} cm^{-3} surface concentration
3	Low-temperature Al paste	Al paste <400°C firing temperature; <1.5× resistivity	~550°C firing temperature; ~2× resistivity
4	Baseline point-back contact n-type cell	Target cell efficiency ~15%	Postponed to Phase II
5	Grain boundary passivation in multi-Si	Improved minority carrier lifetime >10%	Postponed to Phase II
6	Passivation of textured and multi-Si	Schottky barrier <0.1 eV; thermal stability >300°C	Schottky barrier <0.1 eV; thermal stability ~300°C
7	Improved baseline n-type Si cell	Target cell efficiency >15% with vacuum-deposited	Actual cell efficiency 15.3%
8	Improved low-temperature Al paste	Al paste <400°C firing temperature; <1.5× resistivity	Electroplated Al with firing temp. ~200°C; resistivity ~0.5×
9	All-Al Si cell with valence-mending passivation	Target cell efficiency >15%	All-Al Si cell based on industrial cell 14.8%
10	Point-back contact Si cell	Target cell efficiency >15%	Actual cell efficiency 13.4%
11	Improved grain boundary passivation	Improved minority carrier lifetime >10%	Best improved carrier lifetime ~6800%

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Project Objective

We plan in this project to integrate a new surface passivation technique, valence-mending passivation, into crystalline-Si solar cells for significant efficiency improvement and cost reduction using an ultra high-vacuum chemical vapor deposition system (CVD). It targets some of the most critical problems in crystalline-Si solar cells. The most fundamental advances of this project lie in the development of CVD-based valence-mending passivation, which is expected to enable high efficiency, low cost and terawatt-scale deployment of crystalline-Si solar cells. The original objectives of this project include:

1) Development of CVD recipes to passivate textured Si(100) and multicrystalline-Si surfaces;

2) Characterization of passivated Si surfaces, including thermal stability, Schottky barrier height, contact resistance and surface recombination;

3) Development of an n-type base p-type emitter crystalline-Si solar cell;

4) Development of a low-temperature Al paste to be compatible with valence-mending passivation;

5) Integration of valence-mending passivation with the n-type base crystalline-Si solar cell to produce an all-Al Si solar cell;

6) Development of a point back contact, n-type base, all-Al crystalline-Si cell

with passivated back contact; and

7) Development of diffusion recipes for valence-mending passivation of grain boundaries in multicrystalline-Si.

The most significant deliverable of this project is a new crystalline-Si solar cell with an n-type base and a p-type emitter, and with Al as both the front and back electrodes. The efficiency target by the end of this project (in three years) is 15% on monocrystalline-Si, but the ultimate efficiency target (in five years) for this cell is 20% on monocrystalline-Si. Other deliverables of this project include diffusion recipes for valence-mending passivation of grain boundaries to increase the efficiency of multicrystalline-Si solar cells, a low-temperature Al paste fired below 400°C and a new point back contact crystalline-Si solar cell with all-Al electrodes.

Background

We pioneered valence-mending passivation over the last 10 years. The concept is to deposit a single atomic layer of a suitable element on a crystalline semiconductor surface, in order to terminate dangling bonds and thus minimize surface states associated with dangling bonds. For the Si(100) surface, valence-mending elements include group VI sulfur and selenium. For the Si(111) surface, valence-mending elements are group VII fluorine and chlorine. Our prior results demonstrate a high potential for this approach to solve several critical problems in crystalline-Si solar cells:

1) It enables Earth-abundant Al to replace Ag as the electrode to the n-side of the cell;

2) It allows a new grain boundary passivation approach immune to light-induced degradation;

3) It allows a much smaller metal contact area to reduce recombination through contacts; and

4) It makes selective emitter easier to fabricate, as it naturally forms selective emitter.

The prior results were obtained through two National Science Foundation grants of the PI. The most noticeable of these results as related to photovoltaic applications are:

1) Record-low Schottky barrier (0.08 eV) between Al on n-type Si(100), and

2) Suppression of interfacial reactions (up to 400°C) between metal and Si.

The record-low Schottky barrier allows a significant reduction in contact resistance between Al and n-type Si, allowing Al to replace Ag as the electrode to n-side of the cell. The low contact resistance also allows a much smaller contact area to minimize recombination through contacts. The thermal stability of the metal/Si interface by valence-mending passivation allows its practical applications in crystalline-Si solar cells, if the process temperature after passivation stays below 400°C.

The unprecedented results mentioned above were obtained through a molecular beam epitaxy (MBE) process for passivation. We have investigated solution processes for valence mending passivation, but the thermal stability, ambient stability and surface recombination of solution-passivated samples are inferior to MBE-passivated samples. The poor quality of solution passivation necessitates CVD-based processes for low-cost, high-throughput and high-quality passivation.

This project addresses several metrics parameters for crystalline-Si solar cells. The most important parameter is terawatt-scale deployment of crystalline-Si solar cells. Ag, as the finger electrode in crystalline-Si solar cells, is one of the rarer materials on this planet and substitution of Ag with Al enables crystalline-Si solar cells to become a major source of energy in the future. The second key parameter is cell cost, as the price of Ag has been fluctuating between $15–45/oz since 2010. Al is much lower cost as an alternative than Ag and should reduce the module cost by ~$0.1/$W_p$. There should also be efficiency gains in crystalline-Si solar cells by either the low contact resistance, small contact area or grain boundary passivation.

Significant Accomplishments

Ⅰ. Surface Passivation (Task 1.0 & Task 6.0)

1.1 Task 1.0 Surface passivation for monocrystalline-Si

In the course of performing surface passivation for monocrystalline-Si(100) surface, we carried out a systematic study to optimize the in-situ cleaning and passivation conditions using an ultrahigh vacuum CVD system. Two dozen experiments were completed to identify the proper cleaning and passivation conditions including:

1) The start temperature of HCl for cleaning: 700°C, 750°C and 800°C;
2) The stop temperature of HCl for cleaning: 200°C, 300°C, 400°C, 500°C and 600°C;
3) The start temperature of H_2S for passivation: 500°C, 600°C, 700°C and 750°C;
4) The stop temperature for H_2: 150°C, 300°C, 500°C and 700°C; and
5) The effect of CVD base vacuum on passivation quality: 2×10^{-8} torr and 8×10^{-8} torr.

All the experiments were carried out on p-type Si(100) wafers of ~2×10^{16} cm^{-3} boron doping. Al contacts were e-beam evaporated onto valence-mended samples through a shadow mask. Current-voltage, capacitance-voltage and activation energy measurements were performed to determine the Schottky barrier height. As a quick indicator, we monitored the reverse saturation current of the Al/valence-mended p-type Si junctions, as better-quality passivation leads to a higher Schottky barrier and thus a smaller reverse saturation current. Once the cleaning and passivation conditions were optimized, different types of Si(100) wafers were used for passivation, including n-type Si(100) wafers of ~1×10^{16} cm^{-3} phosphorous doping and p-type Si(100) wafers of ~1×10^{17} cm^{-3} boron doping, to demonstrate a record-low Schottky barrier on valence-mended n-type Si. Different metals such as Ni were also deposited on valence-mended samples to study the thermal stability of the passivation using SEM, TEM and XRD.

1.1.1 Cleaning and passivation conditions

p-type Si(100) wafers were cleaned in 2% HF for 30 s and were subsequently dried with nitrogen. When loaded into the CVD reactor, the wafer was preheated to 300°C for a few minutes in a flow of high-purity nitrogen (99.9999%) to drive out moisture. The CVD reactor was then pumped down to a base pressure of 2×10^{-8} torr. At that time the wafer was heated to 700–800°C and HCl and H_2 were introduced into the reactor for 20 min for in-situ wafer cleaning. The wafer was then cooled down to a preset temperature while HCl and H_2 continued to flow. At the preset temperature, H_2S was introduced into the reactor for passivation. All the three gases continued to flow, while the wafer temperature kept dropping. HCl was stopped first at a preset temperature, with H_2 and H_2S flowing. At 150°C, H_2 and H_2S were cut. The wafer temperature further dropped to below 100°C and the sample was unloaded. The following is a summary of the main conclusions from the cleaning and passivation experiments:

1) HCl plays a critical role in removing impurities from the Si surface and keeping the surface clean during passivation. On the other hand, Cl with high chemical reactivity can etch Si and create new dangling bonds. Therefore, there is an optimal temperature range for HCl cleaning. Fig. 1(a) shows the current-voltage characteristics of Al/valence-mended p-type Si(100) junctions at different HCl start temperature. When HCl is

introduced at 750°C, the lowest reverse saturation current of ~3.5×10^{-7} A/cm^2 was obtained. This reverse saturation current is lower than what we reported previously by solution passivation, suggesting that the CVD passivation has a much better quality than solution passivation. Fig. 1(b) shows the corresponding reverse saturation current as a function of HCl start temperature. 750°C provides a much lower reverse saturation current than 700°C and 800°C.

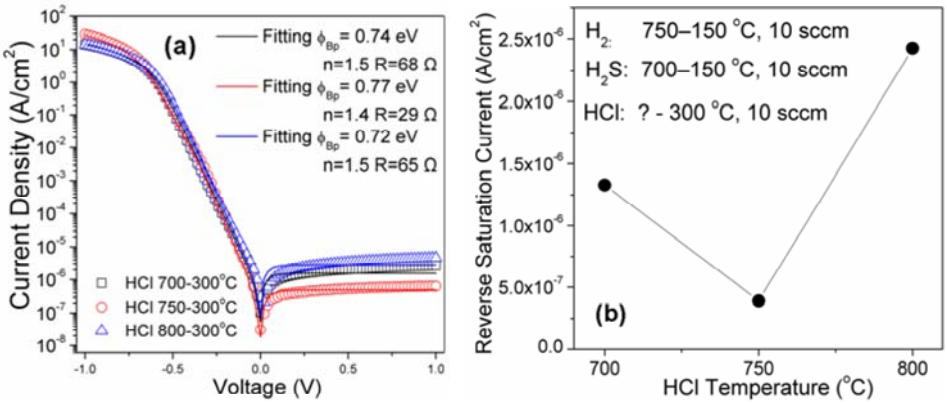


Figure 1. (a) Current-voltage characteristics of Al/valence-mended p-type Si junctions with HCl introduced at different temperatures for Si surface cleaning. (b) Reverse saturation current as a function of HCl start temperature.

Fig. 2(a) shows the current-voltage characteristics of Al/valence-mended p-type Si junctions at different HCl stop temperatures (200, 300, 400, 500 and 600°C). Fig. 2(b) shows the reverse saturation current as a function of HCl stop temperature. Obviously, cutting HCl at 300°C gives the best results. This may be attributed to the dual effect of HCl. On one hand, HCl is indispensable in removing surface impurities and keeping surface clean. On the other hand, Cl can etch Si and create new dangling bonds on the surface. It may also replace sulfur atoms which are already bonded to the dangling bonds. In this case Cl should be stopped as soon as sulfur has terminated all the dangling bonds.

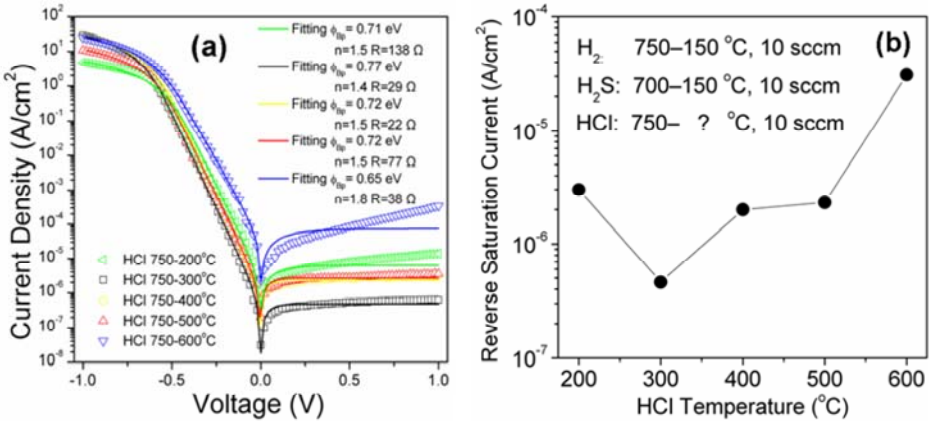


Figure 2. (a) Current-voltage characteristics of Al/valence-mended p-type Si junctions with HCl stopped at different temperatures. (b) Reverse saturation current as a function of HCl stop temperature.

2) H_2S as the source of sulfur dominates the passivation quality. Fig. 3 shows the

current-voltage characteristics of Al/valence-mended p-type Si(100) junctions as a function of H_2S start temperature (500, 600, 700 and 750°C), along with the corresponding reverse saturation current as a function of H_2S start temperature. It can be seen that introducing H_2S at 700°C gives the lowest reverse saturation current, and thus the highest barrier height. Since sulfur atoms bonded to the Si surface are unstable at high temperatures, we keep H_2S flowing until 150°C.

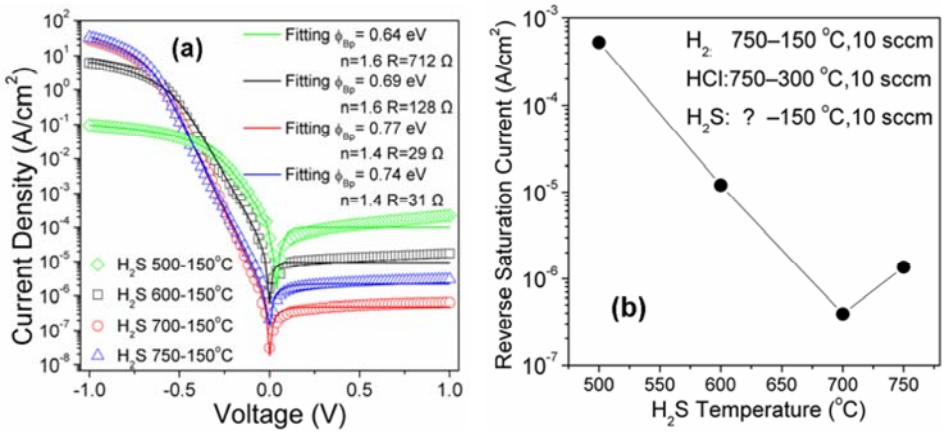


Figure 3. (a) Current-voltage characteristics of Al/valence-mended p-type Si junctions with H_2S introduced at different temperatures. (b) Reverse saturation current as a function of H_2S start temperature.

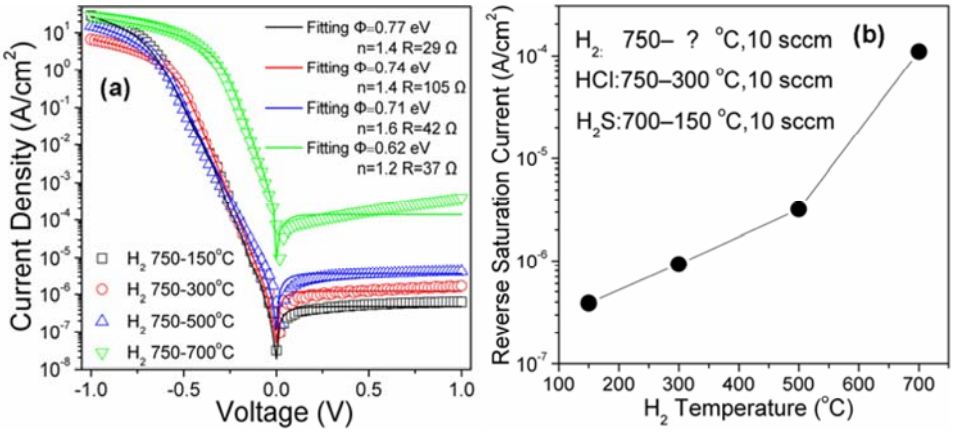


Figure 4. (a) Current-voltage characteristics of Al/valence-mended p-type Si junctions with H_2 stopped at different temperatures. (b) Reverse saturation current as a function of H_2 stop temperature.

3) In the cleaning and passivation process, the role of H_2 is multiple. It is used to remove native oxide from the Si surface. It can keep the Si surface clean and serve as a valence-mending passivant for single dangling bonds on Si surface. It is also a carrier gas for HCl and H_2S. Shown in Fig. 4(a) is the current-voltage characteristics for Al/valence-mended p-type Si(100) junctions with H_2 stopped at 150, 300, 500 and 700°C. Fig. 4(b) shows the corresponding reverse saturation current as a function of H_2 stop temperature. The reverse saturation current decreases with lower H_2 stop temperature, and cutting H_2 at 150°C gives the lowest reverse saturation current.

4) The effect of CVD base pressure on passivation quality is shown in Fig. 5, where the

current-voltage characteristics of Al/valence-mended p-type Si junctions with different base pressures: 2×10^{-8} torr and 8×10^{-8} torr, are given. The base pressure is determined by the pumping time of the CVD reactor. With overnight pumping by a turbo molecular pump, the pressure in the reactor goes down to 2×10^{-8} torr, while ~5 hr pumping by the turbo only reaches 8×10^{-8} torr. From Fig. 5, a lower base pressure works better.

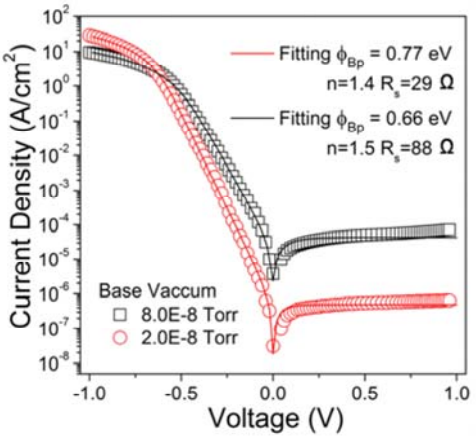


Figure 5. Current-voltage characteristics of Al/valence-mended p-type Si junctions with different base pressures.

1.1.2 Schottky barrier height measurement

Current-voltage, capacitance-voltage and activation energy measurements were performed to determine the Schottky barrier height of Al on valence-mended p-type and n-type Si(100) surfaces.

The capacitance-voltage characteristics of an Al/valence-mended p-type Si junction at frequency of 1 MHz is shown in Fig. 6. The extracted doping concentration from the slope is ~1.8×10^{16} cm^{-3}, in agreement with the wafer specification (2×10^{16} cm^{-3}). The barrier height from capacitance-voltage measurements is ~1.33 eV without considering image-force lowering. With image-force correction, the barrier height becomes 1.14 eV, which is a new record for Schottky barrier height on p-type Si(100).

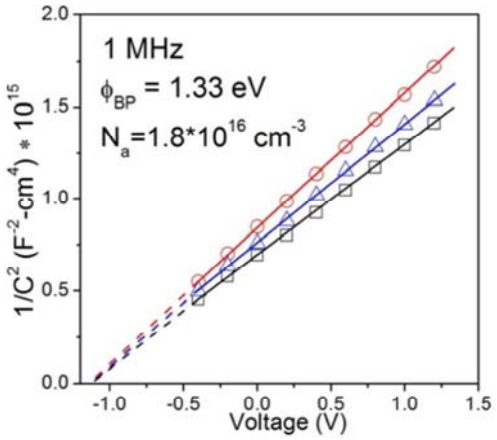


Figure 6. Capacitance-voltage measurements on an Al/valence-mended p-type Si junction.

A low Schottky barrier is expected between Al and n-type Si(100) with good-quality passivation. Fig. 7 shows the current-voltage characteristics of two back-to-back

Al/valence-mended n-type Si(100) junctions at different temperatures down to 100 K. A simple-minded fitting of the thermionic-emission model to the low-temperature data at 100 K suggests a barrier height no more than 0.087 eV, along with a series resistance of 23 Ω. This near-record Schottky barrier indicates good-quality passivation by CVD.

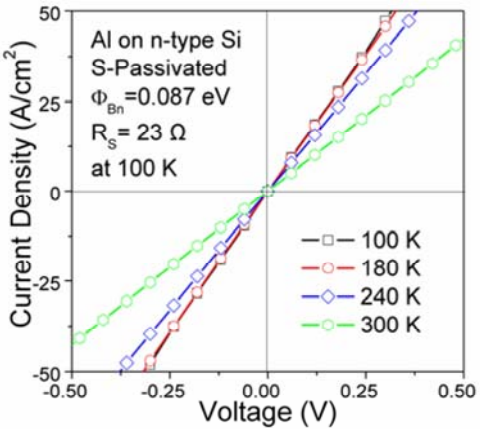


Figure 7. Current−voltage characteristics of two back-to-back Al/valence-mended n-type Si junctions at different temperatures.

The activation-energy measurements of an Al/valence-mended n-type Si junction under different bias were carried out to verify the low Schottky barrier. The temperature range was from 77 K to 300 K. As shown in Fig. 8, the negative slopes indicate extremely low barriers, again confirming good-quality passivation.

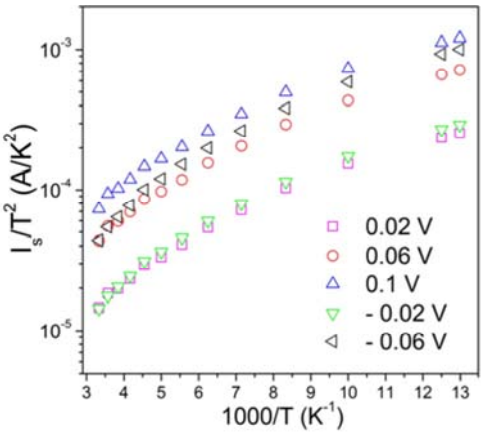


Figure 8. Activation-energy measurements of an Al/valence-mended n-type Si junction at different bias.

1.1.3 Metal deposition conditions

We upgraded the Lesker e-beam evaporator in Center for Solid-State Electronics Research with ASU funds, which primarily benefit this project. The upgrade includes a new substrate heater for the e-beam evaporator to allow sample heating before metal deposition. When valence-mended wafers are transferred from the CVD reactor to the e-beam evaporator, the wafer surface is covered with adsorbates such as CO_2, H_2O or O_2. Fig. 9 is a cross-sectional TEM image of an Al/Si interface with the valence-mended Si wafer exposed to the ambient. ~1.5 nm of adsorbate is visible. This interfacial adsorbate layer affects the behavior of the metal/passivated Si interface and makes the

barrier height measurements inaccurate. Our past experience suggests that desorption of the adsorbates takes place at 100–200°C in vacuum. With the upgrade in our e-beam evaporator, we investigated the effect of metal deposition temperature on reverse saturation current of the Al/valence-mended p-type Si junctions.

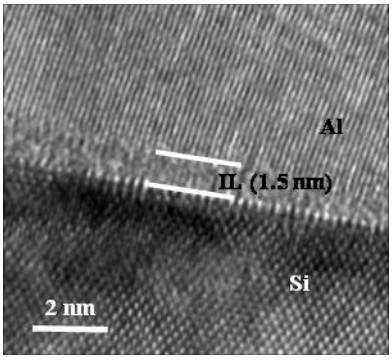


Figure 9. Cross-sectional TEM image of an Al/Si interface with the valence-mended Si wafer exposed to the ambient. The interfacial layer of 1.5 nm is due to adsorbates.

The e-beam chamber was first pumped to a base pressure of 3×10^{-6} torr, and then the substrate was heated to 85°C, 150°C, 220°C and 270°C, respectively, with a temperature ramp rate of 10°C/min. Al deposition began when the substrate temperature became stable. Fig. 10(a) shows the current-voltage characteristics of the Al/valence-mended p-type Si junctions with different metal deposition temperatures. The corresponding reverse saturation current as a function of metal deposition temperature is shown in Fig. 10(b). The room temperature sample gives the lowest reverse saturation current. At 150°C, the reverse saturation current has a small dip and the ideality factor becomes 1.2. This is the smallest ideality factor for all the samples in Fig. 10. The reverse saturation current at 150°C is higher than that at room temperature. The reverse saturation current increases significantly at 270°C, suggesting possible damage to the passivation layer at 270°C.

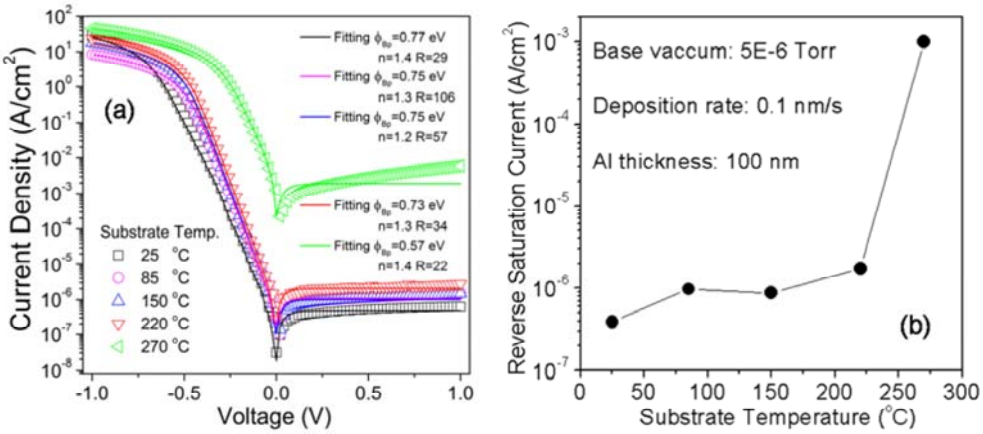


Figure 10. (a) Current-voltage characteristics for Al/valence-mended p-type Si junctions with Al deposited at different temperatures. (b) Reverse saturation current as a function of Al deposition temperature.

1.1.4 Thermal stability of metal/valence-mended Si interface

The thermal stability of valence-mending passivation upon annealing determines its

suitability for device applications. We carried out a series of experiment to investigate the thermal stability of the passivation using the Ni/valence-mended Si interface. A 100-nm Ni film was deposited on a valence-mended n-type Si sample by e-beam evaporation. Thermal annealing at 300°C for 30 s was carried out on a hotplate in air. Normally, Ni reacts with Si at ~200°C resulting in Ni_2Si. Our prior work demonstrates that good-quality valence-mending passivation can delay Ni silicidation to a much higher temperature, ~400°C. In order to check the quality of CVD passivation, we employed SEM, XRD and TEM to examine the structure of the Ni/valence-mended Si interface before and after annealing. We also examined the thermal stability of the Al/valence-mended n-type Si junction by current-voltage measurements.

1) SEM characterization

Before annealing, there is a clear boundary between Ni and Si as shown in Fig. 11(a) and (b). Fig. 11(c) and (d) show the structure of the Ni/valence-mended Si interface after annealing at 300°C for 30 s. The clear boundary between Ni and Si remains intact, and no Ni_2Si or NiSi is observed at the Ni/valence-mended Si interface. The stable interface upon annealing demonstrates the good quality of the CVD passivation.

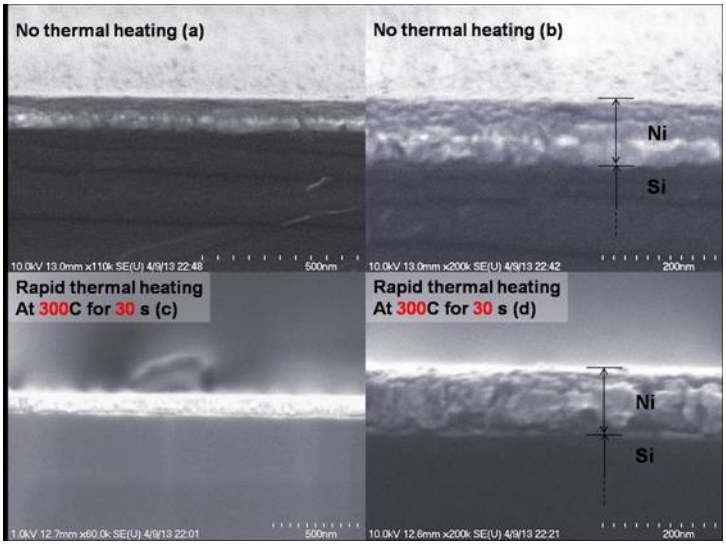


Figure 11. Cross-sectional SEM images of Ni/valence-mended Si interface before and after annealing. (a) and (b) Before annealing. (c) and (d) After annealing at 300°C for 30 s.

2) TEM characterization

Fig. 12 shows cross-sectional TEM images of the Ni/valence-mended Si interface before and after annealing. An interfacial adsorbate layer of ~5 nm is visible before annealing in Fig. 12(a), which is in agreement with Fig. 9. After annealing at 300°C for 30 s, the interface remains largely intact and no Ni_2Si or NiSi is observed. That is, the thermal stability of CVD-based valence-mending passivation is at least 300°C. The insert in Fig. 12(b) zooms into the only region across the Ni/valence-mended Si(100) interface where a black spot is observed after annealing. This particular region may have poor-quality passivation and silicidation may just be starting. Further work is needed to obtain more uniform passivation quality.

3) XRD characterization

The crystal structure of the Ni film on valence-mended Si upon annealing was also studied using XRD. Fig. 13(a) shows the XRD pattern of the Ni film before and after annealing. They are similar, suggesting no silicidation of Ni. The standard JCPDS PDF card of Ni is also included for comparison. All the peaks are accounted as Ni peaks, not Ni_2Si or NiSi peaks. The XRD pattern of Ni_2Si is shown in Fig. 13(b). None of the Ni_2Si peaks is observed in Fig. 13(a), again indicating no silicidation between Ni and Si and thus good-quality passivation.

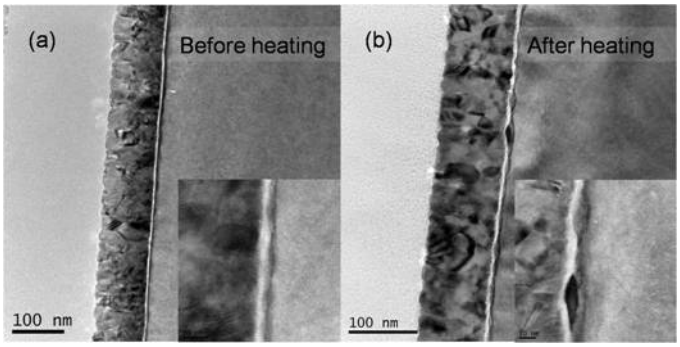


Figure 12. Cross-sectional TEM images of Ni/valence-mended Si interface: (a) before annealing and (b) after annealing at 300°C for 30 s. The interfacial layer of ~5 nm is due to adsorbates.

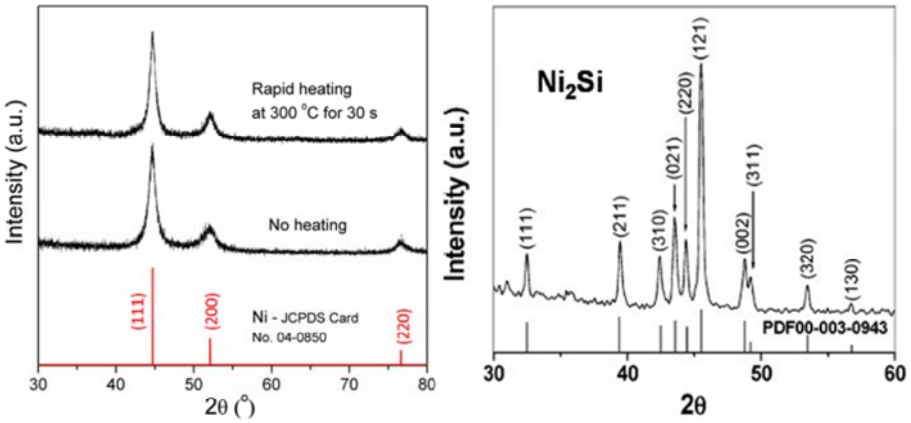


Figure 13. (a) XRD patterns of the Ni/valence-mended Si structure before and after annealing. (b) XRD pattern of Ni_2Si (Y. Song et al, Nano Letters 7 (2007) 965).

4) Current-voltage characterization

For the Al/valence-mended n-type Si junction that illustrates a near record-low Schottky barrier of 0.087 eV, we monitored its current-voltage characteristics upon annealing up to 500°C. The annealing was performed on a hotplate in air. As shown in Fig. 14, the ohmic current-voltage characteristics of the Al/valence-mended n-type Si(100) junction remains largely unchanged after 47 days. After annealing at 300°C, 350°C, 400°C, 450°C and even 500°C for 30 s, the current-voltage characteristics exhibits excellent thermal stability, i.e. remains linear. Both the long-term and thermal stability of CVD-based valence-mending passivation looks promising.

The thermal stability of Al/valence-mended p-type Si(100) junctions was also determined by monitoring their current-voltage behavior before and after annealing. Fig. 15 shows the current-voltage characteristics of Al/valence-mended p-type Si(100) junctions before and after annealing at 300°C for 30 s in air. Before annealing the

reverse current density at 0.5 V is 5.1×10^{-7} A/cm^2. After annealing it increases to 9.1×10^{-7} A/cm^2. The relatively-small change in reverse current density suggests a thermally-stable high Schottky barrier up to 300°C. The thermal stability of the Al/valence-mended Si(100) junctions is due to the suppressed chemical reactivity of the Si(100) surface by valence-mending passivation.

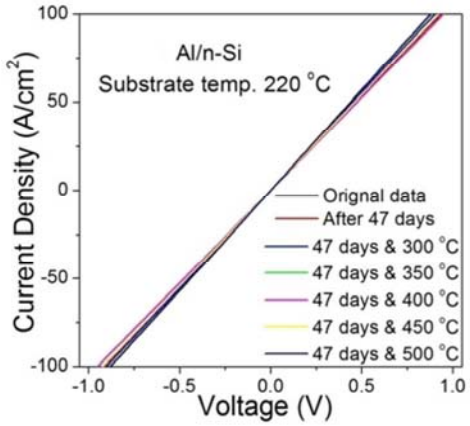


Figure 14. Long-term and thermal (300–500°C) stability of an Al/valence-mended n-type Si(100) junction by current-voltage characterization.

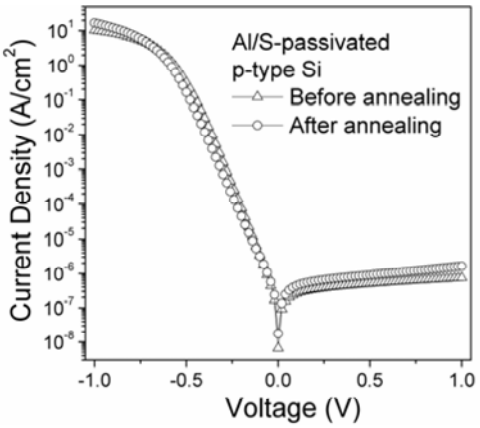


Figure 15. Current-voltage characteristics of Al/valence-mended p-type Si(100) junctions before and after annealing at 300°C for 30 s. The junctions are thermally stable to 300°C.

1.2 Task 6.0 Surface passivation for multicrystalline Si

1.2.1 Two-step passivation process

On a multicrystalline-Si surface, the orientation of the crystal grains is random, so a two-step passivation process has to be developed. The first step will passivate double-dangling-bond sites and the second step will passivate single-dangling-bond sites. As summarized earlier in this report, passivation of double-dangling-bond sites has been carried out. In this section of the report, we focus on the second step to passivate Si(111) surface with single-dangling-bond sites.

p-type Si(100) wafers of ~2×10^{16} cm^{-3} boron doping was textured to create Si(111) faces. The samples were first immersed into a 3% NaOH solution with 10% IPA at 80°C for 30 min. After texturing, the samples were placed in a 5% HCl solution to remove Na

ions. After a short dip in 2% HF, the sample was loaded into the CVD reactor though a load-lock. A SEM image for a textured Si surface is shown in Fig. 16. Fig. 17 shows the reflectance of Si samples with and without textured pyramids. After texturing, the sample shows a much lower reflectance.

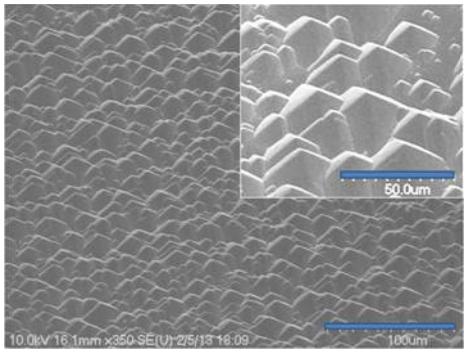


Figure 16. SEM image of a textured Si surface in a 3% NaOH solution with 10% IPA at 80°C for 30 min.

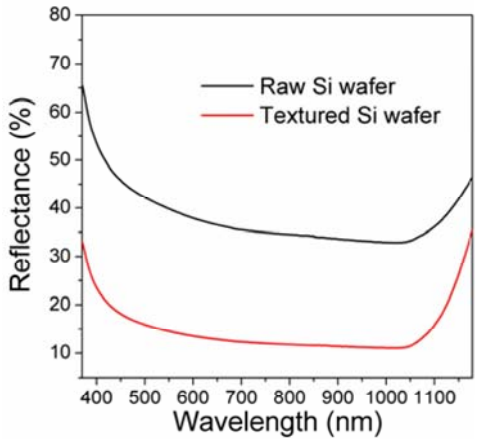


Figure 17. Reflectance of a Si(100) wafer and textured Si(100) wafer.

For the passivation of textured samples, the dangling bonds on Si(111) faces point perpendicular to the surface at one dangling bond per surface atom, which require Group VII atoms such as Cl to terminate. Therefore, the HCl flow in the CVD reactor plays an important role on passivation quality. Fig. 18 shows the current-voltage characteristics of an Al/valence-mended textured p-type Si junction. The sample was passivated using the same process for untextured monocrystalline-Si, in which the HCl starts at 750°C and stops at 300°C. The Schottky barrier height calculated from the lowest reverse saturation current in Fig. 18 is 0.76 eV, similar to that of Si(100) sample. However, the uniformity of the sample is poor and the reverse current does not saturate, indicating a large leakage current. The poor uniformity may come from a poor metal contact due to the nonplanar surface. There are several remedies for the poor metal contact, such as increasing the Al thickness, reducing the deposition rate and heating the substrate during Al deposition. The leakage current will be discussed later.

Fig. 19(a) shows the activation-energy measurements on an Al/valence-mended textured p-type Si junction between 23–120°C. Fig. 19(b) is a plot of $\ln(I/T^2)$ vs 1/T to determine the barrier height. At forward bias of 0.2 V, the barrier height is 0.76 eV,

which agrees with the current-voltage measurement in Fig. 18. The barrier height under reverse bias of –0.2 V is 0.68 eV. The lower value can be attributed to image-force lowering when the junction is under reverse bias.

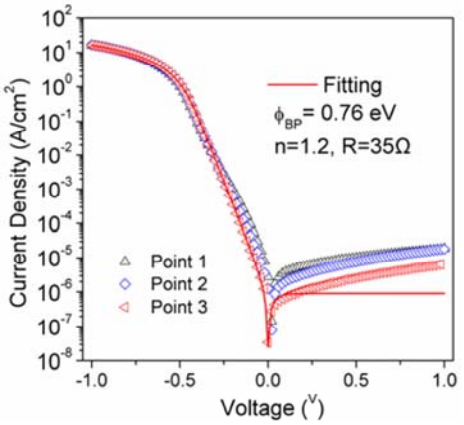


Figure 18. Current-voltage characteristics of an Al/valence-mended textured p-type Si junction.

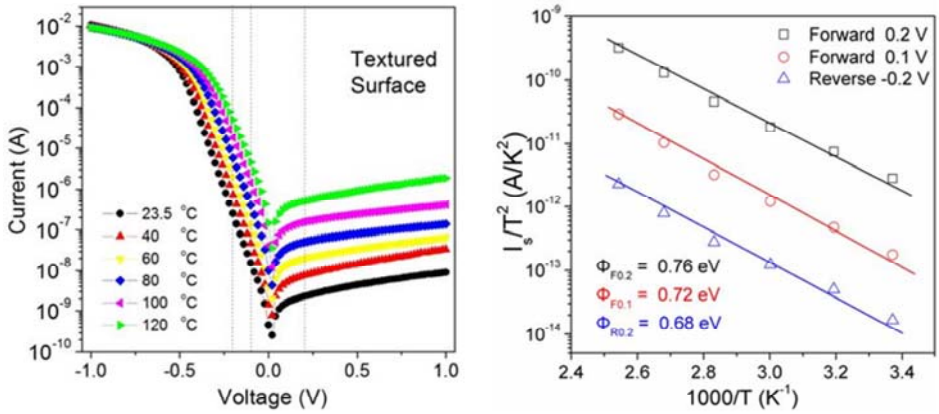


Figure 19. (a) Current-voltage characteristics of an Al/valence-mended textured p-type Si junction at different temperatures. (b) Activation-energy plot to determine the barrier height at bias of –0.2, 0.1 and 0.2 V.

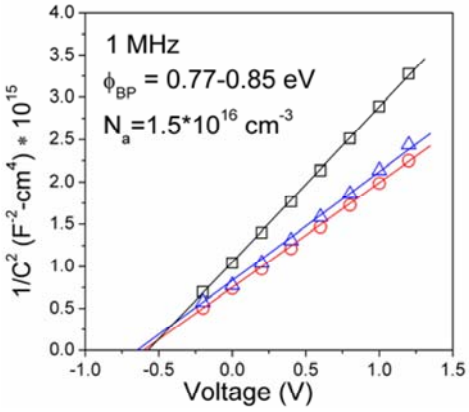


Figure 20. Capacitance-voltage measurements on an Al/valence-mended textured p-type Si junction.

The capacitance-voltage characteristics of an Al/valence-mended textured p-type Si junction at a frequency of 1 MHz is shown in Fig. 20. The extracted doping

concentration is ~1.5×10^{16} cm^{-3}, in line with the wafer specification (2×10^{16} cm^{-3}). The barrier height from capacitance-voltage is between 0.77 eV and 0.85 eV without considering image-force lowering. These values are slightly larger than those from current-voltage and activation energy measurements.

1.2.2 Reduction of leakage current

The non-saturating reverse current in Fig. 18 suggests a large leakage current, which is caused by the high electric field at the Al/Si junction. We also observed a large leakage current for untextured samples. To understand the origin of the leakage current, we fabricated a sample with Al dots of different diameters from 600 μm to 1,200 μm. Fig. 21 shows the reverse current of these dots as a function of their diameter. If the reverse current is dominated by thermionic emission, it is proportional to the area of the Al dot. On the other hand, if the reverse current is dominated by edge effects, it is proportional to the circumference of the Al dot. In Fig. 21, the reverse current increases nearly linearly with Al dot diameter, indicating that the reverse current is dominated by edge leakage.

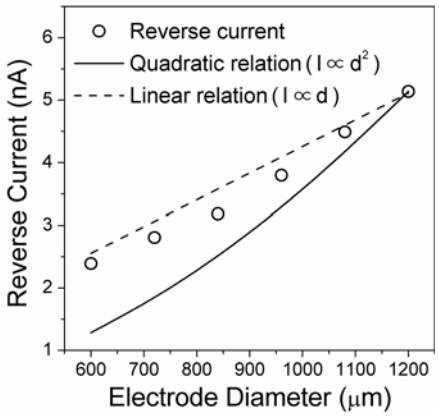


Figure 21. Reverse current of Al/valence-mended p-type Si(100) junctions as a function of Al dot diameter. The largely linear relationship indicates significant edge leakage.

For solar cells, a large reverse current results in a low open-circuit voltage and a low efficiency. We investigated several methods to reduce the reverse leakage current including 1) p/p$^+$ epi-wafer; 2) mesa structure and 3) Al/valence-mended Si n/p junction. The p/p$^+$ wafers were provided by SunEdison (Dr. Seacrist), which is 1×10^{19} cm^{-3} boron-doped substrate with a 1×10^{15} cm^{-3} boron-doped epi-layer. As shown in Fig. 22(a), the epi-wafer was patterned with 100 nm thermal SiO_2 layer to reduce the electrical field along the edge of the Al dot. Although the patterned SiO_2 layer is effective in reducing the reverse leakage current, considerable minority carrier generation can still happen in the lightly-doped epi-layer, resulting in a large reverse current. Therefore, a mesa was fabricated on the epi-wafer to further reduce the reverse current, as illustrated in Fig. 22(b).

The current-voltage characteristics of Al/valence-mended p/p$^+$ Si junctions with and without mesa are shown in Fig. 23. With a patterned SiO_2 layer but without a mesa, a high Schottky barrier of 0.82 eV was obtained. The mesa further increased the Schottky barrier to 0.84 eV. With the smaller mesa area, the reverse saturation current is only ~2×10^{-8} A/cm^2 at 300K, and the rectification ratio is 10^8 at ±1 V bias, which is much

larger than any commercial p-n or Schottky junctions. The series resistance of 4.8 Ω comes mainly from the probe station since the Si substrate is doped to 10^{19} cm^{-3}. These barrier heights are very close to the Schottky–Mott limit which is 0.89 eV for an ideal Al/p-type Si junction, and are some of the highest barriers for Al/p-type Si junctions by current-voltage measurements. SiO_2 and mesa are effective in minimizing the reverse current.

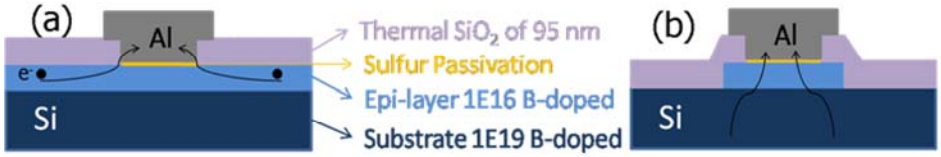


Figure 22. Methods to reduce the reverse current in Al/valence-mended p-type Si junctions: (a) p/p^+ epi-wafer and (b) mesa on p/p^+ epi-wafer.

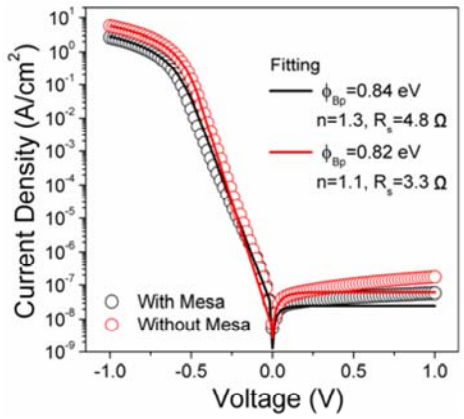


Figure 23. Current-voltage characteristics of Al/valence-mended p/p^+ Si junctions with and without mesa.

A theoretical analysis has been carried out on the Al/valence-mended p/p^+ Si junction to understand the reduced reverse current. Our record-high Schottky barrier makes our Schottky junction act like a p-n junction. Fig. 24 is the band diagram of the the Al/valence-mended p/p^+ Si junction. Due to the high barrier of 0.84 eV, the energy bands bend downward so much at the Al/Si interface that the Fermi level E_f is located above the midgap E_i, leading to degenerate inversion of the interfacial Si. This unique feature allows us examine whether the edge leakage current is reduced in the mesa structure.

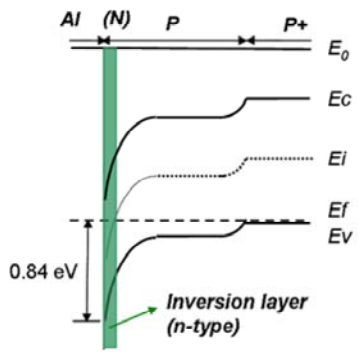


Figure 24. Band diagram of the Al/valence-mended p/p^+ Si junction.

The Al/valence-mended Si n/p junction was fabricated using ion implantation on the p/p$^+$ epi-wafer. The wafer has a SiO_2-patterned surface but without mesa, and the structure of the junction is shown in Fig. 25(a). Fig. 25(b) illustrates the conditions for ion implantation and rapid thermal annealing for the formation of the n region. For comparison, an Al/valence-mended p/p$^+$ Si junction was fabricated on a mesa.

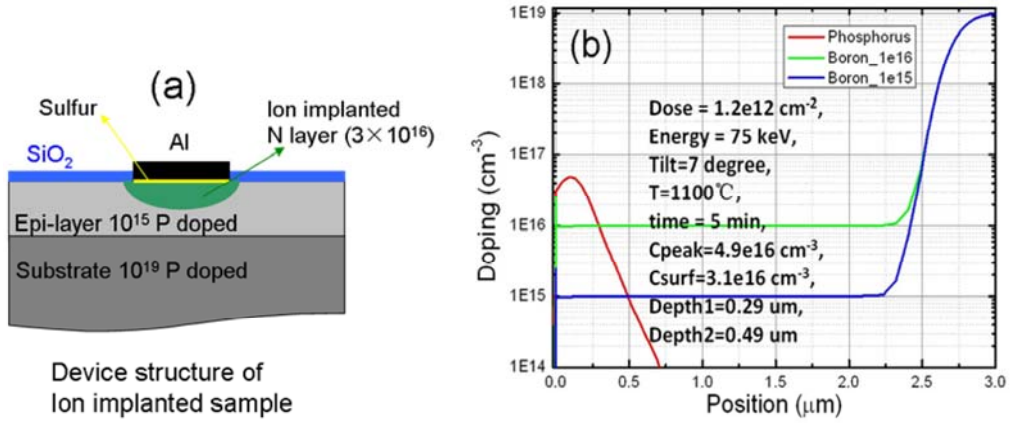


Figure 25. (a) Structure of an Al/valence-mended Si n/p junction by ion implanted sample. (b) Simulation results for ion implantation.

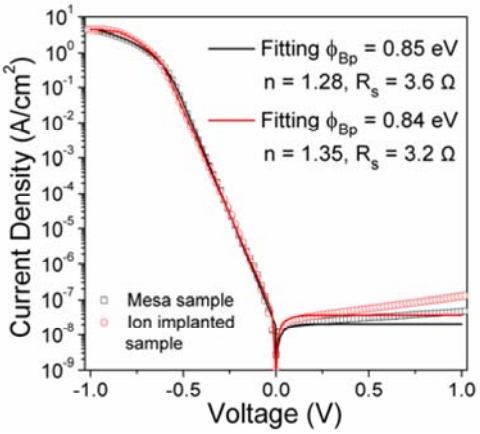


Figure 26. Current-voltage characteristics of an Al/valence-mended Si p/n junction by ion implantation and an Al/valence-mended p/p$^+$ Si junction on a mesa.

Fig. 26 shows the best current-voltage characteristics of implanted and mesa samples. The mesa sample exhibits the highest barrier height we achieved so far, 0.85 eV, corresponding to a reverse saturation current of 1.8×10^{-8} A/cm^2. Its series resistance comes mainly from the probe station, and the high ideality factor is attributed to recombination in its depletion region. It can be seen that both samples show similar current-voltage characteristics, indicating that our Schottky junction with a mesa structure behaves like a p-n junction. Different from a Schottky junction, the reverse saturation current of an ideal p-n junction is given by:

$$J_0 \equiv \frac{qD_p p_{no}}{L_p} + \frac{qD_n n_{po}}{L_n} \equiv \frac{qD_p n_i^2}{L_p N_D} + \frac{qD_n n_i^2}{L_n N_A} \quad (1)$$

where n_i is the intrinsic concentration, D_n/D_p, L_n/L_p and N_D/N_A are the diffusion

coefficients, diffusion lengths and doping concentrations for electrons and holes, respectively. For planar Si p-n junctions, the edge leakage current is generally smaller than the generation-recombination current in the depletion region, which is:

$$J_{ge} = \int_0^{W_D} q|U|dx \approx q|U|W_D \approx \frac{qn_iW_D}{\tau_g} \quad (2)$$

where W_D is the depletion width, τ_g the generation lifetime. The total reverse saturation current of a p-n junction contains three parts:

$$J_0 \equiv \frac{qD_pn_i^2}{L_pN_D} + \frac{qD_nn_i^2}{L_nN_A} + \frac{qn_iW_D}{\tau_g}. \quad (3)$$

If we assume typical W_D = 1 μm, and typical τ_g = 10 μs, the reverse saturation current is estimated to be ~10^{-8} A/cm^2, which agrees well with our results. The 1.8×10^{-8} A/cm^2 reverse current for the mesa sample should be the theoretical limit for a standard p-n junction, and we have reached the limit.

1.2.2 Cleaning and passivation conditions

As soon as we obtained good-quality passivation on both Si(100) surface and Si(111) faces, we shifted our focus to multicrystalline-Si wafers. First we needed to develop an ex-situ cleaning recipe for multicrystalline Si wafers. Cleaning is a key step in surface passivation for multicrystalline Si because multicrystalline-Si wafers are as-cut. There is a damaged layer of a few microns due to the sawing, which has to be removed. In addition, organic, native oxide and metallic contaminants on multicrystalline Si must be removed. Table 1 shows the ex-situ cleaning recipe for multicrystalline-Si wafers, which contains four steps to clean multicrystalline-Si wafers: damage layer removal, organic removal, native oxide removal and metal removal. The whole cleaning process takes ~40 min to finish.

Table 1. Ex-situ cleaning recipe for multicrystalline-Si wafers.

Parameter / Step	Solution	Temperature	Time (min)
1 Damage layer removal	NaOH (30%)	80°C	1–5
2 Organic removal	$NH_3OH/H_2O_2/H_2O$ (1:1:5)	70–80°C	10–15
3 Native oxide removal	HF/H_2O (1:50)	25°C	0.5–2
4 Metal removal	$HCl/H_2O_2/H_2O$ (1:1:6)	70–80°C	10–15

Fig. 27 shows the current-voltage characteristics of multicrystalline-Si samples with different ex-situ cleaning recipes. The in-situ cleaning recipe is the same for all the samples, i.e. HCl introduced at 750°C and stopped at 300°C. The sample with only damage removal and metal removal gives a higher barrier height of 0.69 eV, thus better quality passivation. The removal of saw damage by NaOH generates a clean and fresh surface, and the only contaminant on this fresh surface is Na ions from the NaOH solution. Additional cleaning steps such as organic removal may introduce additional contamination.

With the ex-situ cleaning recipe established for multicrystalline Si, we investigated in-situ surface cleaning, which is a prerequisite for valence-mending passivation. As mentioned before, H_2 serves as the carrier gas and also helps clean the surface. HCl

plays a critical role in removing surface contaminants such as metals. The flow rates and cleaning times of H_2 and HCl were optimized for multicrystalline-Si wafers. As shown in Fig. 28(a), 20 sccm H_2 and 20 sccm HCl provide a much lower reverse current, and Fig. 28(b) suggests the cleaning time to be at least 20 min.

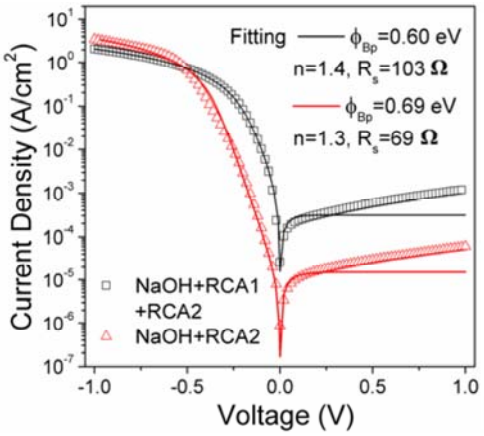


Figure 27. Current-voltage characteristics of Al/valence-mended p-type multicrystalline-Si junctions with different ex-situ cleaning recipes.

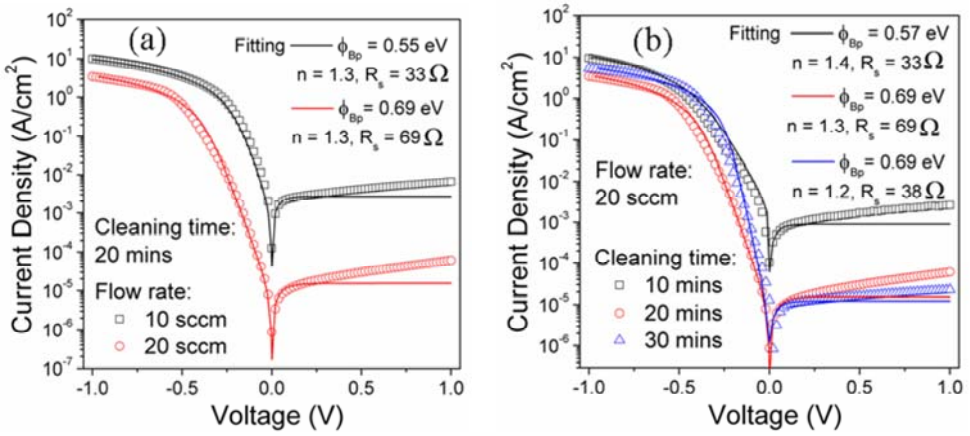


Figure 28. In-situ cleaning conditions for multicrystalline Si: (a) Flow rate of H_2 and HCl at 750°C and (b) cleaning time of H_2 and HCl at 750°C.

A barrier height of 0.69 eV obtained for 30 min of H2 and HCl in Fig. 28(b) is reasonable for multicrystalline Si, suggesting that the ex-situ and in-situ cleaning recipes work well. We then shifted our efforts to the passivation process. The surface of multicrystalline Si contains both single-dangling-bond and double-dangling-bond sites. The single-dangling-bond sites require Group VII elements such as Cl to passivate. Cl is available in our CVD system in the form of HCl.

Fig. 29(a) shows the current-voltage characteristics of Al/valence-mended multicrystalline-Si junctions at different HCl start temperatures. When HCl is introduced at 750°C, the lowest reverse saturation current obtained is ~2×10^{-6} A/cm^2. This reverse current is two orders of magnitude higher than that of the Al/valence-mended monocrystalline-Si junction. Fig. 29(b) is the reverse saturation current as a function of HCl start temperature. 750°C provides a much lower reverse current than 700°C or 800°C.

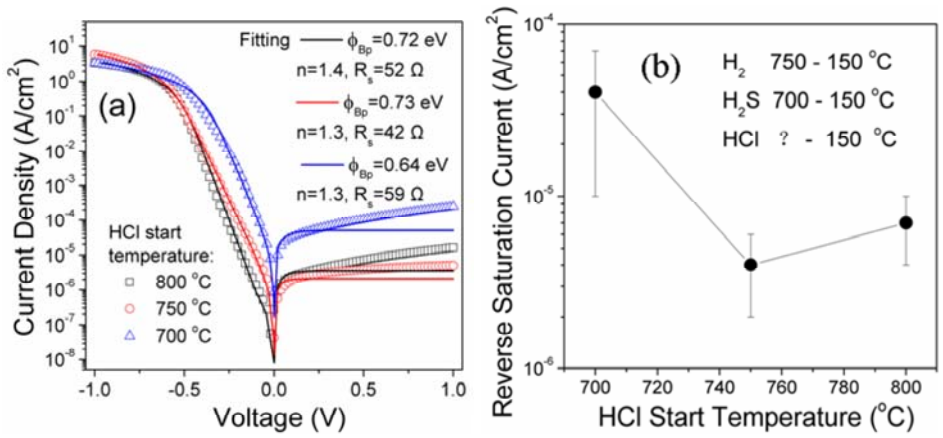


Figure 29. (a) Current-voltage characteristics of Al/valence-mended p-type multicrystalline-Si junctions with HCl started at different temperatures. (b) Reverse saturation current as a function of HCl start temperature.

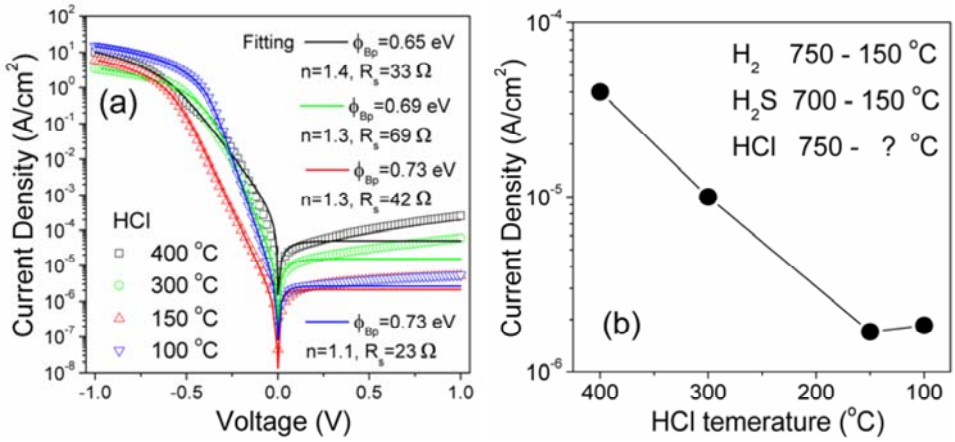


Figure 30. (a) Current-voltage characteristics of Al/valence-mended p-type multicrystalline-Si junctions with HCl stopped at different temperatures. (b) Reverse saturation current as a function of HCl stop temperature.

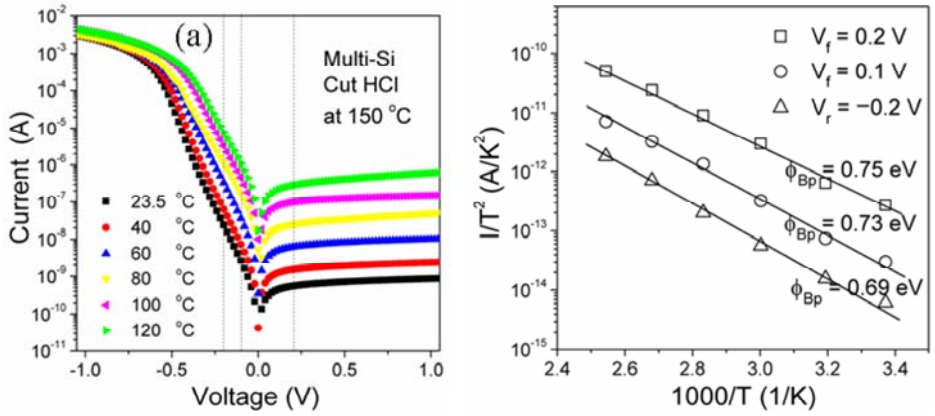


Figure 31. (a) Current-voltage characteristics of an Al/valence-mended p-type multicrystalline-Si junction at different temperatures. (b) Activation-energy plot to determine barrier height at bias of –0.2, 0.1 and 0.2 V.

Fig. 30 shows the current-voltage characteristics of Al/valence-mended p-type

multicrystalline-Si junctions as a function of HCl stop temperature (400, 300, 150 and 100°C), along with the reverse saturation current as a function of HCl stop temperature. When the HCl stop temperature decreases from 400°C to 150°C, the reverse current deceases significantly, and a barrier height of 0.73 eV is obtained at 150°C of HCl stop temperature. Further decrease in HCl stop temperature to 100°C does not lead to a lower reverse current but a lower ideality factor of 1.1. This suggests that termination dangling bonds by Cl takes place between 150–400°C.

Fig. 31(a) shows the activation-energy measurements on an Al/valence-mended p-type multicrystalline-Si junction between 23–120°C. Fig. 31(b) is a plot of $\ln(I/T^2)$ vs 1/T to determine the barrier height. At forward bias of 0.2 V, the barrier height is 0.75 eV, which is 0.02 eV larger than the I-V measurements. The barrier height under reverse bias of –0.2 V is 0.69 eV. This lower value is attributed to image-force lowering when the junction is under reverse bias.

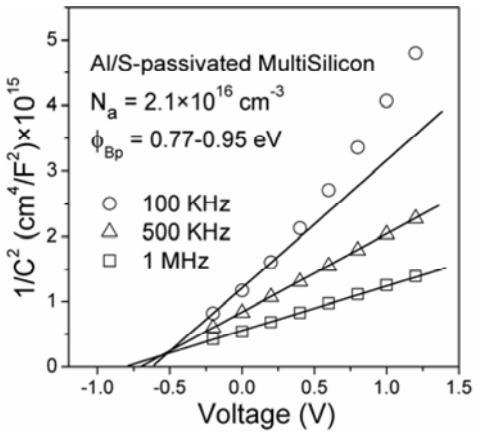


Figure 32. Capacitance-voltage measurements on an Al/valence-mended p-type multicrystalline-Si junction.

The capacitance-voltage characteristics of an Al/valence-mended p-type multicrystalline-Si junction at frequencies of 100 kHz, 500 kHz and 1 MHz are shown in Fig. 32. The extracted doping concentration is ~2.1×10^{16} cm^{-3}, in agreement with the wafer specification (2×10^{16} cm^{-3}). The barrier height from capacitance-voltage is 0.77–0.95 eV without considering image-force lowering. This value is slightly larger than the values obtained from current-voltage and activation energy measurements. In addition, the uniformity of the sample needs to be improved, as capacitance-voltage measurements results in a range of barrier height.

Surface passivation on multicrystalline Si has several difficulties. One difficulty is that multicrystalline Si has a contaminated surface to begin with, while monocrystalline Si has a polished surface to begin with. The randomly orientated crystal grains on multicrystalline require more thorough and comprehensive surface passivation than monocrystalline Si. The grain boundaries may also cause a larger reverse current between Al and valence-mended multicrystalline Si in current-voltage measurements.

1.2.3 Thermal stability of metal/valence-mended multicrystalline-Si interface

We investigated the thermal and ambient stability of valence-mended multicrystalline-Si samples by XRD and SEM. Multicrystalline-Si samples were cleaned ex-situ in 20% NaOH at 80°C for 6 min. The samples then went through in-situ cleaning in our CVD

reactor, followed by the two-step valance-mending passivation process with H_2S and HCl. After passivation, a 50-nm Ni film was deposited on the valence-mended multicrystalline-Si samples by e-beam evaporation. Thermal annealing at 300°C for 30 s was carried out on a hotplate in air. As shown in Fig. 33, the crystal structure of the Ni film on valence-mended multicrystalline Si upon annealing was revealed by XRD. Fig. 33(a) is the XRD pattern of Ni_2Si for reference. Fig. 33(b) is the XRD patterns of the Ni film before and after annealing, and they are similar, suggesting no silicidation of Ni. The standard JCPDS PDF card of Ni is also included for comparison. All the peaks from our Ni/Si sample are accounted as Ni peaks. None of the Ni_2Si diffraction peaks is observed in Fig. 33(b), indicating no silicidation between Ni and Si during annealing and thus good-quality passivation.

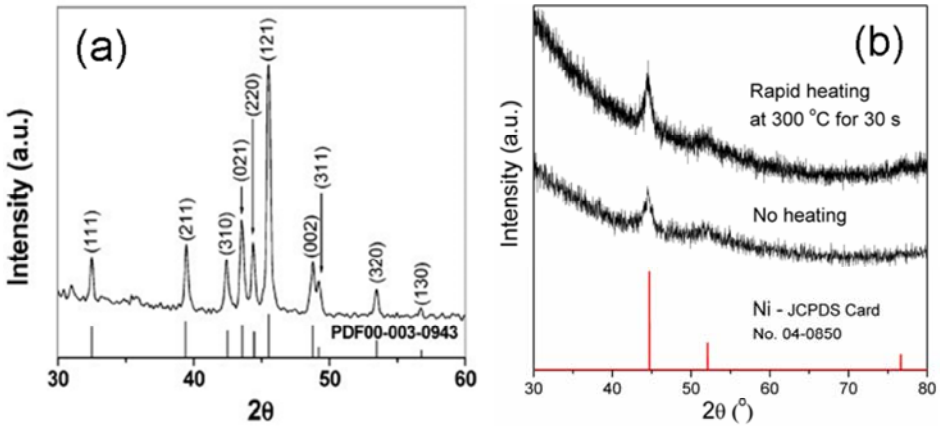


Figure 33. (a) XRD pattern of Ni_2Si (Y. Song et al, Nano Letters 7 (2007) 965). (b) XRD patterns of the Ni/valence-mended multicrystalline-Si structure before and after annealing.

The interface between Ni and valence-mended multicrystalline Si upon annealing was studied with cross-sectional SEM. As shown in Fig. 34(a), there is a clear boundary between Ni and Si before annealing. Fig. 34(b) shows the Ni/valence-mended multicrystalline-Si interface after annealing at 300°C for 30 s. A clear boundary between Ni and Si remains intact, and no Ni_2Si or NiSi is observed at the Ni/Si interface. This again suggests a stable interface upon annealing and good-quality passivation by CVD.

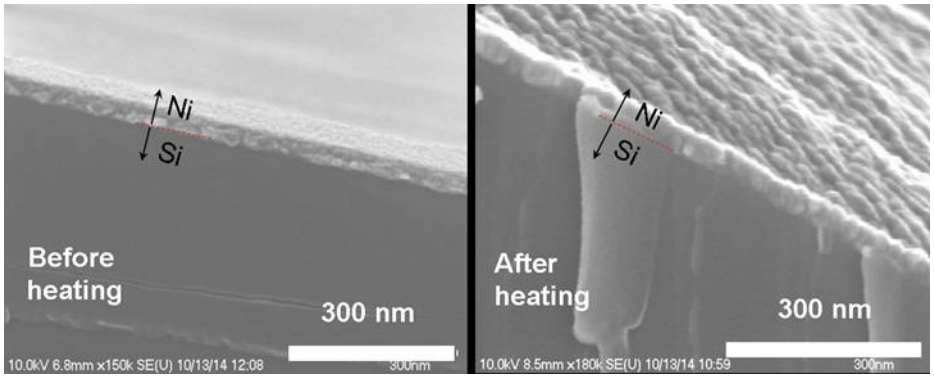


Figure 34. Cross-sectional SEM images of the Ni/valence-mended multicrystalline-Si interface before and after annealing. (a) Before annealing. (b) After annealing at 300°C for 30 s.

Ⅱ. N-Type Solar Cell (Task 2.0 & Task 7.0)

N-type Si solar cells have been under development for many years with efficiencies over 20%. The p/n junction in n-type cells is typically created through boron diffusion into the n-type wafer to form a p-type layer. Boron diffusion requires high temperatures and long times, thus it is challenging to incorporate boron diffusion into industrial production of Si cells. An industrially compatible p-type diffusion process has hampered the introduction of n-type cells despite the inherent advantages of n-type cells.

Junction formation has been a challenge even in p-type cells with n-type emitters. In phosphorous diffusion, the $POCl_3$ process is a long established technique to produce n-type emitters but as cell efficiencies continue to rise there is a need for a more precisely controlled dopant profile in the emitter. This prompted the development of ion implantation despite challenges with cost and throughput. We see similar challenges with the creation of p-type emitters for n-type cells. Our solution is the creation of a diffusion source that provides the benefits of ion implantation without the cost.

2.1 Amorphous Si as a diffusion source

The use of PECVD is well established in the industry for the deposition of SiN_x and amorphous Si. For this project we deposited a layer of amorphous Si that is very heavily doped with boron. We then used the layer as the diffusion source in a subsequent drive-in step. The key advantage of our process over traditional processes using solid or liquid diffusion sources is that the diffusion uniformity is much better and more controllable. Fig. 35 shows the dopant profiles that were performed with a solid source. The uniformity of the dopant profiles is poor at over 18% and insufficient for the development of high-efficiency cells.

Our solution was to add a $B(CH_3)_3$ source to our existing Applied Materials PECVD tool. We further simulated the boron profiles in both rapid thermal annealing and tube furnace annealing. We used a design of experiments methodology to develop the boron diffusion recipe.

The response surface methodology focused on obtaining optimal value for a continuous factor or set of factors. It was fitted with a curved surface and we used the software tool JMP to mathematically analyze the data for process maximum. A rotatable central composite design (CCD) was employed. The deposition temperature, $B(CH_3)_3$ flow, SiH_4 flow, and gap parameters were fixed, and the power, pressure, and H_2 flow systematically varied. There were 20 runs, randomized, including 6 center points for repeatability.

The model predicted an optimal condition with 27.7 kΩ-cm film resistivity and 1.29 nm/s deposition rate. Subsequent experimental depositions were measured and confirmed this value, within the bounds of experimental error and used for all later work. There is an opportunity to revisit these conditions now that we have a solar cell fabrication process flow.

The SIMS measurement as shown in Fig. 36 demonstrates that we had sufficient concentration of boron in the diffused layer. The uniformity was excellent at 2.7%. With the PECVD recipe we developed the drive-in process using Silvaco Athena computer simulation. A typical simulation is shown in Fig. 37.

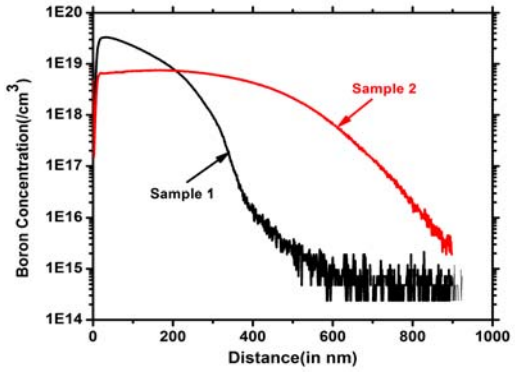
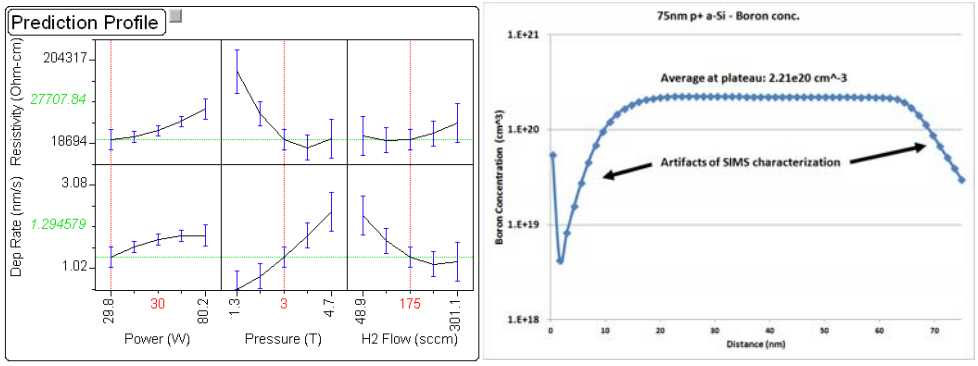


Figure 35. SIMS measurements of solid source boron diffusion.



(a) (b)

Figure 36. (a) Optimization of PECVD boron deposition conditions using a design of experiments response surface methodology. (b) Resultant boron concentration by SIMS.

The following figures (Fig. 38–39) show the results of the Athena computer simulations. In each case the red line indicates the target value derived from computer simulations of the full solar cell structure using Synopsys Sentaurus. There are a variety of times and conditions that will achieve the desired results giving flexibility when incorporating the process into the full solar cell process flow. We chose a diffusion layer thickness of 35 nm that resulted in an emitter sheet resistance below 150 Ω/□.

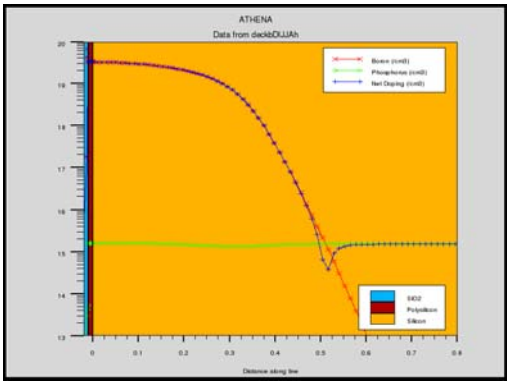


Figure 37. Boron diffusion profile from Silvaco Athena with a temperature of 1075°C for 7 min.

The diffusion profiles from the predictions were run through rapid thermal annealing and the resultant profile was measured using SIMS as shown in Fig. 40. The surface concentration matches closely between SIMS measurements and simulations.

Experimentally we found a deeper junction than predicted from simulations. The deeper junction is likely due to a combination of the ramp up and ramp down times in the system and the inaccuracy of our SIMS system at lower doping concentrations. We have installed an electrochemical capacitance voltage system that is now up and running for phosphorous diffusion and it will be used to examine boron diffusion moving forward once we have received the calibrated doped wafers.

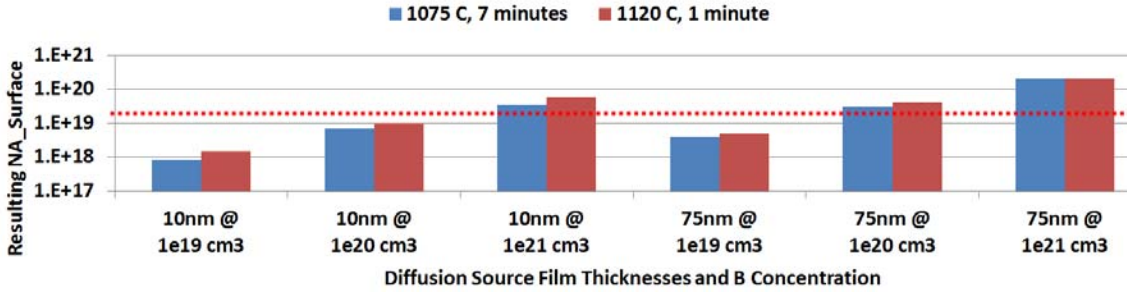


Figure 38. Surface boron concentration. A high surface concentration is necessary for low contact resistance.

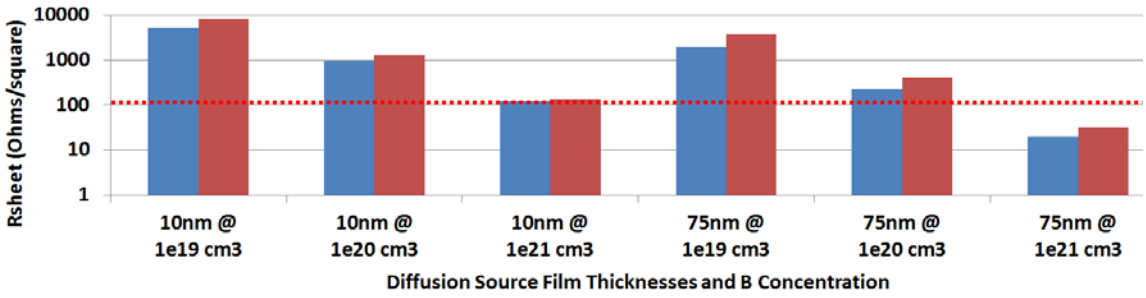


Figure 39. Sheet resistance. Lower than 150 Ω/□ is needed to reduce resistive loses in the emitter to below 0.2 Ω-cm^2.

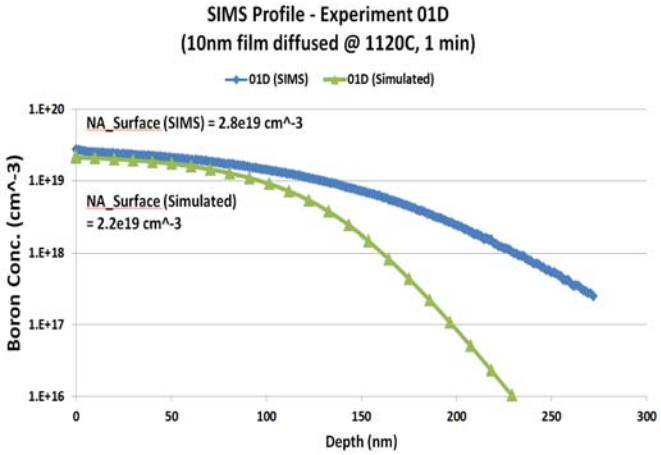


Figure 40. Comparison of predicted diffusion profile from Silvaco Athena with experimental diffusion profile by SIMS.

The sheet resistance was mapped across the entire wafer. We found that the uniformity after diffusion matched the uniformity in thickness of the PECVD film. The uniformity after the diffusion as shown in Table 2 below is between 3 and 6%, which is more than adequate for a high-efficiency cell.

Table 2. Uniformity of boron diffusion at various temperatures for different times.

		p+ film Thickness	
		10 nm	75 nm
Annealing Profile	1075C, 7 min	01B: 7%	02B: 3%
	1100C, 4 min	01C: 5%	02C: 3%
	1120C, 1 min	01D: 3%	02D: 6%

In this section we demonstrated that we can achieve an excellent uniformity of 3% as compared to the uniformity of 18% evidenced in the solid source diffusion.

2.2 Solar cell fabrication

The next challenge is to incorporate the new diffusion process into the cell process flow. The cell structure is shown in Fig. 41. It consists of front boron diffusion, rear phosphorous diffusion and Al contacts on both sides. The front has a SiN_x antireflection coating only. The lack of texturing will reduce the efficiency of the cell due to the lower current. Adding texturing on cells typically increases the efficiency by ~2% absolute.

The process was tracked via photoluminescence and minority carrier lifetime. In Fig. 42 we see the result of optimization using photoluminescence. The dark spots on the wafers are areas of very low lifetime. The average lifetime as measured using QSSPC was under 10 μs for image (a) and the resulting cell efficiency was 5.1%. In subsequent process development we achieved the photoluminescence image on the right. The dark areas were eliminated by: better wafer handling, coating the carriers with SiN_x barrier layers, and by optimizing the etch time for the removal of the boron layer after diffusion. The wafer of image (b) had a much higher lifetime of 291 μs and the potential for cell open-circuit voltage over 630 mV.

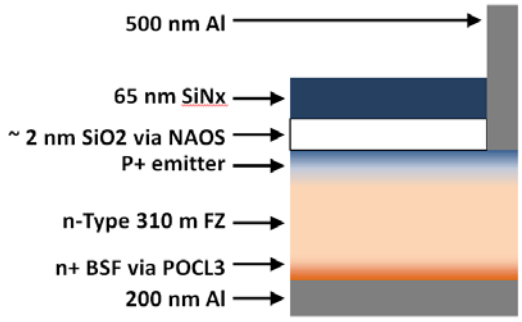


Figure 41. Structure of the solar cell fabricated. There is only a SiN_x antireflection coating and no texturing.

These cells were to demonstrate the integration of the boron diffusion process we developed into a n-type cell process flow. As noted previously, these cells were untextured. By adding texturing, we demonstrated a solar cell with 15.4% efficiency using Al contacts. Table 3 below lists the pertinent details.

Fig. 43 is the current-voltage characteristics of the 15.4% cell. A significant loss is the voltage drops at the contacts. With the lifetime test we can predict the cell open-circuit voltage by calculating what has been dubbed Implied Open-Circuit Voltage. When we measured the Implied Open-Circuit Voltage for the samples in Table 3 we obtained

voltage of 615–630 mV. Recovering the loss in open-circuit voltage would increase the cell efficiency by another 2% absolute. The loss is confirmed to be due to a Schottky diode as explained in the following section.

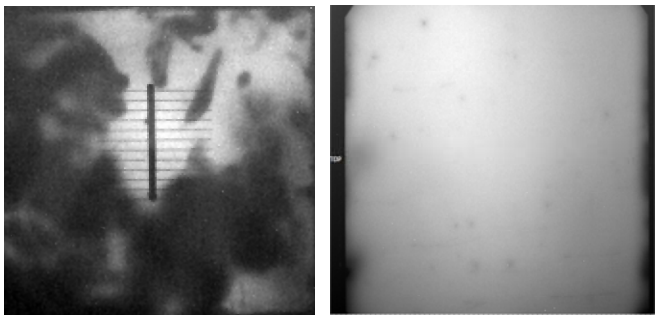


Figure 42. Photoluminescence of boron diffused wafers. (left) Initial diffusions had large areas of high recombination leading to very low average lifetimes. (right) Later diffusions resulted in much higher lifetimes.

Table 3. Performance parameters of a 15.4% efficient solar cell with all-Al contacts.

Efficiency (%)	V_{OC} (V)	J_{SC} (mA/cm²)	FF	Pseudo FF
15.4	0.593	33.7	76.8	78.7

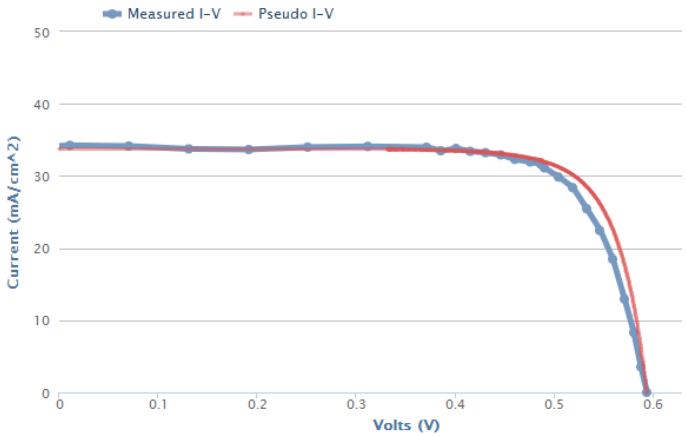


Figure 43. Current-voltage characteristics under one sun illumination of a 15.4% efficient cell with all-Al contacts.

2.3 Identification of Schottky diodes

The cell in Table 3 has an ideality factor less than one, which is clear evidence of the presence of Schottky diode at the contacts.

$$I = I_0\left(\exp\left(\frac{qV}{nkT}\right) - 1\right) \quad (4)$$

In the equation above *I* is the cell current, *V* the voltage, *T* the temperature, and *q* and *k* are constants. The ideality factor, *n*, is a measure of how close the diode current-voltage curve is to ideal. By measuring the cell open-circuit voltage as a function of light intensity using Suns VOC we are able to measure the current-voltage curve of the cell without the effect of series resistance and extract the ideality factor. For most Si solar cells the ideality factor is between 1 and 2. In our cells we see an ideality factor of 0.9. The low ideality factor is due to a Schottky diode at the contacts and is often seen in

solar cells such as ours where there is a lower doping near the contacts. The lower doping is necessary to achieve low recombination and is usually overcome through the use of a selective emitter. The elimination of the Schottky contact is the primary focus of this grant and incorporating the valence-mending passivation will allow a jump in efficiency.

Ⅲ. Low-Temperature Al Paste (Task 3.0 & Task 8.0)

In Phase I of this project, ASU was working with our industrial partner, Heraeus, to develop a low-temperature Al paste. Heraeus was quick in providing ASU with samples of their current products such as conventional and low-temperature Ag pastes. This low-temperature Al paste requires significantly-more efforts, and the downturn in the industry shifts the focus of companies to survival over new technologies. Nevertheless Heraeus made several rounds of attempts to develop a low-temperature Al paste. Initially they used the same organic system they have for the low-temperature Ag paste, and they noticed serious stability issues, i.e. the organic system is incompatible with Al powder. The resultant paste was unprintable. After months of additional efforts, Heraeus developed a new organic system specifically for Al powder, and the remaining issue with the new Al paste is the low loading factor, which is in the 50% range. This will negatively affect the resistivity of the Al electrode.

In searching for alternative vendors, ASU found a small company, Applied Nanotech, which supplies a prototype low-temperature Al paste, but the lowest firing temperature for it is ~550°C, still too high for the valence-mending passivation. We discussed our requirements with DuPont and were told that 550°C is likely the minimum temperature for firing Al. Below this temperature, the Al powder does not fuse together. This, plus the fact that firing in air leads to formation of Al_2O_3 on Al power, results in unacceptably-high resistivity of the Al electrode.

As an alternative to low-temperature Al paste, ASU developed an Al electroplating process. It is performed below 150°C deposition temperature and can be fired between 150°C and 350°C, which are compatible with valence-mending passivation. The electroplating solution is an ionic liquid. With a sacrificial Al anode, the electroplating solution is reusable for cost reasons. The electroplating process is performed without vacuum, further reducing its cost. The resultant Al has a resistivity in the mid-to-high 10^{-6} Ω-cm range, similar to that of screen-printed Ag. Based on electroplated Al, ASU developed a complete process flow for all-Al Si solar cells, with efficiencies approaching 15%. A U.S. patent application has been filed on this technology.

3.1 Characteristics of Electroplated Al

Al electroplating requires a nonaqueous solution. The options include molten salts, organic solvents and room-temperature ionic liquids. After an extensive literature study, we decided to focus on ionic liquids that are characterized by high electrical conductivity, low vapor pressure, low viscosity, low toxicity, non-flammability, high thermal and chemical stability, wide electrochemical window and room-temperature deposition. Ionic liquids are typically mixtures of $AlCl_3$ and an organic halide. We then selected a commercially-available ionic liquid, 1-ethyl-3-methylimidazolium chloride ([EMIm]Cl), for Al electroplating.

We first examined the deposition conditions for Al electroplating, such as solution pre-bake conditions, deposition temperature and post-deposition annealing conditions. Fig. 44 shows the sheet resistance of electroplated Al as a function of pre-bake temperature and time of the solution. Ionic liquids are sensitive to moisture, and the pre-bake helps drive out the moisture in the solution. The electroplating process in a dry nitrogen box, where the humidity is ~20%. As shown in Fig. 44, there is a significant drop in Al sheet resistance at ~100°C, which is the boiling point of water. From Fig. 44, 1 hr and 120°C were selected as the pre-bake conditions for all future experiments.

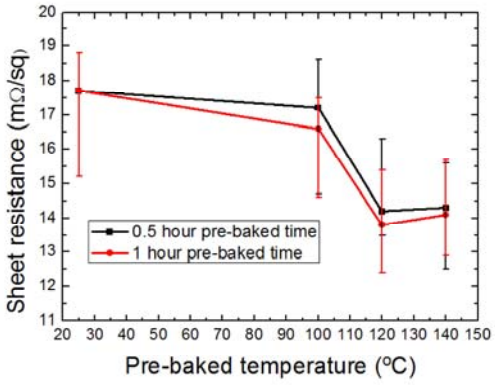


Figure 44. Sheet resistance of electroplated Al as a function of pre-bake temperature and pre-bake time.

Textured n-type monocrystalline Si wafers of 0.3–0.5 Ω-cm were used for Al electroplating. The electroplating current was constant at ~15 mA/cm^2 and the plating time was 1 hr. Assuming 95% current efficiency, the thickness of the electroplated Al is ~9 μm. Fig. 45 shows the sheet resistance of electroplated Al as a function of deposition temperature. The sheet resistance decreases with deposition temperature. At 115°C, the sheet resistance reaches 8.5 mΩ/□, which meets the requirements for solar cells.

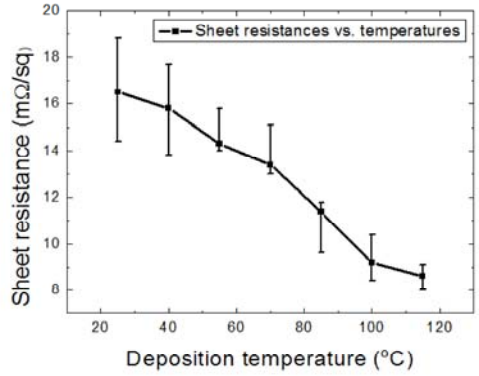


Figure 45. Sheet resistance of electroplated Al as a function of deposition temperature.

Vacuum annealing of electroplated Al was performed to further reduce the sheet resistance. Fig. 46 shows the sheet resistances vs. deposition temperature for electroplated Al before and after post-deposition annealing. The annealing takes place at 350°C for 20 min. There is a small drop in sheet resistance. The lowest sheet resistance obtained is 7.9 mΩ/□, corresponding to a resistivity of 7×10^{-6} Ω-cm. This

value is lower than sputtered Al or screen-printed Ag, which are in the high 10^{-6} Ω-cm range.

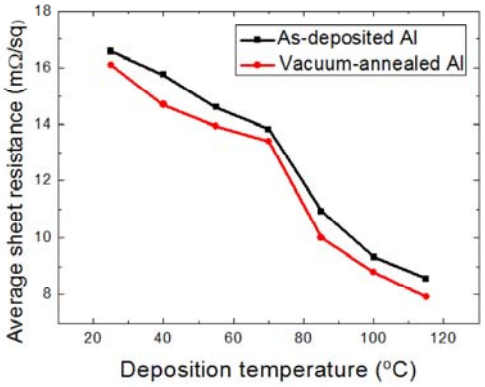


Figure 46. Sheet resistance of electroplated Al as a function of deposition temperature before and after post-deposition vacuum annealing.

3.2 All-Al Si cells by Al electroplating

The Al electroplating process has been integrated in both n-type and p-type Si cells as the front finger electrode. These all-Al cells feature a screen-printed Al back electrode and an electroplated Al front electrode, and the front electrode is on n-type Si. Our focus now is to improve the efficiency of these cells. Fig. 47(a) is the structure of the n-type all-Al cell. It has a back emitter. The fabrication of this cell involves one diffusion step for the front surface field. Fig. 47(b) is a photograph of the all-Al cell. The I-V characteristics of the cell under 1-sun illumination is shown in Fig. 48. This cell exhibits a lower-than-expected efficiency, 12.3%, due to the lack of a baseline process for n-type cells at ASU.

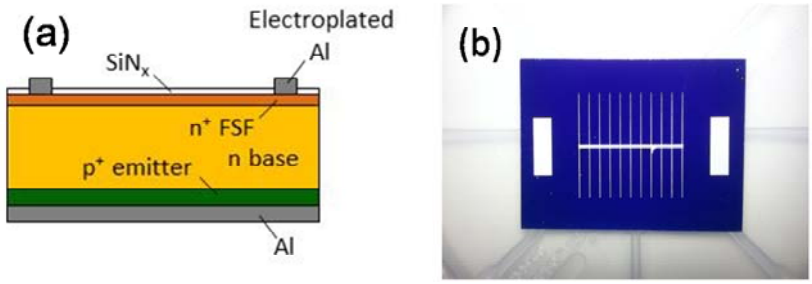


Figure 47. (a) Structure of an n-type Si cell with an electroplated Al front electrode. (b) photograph of our first n-type all-Al cell with an electroplated Al front electrode.

For p-type all-Al cells, we used partially-finished commercial p-type cells with a front SiN_x layer, an n^+ front emitter, a p^+ back-surface field and a screen-printed Al back electrode, without the front Ag electrode. They were obtained from Hareon Solar and ASU performed front metallization. The front SiN_x layer was photolithographically patterned, followed by sputter deposition of Ni (~200 nm) over the patterned photoresist. After lift-off, electroplating of Al on Ni was carried out and the electroplated Al was self-aligned to the Ni seed layer. The thickness of the Al layer was ~25 μm. A final annealing was performed by rapid-thermal annealing in air between 150°C and 400°C for 1 min to improve the front Al/Ni contact. Fig. 49 is the structure of the all-Al p-type cell with an electroplated Al front electrode.

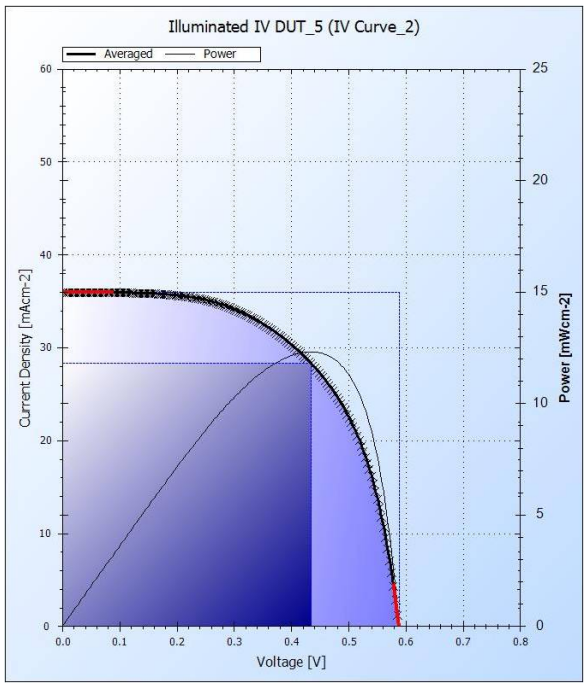


Figure 48. Current-voltage characteristics under 1-sun illumination of an n-type all-Al cell with an electroplated Al front electrode.

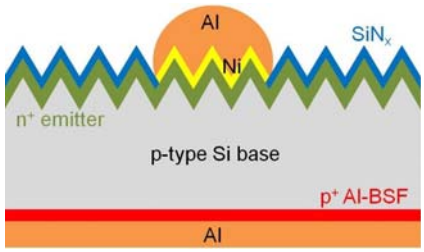


Figure 49. Structure of an all-Al p-type Si cell with an electroplated Al front electrode.

The effect of final annealing in air at temperatures from 150°C to 400°C on cell efficiency. Table 4 summarizes the one-sun parameters of the all-Al p-type Si cell at three different annealing temperatures. Fig. 50 shows the normalized efficiency of the cell as a function of annealing temperature. The normalized efficiency is defined as the ratio of η/η_o, where η is the measured efficiency and η_o is the efficiency of the cell before annealing.

Table 4. One-sun parameters of an all-Al Si solar cells with three different annealing temperatures.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	R_{sh} (Ωcm^2)	R_s (Ωcm^2)
No annealing	617	35.84	64.3	14.2	181	0.75
Annealed at 200°C (best)	626	35.98	64.6	14.6	212	0.79
Annealed at 400°C	601	35.56	50.9	10.7	23	1.65

In Table 4, the cell before annealing already shows a low shunt resistance (R_{sh}) of 181 Ω-cm^2, which we believe is the reason for the low fill-factor of 64.3%. A possible reason for the low shunt resistance is the possible damage to the shallow emitter junction during front SiN_x patterning by photolithography. Multiple rounds of cell fabrication have

been carried out to optimize the shunt resistance, as shown in Fig. 51. In each fabrication round, we modified only the photolithography step. The cell efficiency improves with an increasing shunt resistance. Further optimization of the front patterning process is needed. On the other hand, the cell without annealing shows good performance in short-circuit current density (J_{sc}) and series resistance (R_s), suggesting that the electroplated Al is continuous without voids and thus low resistivity.

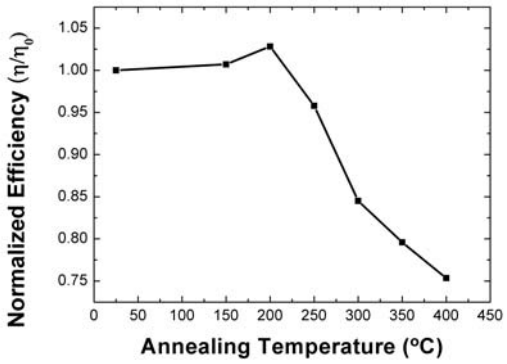


Figure 50. Normalized efficiency of an all-Al p-type cell as a function of annealing temperature.

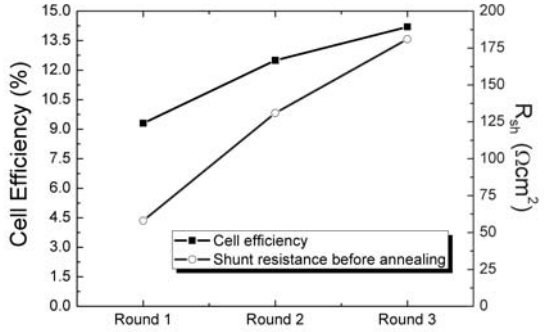


Figure 51. Comparison of cell efficiency and shunt resistance between fabrication rounds.

As shown in Fig. 50 and Table 4, annealing at 200°C results in a slightly-increased open-circuit voltage (V_{oc}) and fill factor (FF). However, the efficiency drops drastically when the annealing temperature exceeds 200°C. As the annealing temperature goes above 250°C, the shunt resistance starts to decrease and eventually reaches 23 Ω-cm^2 and the series resistance starts to increase all the way to 1.65 Ω-cm^2 at 400°C. At the same time, the open-circuit voltage is reduced by 25 mV between 200°C and 400°C. There are multiple reasons for the effect of annealing temperature on cell efficiency. The formation temperature of Ni_2Si starts at 250°C. Its formation at the Ni/Si interface increases the series resistance while thinning the emitter junction. The later reduces the shunt resistance of the cell. Another possibility for the increased series resistance is the increased Al_2O_3 thickness in the Al electrode when the annealing temperature exceeds 200°C.

Figure 52 is the current-voltage curve under 1-sun illumination for the all-Al p-type cell after annealing at 200°C. The efficiency is 14.6% with an open-circuit voltage of 626 mV, a short-circuit current of ~36 mA/cm^2, and a fill factor of 64.6%. The fill factor still has room for improvement. If a higher fill factor of 80% can be achieved, the efficiency of this all-Al cell will reach 18%. It is reminded that these are commercial cells and their efficiencies are capped at ~18%. This shows both the potential of Al electroplating as the metallization process for the front finger electrode on n-type Si.

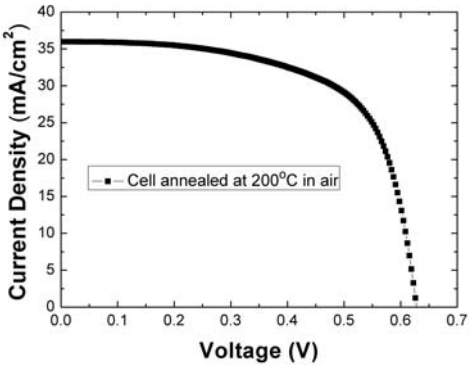


Figure 52. Current-voltage curve under one-sun illumination for an all-Al p-type Si solar cell annealed at 200°C.

Ⅳ. Point Back Contact PV Cell (Task 4.0 & Task 10.0)

The fabrication of high-efficiency Si cells by depositing metal directly on a lightly-doped wafer has attracted significant attention over the decades. However, the experimental realizations of these devices were mostly futile. A primary reason is the high density of surface states at the metal/Si interface, resulting in the pinning of the Fermi level at the mid-gap which severely degrades the performance of the cell. Valence-mending passivation is a novel technique that addresses this challenge. By using valence-mending passivation, the barrier height at the metal/Si interface is determined by the difference between the electron affinity of Si and the workfunction of the metal, and the monolayer passivation does not impede carrier transport. In this section, we use device modeling to understand the efficacy of valence-mending passivation in improving cell performance. The cell structure for simulation is in Fig. 53.

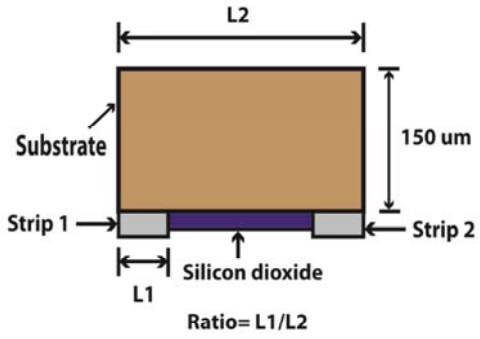


Figure 53. Point back contact cell structure for simulation.

4.1 Simulation of point back contact cell

We used commercial Sentaurus to model a point back contact cell structure. Fig. 53 shows the cell structure. The substrate is n-type Si with a thickness of 150 μm and resistivity 1 Ω-cm, with boron diffusion at the front surface. The doping profile is a Gaussian function with a peak concentration of 5×10^{19} cm^{-3} and a junction depth of 0.6 μm. On the rear, strip 1 and strip 2 are layers of Al with direct contact to the lightly-doped substrate. The surface recombination velocity at the interface between Al and Si is one adjustable input as it may be sensitive to the passivation process. Additionally, the model uses an adjustable barrier height between Al and Si to study the effects on contact resistance and cell performance. A 100 nm of SiO_2 passivates the region between two metal contact strips with an assumed surface recombination velocity of 10 cm/s. As the major focus of the model is to understand the efficacy of valence-mending passivation, additional solar cell features like texturing and antireflection coatings are not included. We will discuss the results of the simulation by studying three inter-related metrics: (1) First, the effect of surface recombination velocity at the interface between Si and Al on cell performance is explored by studying the effect on open-circuit voltage. (2) Second, the effect of barrier height at the interface between Si and Al on contact resistance is simulated. (3) Third, the effect of contact size on cell efficiency is calculated.

The surface recombination velocity of the metal/Si interface is varied from 10 cm/s to 1×10^7 cm/s. In this simulation the width (L1) of strip 1 and strip 2 (Fig. 53) is fixed at 1/10th of the total width (L2) and the work function of Al is 4.1 eV. Fig. 54 shows the results of the simulation; on the x-axis are the values of surface recombination velocity and on the y-axis is the absolute difference of open-circuit voltage from its value at 0 cm/s surface recombination. Even with a reduced contact area, high values of surface recombination velocity significantly decrease the open-circuit voltage. The results show that in these cells, the open-circuit voltage is almost unaffected up to a surface recombination velocity of ~1000 cm/s and changes thereafter. This provides a target surface recombination velocity for the passivation at L1/L2 = 0.1 that will not degrade cell performance. A point contact cell will have an even higher tolerance towards larger surface recombination velocities because of the further reduction of contact area.

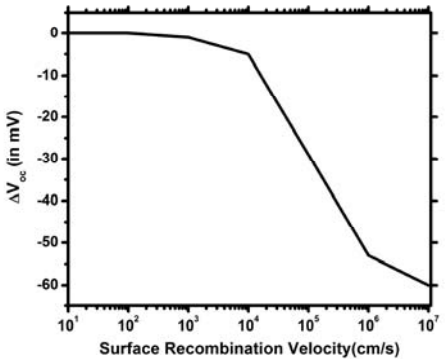


Figure 54. Effect ofsurface recombination on open-circuit voltage. At 1×10^7 cm/s, the open-circuit voltage drops by ~60 mV from its value without any surface recombination.

The barrier height between Al and Si affects the contact resistance. We modelled the

specific contact resistance (in $m\Omega$-cm^2) as a function of barrier height as the barrier height was varied from 0.05 to 0.55 eV. In an ideal case (without any surface states), the barrier height between n-type Si and metal is simply the difference between the workfunction of the metal (4.1 eV for Al) and electron affinity of Si (4.05 eV). The barrier height of 0.05 eV corresponds to this ideal contact. In the scenario where there is Fermi-level pinning, the barrier height is given by roughly half of the bandgap, which is ~0.55 eV for Si. The results in Fig. 55 show a negligible contact resistance at a barrier height of 0.05 eV while the value increases by more than 10^7 with a barrier height of 0.55 eV. The valence-mending passivation allows barrier heights approaching 0.05 eV, resulting in almost negligible contact resistance at the Al/Si interface.

The predicted values of specific contact resistance are much smaller than those achieved in screen-printed Ag electrode on Si solar cells and this provides two benefits. First, for the same contact area, it reduces the series resistance which improves the fill factor and efficiency. Second, it gives the cell designer the option of smaller contact area (such as in point contact cells) without suffering from severely increased series resistance, allowing a greater percentage of the surface to be passivated with dielectric films which in turn improve cell efficiencies. This is illustrated in the next paragraph.

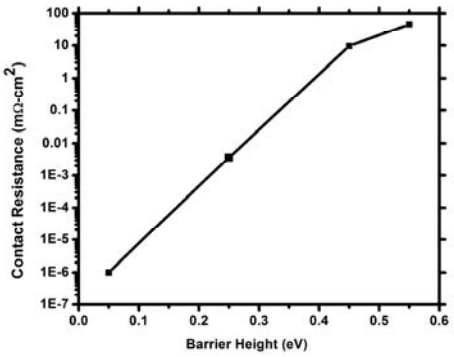


Figure 55. Effect of Schottky barrier height on specific contact resistance between Al and Si.

We investigated the effect of contact size on cell efficiency by varying the value of L1 at a constant L2 (Fig. 53). L2 was kept fixed at 1000 μm, while L1/L2 was varied from 0.005 to 0.1. The calculations were done for two barrier heights of 0.05 and 0.55 eV, with the achievable efficiency at different values of L1/L2 as the output parameter. The results are relative since a cell structure without surface texturing and antireflection coating is used to simplify the simulations.

The results in Fig. 56 show a large difference in cell efficiency with barrier heights of 0.05 and 0.55 eV. In this simulation, the maximum efficiency for the barrier heights of 0.05 and 0.55 eV are 18.4% and 9.8% respectively, with a short-circuit current of approximately of 33 mA/cm^2. The short-circuit current is lower than the state-of-the-art cells because the simulations excluded surface texturing and antireflection coating. Another significant observation is the effect of contact size on cell efficiency. In cells with a barrier height of 0.05 eV, the efficiency increases with a smaller contact size because the open-circuit voltage increases without a significant reduction in fill factor. This occurs because the relatively-high recombination Al/Si interface is replaced by a low recombination dielectric/Si interface, increasing the open-circuit voltage without

significantly increasing the series resistance. But, for the cell with a barrier height of 0.55 eV, the efficiency starts to drop even further below a certain ratio (0.05) of L1/L2.

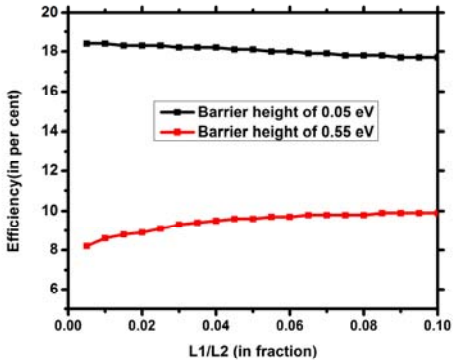


Figure 56. Effect of contact size on cell efficiency. L1 is the width of the Al strip. L2 is the total width of the simulated structure.

In conclusion, the device modeling results illustrate the potential of valence-mending passivation. The results show that in a cell where the metal is contacting lightly-doped Si, the barrier height at the metal/Si interface is one of the single most important device parameters. Valence-mending passivation allows a means to alter the barrier height and through a suitable selection of metal/Si combination, it is possible to fabricate cells with negligible contact resistance. In addition, it is interesting to note the remarkably-high efficiency improvement that is feasible through the manipulation of barrier height.

Table 5. Performance parameters of a point back contac cell, DI0205-09A.

Efficiency	J_{SC}	V_{OC}	R_{series}	Fill Factor	R_{sheet}
13.4%	32.5 mA/cm^2	575 mV	1.3 Ω-cm^2	71.7%	86 Ω/□

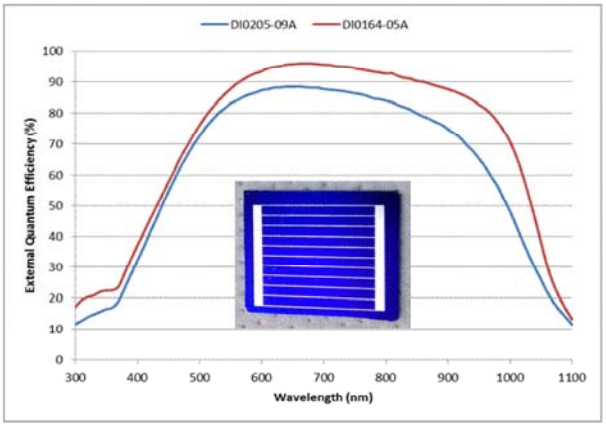


Figure 57. External quantum efficiency of point contact cell (DI0205-09A) vs. >15% cell (DI0164-05A). Inset shows a photograph of cell DI0205-09A.

4.2 Fabrication & measurement of point back contact cells

Further progress was made on developing a baseline process flow for point back contact cells. A single device (DI0205-09A) was fabricated with an efficiency of 13.4% with all-Al contacts. Table 5 presents the performance parameters of this cell (visible in the inset of Fig. 57). A simple sequence of photolithographic steps was used to produce

a grid of contact windows measuring 100×100 μm^2, spaced 1000 μm apart. The remainder of the back surface was passivated with ~125 nm of SiN_x. Fig. 57 presents the external quantum efficiency of this cell as well as the current champion cell from the baseline process (DI0164-05A). The point contact cell has poor performance in short wavelengths and low open-circuit voltage. These results suggest an insufficient etch back of the B-rich layer after B diffusion.

Ⅴ. Grain Boundary Passivation (Task 5.0 & Task 11.0)

Although we have demonstrated surface passivation of multicrystalline Si by ex-situ and in-situ cleaning along with a two-step passivation recipe, significant recombination still happens at its grain boundaries. Passivation of grain boundaries in multicrystalline Si by S was investigated. Our objective was to increase the efficiency of multicrystalline-Si cells by minimizing the recombination at grain boundaries.

5.1 Flow chart for grain boundary passivation

To conduct grain boundary passivation for multicrystalline Si, a quartz tube furnace has been setup. The ex-situ cleaning recipe for multicrystalline Si was the same as mentioned in Table 1. Fig. 58 is the flow chart for grain boundary passivation.

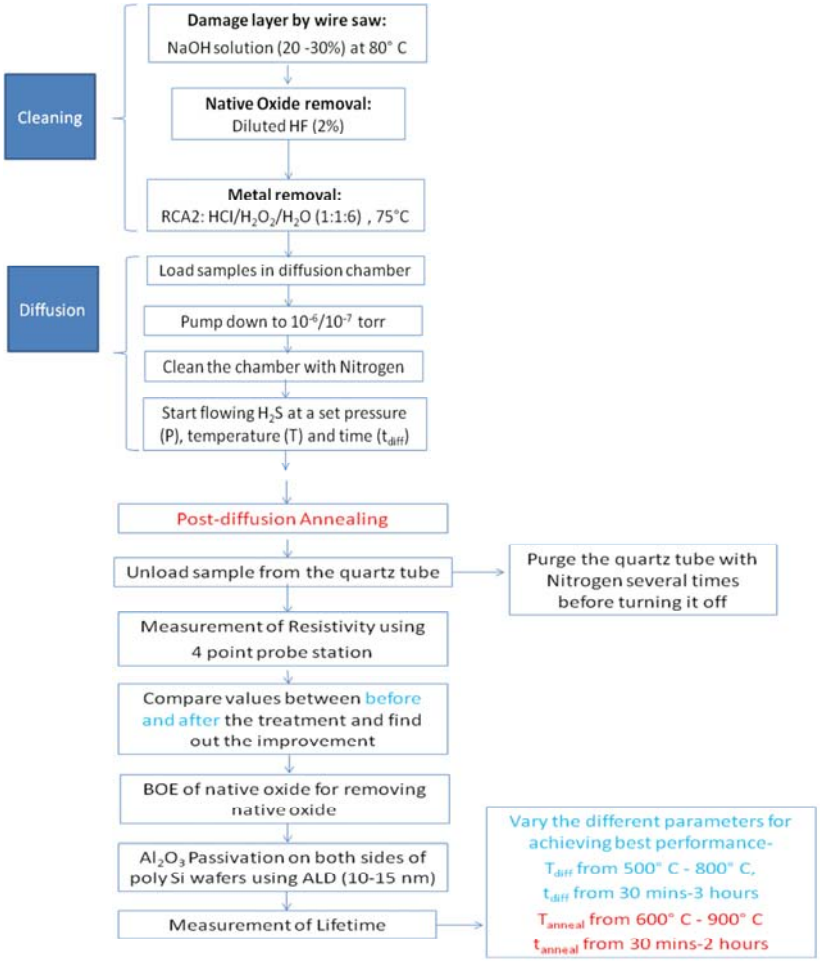


Figure 58. Flow chart for grain boundary passivation in multicrystalline Si.

5.2 Results of grain boundary passivation

Before passivation, multicrystalline-Si samples were thoroughly cleaned. Before loaded into the furnace, the samples were dipped in 2% HF for 30 s. When the pressure in the furnace reached 5×10^{-6} Torr, the furnace was heated to a preset temperature. At the temperature, the pump was stopped and the furnace sealed. H_2S was then introduced to 700 Torr. The furnace was maintained at the temperature and pressure for 20, 30 or 40 min to diffuse sulfur in the grain boundaries. After passivation, both sides of the p-type samples were deposited with 10 nm of Al_2O_3 by atomic layer deposition. Minority carrier lifetime of the samples was measured with a Sinton lifetime tester.

We first examined the effect of diffusion temperature and time on minority carrier lifetime. Fig. 59 shows the lifetime gain as a function of diffusion temperature for 20 and 40 min. Lifetime gain is defined as τ/τ_0, where τ is the measured lifetime and τ_0 is the lifetime of the starting wafer. All the samples in Fig. 59 were from the same wafer so the results are directly comparable. Passivation improves the lifetime by about an order of magnitude. The most noticeable feature of Fig. 59, however, is the two peaks in lifetime gain: one is at ~450°C and the second at ~550°C.

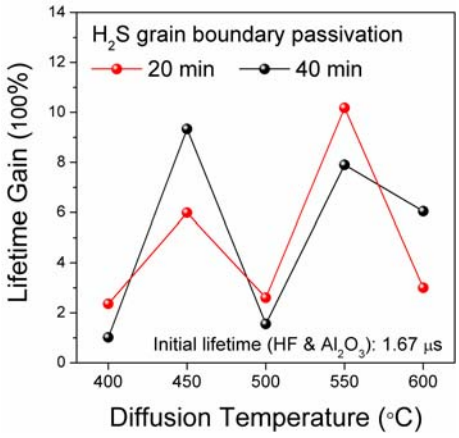


Figure 59. Minority carrier lifetime gain as a function of diffusion temperature for different diffusion times.

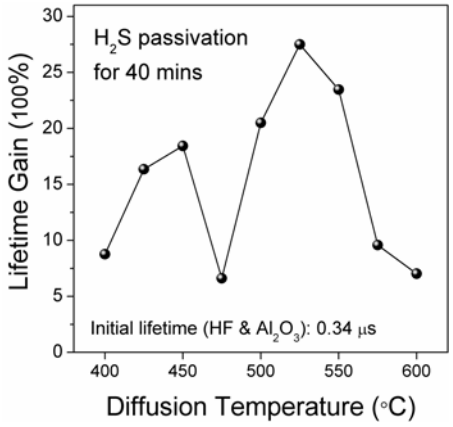


Figure 60. Minority carrier lifetime gain as a function of diffusion temperature with a small temperature interval.

To confirm the two peaks in Fig. 59, the same experiment was repeated with another

multicrystalline-Si wafer. As shown in Fig. 60, the minority carrier lifetime gain still shows two peaks at roughly the same temperatures, ~450°C and ~550°C. In this experiment, the lifetime gain at 550°C is ~2800%. It suggests termination of a significant portion of the dangling bonds at the grain boundaries by H_2S, thus the effectiveness of H_2S in grain boundary passivation.

These significant results raise two questions:

1. Why there are two peaks in lifetime gain?
2. Is the effect due to H or S in H_2S?

Another experiment was carried out in which multicrystalline-Si samples were annealed in H_2 instead H_2S to eliminate any effect from S. As shown in Fig. 61, H_2 passivation shows inferior lifetime gain (~300%) compared with H_2S (~1000%). Most importantly, there is only one peak at ~400°C. These results suggest that S is responsible for the second peak at ~550°C in Figs. 59 and 60, and S is more effective in grain boundary passivation than H.

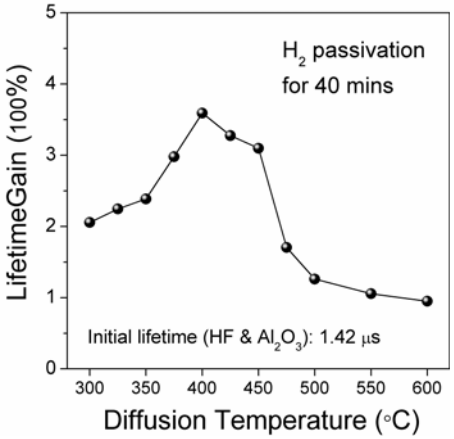


Figure 61. Minority carrier lifetime gain as a function of diffusion temperature in H_2.

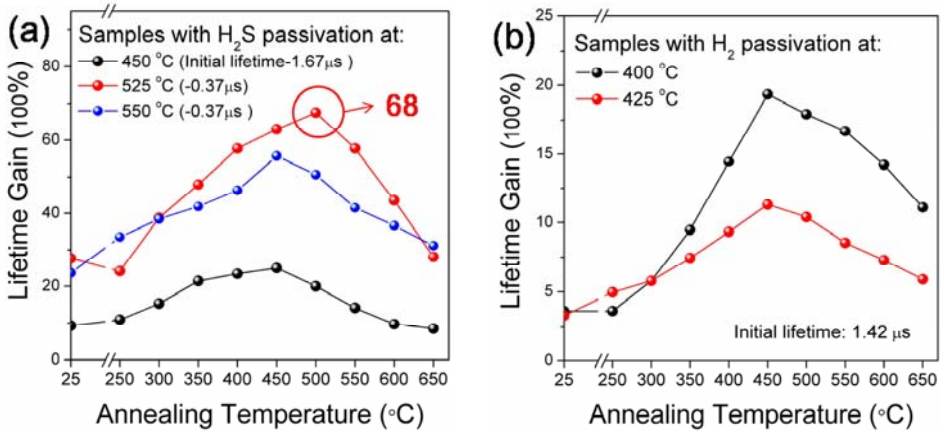


Figure 62. Minority carrier lifetime gain as a function of post-annealing temperature. (a) Samples annealed in H_2S. (b) Samples annealed in H_2.

Post-annealing in air was performed on the best samples in Figs. 59, 60 and 61. Fig. 62 shows the lifetime gain as a function of post-annealing temperature for both H_2S and H_2 annealed samples. Lifetime gain for all the samples is improved after post-annealing.

For both H_2S and H_2 annealed samples, a similar trend is observed, i.e. the lifetime first increases and then decreases with temperature, with a peak at ~450°C. It is noted that the samples annealed in H_2S at 525°C and post-annealed at 500°C has a remarkable lifetime gain of 6800%! This result is way above the original goal in the proposal, i.e. 10% improvement in lifetime.

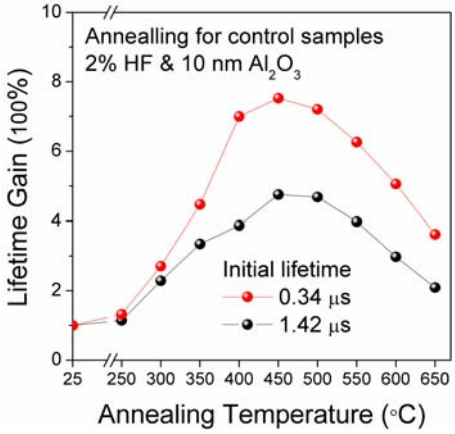


Figure 63. Minority carrier lifetime gain as a function of post-annealing temperature for control samples without H_2S or H_2 annealing.

For comparison, post-annealing was performed on control samples with 10-nm Al_2O_3 surface passivation but without H_2S or H_2 annealing. As shown in Fig. 63, post-annealing results in a peak lifetime gain of ~800%. Its dependence on post-annealing temperature is similar to Fig. 62. Therefore, the additional lifetime gain by post-annealing in Fig. 62 is attributed to the Al_2O_3 layers on the p-type samples. We conclude that before post-annealing, S passivation of grain boundaries is the dominating factor in lifetime gain, while after post-annealing, surface passivation by Al_2O_3 is responsible for the further lifetime gain.

Ⅵ. All-Al PV cell w/ Valence-Mending Passivation (Task 9.0)

6.1 Al/valence-mended Si(100) contact resistance

The specific contact resistance of Al/valence-mended Si(100) contact plays a key role in cell efficiency. We carried out characterization on the contact resistance of Al/valence-mended Si(100) contact. It is reminded that there is a layer of adsorbate sandwiched between the valence-mended Si(100) surface and the Al layer when the valence-mended wafer is exposed to air (Fig. 9). Oxygen in the adsorbate layer can react with the S passivation layer at elevated temperatures and damage the passivation. It is suggested that by heating the valence-mended wafer in vacuum, the adsorbates can be driven off and a cleaner Al/valence-mended Si(100) interface can be obtained, leading to significantly-better thermal stability. Therefore, the specific contact resistance of Al/ valence-mended Si(100) contacts are studied as a function of substrate heating conditions.

A 4" n-type CZ Si(100) wafer (resistivity 2 Ω-cm) was processed through the standard clean/valence-mending passivation process and cleaved into four quarters, each of which received a different preheat cycle in the e-beam evaporator before Al deposition.

Exposure to air was minimized by storing the samples in the CVD load lock until just prior to loading into the e-beam evaporator. Resist patterns were stencil printed on the Al followed by a wet etch to create the typical transfer line method test pattern, after which thin strips were further cleaved through these patterns to isolate the test structure.

Current-voltage measurements of these test structures were all well behaved, showing clean Ohmic behavior. Using standard methods, the substrate sheet resistance and the specific contact resistance were extracted. Sheet resistance values agreed well with the four point probe measurements of the starting substrate, adding confidence to the measurements. Plots from one of the splits are copied in Fig. 64 with the other splits appearing similar in nature.

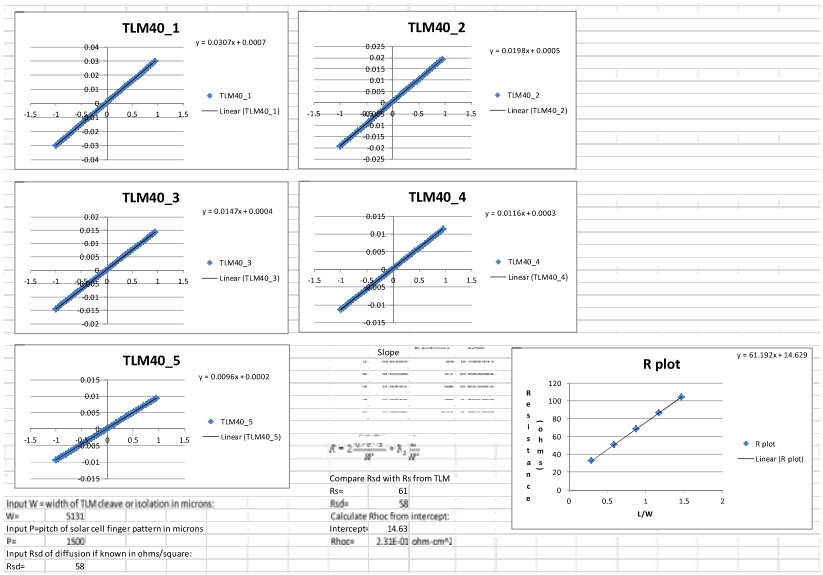


Figure 64. Current-voltage measurements of the samples and the extracted resistance.

The four preheat splits do not show a trend. Since the heater set point and the platen temperature relationship is not known, the approach taken was to preheat for a defined time (40, 67, 94 and 120 s) before initiating the evaporation. The results from each split are shown in Table 6.

Table 6. Specific contact resistance vs. e-beam preheat time

e-beam preheat time (s)	Substrate R_s (Ω/□)	Specific contact resistance (Ω-cm^2)
40	61	$2.3x10^{-1}$
67	63	$2.3x10^{-1}$
94	62	$1.6x10^{-1}$
120	64	$2.5x10^{-1}$

Following this experiment, we obtained data for the new e-beam with a similar heater arrangement which plots setpoint and thermocouple measurements of upper/lower platen surface temperatures over time as shown in Fig. 65. A closer examination of the raw data shows a ~10°C temperature rise of the lower platen surface 120 s after heater current begins to flow. This suggests that none of the splits in this experiment underwent significant preheating in the e-beam evaporator. The potential therefore exists that a more appropriate preheat process could substantially improve the contact resistance.

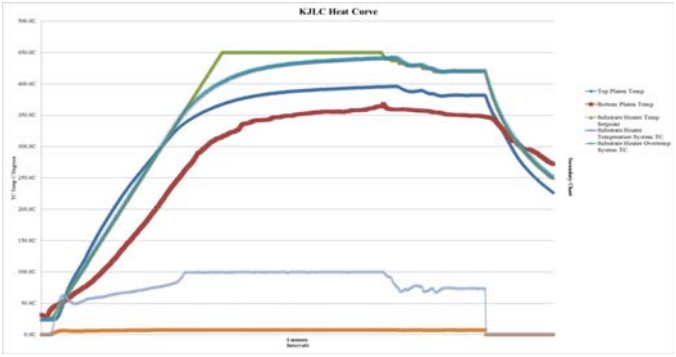


Figure 65. Setpoint and thermocouple measurements of upper/lower platen surface temperatures over time in the e-beam evaporator.

Transfer line method measurements of the specific contact resistance for e-beam evaporated Al on valence-mended lightly-doped n-type Si(100) yield an average result of 2.2×10^{-1} Ω-cm^2 with little differences between the four preheat splits. This is not sufficient for the back point contact cells now being processed. More efforts are needed on substrate heating conditions to minimize the contact resistance.

6.2 Fabrication of all-Al cell w/ valence-mending passivation

A pipe-cleaner lot (DI0185) of cells were taken through the fabrication process flow consisting of four total substrates (Fig. 66). Two substrates (samples 05, 07) were fabricated with the baseline process flow, without valence-mending passivation, as a control. The other two substrates (01, 03) were fabricated with the valence-mending passivation process.

Samples 01 and 05 were fabricated in such a way to produce four experimental cells per sample. The structure of these samples is visible in Fig. 67. Samples 03 and 07 were initially fabricated as samples to provide solely an open-circuit voltage measurement. The structure was essentially the same however the front metallization was initially not applied.

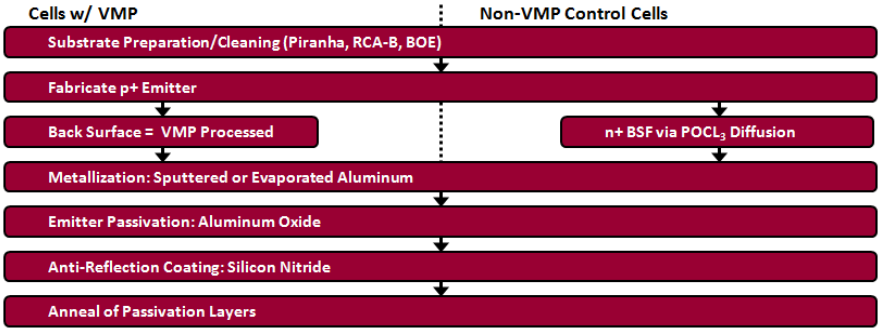


Figure 66. High-level comparison of fabrication process flows for valence-mended cells vs. baseline cells without valence-mending passivation.

Samples 01 and 05 yielded undesirably high series resistance caused by front screen printing of a resist used in an attempt to simplify the metallization process. The resulting front metal patterns were of incredibly low quality and thus their results should not be reliably considered for performance analysis.

Samples 03 and 07 were measured on a current-voltage tester to capture a 1-sun open-circuit voltage measurement. Valence-mended sample 03 yielded an open-circuit

voltage of 572 mV. Control sample 07 yielded an open-circuit voltage of 569 mV. Although the voltages were low, it should be noted that the valence-mended sample had a similar voltage as the n^+ back surface field control sample. These samples were then taken through further non-conventional processing in an attempt to make functional cells. This required usage of: negative photoresist, wet etch through the front passivation layer and subsequent sputtering and liftoff of front Al. The resulting cells had very low shunt resistance and thus low efficiency.

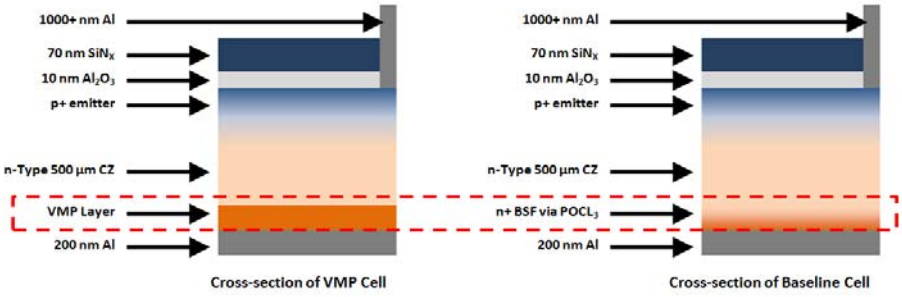


Figure 67. Cross-sectional structure of valence-mended cell and baseline cell without valence-mending passivation.

A new batch of cells has been fabricated, incorporating lessons learned from the first batch (DI0185), primarily usage of the reliable metallization process that is standard in the baseline process. In this new batch, a total of eight samples are fabricated: four valence-mended samples and four control samples passivated with an n^+ back surface filed. Further, two samples each of the four are fabricated with back point contacts. The other two samples are fabricated with full back contacts. The efficiency of these cells is ~13%.

Deliverable / Milestone Deviations

In this project we have met or surpassed most of the milestones and deliverables. The biggest deviation in deliverable is, instead of a low-temperature Al paste, we delivered an Al electroplating process. This is Task 3.0 and Task 8.0. Although not planned, the Al electroplating process is actually superior to a low-temperature Al paste in terms of process cost, manufacturability and performance. The target performance for the Al paste was: 1) firing temperature below 400°C and resistivity below 1.5 times that of screen-printed Al. What we have delivered with electroplated Al is: 1) firing temperature as low as 200°C and 2) resistivity ~0.5 times that of screen-printed Al. In addition, the Al electroplating process can take advantage of the peripheral technologies developed for the Cu electroplating process such as electroless Ni plating and laser patterning of the SiN_x layer. This should speed up the commercialization of the Al electroplating process.

For Task 9.0, we are a little short of the target. Instead of a 15% all-Al cell, we delivered a 14.8% all-Al cell. Our analysis suggests the low fill factor as the primary reason for the below-target efficiency, which is caused by damage to the emitter junction by the photolithographic step in cell fabrication. Multiple rounds of cell fabrication have been carried out, and further improvement in cell efficiency may require less-damaging laser patterning and/or electroless Ni plating. ASU has none of these capabilities. One of the ASU students will join imec in Belgium in summer 2015 for a 6-month internship. This will provide us access to laser patterning and electroless Ni plating capabilities. We expect the efficiency of the all-Al p-type cell to approach 18% in ~12 months.

We are behind the efficiency target for Task 10.0 by ~2% absolute. This is due to a number of factors. The specific contact resistance between Al and valence-mended Si(100) is unexpectedly high, in the 10^{-1} Ω-cm^2 range. At this time we do not quite understand the reason, but suspect the adsorbate layer sandwiched between Al and Si when the valence-mended wafer is exposed to air. The quality of valence-mending passivation is also an issue, as there is no direct verification of the passivation quality. All the current-voltage, capacitance-voltage and activation-energy measurements are indirect methods for passivation quality. Finally, only two fabrication rounds were carried out on point back contact cells with valence-mending passivation, so there are still rooms for process and device optimization.

In the last 6 months of the project, the funds were enough to support one more PhD student. The student was assigned to a project directly related to terawatt-scale deployment of crystalline-Si solar cells, i.e. recycling of Si cells. Solar-grade Si can be recycled from end-of-life crystalline-Si solar cells and this recycled Si can be a new feedstock for the growth of Si ingots. A simple green process with low energy input has been developed for this purpose. It involves three chemicals, HCl, HF and NaOH. The HCl and NaOH cam form benign NaCl solutions, and the only chemical waste which requires some effort is HF. The maximum process temperature is 50°C, which can be achieved by solar heating. More importantly, over 90% of the Si in the original cells is recovered within 30 min, and a simple technique to monitor the removal of heavily-doped layers from Si cells is demonstrated.

Fig. 68 shows the reciprocal sheet resistance, by a four-point probe, of a Si in a 3% NaOH aqueous solution at 50°C. The sheet resistance was measured from both the front and back sides of the cell. With the p/n junction in the cell, the front sheet

resistance (red dots) is from the emitter, while the back sheet resistance is from the back surface field and the base. At ~15 min, the front and back sheet resistances coincide, indicating that the emitter is completely removed and we are measuring the remaining base and back surface field. As the back surface field is thinned down, the sheet resistance increases. At ~30 min, the slope changes indicating that the back surface field is completely removed. The remaining base meets the specifications of solar-grade Si and can be directly fed into Si ingot growth.

Fig. 69 shows the remaining percentage weight of Si from the starting cell as a function of etch time. 30 min leaves ~91% of the Si in the cell, i.e. over 90% of the Si is recovered for a Si cell.

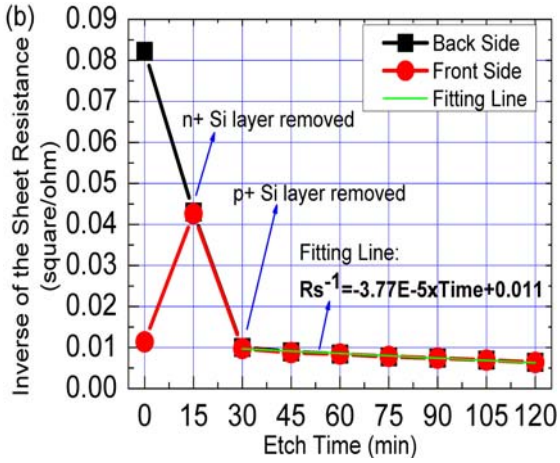


Figure 68. Reciprocal sheet resistance of a Si cell in a 3% NaOH aqueous solution at 50°C, which clearly indicates the time to remove heavily-doped emitter and back surface field.

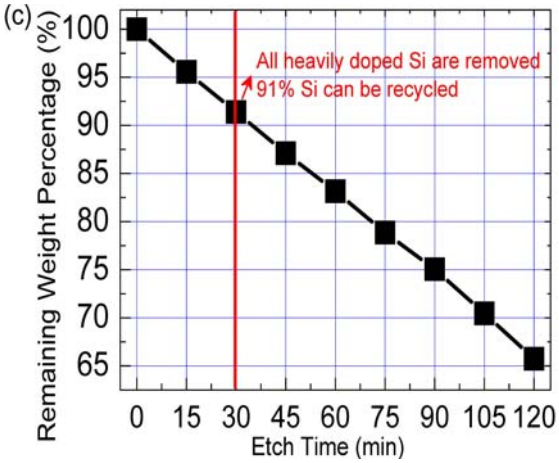


Fig. 69. Remaining percentage weight of a Si cell in a 3% NaOH aqueous solution at 50°C. 30 min leaves ~91% of the Si in the starting cell.

Products Developed Under the Award

Ⅰ. Patents / Licensing Agreements

1. M. Tao, W.-C. Sun and X. Han, Aluminum Electroplating of Solar Cells, U.S. patent application filed by ASU in November 2014
2. S. Bowden, T. Reblitz, B. Dauksher and C. Tracy, Silicon Devices Using Amorphous Silicon Dopant Sources and Deposited Contacts, Invention Disclosure filed with ASU in 2013

Ⅱ. Honors and / or Awards

1. A poster entitled “Zn as the protective layer for Cu electrode in wafer-Si solar cells”, by X. Han, B. Zhou, D. Yang and M. Tao, was nominated for the best poster at the 40th IEEE Photovoltaic Specialist Conference in Denver in June 2014.
2. An invited talk by M. Tao entitled “Valence-mending passivation of Si(100) surface: principle, practice and application” will be presented at GADEST 2015 - Gettering and Defect Engineering in Semiconductor Technology (Bad Staffelstein, Germany, 2015).
3. An invited talk by M. Tao entitled “Implications of resource limitations to terawatt thin-film photovoltaics” was presented at the 20th International Workshop on Active-Matrix Flat Panel Displays and Devices (Kyoto, 2013).
4. An invited talk by M. Tao entitled “Roadblocks and bottlenecks to a sustainable silicon photovoltaic industry: was presented at China Semiconductor Technology International Conference (Shanghai, 2014).
5. An invited talk by M. Tao entitled “Resource limitations to terawatt-scale solar cells”, 3M Company (St Paul, MN, 2012).
6. An invited talk by M. Tao entitled “Terawatt silicon photovoltaics: bottlenecks and our approaches”, Hanwha Solar America (Santa Clara, CA, 2013).
7. An invited talk by M. Tai entitled “Natural resource limitations to terawatt solar photovoltaics”, IEEE Phoenix Chapter (Tempe, AZ, 2013).
8. An invited talk by M. Tao entitled “Natural resource limitations to terawatt solar photovoltaics”, Northern Arizona University Engineering Seminar Series (Flagstaff, AZ, 2014).

Ⅲ. Publications

1. Book title: Terawatt Solar Photovoltaics: Roadblocks and Opportunities

   Author: Meng Tao

   Publisher: Springer (2014)

   ISBN: 978-1-4471-5642-0
2. H. Zhang, A. Saha, W.-C. Sun and M. Tao, “Characterization of Al/Si junctions on Si(100) wafers with chemical vapor deposition based sulfur passivation”, Applied Physics A **116**, 2031-2038 (2014)

3. W.-C. Sun, X. Han, H. Zhang, C. J. Tracy and M. Tao, “Non-vacuum electroplated Al for n-side electrode in Si solar cells”, in Proceedings of the 40th IEEE Photovoltaic Specialists Conference (Denver, 2014)
4. X. Han, B. Zhou, D. Yang and M. Tao, “Zn as the protective layer for Cu electrode in wafer-Si solar cells”, in Proceedings of the 40th IEEE Photovoltaic Specialists Conference (Denver, 2014)
5. W.-C. Sun, X. Han and M. Tao, “Electroplating of aluminum on silicon in an ionic liquid”, Electrochemical Letters, in press
6. A. Saha, H. Zhang, W.-C. Sun and M. Tao, “Grain boundary passivation in multicrystalline silicon using hydrogen sulfide”, submitted to ECS Journal of Solid State Science and Technology
7. C. S. Tao, J. Jiang and M. Tao, “Natural resource limitations to terawatt-scale solar photovoltaics”, in Proceedings of 20th International Workshop on Active-Matrix Flat Panel Displays and Devices (Kyoto, 2013)

Ⅳ. Presentations

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3. A. Saha, H. Zhang, W.-C. Sun, and M. Tao, “A new method for bulk passivation of multicrystalline-Si by sulfur”, submitted to the 42nd IEEE Photovoltaic Specialist Conference (New Orleans, 2015)
4. M. Tao, “Substitution of silver electrode in wafer-Si solar cells by an abundant metal”, China Photovoltaic Technology International Conference (Shanghai, 2012)
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Ⅴ. Software

N/A

Ⅵ. Other

N/A