Final Scientific Report for DOE/EERE

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Executive Summary

This project aimed to demonstrate increased electronic coupling in silicon nanostructures relative to bulk silicon for the purpose of making high efficiency intermediate bandgap solar cells using silicon. To this end, we formed nanowires with controlled crystallographic orientation, small diameter, <111> sidewall faceting, and passivated surfaces to modify the electronic band structure in silicon by breaking down the symmetry of the crystal lattice. We grew and tested these silicon nanowires with <110>-growth axes, which is an orientation that should produce the coupling enhancement. Although we did not observe an intense optical signal indicative of the effect that we were trying to measure, we did expand the knowledge base of silicon nanowires. Throughout the project, we extended the capabilities of nanowire processing using gold catalyzed VLS nanowires, aluminum catalyzed VLS wires, and silver enhanced etched wires. For gold catalyzed wires, we pushed the diameters smaller than what is normally published in the literature. In addition, we characterized regimes that allowed for control over the crystallographic orientation of the nanowires. Aluminum VLS is less established than gold VLS, and so we explored much more experimental space that had never been explored. We learned how to make the runs more reproducible by adding a conditioning step. We found processing conditions that grow wires epitaxial and we learned how to control the crystallographic orientation of these wires. For the Au VLS wires we characterized them with TEM and learned that many of the wires are faceted. For both Au and Al VLS, we determined that supersaturation controlled the crystal growth, which helps us better understand the growth mechanism of the nanowires.

For metal enhanced etching, we developed a two-step process that gives lower defect longer nanowires from this process. We also developed methods to passivated our nanowires.

This report details some of our studies and proposes future methods of exploring Bandgap Activation.

Comparison of Proposed versus Realized Project Goals

The following table summarizes the project's proposed goals versus actual progress for each task. Deviations between an Initial negotiated deliverables / milestones and an actual deliverable / milestone are discussed in the "Deliverable / Milestone Deviations" section of the Technical Narrative.

Task #	Task description	Initial Negotiated Deliverable / Milestone	Actual Deliverable / Milestone
1.1	**Study growth direction with Au catalyst**	**Demonstrate well-ordered <110> Si nanowire arrays using Au catalysts with wire diameters <100 nm**	**Demonstrate well-ordered <110> Si nanowire arrays using Au catalysts with wire diameters <100 nm**
1.2	**Study of growth direction with Al catalyst**	**Demonstrate well-ordered <110> Si nanowire arrays using Al catalysts**	**Demonstrate well-ordered <110> Si nanowire arrays using Al catalysts**
1.3	**Prepare samples with varying nanowire diameters**		**complete**
1.4	**Investigate the effect of nanowire diameter, catalyst type, and post growth H2 annealing on sidewall faceting of nanowires**	**Develop a method to obtain <110> oriented Si nanowires with well-defined (111) sidewall facets**	**Develop a method to obtain <110> oriented Si nanowires with well-defined (111) sidewall facets**
2.1	**Characterize the absorption and photoluminescence properties of <111> and <110> oriented Si nanowire arrays as a function of wire diameter, catalyst type, and surface passivation**		**complete**
2.2	**Two photon measurements**		
3.	**Studies of surface passivation**	**Develop methods to conformally coat the Si nanowire sidewalls with passivation layers**	**Develop methods to conformally coat the Si nanowire sidewalls with passivation layers**

Technical Narrative

Project Objective

This project aimed to demonstrate increased electronic coupling in silicon nanostructures relative to bulk silicon for the purpose of making high efficiency intermediate bandgap solar cells using silicon. To this end, we formed nanowires with controlled crystallographic orientation, small diameter, <111> sidewall faceting, and passivated surfaces to modify the electronic band structure in silicon by breaking down the symmetry of the crystal lattice. We grew and tested these silicon nanowires with <110>-growth axes, which is an orientation that should produce the coupling enhancement.

Background

The efficiencies of traditionally single bandgap solar cells are theoretically limited to around 31%. One approach to overcome this limitation is to implement an Intermediate Bandgap (IB) Solar Cell (IBSC), a single junction solar cell with an intermediate band inside the bandgap. In an IBSC, photons with energy below the valence to conduction bandgap energy can excite electrons from the valence band into the intermediate band. Another photon can then excite the electron from the intermediate band into the conduction band. Thus the intermediate band acts as a stepping-stone for the electron, and thus, two sub-bandgap photons can together contribute to the photocurrent, producing electricity from sub-bandgap radiation. If the energies of the conduction, valence, and intermediate bands are spectrally matched to the solar spectra, the IBSC will have a higher obtainable short circuit current density (J_{sc}) than a single bandgap solar cell. In addition, the ideal bandgap for an IBSC is larger than for a single bandgap solar cell and therefore also has a higher possible open-circuit voltage (V_{oc}). As a result of the higher J_{sc} and V_{oc}, the theoretical maximum of an IBSC is over 60% under full concentration and is higher than that of a double tandem cell under identical illumination conditions [Luque 2010]

Nanostructuring turns Si into an IB material by breaking down the symmetry of the lattice. By controlling the crystallographic orientation of our nanowires, we can control the coupling of indirect states, an approach we refer to as Bandgap Activation (BA). When the lattice of a crystal is finite, such as in a nanowire, the infinite periodic potential assumption used to derive the E vs. k diagrams is no longer valid. The truncation of the lattice results in mixing of certain electronic states, which in bulk contain electrons moving in different directions and are therefore represented by different symmetry points in the Brillouin Zone. This effect is analogous to the mixing of electronic states across a heterojunction. [Malhiot 1983, Chang 1985] Classically, Bandgap Activation can be thought of as bouncing a ball off of a wall and using the angle of the wall to control the direction that the ball bounces. By controlling the crystallographic orientation of the nanowire, we are effectively controlling the direction of the wall, and the mixing of states can be controlled and predicted by group theory. The direction of the interface or truncated lattice controls which bulk states mix; and the strength of the optical absorption increases the smaller the crystal. Hence, Bandgap Activation offers a new method of bandgap engineering. It is possible, and even likely, that the changes resulting from a truncated lattice in nanostructured materials dominates many materials' electro-optical properties and is a larger effect than quantum confinement at some wire diameters.

In silicon, enhancement of the gamma point valence band to L-point conduction band electronic transition is needed to realize a solar spectra matched IBM. Si has an indirect bandgap at the Δ-point, (at 1.12eV) and a second indirect band gap at the L point (at 1.6-2.0 eV [Foreman 1974 and Masovic 1983]) Fortuitously, these energies are very close to the ideal energy values for an IBSC. Furthermore, the theoretical band calculations of Si predict no direct non-radiative decay route between the carrier pockets at the L pt. and the Δ pt. Hence carriers excited to the L pt. have a chance of leaving through a contact before decaying to the intermediate band. So, if the optical transition probabilities between the valence band (Γ pt.), the intermediate band (Δ pt.), and the conduction band (L pt.) can be varied and optimized, an IBM can be made out of silicon.

The gamma-point is <000> in the Brillouin zone whereas the L-point has electron pockets in the <111> directions. In order for the surface of the nanowire to break the symmetry requirements of this transition, the nanowire needs to have an interface in the <111> direction, and therefore

the wire's longitudinal axis must be perpendicular to the <111> (or one of the other 3 L-points). Consequently, Si nanowires with a <110> growth direction should exhibit enhanced gamma to L point optical transitions compared to nanowires that are aligned along the <111> or <100> directions. Si will become an IB material if the transition can be enhanced to a level at which photons with energies above the L pt. will be absorbed into this higher energy band, leaving photons with energies less than the L pt. to excite electrons to the Δ pt. electron band. Si nanowires aligned in the <110> direction that assume an equilibrium shape predicted by a Wulff construction [Hong 2000] have four surfaces in equivalent <111> directions, while <111> surfaces are missing for nanowires along the <111> and <100> directions. Hence, nanowires in the <110> direction should show an extra absorption and photoluminescence (PL) peak near the energy of the Γ-L pt. electronic transition relative to wires in the <111> and <100> directions. In addition, since the coupling is related to the mean-free path of carriers in the material, the enhancement is also expected to be strongly dependent on the nanowire diameter and doping level in addition to faceting and orientation.

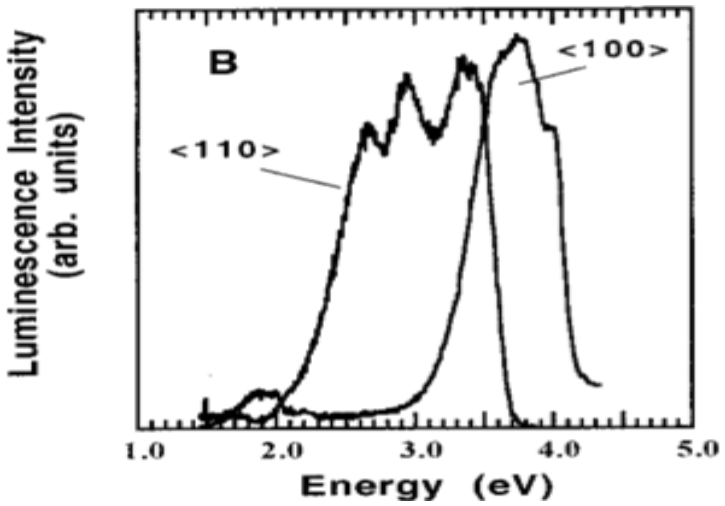


Figure 1: PL of nanowires dispersed in hexane with excitation energies of 4.46eV (277 nm <100>) and 4.12eV (300nm, <110>) (from reference **Error! Bookmark not defined.**)

Previously published PL of single Si nanowires, shown in Figure 1, reveals a strong crystallographic orientation dependence, with a large PL signal at the energy of the Γ to L pt. transition for <110> wires and not for <100> wires [Holmes 2000]

Significant Accomplishments

Task 1.1 - Study growth direction with Au catalyst

Gold (Au) catalyzed VLS growth of silicon nanowires is by far the most extensively studied method for making silicon nanowires. However, for other applications, the crystal orientation is not important, the diameters can be larger than what our project requires, and the sidewalls need not be faceted. Thus we focused our work on obtaining smaller diameter wires, with controlled crystallographic orientation, and with faceted sidewalls.

The growth of VLS wires has two basic steps: depositing the metal catalyst and growing the wires in a chamber with a precursor. For Au-VLS wires, we experimented with two methods of depositing metal catalysts – thin films of gold and Au colloids/nanoparticles. Thin films are separated into discrete catalyst particles by heating while the Au colloids are deposited as nanoparticles. In addition, we experimented with two reaction chemistries – SiH_4 and $SiCl_4$. The SiH4 and the SiCl4 have much different chemistries since the HCl is a by-product when SiCl4 is used and not when SiH4 is used. The presence of HCl changes the reaction. We were able to get epi growth with SiH4 chemistry, but we were not able to grow wires in the <110> direction. However, with SiCl4, we were able to get nicely formed wires, with a uniform diameter across the length of the wire. So even though SiH4 is most commonly used for gold VLS, all of the gold VLS growth described in this section was done with SiCl4. In addition, we were able to control crystallographic orientation with this chemistry.

Au nanoparticle catalyst development

Our most successful method for producing <110>-oriented nanowires has been using thin films of Au for the catalyst and $SiCl_4$ for the precursor. The nanowires synthesized in this method are well-oriented and can even have the desired sidewall faceting. However, we expect the effects of Bandgap Activation™ to become observable at smaller diameters than those obtainable via thin films of gold. In addition, the agglomerated Au thin film creates a wide distribution of catalyst diameters. Thus, in an effort to grow a tighter distribution of smaller diameter nanowires, we systematically studied a growth recipe for growing <110> nanowires from Au nanoparticles. This involved exploring nanoparticle deposition techniques, the size evolution as a function of annealing temperature and particle density, and a growth series over various temperatures and substrates. This method of depositing nanoparticles of Au ended up not being as fruitful as depositing thin films of Au, but we include the results here from completion.

We can control the catalyst dispersion and, to some extent the nanoparticle interaction with the silicon substrate through the nanoparticle deposition method. While, VLS-grown nanowire diameters correlate with the starting catalyst diameters, the nanowire diameters are larger than the catalysts diameters. This difference can be caused by lateral growth, Au nanoparticle clustering, or volume expansion when incorporating Si to reach the eutectic composition. The last is inherent to VLS growth. The first can be mitigated by tuning the growth to avoid thin film deposition conditions. Au particle clustering occurs as the substrate heats up, allowing the Au to migrate across the Si surface. For a given growth temperature, agglomeration can be limited by increasing the pitch between particles.

We looked at a number of nanoparticle deposition methods and compared the initial particle dispersion and the average particle size after annealing in order to better control nanowire diameter. In all cases, the anneals were performed under H_2 for 5 minutes.

We used two methods to deposit the nanoparticles. In the first method, the particles were self-assembled on silicon wafers with native oxides using block co-polymer lithography. The supporting polymer was subsequently removed by an oxygen plasma and the Au transformed from salt to metallic form by baking. As seen in Figure, the as-deposited nanoparticle diameters were fairly uniform around the 30nm diameter target with ~100nm pitch. At 700°C, there was little to no change, however at higher temperatures, the particles have clearly begun to agglomerate. The larger particles appear to gouge tracks into the substrate surface.

In the second method, citrate-stabilized Au colloids (Ted Pella, Inc) were diluted in a hydrofluoric acid mixture and pipetted onto the substrates. The solution was rinsed off after a set residence time. Controlling the dilution ratio allows control over the density of particles deposited. We found the behavior of particles upon annealing differed depending on the substrate. While the Au nanoparticles on SiO_x do not agglomerate as readily as the Au does on Si substrates (Figures 3 and 4), the growth on SiO_x using $SiCl_4$ has proven challenging. Nanowires from Au nanoparticles on oxidized silicon substrates did not grow with $SiCl_4$ between 975-1050°C using otherwise standard conditions from Au thin film catalyzed growth.

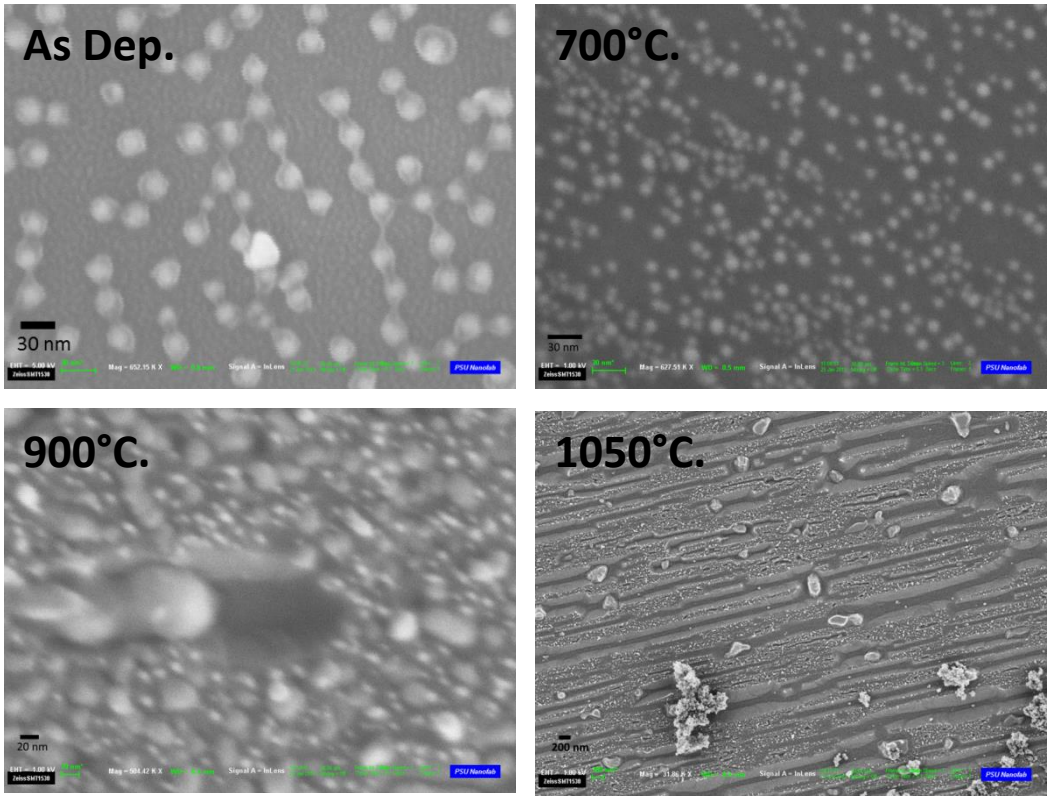


Figure 1: Evolution of Au-nanoparticles as-deposited and as a function of annealing temperature (700°C, 900°C, 1050°C). The nanoparticles were deposited on Si substrates by a block-copolymer method (Hanako Materials, La Canada Flintridge, CA).

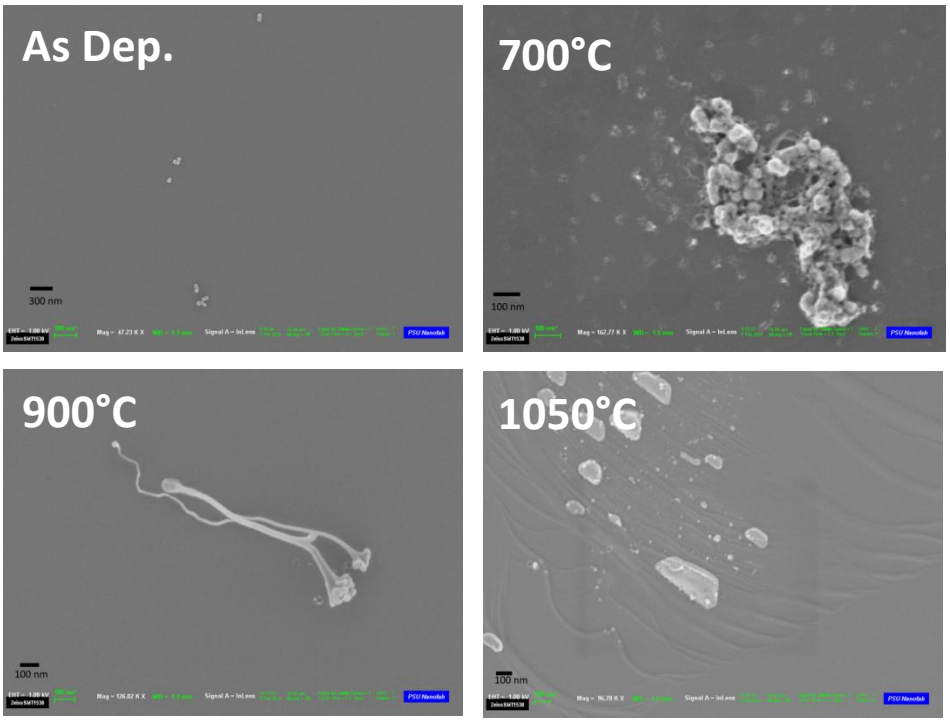


Figure 3: 50nm Au nanoparticles deposited Si substrates at PSU, shown as-deposited and after 700°C, 900°C, and 1050°C anneals.

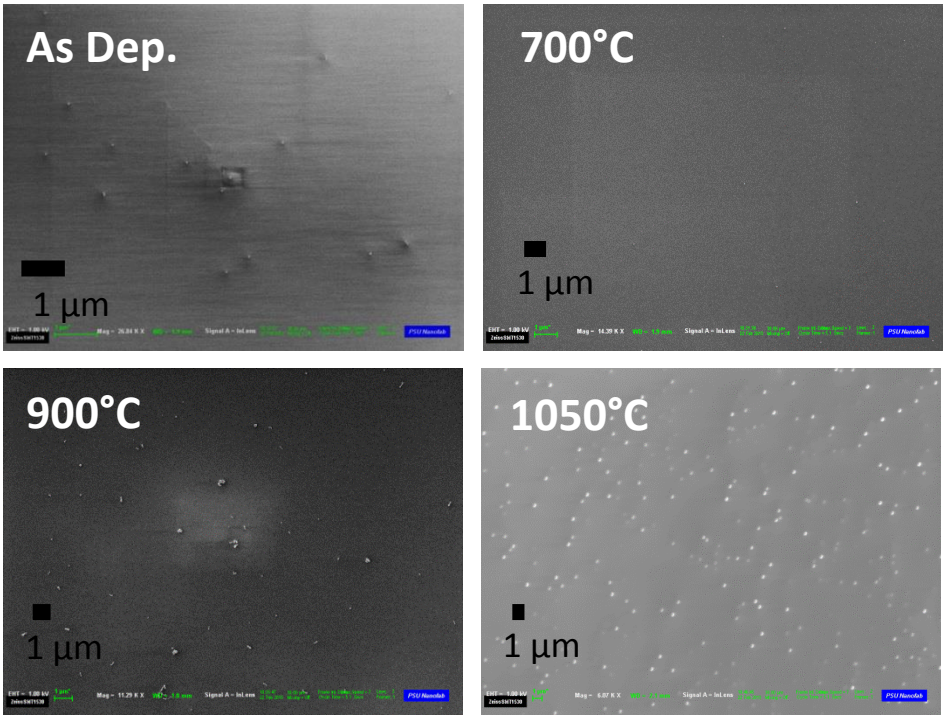


Figure 4: 50nm Au nanoparticles deposited SiO_x substrates at PSU, shown as-deposited and after 700°C, 900°C, and 1050°C anneals.

Au Source	SiNW diameter [nm] *Std dev.*	Average nanoparticle diameter [nm] *Standard deviation*			
			Anneal temperature		
		As-deposited	700°C	900°C	1050°C
1 nm Au Thin Film	136 +/- 46 nm				
50 nm Au Nanoparticles	94 +/- 28 nm	50 *6*	50	94	135
5 nm Au Nanoparticles	37.4 +/- 13 nm				

Table 1: Au nanoparticle diameters as-deposited on Si and after 700°C, 900°C, and 1050°C anneals starting from a 50nm Au nanoparticle. The resultant average nanowire diameter from standard growth conditions are also listed for comparison.

Although nanoparticles should allow us to make smaller diameter nanowires, working with the nanoparticles has proven to be more challenging than with thin films. The gold colloids, obtained commercially (British BioCell International/Ted Pella), are stabilized in a citrate solution that is believed to prevent the substrate interaction necessary to achieve epitaxial growth. We therefore focused on Au thin film VLS.

Au thin film catalyst development

Our most successful method of growing Au VLS wires was by depositing a thin film of gold prior to growth and using this metal to catalyze growth. For this technique, we determined that three parameters were particularly important for controlling orientation and obtaining small diameter wires: chemical composition, pressure, and catalyst film thickness. Thus we performed systemic studies on how the growth parameters change the resultant nanowires with a focus on silicon tetrachloride ($SiCl_4$) partial pressure and Au catalyst film thickness. The goal was to identify the region in parameter space where small diameter <110>-oriented nanowires result with high yield. In the images shown, all samples were grown on <110> silicon wafers, therefore vertical nanowires are in the desired <110> direction.

The effect of growth temperature on nanowire orientation was initially investigated. SiNWs were grown by varying the reactor temperature from 900°C to 1050°C in 50°C increments using a constant $SiCl_4$ partial pressure of 3 Torr. As shown in Figure 5(a) and (b), SiNWs grown at 900°C and 950°C grow at an angle of ~57° relative to the (110) Si surface which is consistent with a <111> growth direction. As the temperature is raised to 1000°C, however, vertical SiNWs appear which would be consistent with a <110> growth direction (Figure 5(c)). The yield of <110> SiNWs further increased at 1050°C (Figure 5(d)). Increasing the growth temperature an additional 50°C to 1100°C resulted in a significant decrease in the NW growth rate (not shown). These results are consistent with the early report of Wagner and Doherty which

demonstrated <110> Si whiskers by VLS growth using $SiCl_4$ at a growth temperature of 1050^oC. [Wagner 1968]

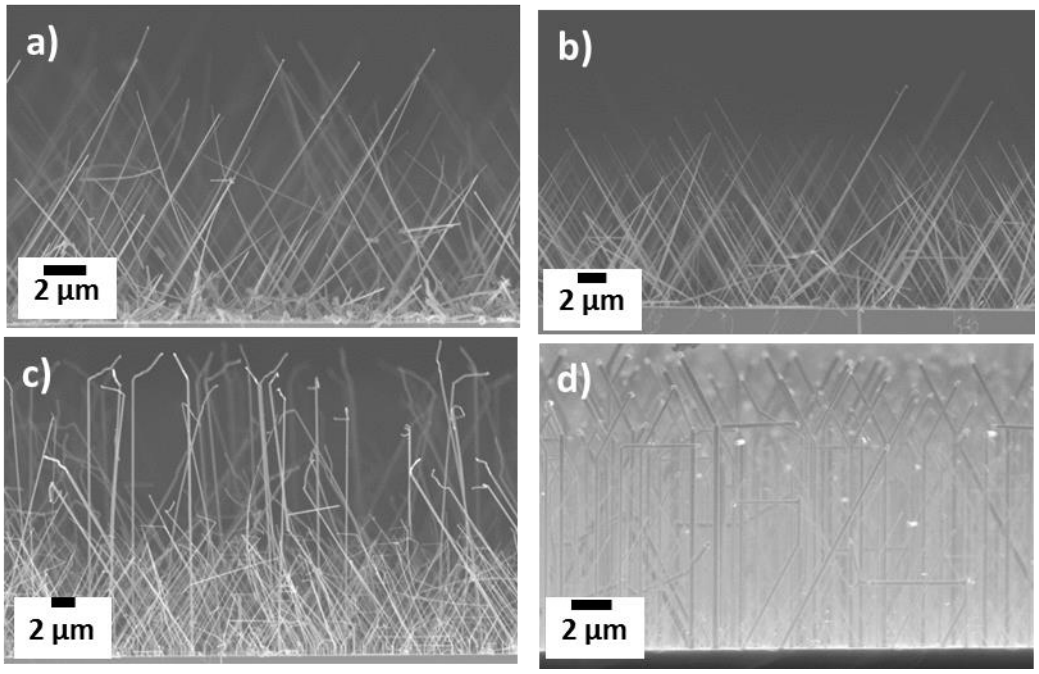


Figure 5- Cross-sectional SEM images of Si nanowires grown on (110) Si substrates at growth temperatures of a) 900^oC, b) 950^oC, c) 1000^oC and d) 1050^oC using a $SiCl_4$ partial pressure of 3 Torr.

The vertically aligned [110] SiNWs were observed to kink back toward the <111> near the wire tips as shown in Figure 6(a). In this case, the growth was terminated by simultaneously turning off the $SiCl_4$ precursor flow and decreasing the reactor temperature. Consequently, the kink from [110] to a <111> direction was believed to occur at the start of the cool down when residual $SiCl_4$ was still present in the growth chamber. To investigate this, the $SiCl_4$ precursor flow was turned off one minute before the growth temperature was decreased. In this case (Figure 6(b)), the SiNWs remained vertical throughout the entire growth, however, the gold catalyst was not present at the tip but instead was observed to have rolled down the sidewall of the nanowires.

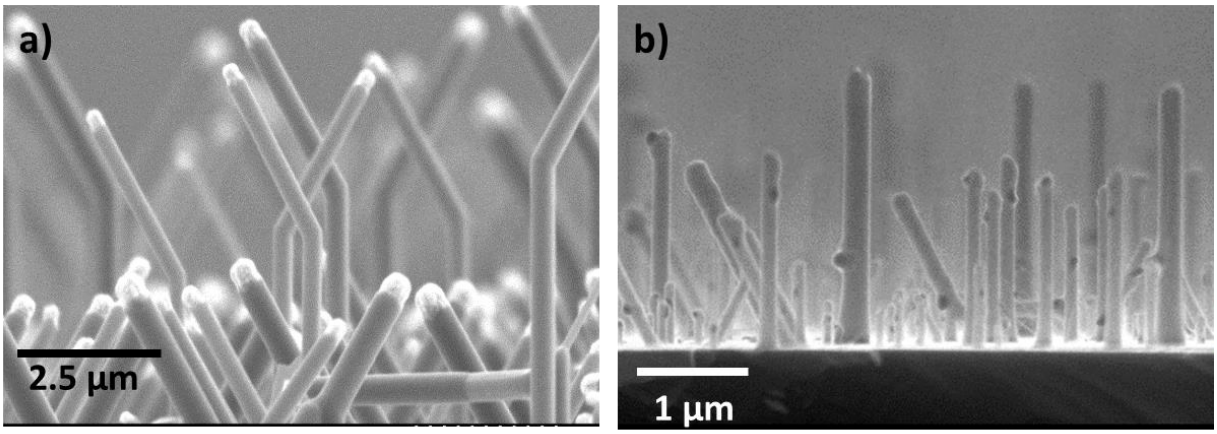


Figure 6- Cross-sectional SEM images of samples grown at 1050°C and 3 Torr $SiCl_4$ partial pressure using cool down procedure after nanowire growth where a) $SiCl_4$ flow was turned off at same time the furnace temperature was reduced and b) $SiCl_4$ flow was turned off one minute before the furnace temperature was decreased. The kink at the tips of the wires in a) is from growth during the cool down process.

The $SiCl_4$ partial pressure was found to significantly influence the yield of <110> SiNWs. The percentage of <110> SiNWs was found to decrease from 78% to 20% to 0% as P_{SiCl4} was varied from 3 Torr to 6 Torr to 9 Torr, respectively, as shown in Figure 7. From our earlier work, we demonstrated that the growth rate of <111> SiNWs using $SiCl_4$ exhibits a maximum value as the $SiCl_4$ partial pressure is increased. [Eichfeld 2011] This was explained as arising from the balance of SiNW growth and etching that occurs with $SiCl_4$ as a result of the near-equilibrium growth process. A similar behavior was observed in this sample set where the <111> SiNW growth rate was observed to increase from 3.4 mm/min at P_{SiCl4}=3 Torr to 5.0 mm/min at P_{SiCl4}=9 Torr and then decrease again to 3.9 mm/min at P_{SiCl4}=14 Torr. The SiNW growth rate is determined by the rate of crystallization of Si out of the liquid phase which is proportional to the supersaturation of Si in the liquid catalyst. Consequently, the higher growth rate obtained at P_{SiCl4}=9 Torr indicates a higher catalyst supersaturation under these conditions. It is interesting to note that no <110> SiNWs were observed using P_{SiCl4}=9 Torr. This suggests that a higher catalyst supersaturation does not promote the growth of nanowires in the <110> direction.

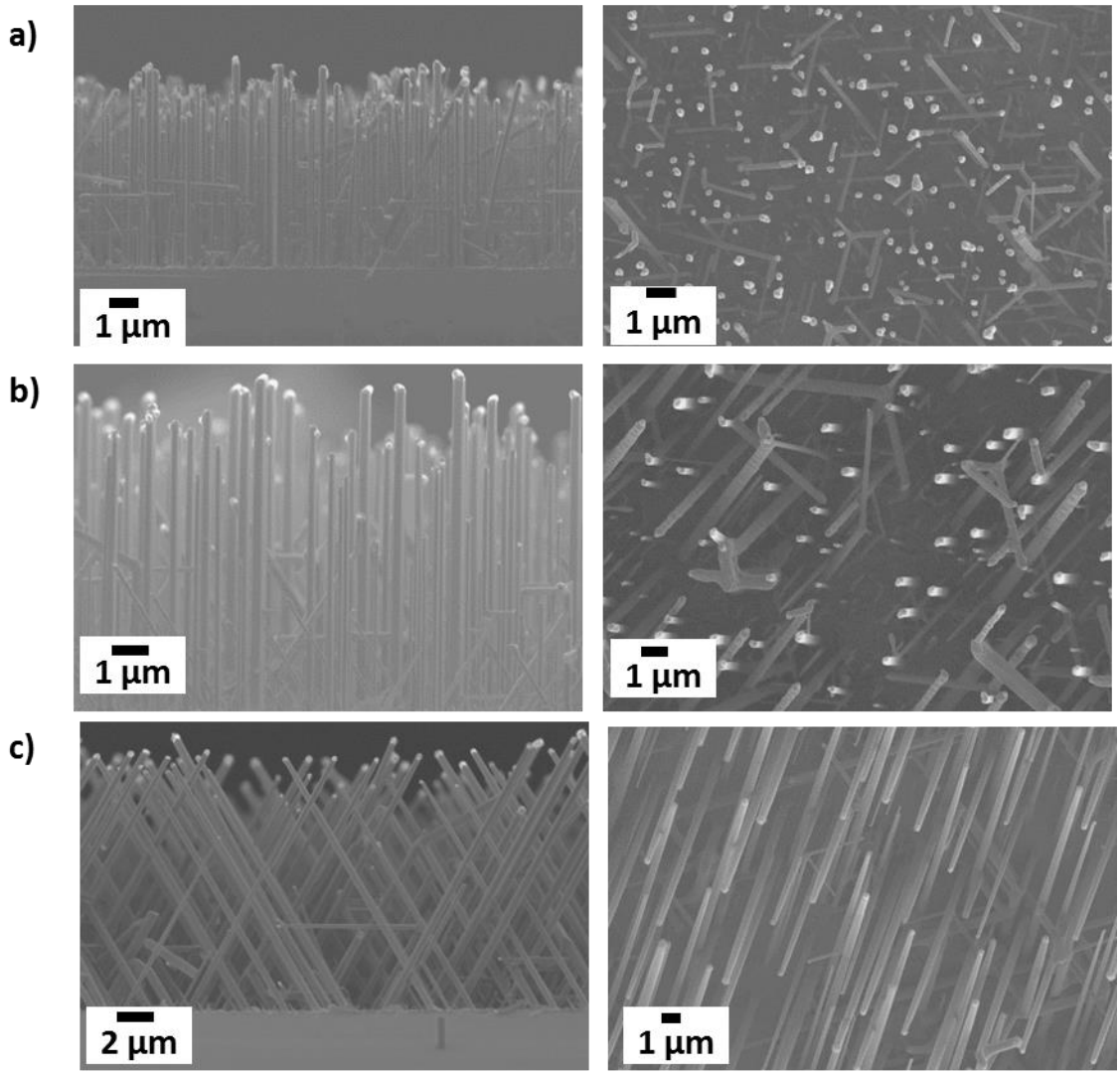


Figure 7- (Left) Cross-sectional and (right) plan-view SEM images of SiNWs grown on (110) Si substrates at 1050^{o}C using $SiCl_4$ partial pressures of a) 3 Torr, b) 6 Torr and c) 9 Torr.

Using this result, we then measured the dependence of silicon nanowires on the thickness of the Au film used to catalyze the nanowire growth. We learned that thinner Au films produce smaller diameter silicon nanowires. By decreasing the Au thickness from 10nm to 1nm, the average diameter decreased from ~450nm to ~150nm. In addition, the percentage of <110> nanowires was higher for thinner films of gold. The result was observed in two independent experiments. The observed <110> preference at smaller diameters agrees with the trend observed for Au nanoparticle catalyzed silicon nanowires [Wu, 2004].

In addition, we also noticed that there was significant run-to-run variation even for Au-catalyzed growths if there was too much down-time between runs. This also influenced our decision to change the pre-conditioning runs.

The disadvantage of using gold catalyzed VLS wires is that the Au catalyst must be removed from the nanowires to prevent minority carrier recombination at the metal. This removal process is known in the literature, and we brought this technique into our lab and refined it. The procedure, which is available in the literature [Kendrick, 2010], prescribes a thorough clean to remove gold along the length of the nanowires in addition to the obvious Au ball at the tips. The clean starts with an HF dip to remove the oxide surrounding the metal, then follows with the standard potassium iodide gold etch. These initial steps remove any Au that may be on the surface, including at the tip. Subsequent repetitions of these steps including an oxidation process before the HF dip serves to move Au to the Si/SiO_2 interface during the oxidation and etch them away. A further description of removing the Au from VLS wires is described in section 1.3 under oxidation.

Figure 8: The $SiCl_4$ system used to grow Au-catalyzed nanowires.

Summary

By the end of our grant period, we had successfully pushed the growth of Au-VLS wires to a region that was not possible prior to our work. We are now able to consistently grow nanowires with a controllable crystallographic orientation using Au-catalyzed VLS. This growth is done at high temperature with a $SiCl_4$ precursor. A high percentage (>75%) of <110> SiNWs was obtained under conditions of high temperature and reduced $SiCl_4$ partial pressure which also yielded a lower growth rate. The Au precursor is deposited as a thin layer and then agglomerates when exposed to the temperature of the furnace. Although this technique has been successful in allowing us to control the crystal orientation of the silicon nanowires by choosing the crystal orientation of the silicon wafer substrate, the diameters of the wires are too large to see the effect we are looking for (averages down to around 150nm). In order to decrease the diameter, we first tried to decrease the thickness of the gold film. This worked to some extent, but if the film was too thin we either move out of a region of epitaxial growth or we had a low yield of <110> wires. We then tried to use small colloidal catalysts but were unsuccessful in decreasing the diameter of the nanowires and we had difficulties growing <110> wires. The catalyst particle agglomerated,

producing large diameter wires. In addition to being larger diameter, these wires had a low yield of the desired <110> orientation. Hence our focus for Au catalyzed VLS wires was to reduce the diameter after growth. (see section 1.3)

Task 1.2 - Study of growth direction with Al catalyst

Most of the silicon nanowire growth studies have focused on gold-catalyzed nanowire growth, but gold is a minority carrier lifetime killer in silicon and hence not good for solar applications. Even with careful removal of gold-impurities inherent in gold-catalyzed VLS silicon nanowires, deep traps will form and might dominate the optical signature, masking any change in the electronic structure. We therefore pursued methods of obtaining <110>-oriented silicon nanowires without using gold. We made two types of <110> oriented nanowires without the use of gold; metal-enhanced etching with silver and aluminum-catalyzed VLS CVD synthesis.

Au-free nanowires by Al-catalyzed VLS

At the beginning of this grant, our team was able to grow Al catalyzed VLS wires, but they weren't epitaxial to the substrate and they were not perpendicular to the substrate, thus even if they were crystalline, we wouldn't have been able to control the crystallographic orientation. Rather quickly we were able to obtain epitaxial wires by tuning the pressure and temperature of the growth process. However, when we used a <110> substrate, the wires would mostly grow in the <111> direction, at an angle to the substrate. In addition, our process was not reproducible, which made doing experiments difficult. Now, at the completion of the grant, we are able to reproducibly grow wires in the preferred <110> direction with high yield.

For Al-catalyzed VLS wires, we were not able to use SiCl4 that we used for the Au-catalyzed VLS wires. The SiCl4 requires temperatures above 950C, which is above the eutectic temperature of Al and Si. In addition the Cl by product of the SiCl4 reaction reacts with the Al. Therefore for Al VLS we could only use SiH4, and not SiCl4.

Reproducibility

At the beginning of our project, we were not able to get reproducible results from our Al-catalyzed VLS growth. This made doing experiments impossible. Thus our first focus was to determine the cause of the variation from run to run and control for it. Figure 9 shows a typical day and the conditions of the furnace throughout the day.

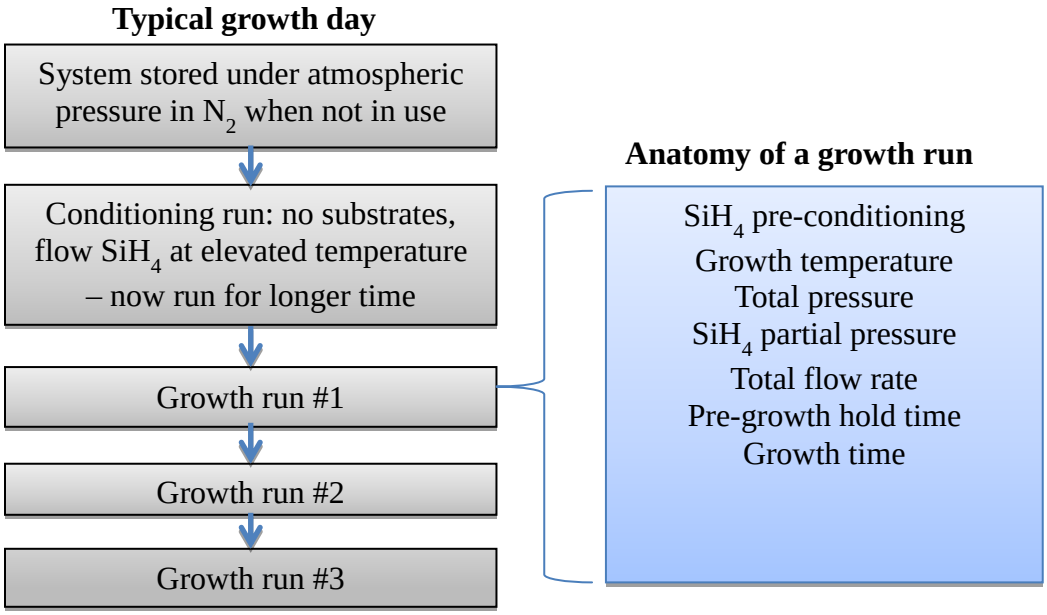


Figure 9- The sequence of events on a typical growth day and the parameters of a growth run. The conditioning, or dummy, run has the same parameters, except no substrates are used and no nanowires are collected.

We observed that the same growth recipe yielded different results depending on when the recipe was run. A typical day of nanowire growth starts with a "dummy run" without substrates to condition the process tube, followed back-to-back by up to three growth runs (Figure 9). Tellingly, the first growth after a long hiatus was particularly anomalous. Therefore, to improve the consistency, we experimented with various changes to the conditioning run. We compared the nanowire growth after a single-crystal silicon deposition to an amorphous silicon deposition for the conditioning run. During the conditioning run, the sidewalls of the process tube are coated and residual moisture is locked away. It is essential for the growth of Al-catalyzed wires that residual water be eliminated, as aluminum oxide reactions between water and the catalyst layer can inhibit growth. We also experimented with increasing the hold time and varying the hold temperature. Most growth was still epitaxial and <111>-directed. We have settled on new conditioning run parameters of 600°C for 20min using 5torr SiH_4, which is twice as long as previously used. In contrast to the strikingly variable results using the old conditioning parameters, the new conditioning run produces uniform results from repeat recipes (Figure 10).

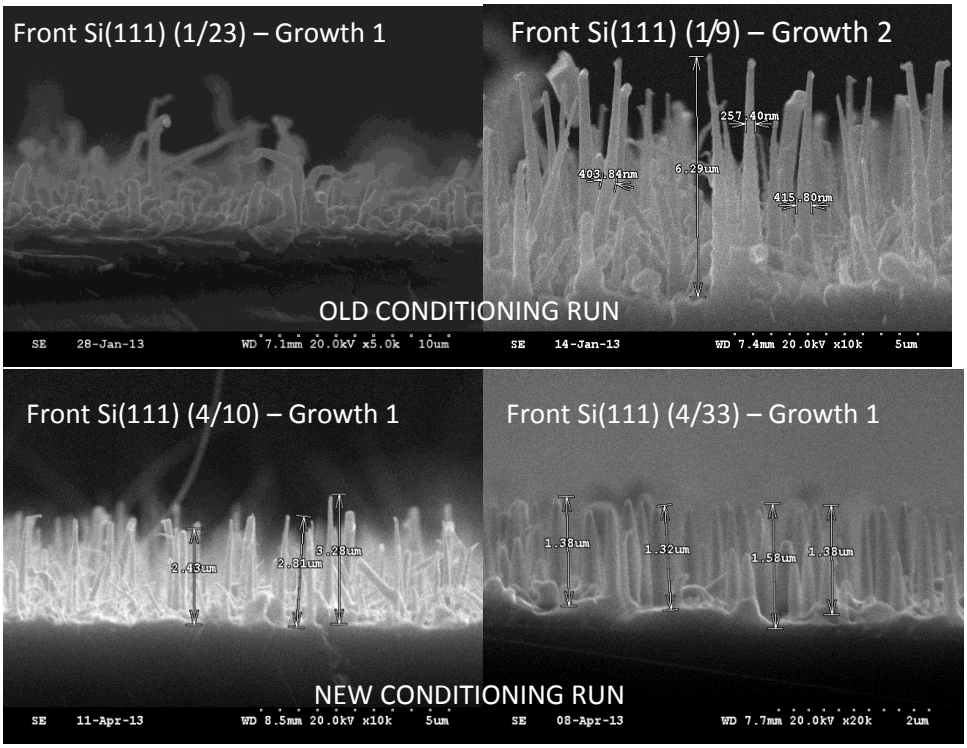


Figure 10- Al-catalyzed VLS nanowires synthesized with the same growth parameters (temperature, SiH_4 partial pressure, flow rates, etc.). Using the old conditioning run parameters, the resultant nanowires differed from run-to-run (top row). After implementing the new conditioning procedures, the run-to-run reproducibility increased (bottom row).

After these changes, we were able to reproducibly grow <111> nanowires in both nitrogen and hydrogen atmospheres. We have learned that we need to monitor the hold times (annealing period prior to the introduction of source gas which is used to pre-condition the catalyst thin film) as well as the location of the samples in the furnace. Obtaining this reproducibility between runs is the result of much work troubleshooting and doing maintenance to the silane growth system.

Pressure

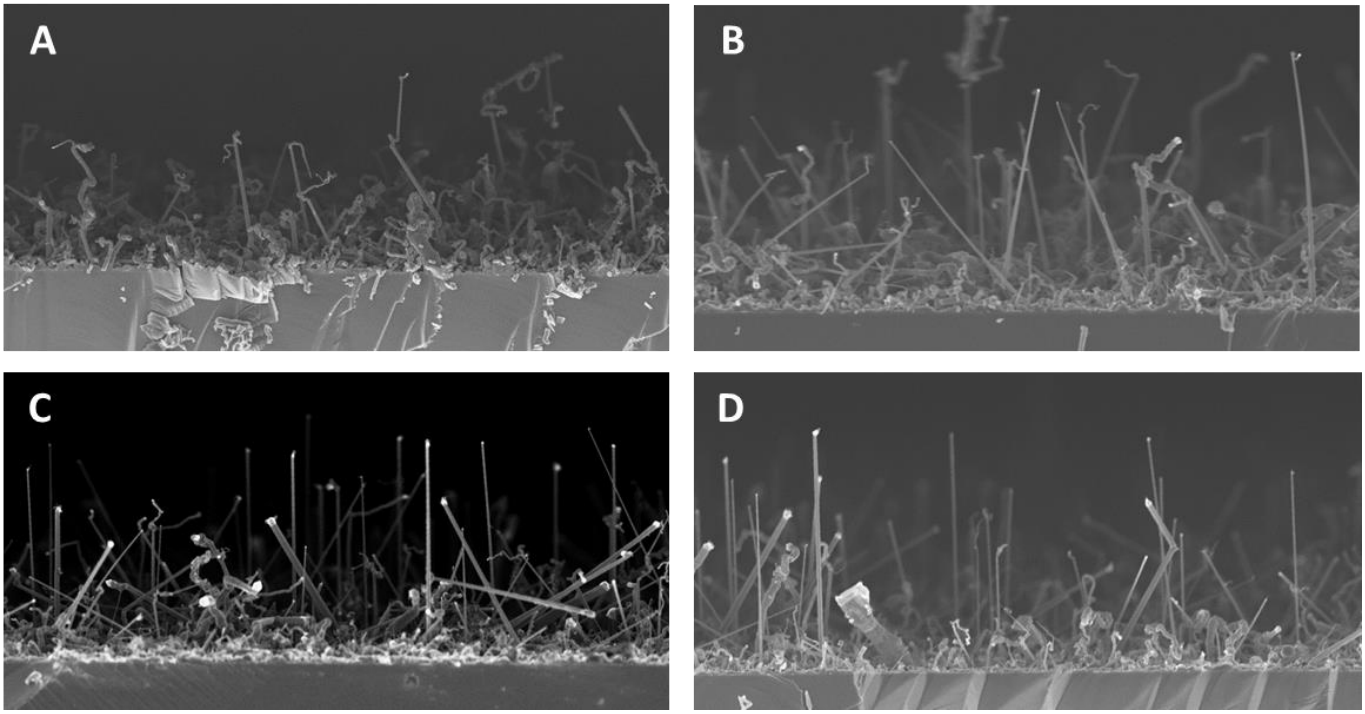


Figure 11- Increased <110> yield occurs with increasing total pressure from A) 100 Torr B) 200 Torr C) 300 Torr D) 500 Torr. Beyond 300 torr, <110> yield appears consistent. The wires were grown on a <110> oriented substrate.

The pressure during nanowire growth is a very important parameter to determine the nanowire morphology. Figure 11 shows the effect of growth pressure on the growth. Growths were initially done at 100 Torr total pressure with 2.5 Torr SiH_4 partial pressure. Wire growth at this partial pressure is non-epitaxial and the <110> yield is minimal. This is likely due to vapor-solid deposition of amorphous silicon on the tip and sidewalls of the nanowires during growth. The amorphous coating may destabilize the Al catalyst/ wire interface promoting wire kinking during growth. Upon increasing total pressure to 300 Torr, the <110> yield increases as thin film deposition is reduced. This is evident in C) where the percentage of the vertical wires (these are <110>) increased and the amount of kinked wires decreased. Above 300 Torr there does not appear to be a significant improvement in <110> wire yield. There is thin film deposition on the side walls at lower pressures. This amorphous silicon coating is a result of Si vapor solid deposition in which no catalyst is required so silicon can be deposited directly onto the sides of the wire.

Previous reports on silicon CVD in hydrogen describe how increased hydrogen partial pressures can suppress thin film deposition by interfering with SiH4 adsorption on the silicon surface. [Tao 1997]. Hydrogen must desorb from the surface before SiH4 can be adsorbed, and since increased hydrogen partial pressures reduce the rate of hydrogen desorption, the rates of silane adsorption and subsequent Si thin film deposition are also reduced. By increasing the reactor pressure to 300 Torr, thin film deposition was greatly reduced. Aluminum catalyst droplets are clearly

visible at the wire tips for growth at 300 Torr (Figure 11c) in contrast to growth at 100 Torr (Figure 11a) where the tips appear to be coated with amorphous silicon.

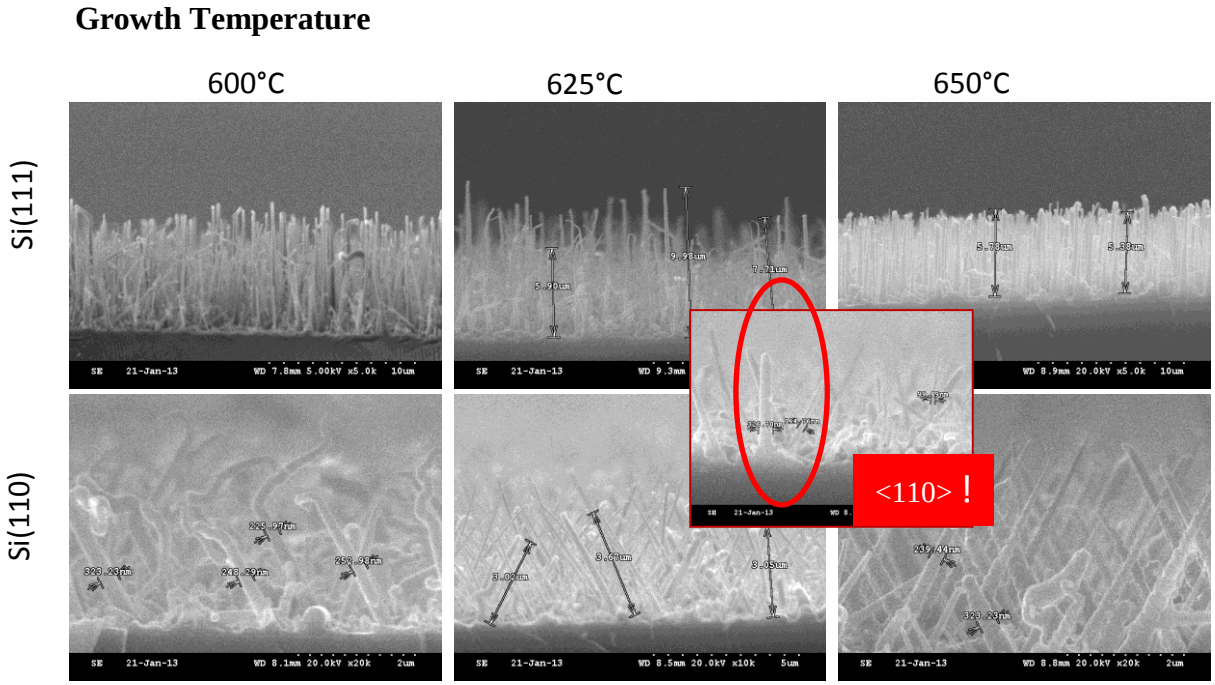


Figure 12- Growth temperature series on Si(111) and Si(110) substrates illustrating increasing epitaxy at increasing growth temperatures for silane Al-VLS. Comparing the top and bottom rows, epitaxy on Si(111) is easier to achieve than on Si(110). Inset: A small number of <110>-oriented wires can be found amongst the epitaxial wires on Si(110) substrates. These results were before the pressure and hold time were optimized.

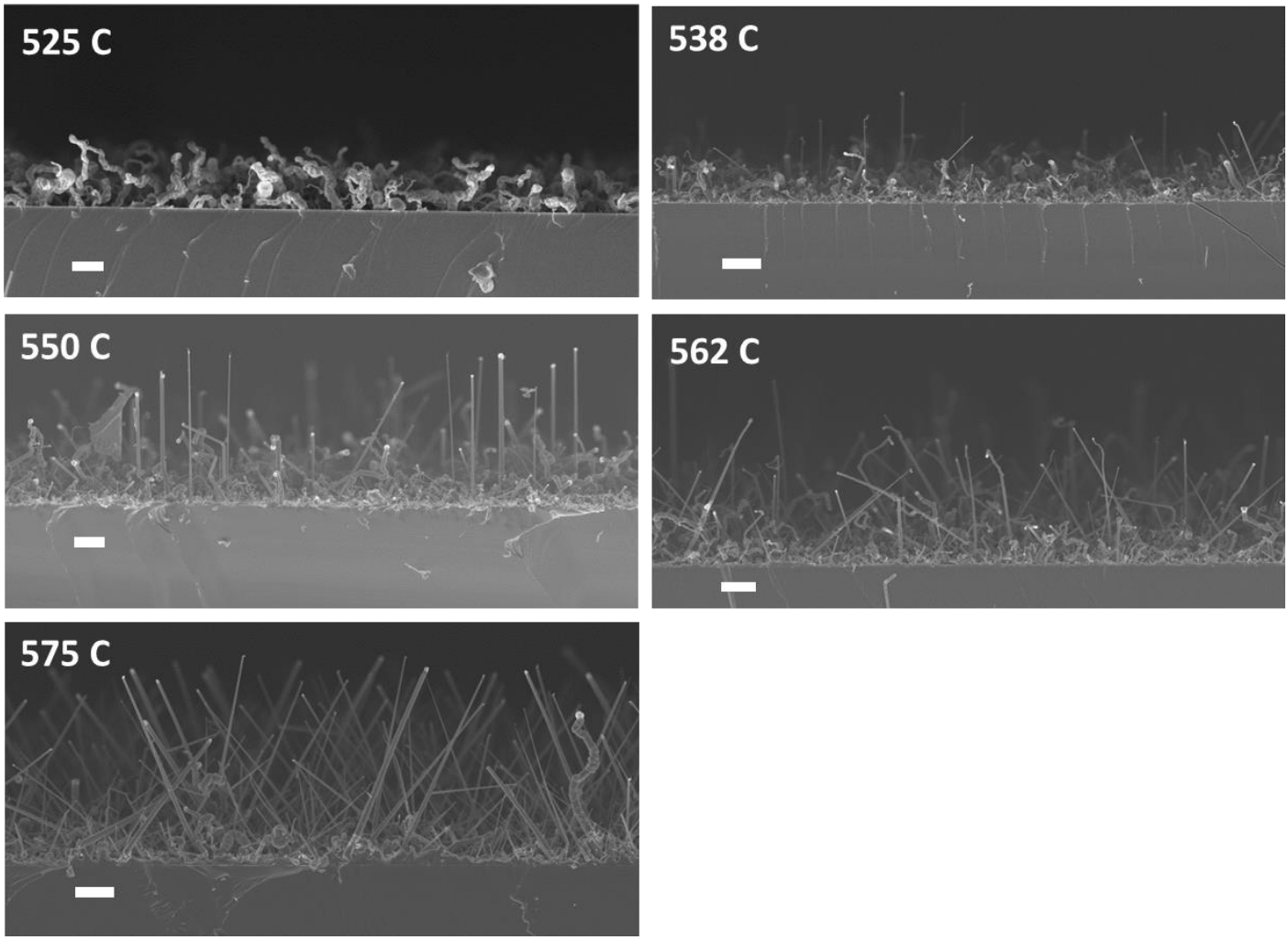


Figure 13- Growth temperature effects on <110> nanowire yield. <110> yield increases as temperatures rise from A) 525°C B) 538°C to C) 550°C. As the temperatures approach the Al-Si eutectic temperature, <110> yield is reduced at D) 562°C and E) 575°C and <111> becomes the preferential growth direction.

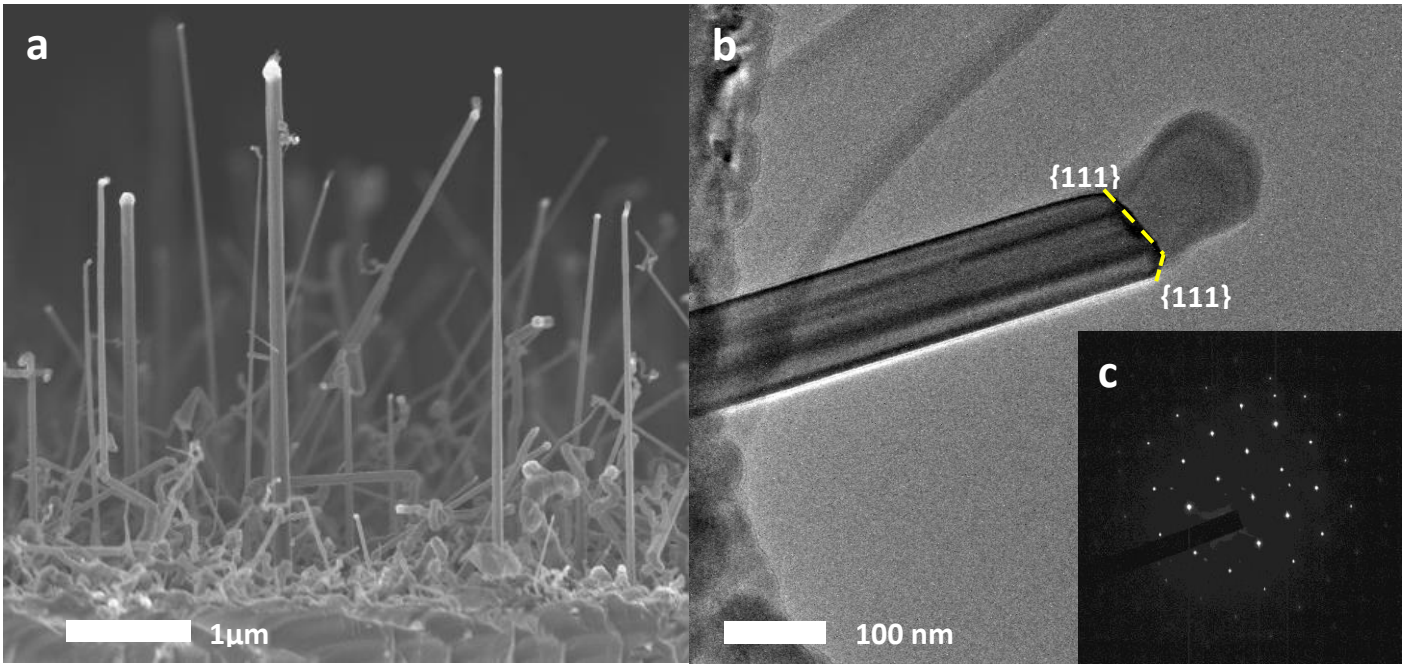


Figure 14 – a) <110> Nanowires growing vertically from Si(110) surface b) TEM showing <110> wire with minimal thin film coating and angled wire/catalyst interface with c) <110> nanowire diffraction pattern

While increased pressure reduced thin film deposition, significant non-vertical growth was still present as shown in Figure pressureAl. In an effort to further reduce the rate of vapor-solid deposition, the growth temperature was reduced to 550°C and a 1 hour anneal was introduced prior to growth to provide additional time for the aluminum film to de-wet from the silicon surface to form catalyst droplets and to promote increased reduction of the native oxide (AlOx) on aluminum through reaction with H2. The results of these changes are shown in Figure 14 a). A larger fraction of wires with diameters ranging from 100-230 nm were observed to grow vertically from the substrate surface. The average length of the wires was 9 um resulting in growth rates on the order of 300 nm/min for a growth time of 30 minutes. The vertical orientation of the wires relative to the (110) substrate plane strongly suggests that they have a <110> growth direction. To confirm this, TEM with selected area diffraction (SAD) analysis was carried out to determine the growth direction and assess the structural properties of the nanowires. As shown in Figure 14b), the SAD pattern confirms that the measured nanowire is oriented in the <110> direction, with two {111} facets making up the Si nanowire tip. The TEM image (Figure 14b)) also shows greatly reduced thin film deposition on the wires in comparison to those grown at 100 Torr. Note that the dark lines running the length of the wire are due to thickness effects from the wire faceting, not thin film deposition.

Figure 12 compares the nanowires grown on both <111> and <110> silicon substrates as a function of temperature. This run was done prior to optimizing the pressure and before we added a hold step and thus only minimal <110> wires were grown.

Figure 13 shows the effect of growth temperature on the yield of <110> wires. While initial growths were done at 575 C, reducing the growth temperature to 550 C was necessary to

promote <110> wire growth. Subsequent growths were done at 300 Torr with a 60 minute hold at 550 C to help break up the Al film. At too low temperature, the wires are kinked and have amorphous silicon deposition indicating that the epitaxy could not be sustained. As the temperature increases towards 550 C (see C)), the amount of <110> growth increases. <110> wire yields are greatest at 550 C. As temperatures increase beyond 550 C and approaches the eutectic temperature, the preferential growth direction shifts from <110> to <111>. <110> yield is reduced at D) 562°C and E) 575°C.

Hold time/understanding crystallographic dependence of nanowire growth

After implementing tube pre conditioning, we were able to get reproducible results. Then by exploring the effects of growth pressure and growth temperature, we were able to get reproducible epitaxial growth, but only with <111> wires. We were stymied in our efforts to encourage preferential <110> growth with an Al catalyst. Unlike the gold-catalyzed growth, at no point in the parameter space (temperature, pressure, etc.) did <110> nanowires dominate. After scouring the literature, we began to understand why we get <111> growth when not using a <111> silicon substrate. In addition, we were able to fix this issue.

The shift in growth direction to <111> from <110> wires with increasing temperature above the eutectic temperature adds to the understanding of controlling growth direction from earlier studies. Early reports on nanowire growth in non-<111> directions on oxidized silicon substrates by Wu [Wu 2004] found that growth in the <110> direction was dominant for wires with diameters below 20nm, with the preferential direction shifting to <112> and then <111> with increasing diameter. This transition was explained by Schmidt et al. [Schmidt 2005] via a thermodynamic model in which preferential growth direction corresponded with a minimization of the catalyst/droplet interface energy and nanowire sidewall surface energies during growth. However, more recent reports by Kwon et al. [Kwon 2010] and now results from this grant (as published in Eichfeld et al.[Eichfeld 2013]), have demonstrated high-yield growth of <110> wires from Si(110) substrates with diameters greater than 100nm, suggesting that preferential growth direction can be determined by other factors as well. For instance, Schwarz et al. [Schwarz 2011] proposed a kinetic model independent of wire diameter to predict the stable facet orientation at the catalyst/nanowire interface based on facet growth rates at the nanowire tip and the chemical potential differences between the catalyst droplet and nanowire facets. Since the growth direction is determined in part by the Si facet orientation at the catalyst/nanowire interface, this model suggests that growth direction may also be influenced by factors such as the chemical potential or supersaturation of Si in the catalyst droplet.

Supersaturation was previously found to play an important role in determining the growth direction of germanium nanowires. Gold-catalyzed Ge nanowire growth in the <111> and <110> directions was previously reported by Kramer et al. [Kramer 2011] and Kolibal et al.[Kolival 2011] using physical vapor deposition (PVD) under ultra-high vacuum conditions. In these reports, the preferential growth direction correlated with the extent of catalyst droplet supersaturation. At low supersaturations obtained by using a low Ge flux during growth under UHV conditions, <110> growth was preferential. However, as the germanium flux was increased, corresponding to an increase in the droplet supersaturation, the <111> growth direction became dominant. Kramer et al. [Kramer 2011] further demonstrated that similar behavior could be observed during silicon nanowire growth, with <110> wires growing from

(111) silicon substrates at very low (0.5Å/s) silicon fluxes [Kramer 2009], suggesting that this phenomena may be applicable to materials beyond gold-catalyzed germanium nanowires.

The observed change in growth direction can be explained by a change in catalyst droplet supersaturation [Kramer 2009, Kolibal 2011]. As the reactor temperature rises from 550°C to 575°C, the droplet changes from a solid to a liquid state and silicon solubility in the aluminum droplet increases from 1.5% towards 12.5%, allowing for far greater droplet supersaturation [Murray 1984]. Following the model of Kramer et al. [Kramer 2011], the nucleation of (110) surfaces and subsequently <110> growth is energetically favorable at lower supersaturation, while increased supersaturation results in (111) nucleation and <111> growth being most favorable [Kramer 2009]. Furthermore, this model predicts a reduction in the critical supersaturation needed to shift the preferential growth direction from <110> to <111> as the growth temperature is increased, further promoting a shift to the <111> direction at higher temperatures. Note that growths done at 550°C with different SiH4 partial pressures did not show any change in preferential growth direction, suggesting that this range of partial pressures is not sufficient to increase the droplet supersaturation enough to affect the preferential growth direction. Additionally, supersaturation explains why preferential <111> growth is observed at 550°C after holding at 575°C. In an earlier report on Al-catalyzed nanowire growth by Wacaser et al, epitaxial growth of <111> silicon nanowires was reported at growth temperatures of 520°C and 490°C after pre-growth annealing at 600°C [Wacaser 2009]. The catalyst droplets were proposed to exist as liquids at temperatures well below the Al-Si eutectic due to supercooling [Wacaser 2009]. For wires grown at 550°C after a 575°C anneal, the catalyst droplets may also be supercooled, with greater silicon concentration within the catalyst compared to samples where the anneal was performed at 550°C. Therefore, even though the growth temperature is below the eutectic temperature, the catalyst supersaturation is great enough to promote growth primarily in the <111> direction.

Remarkably, the shift in growth direction to <111> from <110> wires with increasing temperature described above occurs any time the substrate is heated above the eutectic temperature, even if the substrate is exposed to the high temperatures before growth and then the growth occurs at sub-eutectic temperatures. The hold step is important in forming <110> wires and to maximize <110> growth. Indeed, a hold step is required to initiate growth, but temperatures of this step must be kept low enough for <110> growth. The <111> growth likely is a consequence of the aluminum interaction with silicon at the hold and growth temperatures. Berthoud [Berthoud 1977] studied the behavior of aluminum on silicon upon annealing and found that Al and Si start reacting as low as 400°C. The Al etches into the silicon, etching slowest on Si(111) planes. Thus, this process exposes Si (111) interfaces on our (110) surface to Al. Since VLS under our conditions prefers <111> growth, the wires grow epitaxially, but in the <111> direction at an angle to the substrate. (Fig. 15). We have confirmed the creation of these Al etch planes under our hold time (annealing) conditions. A similar mechanism maybe active for our Au-colloid catalyzed growth, as similar etch trails have been observed in our annealing experiments.

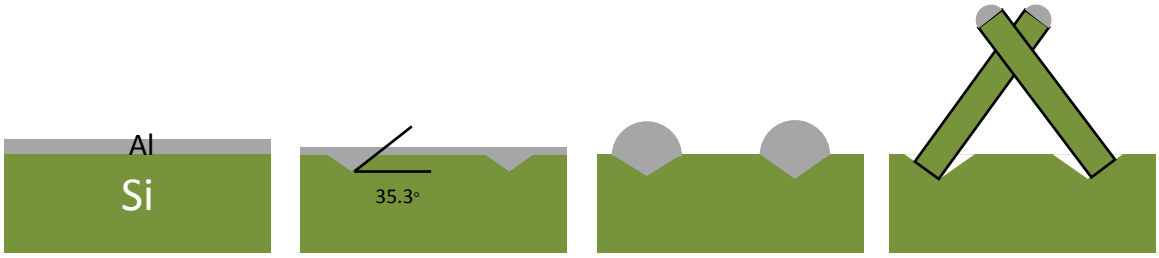


Figure 15- Schematic of Al etching into a Si (110) substrate. From left to right: (1) As the (110) substrate with 10nm Al film reaches the 600°C hold temperature, (2) etching initiates quickly at surface to form {111} facets in (110) surface (<1min at 600°C). (3) Aluminum droplets coalesce on low energy {111} facets. (4) Nanowires grow from droplets in the low-energy <111> direction.

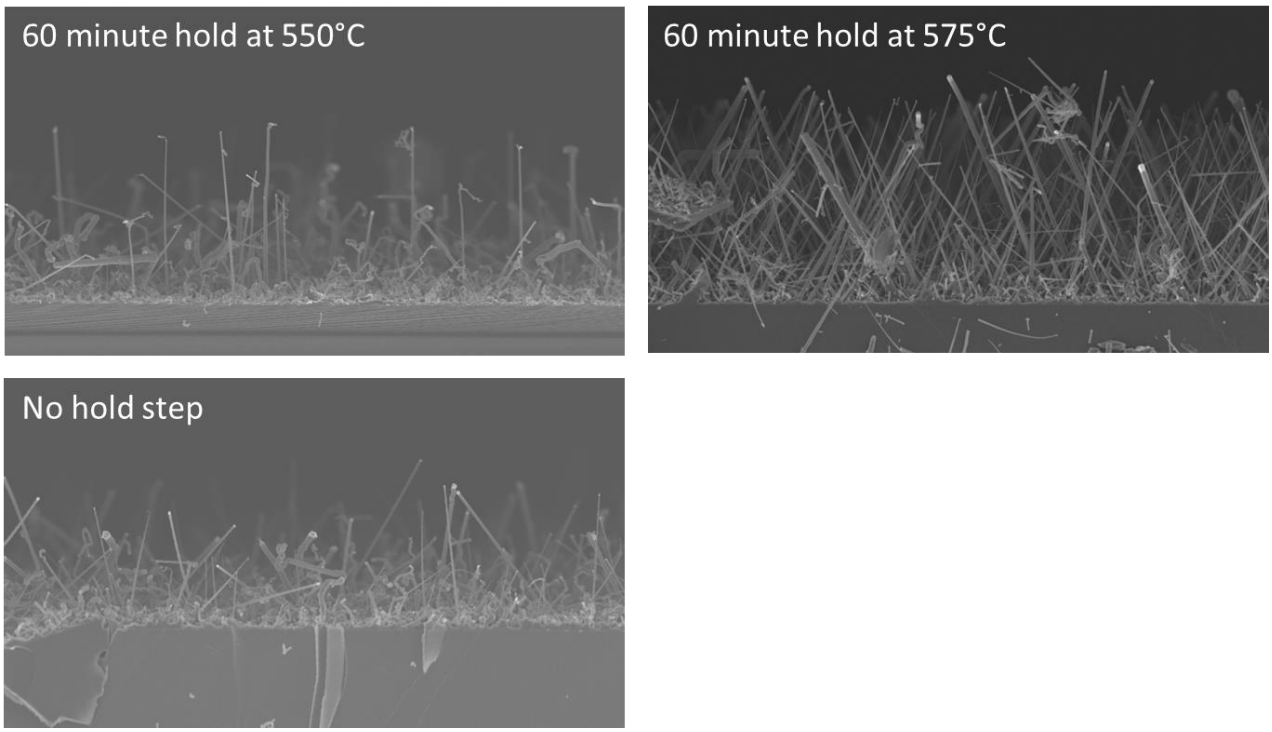


Figure 16- Effect of hold time and hold temperature. A) 60 minute hold at 550°C, showing <110> wire growth. B) 60 minute hold at 575°C, resulting in transition to <111> growth. C) No hold step, resulting in varied growth directions at 550°C.

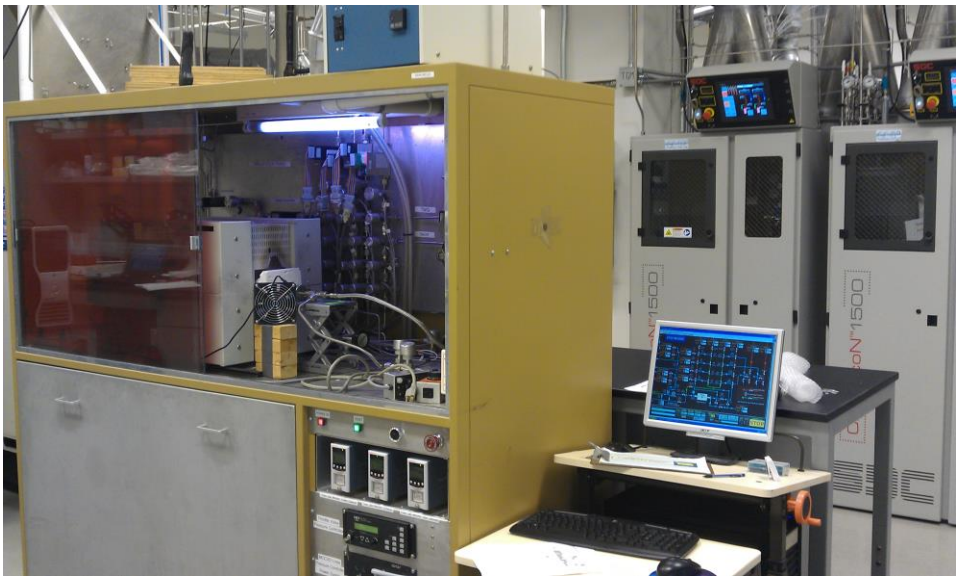


Figure 17: SiH_4 system used for the Al-catalyzed growth.

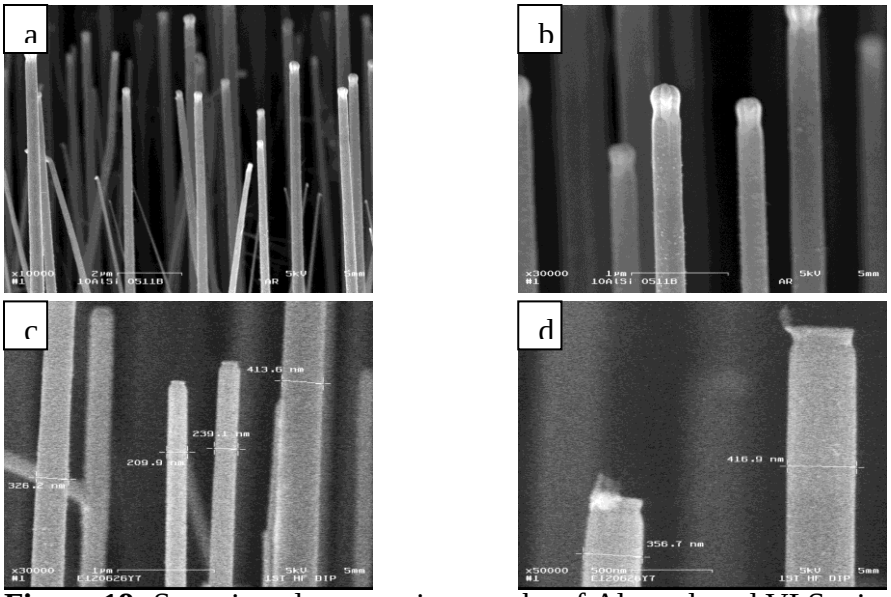


Figure 18- Scanning electron micrographs of Al-catalyzed VLS wires as-grown ((a) and b)) and after the HF etch ((c) and d)).

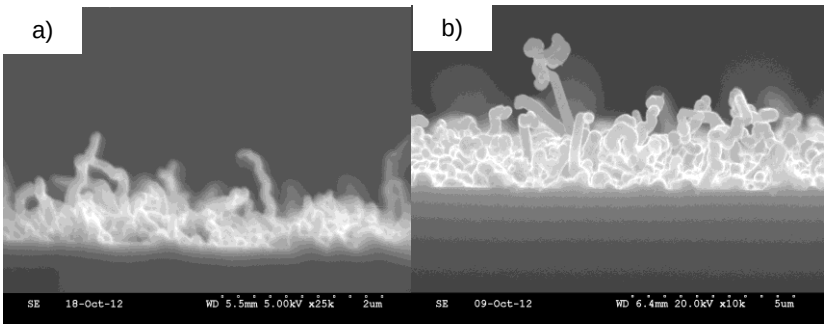


Figure 19- Al-catalyzed growth of silicon structures on a) Si<111> and b) Si<110> substrates as was obtained near the beginning of this grant period.

Conclusion

We were able to successfully grow reproducible <110> and <111> nanowires using aluminum catalyzed VLS. In order to achieve this goal, we learned that we needed to monitor and control growth pressure, growth temperature, and position in the furnace. Reactor pressures of 300 Torr or greater lead to increased hydrogen partial pressures, suppressing thin film deposition and promoting epitaxial <110> growth. In addition we added an anneal period prior to the introduction of source gas which we call the hold time. Growth and hold anneal temperatures must be kept below the Al-Si eutectic in order to grow in the <110> direction. A hold at 550 C is necessary to improve <110> yield. If the reactor temperature approaches the eutectic, increased dissolution of silicon into the catalyst droplet due to the solid to liquid phase change leads to greater droplet supersaturation, making growth in the <111> direction energetically favorable and resulting in predominantly <111> wire growth.

Based on previously measured interfacial energies for the Al/Si(110) system, <110> growth is energetically possible. The 1f nanowire growth mode has been predicted to occur given the balance between catalyst/solid and vapor/solid Al-catalyzed nanowire growth meets these conditions. TEM and SEM images of nanowires and wire/catalyst interfaces confirm this growth mode.

Au-free nanowires by metal-enhanced etching

The goal of this subtask is to make silicon nanowires without using a metal catalyst that acts as a minority carrier lifetime killer. Although at the beginning of the grant we expected to only focus on Al catalyzed VLS, Bandgap's technology of making silicon nanowire arrays using metal enhanced etching of silicon also produces silicon nanowires without serious lifetime killers; we use silver to catalyze the etching of silicon. Bandgap's technology can produce nanowire arrays very inexpensively and over large areas. We have control over diameter, density, taper, and length. Since this is an etch process and the wires can be made vertically aligned, we control crystallographic orientation simply by selecting the crystal orientation of the starting wafer.

Despite our excellent control in the process, we were not able to 1) facet our wires 2) make wire diameters at the dimensions that we expect are required to observe Bandgap Activation, and 3) make nanowires at the length required for measuring Bandgap Activation that are defect free.

When we make long nanowires, with small diameters, the process we use results in damage at the tip of the nanowire. This tip is effectively porous silicon and no longer has a long order

crystallographic structure. By implementing a two-step etch, we avoid the nanowire tip damage commonly observed in single-step electroless etching (Figure 12). For details on this two-step process see patent application 14/329,975.

Using this method of metal enhanced etching, we fabricated tapered nanowires with diameters 30-100 nm at the bases and less than 20nm at the tips. The nanowire lengths are controlled by the etch time. For testing, we often placed these nanowires in solution thus we needed long nanowires, 2-5um long (Figure 13).

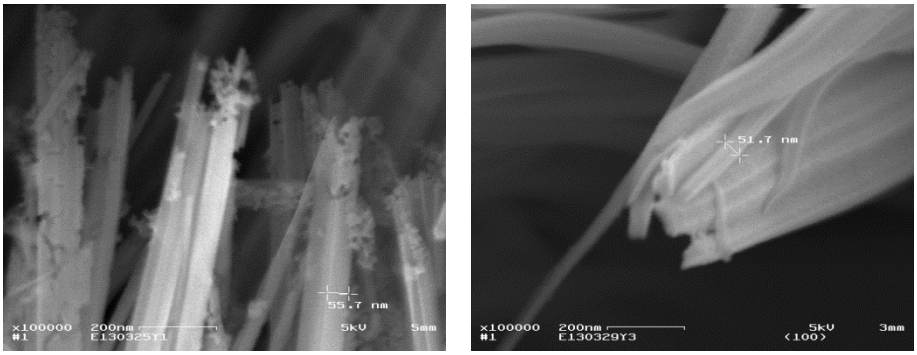


Figure 12- Nanowires grown using metal-enhanced etching. When using a one-step etch process, the tips of the nanowires become porous (left); in comparison, the nanowire tips produced by our two-step etch process are not damaged (right).

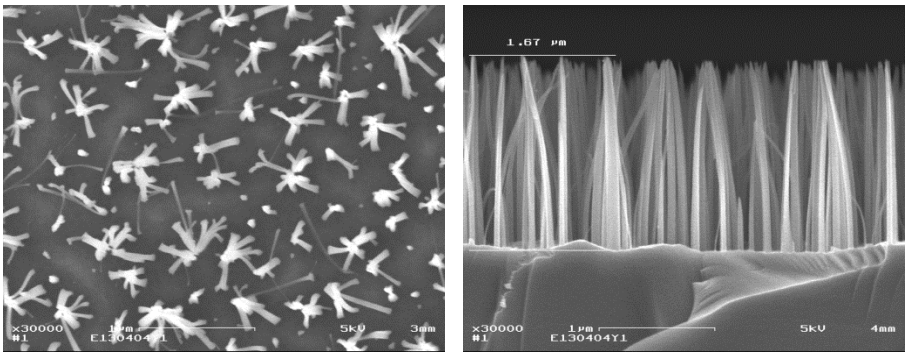


Figure 13- Top-down (left) and cross-section (right) SEM images of nanowires fabricated from Si(110) wafers by two-step metal-enhanced etching.

Task 1.3 Prepare samples with varying nanowire diameters

The morphology and epitaxial growth of silicon nanowires is controlled by the combination of their growth parameters, some of which cannot be decoupled and controlled independently. The growth parameters include: temperature, source gas partial pressure, reactor total pressure, gas flow rate, catalyst, substrate, and substrate pretreatment. For our output features of interest, epitaxial <110> growth axis and nanowire diameter, the catalyst diameter and bonding to the surface are two of the strongest influences. By mapping the parameter space with a series of nanowire growth runs, we are optimizing the growth parameters for small diameter <110> nanowires. The goal is to identify the region in parameter space where small diameter <110>-

oriented nanowires result. In the images shown, all samples were grown on <110> silicon wafers, therefore vertical nanowires are in the desired <110> direction.

Commonly used gold catalysts for nanowire growth include gold thin films and gold colloids. Thin films are separated into discrete catalyst particles by heating. The use of Au thin films in this project has shown a higher yield of <110> nanowires; however, these samples also have a larger variation in particle diameter, which correlates with nanowire diameter. In order to obtain a tighter control over the particle diameter it is beneficial to use gold colloids. This allows for the ability to achieve control over the nanowire density and size and thus allow us to obtain a larger percentage of small diameter nanowires.

Nanoparticles

Figure 14 a, b, and c shows the effect of annealing temperature on the gold particle diameters. As the temperature of the anneal increases, the nanoparticles agglomerate more forming less dense, and larger nanoparticles.

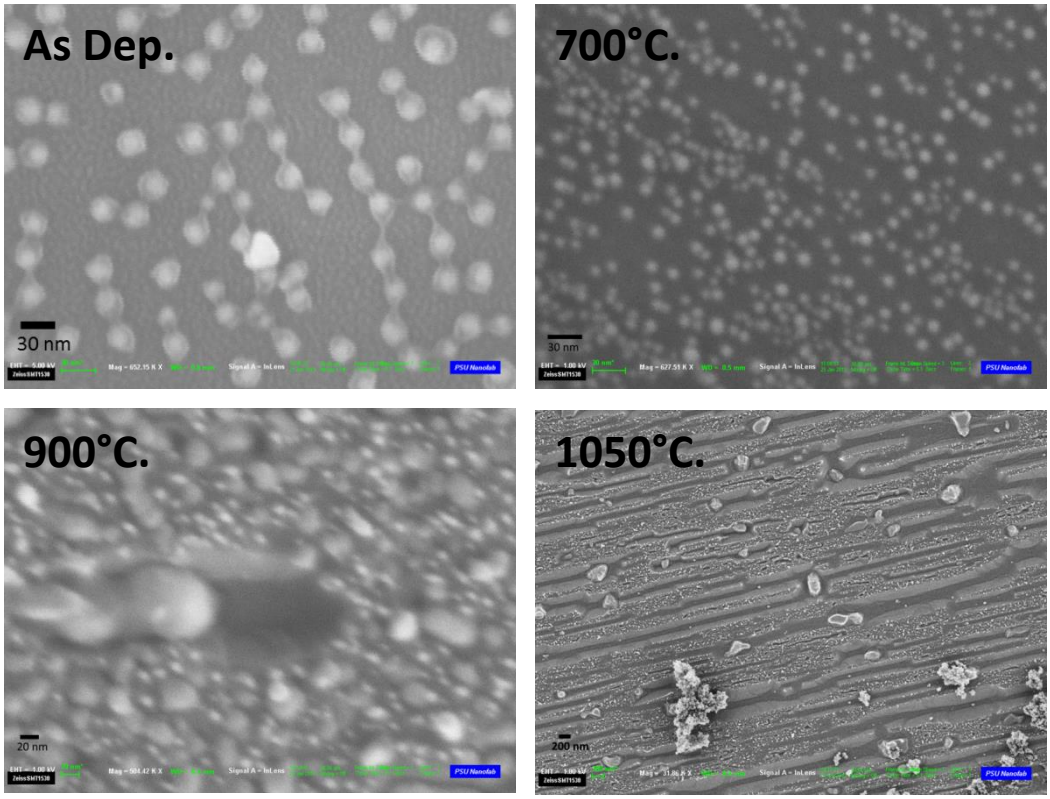


Figure 14- Evolution of Au-nanoparticles as-deposited and as a function of annealing temperature (700°C, 900°C, 1050°C). The nanoparticles were deposited on Si substrates by a block-copolymer method (Hanako Materials, La Canada Flintridge, CA).

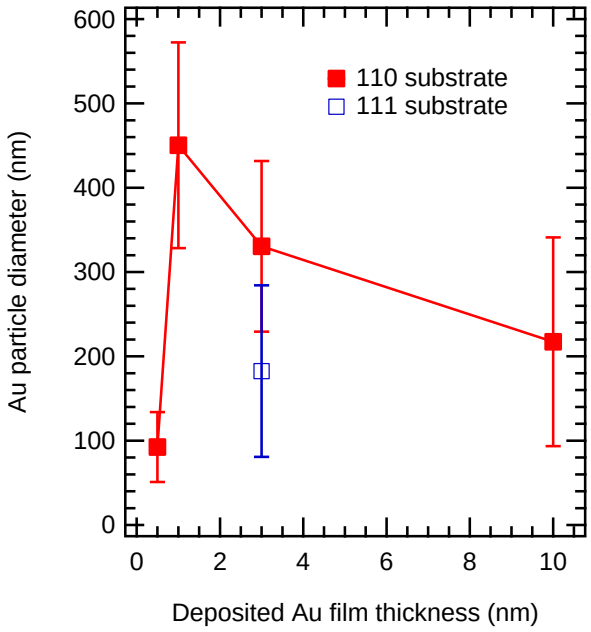
Although nanoparticles should allow us to make smaller diameter nanowires and we were able to control the diameter of the nanoparticles by adjusting the anneal temperature, working with the nanoparticles has proven to be more challenging than with films. The gold colloids, obtained commercially (British BioCell International/Ted Pella), are stabilized in a citrate solution that is

believed to prevent the substrate interaction necessary to achieve epitaxial growth. Thus most of the nanowires we are currently working with were made using a Au thin film as a catalyst.

Thin films

We mapped the diameter of Au particles after heating versus the deposited film thickness on <110> surfaces. While this relation has been studied previously on <111> surfaces, working with <110> surfaces is uncommon. Our results did not show a significant difference between behavior on the <110> and <111> surfaces (Figure 15).

a) b)



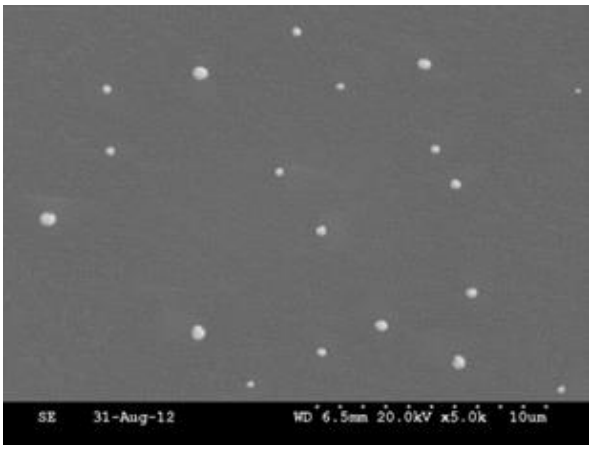
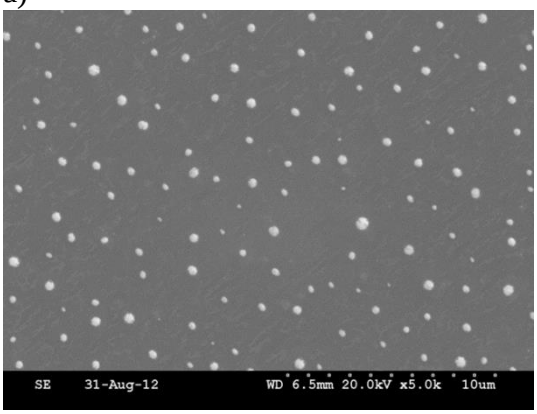


Figure 15 a) Au catalyst size vs deposited Au film thickness on <110> substrates. b) Scanning electron micrograph showing the Au particle size after heating of a 1 nm Au thin film.

a) b)



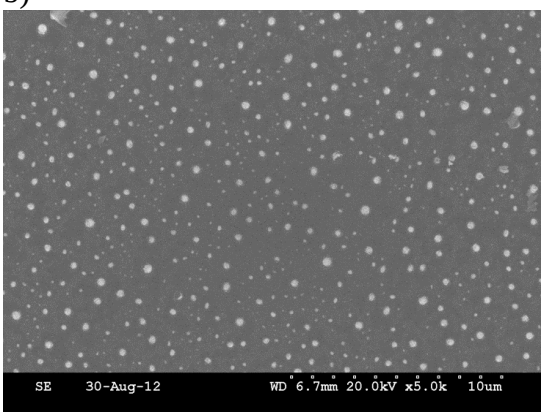


Figure 16- 3 nm Au thin film thickness after heating on a) <110> Si and b) <111> Si. The average diameter for 3 nm Au thin film is approximately 330.5 +/- 101. 2 nm on Si <110> and 182.5 +/- 101.7 nm on Si <111>, with a higher density on the <111> substrate.

In addition to studying the distribution of metal nanoparticle size after annealing a deposited thin film, we also studied the nanowires that resulted in VLS growth catalyzed by these particles. In particular, we studied the growth axis selection and diameter of the nanowires. We studied catalyst size and source partial pressure simultaneously. The results of the partial pressure study are presented in section 1.1.

Using the result of the partial pressure study (see section 1.1), we varied the catalyst size while holding the partial pressure at 3 Torr. The resulting nanowire diameters were found to increase with increasing catalyst size/Au film thickness (Figures 17 and 18).

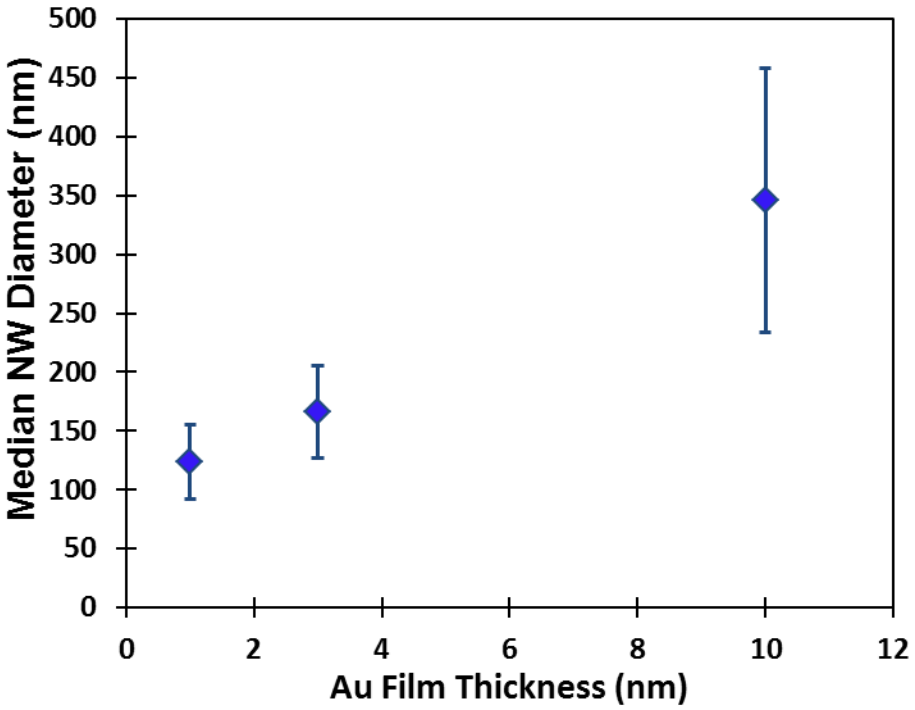


Figure 17- Median SiNW diameter versus Au thin film thickness, as the Au film thickness increases there is an increase in the median nanowire diameter and an increase standard deviation of the nanowire diameters.

The decrease in nanoparticle diameter also increased the percentage of <110> wires in the resulting nanowire arrays. Figure 18 shows two nanowire arrays. One nanowire array was grown using a 1nm gold film and the other using a 10nm gold film. The wire array grown using the 1nm gold film has smaller diameter wires and a greater percentage of <110> wires (vertical) compared to the nanowire array grown using the 10nm film.

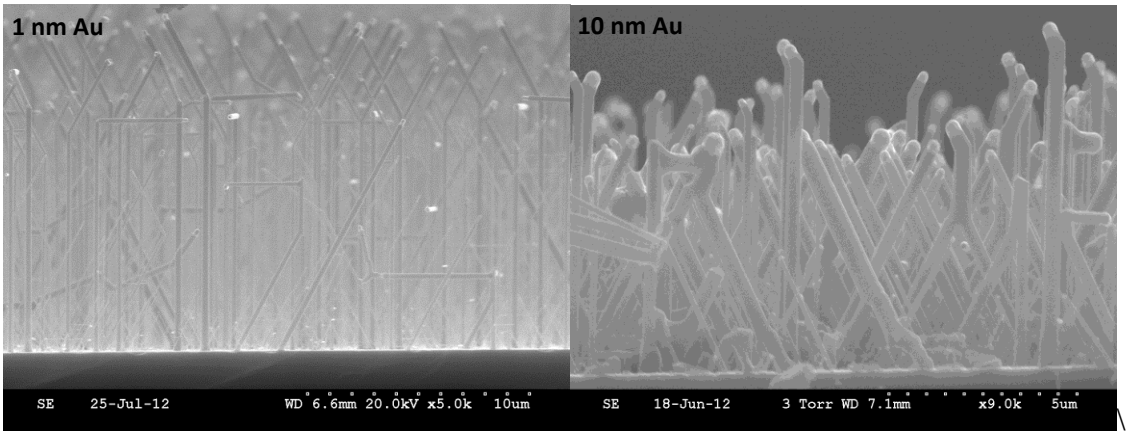


Figure 18- Comparison of cross-sectional SEM images showing increased SiNW diameter with an increase in Au film thickness.

Even when a nanowire has a <110> orientation, often the wire has a kink at the top that is not in the <110> direction but instead grows at the preferred <111> direction. This <111> section of the wires could interfere with the optical measurements and is therefore undesirable. We identified and implemented a process step to prevent the growth of kinked nanowires. We suspected that the kinks in the wires result from growth from residual silicon tetrachloride ($SiCl_4$) in the chamber as it is cooled after completion of the growth run. To test this theory, after a growth run, instead of immediately ramping down the temperature of the chamber, we held a sample at its growth temperature and turned off the source gas. The results are shown in figure 19 and confirm that the kink is a result of excess source gas being incorporated during the temperature cool-down step.

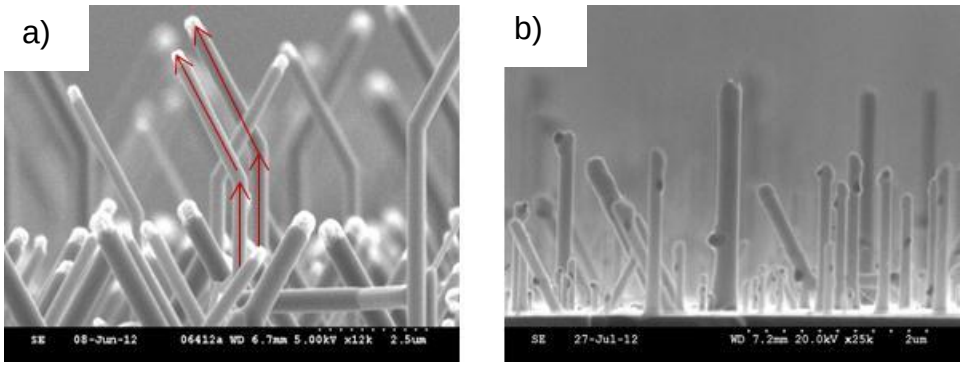


Figure 19- a) SiNWs grown using a standard cool down where the nanowires are cooled immediately after turning off the source gas. The red arrows show the change in growth direction from <110> to <111> and b) SiNWs grown using a 1 minute hold without source gas flowing into the system prior to cooling. The kink is no longer present.

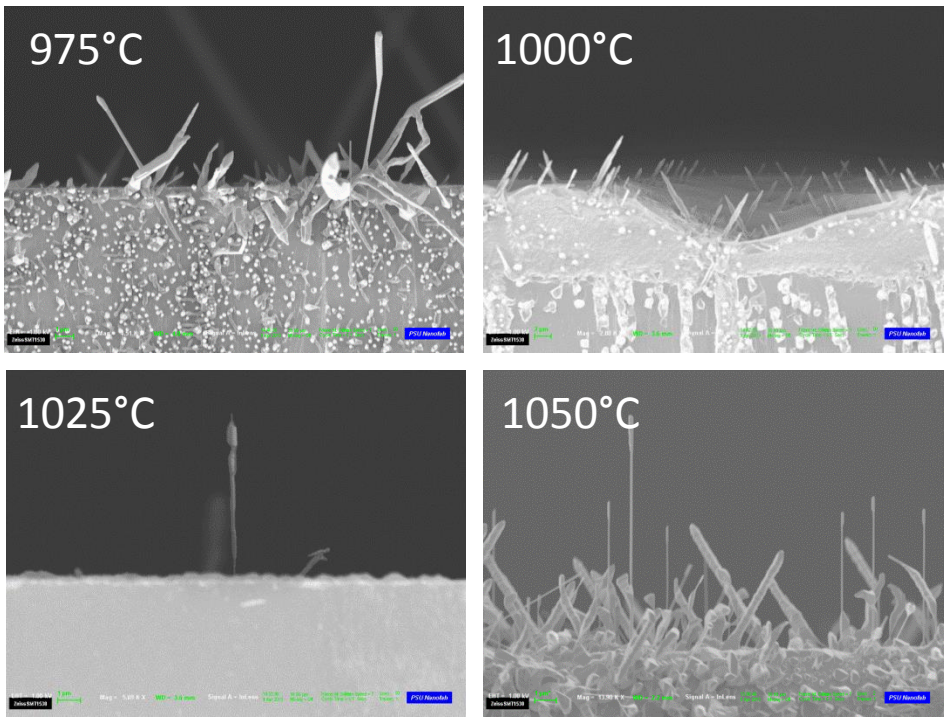


Figure 20- Si nanostructure growth with $SiCl_4$ on Si (110) using Au-nanoparticles at 975-1050°C growth temperatures.

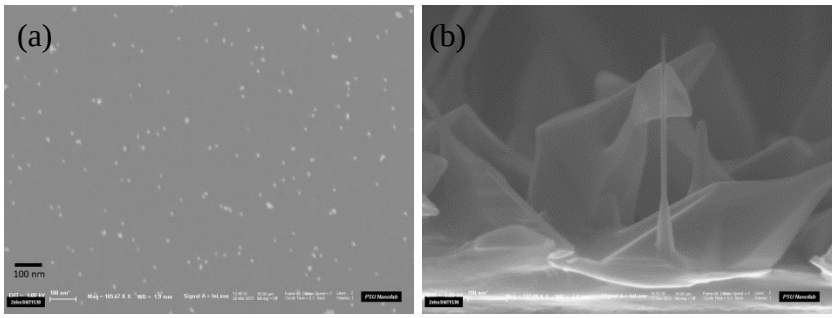


Figure 21- (a) 5nm Au NPs on Si (110). (b) SiNWs grown from 5nm Au NPs on Si (110).

In addition to the challenge of obtaining small catalysts which lead to small diameter nanowires, it is also challenging to obtain a high growth rate from small diameter nanowires. As the nanowire size decreases, the growth rate of the nanowires decreases. This is due to the Gibbs-Thomson effect, which arises in VLS growth from a change in the chemical potential. For growth of the <110>-nanowires we have found this same effect, in which the silicon nanowire growth rate decreases with a decrease in nanowire diameter. Previous studies have shown that the nanowire diameters are similar or slightly larger than the catalyst diameter. A slight increase in the nanowire diameter can occur due to an increase in the volume of the catalyst with the addition of silicon.

Oxidation of nanowires

We are now able to consistently grow nanowires with a controllable crystallographic orientation using Au-catalyzed VLS. This growth is done at high temperature with a $SiCl_4$ precursor. The Au precursor is deposited as a thin layer and then agglomerates when exposed to the temperature of the furnace. Although this technique has been successful in allowing us to control the crystal orientation of the silicon nanowires by choosing the crystal orientation of the silicon wafer substrate, the diameters of the wires are too large to see the effect we are looking for. In order to decrease the diameter, we first tried to decrease the thickness of the gold film. This worked to some extent, but if the film was too thin we either move out of a region of epitaxial growth or we had a low yield of <110> wires. We then tried to use small colloidal catalysts but were unsuccessful in decreasing the diameter of the nanowires and we had difficulties growing <110> wires. The catalyst particle agglomerated, producing large diameter wires. In addition to being larger diameter, these wires had a low yield of the desired <110> orientation. Hence our focus for Au catalyzed VLS wires was to reduce the diameter after growth. We tried two methods to reduce the diameter of the nanowires post growth: (1) oxidation and subsequent HF-etching and (2) KOH-etching. We applied these two techniques to Au catalyzed VLS grown nanowires and nanowires made with metal enhanced etching of silicon wafers using a silver catalyst.

Some of our VLS growth processes results in a bimodal distribution of wires: large diameter <110>-oriented wires normal to the substrate and smaller diameter <111>-oriented wires canted from the surface (Figure 22). The bimodal distribution presents a very feasible processing route toward a homogeneous population of <110>-oriented wires; namely, we can etch away the unwanted <111>-oriented nanowires while leaving the <110>-oriented nanowires intact. Thus, shrinking the wire diameter by wet etching or a combination of oxidation and wet etching attains two desired properties in the same process: it reduces the diameter of the wires hopefully into a regime where the infinite crystal approximation is no longer valid and it removes all non-<110> oriented wires. The idea is shown in the figure below. Larger (vertical) <110> nanowires are combined with smaller (slanted) <111> nanowires.

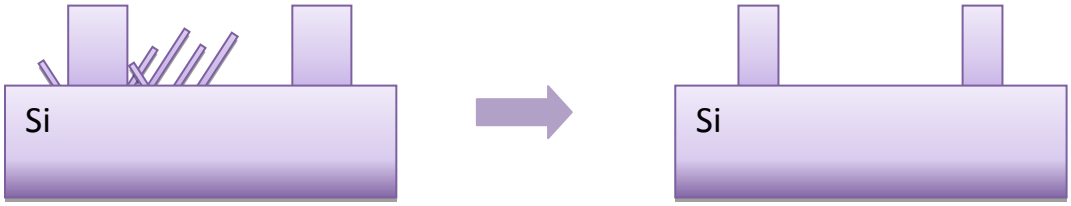


Figure 22- A schematic of how we will remove the smaller nanowires leaving only those with the preferred crystallographic orientation.

For this experiment we used wires grown on <111> wafers, so all nanowires are in the <111> direction, but large and small wires are also observed in this sample as well. We did a gold etch on the samples to remove the gold tips. Removing the tips of the gold is known in the literature, but we brought this technique into our lab and refined the technique. In addition, we followed a procedure from the literature [Kendrick, 2010] which prescribes a more thorough clean to remove gold inside the nanowires. This was then followed by an oxidation at 900C for 2 hours, and then a second gold etch. As can be seen in figure 23 b), the nanowires tend to clump

together making it difficult to determine if the smaller wires were etched and if the larger wires remained. Large wires seem to have fallen over. In addition figure 24 shows a close up picture of wires before and after the gold removal.

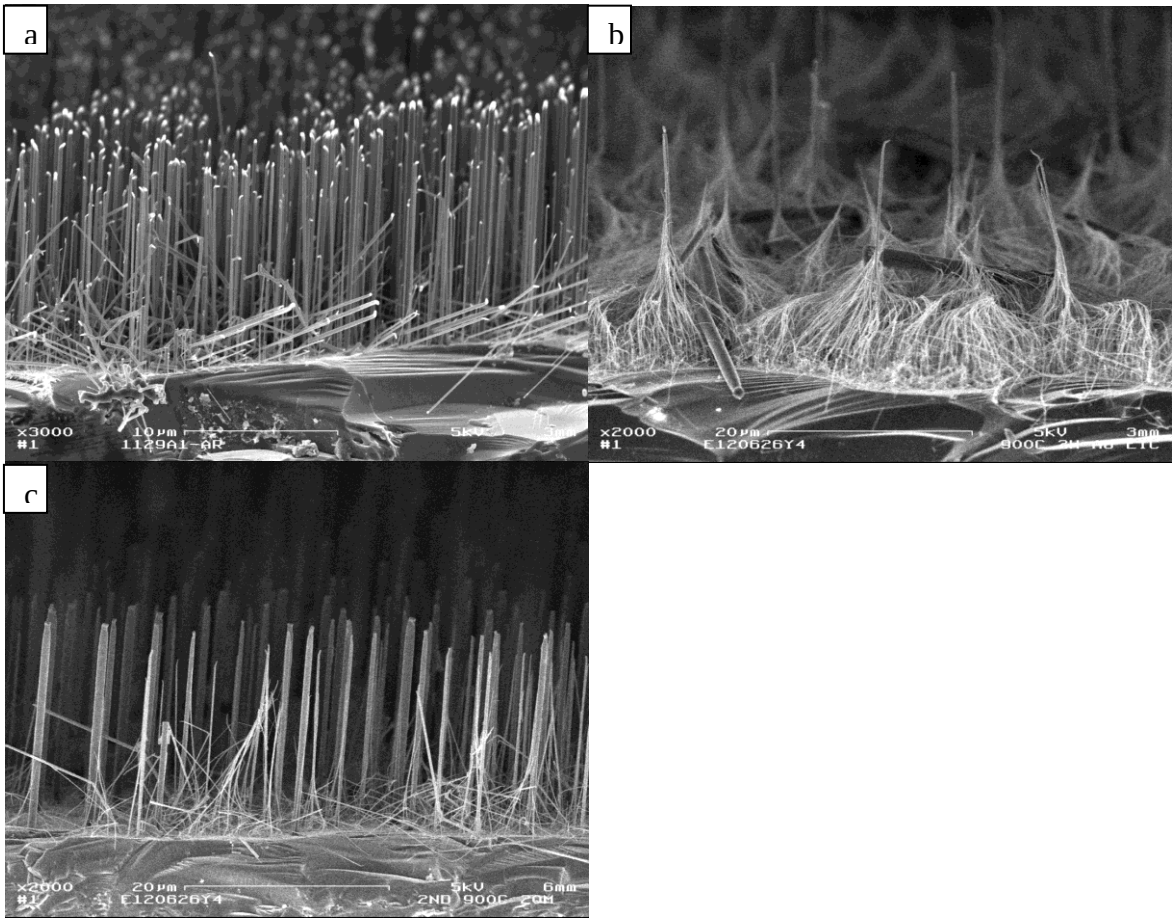


Figure 23- a) Nanowires as-grown. b) Nanowires after an oxidation and gold etch. c) Nanowires after an oxidation and gold etch, but with IPA used in the rinse sequence.

This clean starts with an oxidation and an HF to remove gold inside the nanowires and then follows with the standard potassium iodide gold etch.

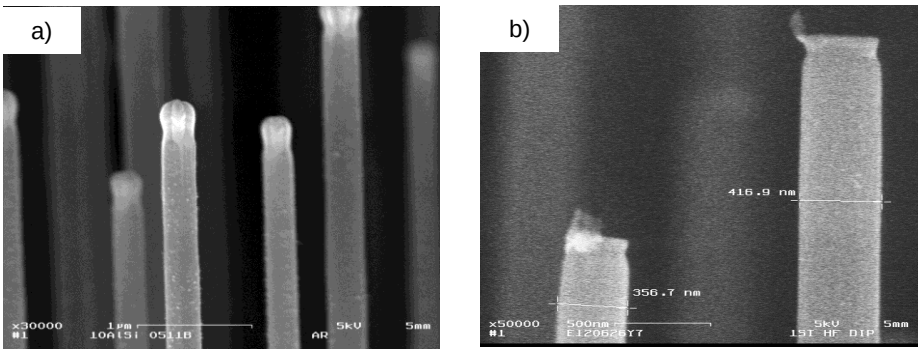


Figure 24 a) As-grown nanowires, with visible gold catalysts still attached to the wire tips. b) Silicon nanowires after a single round of gold etching.

These first attempts to use oxidation to decrease the diameter to the nanowires had uncontrolled conditions and the nanowires formed "tents" upon removal from the etch solution. We then added a final IPA treatment after rinsing in the water. So we did a gold etch, oxidation, and then a second gold etch, and included a final treatment IPA after rinsing in water. This helped fix the clumping problem of the nanowires, but not completely solve it. In addition this result was not repeatable. However, Figure 23 shows that some of the smaller diameter wires have been removed in this sample.

By purchasing a critical point dryer and using this to dry the wafers after the etch process, we fixed the clumping issue. Now both facilities (PSU and Bandgap) are equipped with critical point dryers which reduce the influence of surface tension on the structures when drying and eliminate the tenting effect.

Using the IPA and critical point dryer, we experimented with oxidation of the nanowires to shrink them. One of our oxidation processes involves oxidizing the wires under a nitrogen atmosphere for varying times at 900°C, and then etching with hydrofluoric acid. The samples featured in figure 25 show a non-monotonic decrease in the diameter of the nanowires as the oxidation time increases. This may be due to incomplete etching of the oxide or shearing off of smaller nanowires when the longest oxidation time is used, making the population averages misleading. In addition, we observe some surface defects after the oxide etch. The surface started to roughen if we weren't careful in terms of removing the oxide after oxidation. We discovered that removing the oxide with a plain 10% dilute HF left the wires much smoother than when this oxide was removed with a BOE.

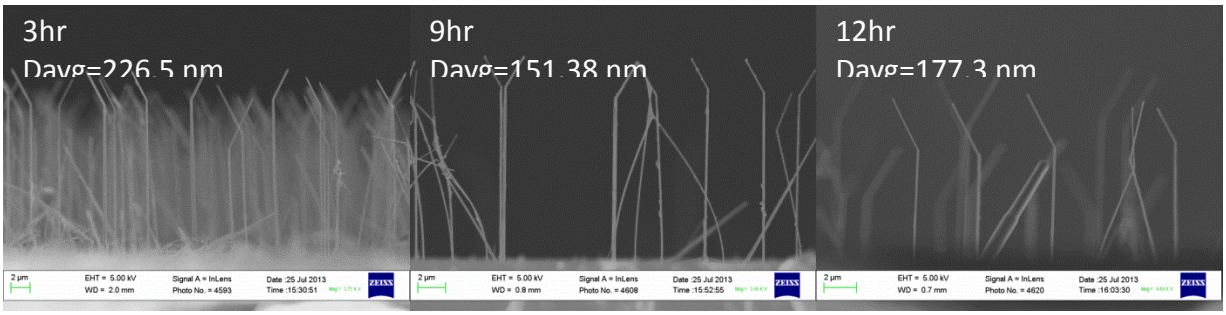


Figure 25- An oxidation-and-etch series of <110> nanowires, with oxidation times of 3, 9, and 12 hours. The average diameter decreased by 60, 139, and 123nm, respectively.

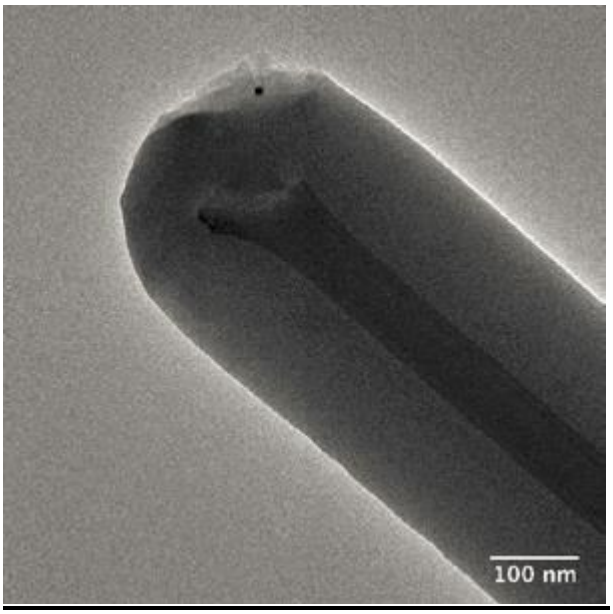


Figure 26- A TEM of an oxidized silicon nanowires after 8 hours of oxidation.

Wet etching of nanowires

We also explored a wet-process for reducing wire size. This has the benefit of being a low temperature process and therefore won't diffuse in any metal contaminants like oxidation might. Furthermore, KOH often leaves <111> surfaces exposed, which should increase the desired Bandgap Activation™ effect.

Figure 27 shows metal-enhanced etched nanowires with base diameters of ~60-70nm which reduce to ~30-40nm after just 5 seconds in 5% KOH. These wires were rinsed in water and then the water was exchanged for ethanol for drying in the critical point dryer. There was no measureable photoluminescence signal from the KOH-shrunken nanowires in our optical setup even after Al_2O_3 coating and activation.

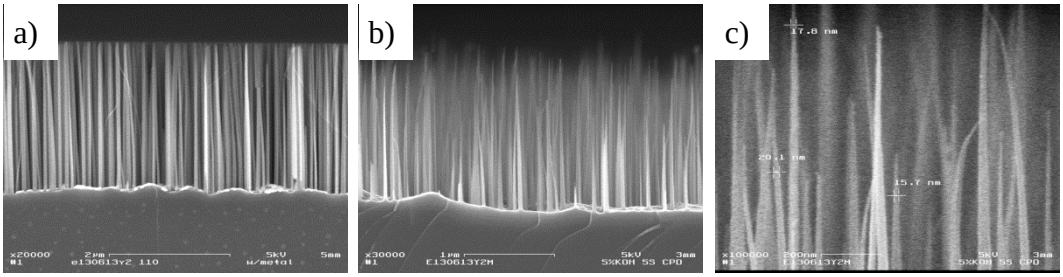


Figure 27 (a) As-made metal-enhanced etched nanowires on a (110) substrate. (b and c) The sample from (a) after a short dilute KOH etch. The wires have reduced in both length and diameter, with the taper becoming more pronounced.

Task 1.4 Investigate the effect of nanowire diameter, catalyst type, and post growth H2 annealing on sidewall faceting of nanowires

In order for the Bandgap Activation™ effect to enhance the coupling between the gamma and the L-point, the wires need to have <111> surfaces. Thus the wire axis needs to be perpendicular to one of the <111> directions. <110> oriented wires are thus an ideal nanowire orientation for this work. Their generally round cross section might have enough of a <111> component to induce Bandgap Activation, but we may need faceted wires with all or mostly <111> sidewalls. We therefore studied faceting of wires.

Sidewall faceting on Au thin film catalyzed nanowires

The heart of Bandgap Activation™ lies in selectively emphasizing {111} planes and causing electronic carriers to "reflect" at these boundaries. Thus, we expect that shrinking the wire dimensions along the <111> directions and increasing the number of those interfaces will increase the probability of observing Bandgap Activation™ in our samples. Hence, the nanowires with smooth and numerous (111) facets are desirable. Using a density-functional tight-binding method, Zhang et al.[Zhang 2005] calculated the cohesive energy and stability of commonly observed low-index surfaces of hydrogen-passivated SiNWs with growth axes along <111>, <110>, <100>, and <112>. They found the surface energy of (111) planes was smaller than that of (110) and (100) surfaces. The volume and surface area interact to determine the most stable outer configuration, so there are a number of allowed cross-sections, some of which are reproduced in Figure 28. We found that some of our Au thin film catalyzed nanowires have sidewall faceting, albeit at larger diameters than might be expected. In figure 28, transmission electron microscopy shows that a nanowire with the <111> growth axis has a cross-section corresponding to a hexagonal (110)-faceted structure and a <110> wire has a (111) and (100)-faceted structure. Future and on-going work involves polishing the nanowire arrays and observing the faceting on a large number of nanowires.

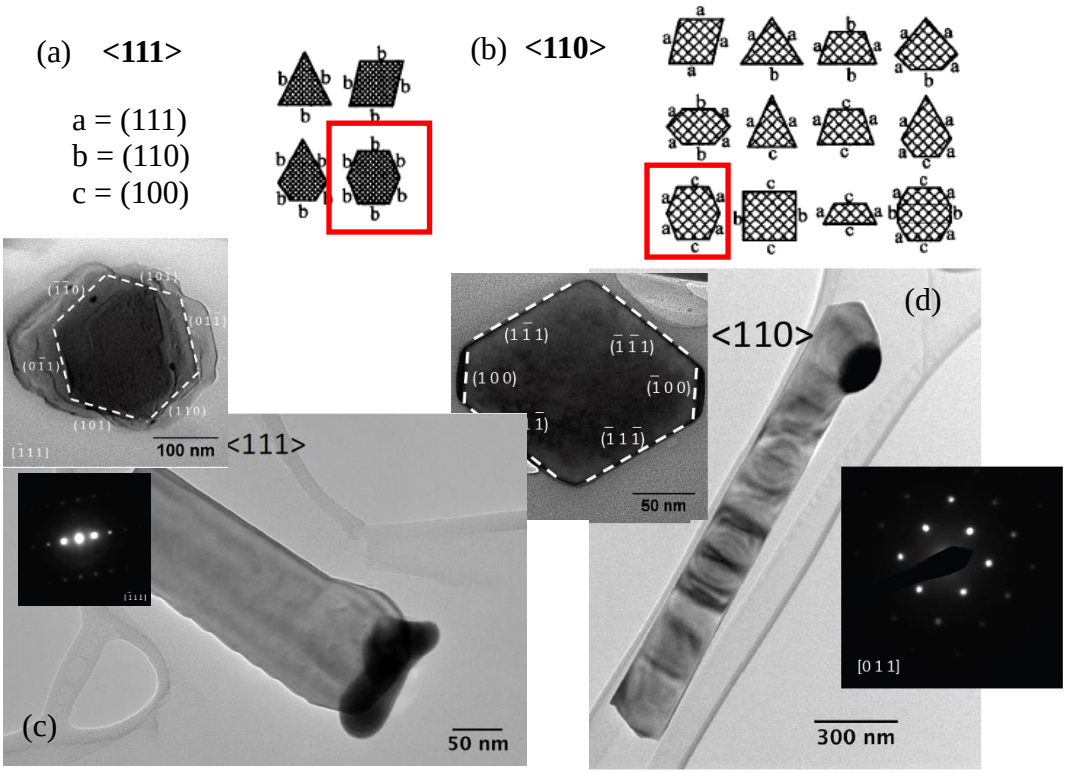


Figure 28: (a) and (b) Possible faceting of <111> and <110> silicon nanowires (figures reproduced from Zhang (2005)). The boxed configurations correspond to the cross-sections observed in the <111> and <110> nanowires shown in the TEM images below in (c) and (d).

KOH

Our synthesis work has been focused on <110>-axis nanowires due to the energetically favored (111) faces expected for that structure. In addition, obtaining (111) planes on silicon is a common process in semiconductor processing. One commonly used process to facet silicon is the anisotropic potassium hydroxide (KOH) etch. Since Si atoms with the highest number of bonds connecting it to the plane behind it (back bonds) are in the (111) plane, this orientation etches the slowest in the KOH etch. Thus KOH etching exposes (111) planes. When etching a flat silicon surface, this creates pyramids. These pyramids are used as an anti-reflective surface texturing for monocrystalline silicon solar cells, where the etch is nucleated at defects on the surface of the wafer (Fig 29(a)).

We wondered if these exposed surfaces would show the photoluminescence that we are looking for since the surface has the desired faceting. However, these pyramids on a bulk substrate did not show photoluminescence, even when passivated with an Al_2O_3 coating. The lack of photoluminescence on these samples is unsurprising because (1) the pyramids created in the usual process are typically on the micron scale, which is larger than desired, and (2) any excited electron-hole pair may be able to find a non-radiative recombination pathway. To address the size of the texturing, we used a variant of Bandgap's metal-enhanced etch process which produces nanometer-scale pyramids and truncated pyramids (Fig 29(b) and (c)). The size of the

pyramids can be further tuned by varying our process. For the second issue of the free carriers escaping to the bulk substrate and recombining, we would need to decouple the nanostructures from a bulk silicon substrate.

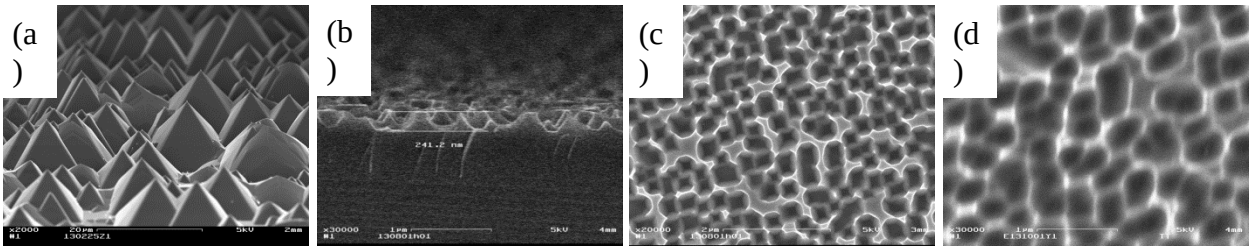


Figure 29- (111)-face dominant structures. (a) Typical pyramids formed with (111) faces on (100) substrates with a standard monocrystalline anti-reflection KOH process. The pyramids are on the order of 10um in height. (b and c) Cross-section and top-down view of a similar field of (111)-faced truncated pyramids created with Bandgap's etch process. Here the pyramids are ~few hundred nanometers in height. A subsequent KOH etch can be done to further highlight (111) faces. (d) Top-down view of an initial attempt to transfer the Bandgap recipe to a thin-film silicon-on-insulator substrate. (111) faces are less pronounced.

In addition to KOH of a bare silicon wafer, we also preformed KOH on silicon nanowires. However, the KOH was either too strong and etched away the wires completely, or too weak and didn't etch at all.

Task 2.1 - Characterize the absorption and photoluminescence properties of <111> and <110> oriented Si nanowire arrays as a function of wire diameter, catalyst type, and surface passivation

The purpose of this project was to demonstrate via optical luminesce the effect of increased electronic coupling between the gamma and L points in silicon and how this increase in coupling is dependent on the direction in which a silicon lattice is truncated in a nanowire. In other words we wished to produce two sets nanowire arrays, one which should show the Bandgap Activation effect, and one that should not, and compare the PL signals of these two sets of nanowire arrays. Previously PL of a single nanowire at the energy of the gamma to L point transition was observed for a nanowire with a crystallographic direction that should couple the gamma and L points and was not observed for a single nanowire with a crystallographic direction that should not couple the gamma and L point directions. However, the nanowires made in this study are not feasible for solar cells. First of all, they are single wires, while commercially viable solar cells need to cover football fields. Secondly, the nanowires were coated in SiO2 making them difficult to electrically contact. Thirdly, they are not aligned and so making arrays of them is challenging.

For this project, we sought to have the same enhanced optical signal as observed in Holmes et al. [Holmes 2000], but made with arrays of nanowires which we could easily contact and make solar

cells out of. We were not successful in finding the optical signal observed in the single wire measurements on the large arrays of nanowires. There are many possibilities for the lack of this optical feature, and likely different nanowire arrays prepared differently have different reasons for why this optical feature was not observed.

In order to see the PL signal from the enhanced transition between the gamma and L point, we expect many properties simultaneously have to be met.

Small diameters Holmes's wires were 4-5nm. This effect was observed in bismuth for 200nm wires. We were able to decrease our nanowires to around 30nm in some cases.

Crystallographic orientation. In order for the electronic states to couple for Bandgap Activation, the wire's orientation needs to be perpendicular to the <111> so that part of the wire edges are in the <111> direction. This will allow coupling between the gamma point and the L point (111). Both the Holmes' <110> and our <110> wires meet this criteria.

Passivation – In order for radiative recombination to dominate an optical signal, all other non-radiative radiation mechanisms need to have a lifetime longer than the radiative recombination lifetime. If a silicon surface is not passivated properly, free carriers recombine very quickly near the surface. In the Holmes study, the wires are passivated with SiO2 and in hexane. We passivated our nanowires with SiO2 grown by wet thermal oxide, SiO2 grown by dry oxide, and alumina oxide grown by ALD.

Faceting – Some VLS wires are faceted and often the facets are in the desired <111> direction. This faceting could increase the coupling as a result of mixing of electronic states. We do not yet know if faceting is required to see this coupling, if it helps, or if it is not needed. Possibly it is needed for larger diameter wires, but not smaller diameter wires.

Impurities – In addition to good surface passivation, high quality silicon is required to have a high lifetime nanowire. If metallic impurities are present inside the nanowire that act as recombination centers for free carriers, these free carriers will recombine non-radiatively and a PL signal as a result of an electronic transition won't be observable.

Testing – In addition to making nanowires of the proper qualities, the nanowires might also need to be tested under proper conditions. Some questions that still need to be answered are: do we need lower temperatures to see this PL? What is the best excitation wavelength to observe the PL? How intense does the light need to be to get a strong PL signal?

The manufacturing capabilities of nanowire arrays were not mature enough at the beginning of our grant to achieve these goals. Unfortunately, we did not have a good sense of which parameter(s) are required to have the enhanced coupling and to what extent. We therefore focused on what we considered most essential: 1) producing <110> nanowires without the use of gold, which is a known minority carrier lifetime killer in silicon 2) producing nanowires with smaller diameter, and 3) passivating these nanowires.

We tried many different nanowires and testing setups. We compared nanowire arrays with bare silicon. This comparison allowed us to determine more accurately which optical signals are a result of the nanowires and which are present in bulk silicon. Since <111> nanowires are made on (111) silicon and <110> wires are made on (110) silicon, we tested both (111) and (110) silicon wafers. We list some of our measurements below to assist others in future experiments.

Originally, we preformed PL on our in-house PL setup. In this setup, we used 405nm laser excitation. The PL off the sample was captured by a large lens, collimated, and refocused onto a spectrometer with a filter that blocked the excitation light. We tried to focus the light as well as leave the light unfocused for these measurements, but neither showed the signal we were searching for.

We then switched to a 266 nm pulsed (10Hz) Nd:YAG laser at Harvard CNS since we expect to see a higher PL for higher energy excitation. We observed PL from the direct transitions at Γ ($E_{\Gamma 1}$=4.2eV and $E_{\Gamma 2}$=3.4eV), which confirms that our setup was well tuned and would have picked up a PL signal if it was roughly the same strength as the direct transition. Both bare Si substrates and NW covered Si showed PL. This was true for both (111) and (110) orientated substrates.

We focused the excitation light onto the sample. This increased the PL signal, but if we focused too strongly it ablated the sample. This confirmed that we were getting sufficient (too much) light intensity per area for the incident light. When we removed the focusing optics, we still had a PL signal, but it was much weaker with less sharp peaks. We decided that the effect we are seeing should be quite intense and so a defocused excitation light source is probably sufficient and doesn't destroy the sample.

Most samples were checked for PL in our in-house setup. We measured Au VLS wires, Al VLS wires, and metal enhanced etched wires. We also measured wires that were as-grown SiNWs, SiNWs with an ALD Al_2O_3 coatings (both <111> and <110> -oriented nanowires).

In addition to oxide passivated nanowires, we also suspended nanowires in an isopropanol solution hoping that the solution passivation would passivate nanowires even if they had porous sections. The nanowires are released from their growth substrate by sonicating in isopropanol for 5 min to 5 hours, depending on nanowire length and diameter (Figure 30). The nanowire solution randomizes the orientation of the nanowires' axes relative to the incident laser beam, eliminating any direction dependencies of the measurement. For these samples we measured photoluminescence, but we also measured transmission/absorption. Photoluminescence is a powerful tool since you only get a signal from nanowires that emit light and so your signal to noise ratio should be quite high. However, any non-radiative recombination mechanism can quench your PL signal. With optical absorption, all of the sample will absorb light, but this measurement is a more direct measurement of the electronic transition strength and is not dependent on other recombination routes.

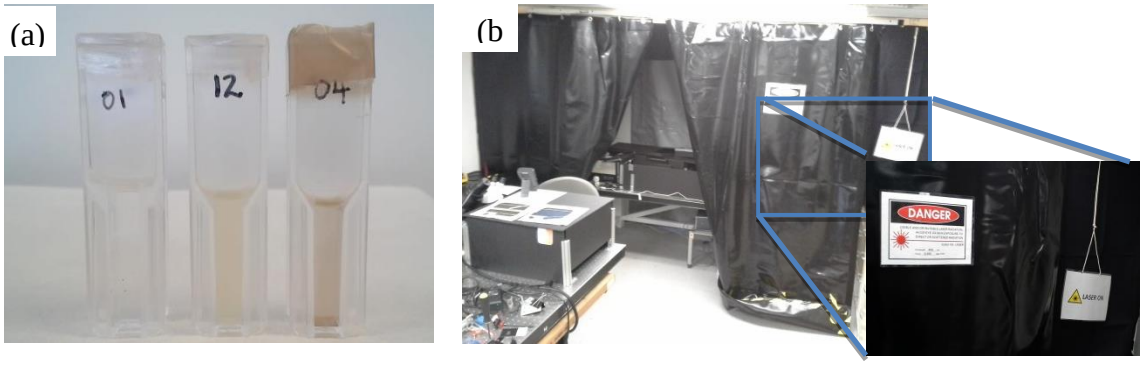


Figure 30: (a) Isopropanol suspension of silicon nanowires for transmission studies and orientation-independent optical studies. The leftmost cuvette has isopropanol only and the other two have nanowire suspensions. (b) Newly installed laser curtain isolating the photoluminescence setup from the rest of the optics lab. Inset: Laser information and warning signs.

The smallest diameter wire arrays that we measured were made by metal enhanced etching using silver as a catalyst. These wires had diameters 30-100 nm at the bases and less than 20nm at the tips. For testing, we often placed these nanowires in solution thus we needed long nanowires, 2-5um long. We tested the as-grown wires on substrate and in solution optically. We also tested them after oxidation and etching and after passivating the surface using various techniques. They did not have measurable PL resulting from Bandgap Activation.

The results from the bare substrates and the silicon nanowire arrays are shown in figures 31 and 32. From these figures, it is clear that the PL from samples with nanostructures have more features in their spectra than plain silicon substrates. Consistently, the nanowire arrays had more features in their optical spectra than the equivalent bulk Si wafer samples. The origins of the additional features in the nanowire arrays are unclear. We were searching for a large optical signal that is consistently present in <110> nanowires and not in bulk (110) Si nor in <111> nanowire arrays. We did not find such a signal.

We can however make some interesting observations from the data. The data show in figure 32, indicates that wires with the wire-shrinking silicon oxide have the same spectra as wires passivated with alumina deposited by ALD. The blue curve is a spectra from a sample with both <110> and <111> silicon nanowires passivated with alumina oxide while the black and green spectra are measurements from nanowires with after the oxidation and with this oxide remaining on the surface. The black and green spectra was also taken on wires with both <110> and <111> wires present. Although the PL features look similar in these two sets of spectra, the features in the sample that was oxidized might be stronger. It is possible that the smaller diameter wires in this sample (blue curve) result in a stronger PL. The intensity of PL is very sensitive to the measurement setup and therefore it would be difficult to conclude on this result without an elaborate study.

In order to compare the <110> and <111> signals, we divided the spectra from a sample with <110> nanowires a spectra with only <111> nanowires. Any features that are only present in <110> wires and not <111> wires, would be prominent by dividing these two spectra. See (Fig. 33). Although they are some smaller features in this graph, the features were so small, that the result is inconclusive. One peak of possible interest is the small peak at 632nm, which can be

seen in the raw data, See figure 32 and the divided spectra figure 33. This feature is near the energy of the gamma to L point transition and therefore could be the optical feature from the electronic transition we are searching for. However, this peak is not present in all <110> samples, which could mean that this is not the optical feature we are looking for, or it could mean that the feature is sensitive to growth or post processing conditions.

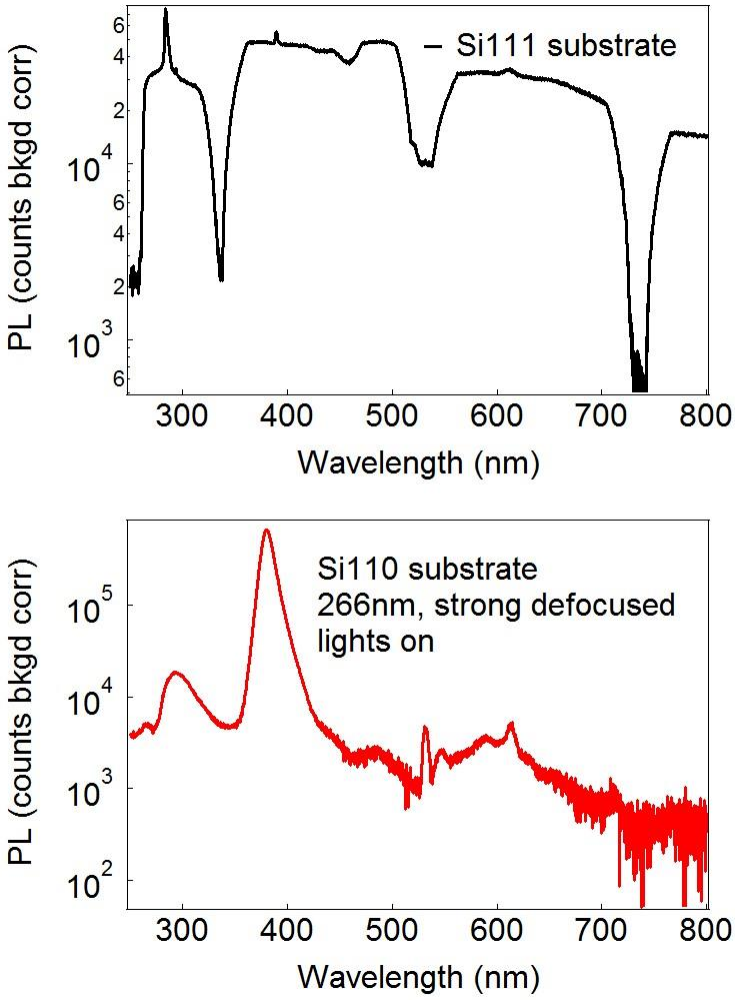


Figure 31- Photoluminescence at room temperature from a Si(111) substrate [top] and a Si(110) substrate [bottom].

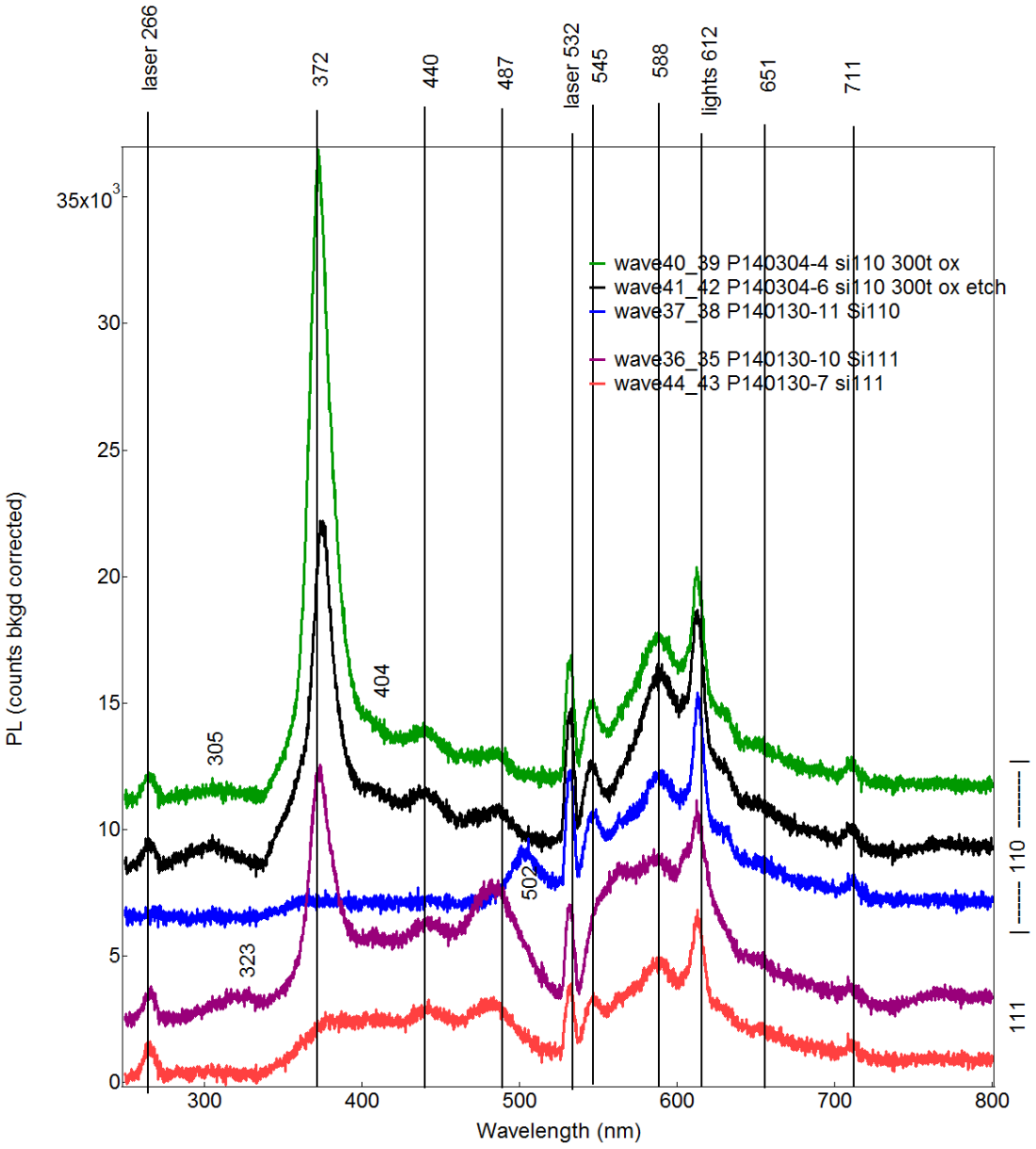


Figure 32- Photoluminescence at Si nanowires on their growth substrates. The top three traces are from a mix of Si(110) nw and Si(111) nw on Si(110) substrates, while the bottom two are from Si(111) nw on Si(111) substrates. All nanowires were grown using Al-VLS. The bottom three samples (blue, purple, red) were passivated with 30nm of alumina deposited by atomic-layer deposition. The top two samples (green, black) were nominally the same and deliberately oxidized to reduce the nanowire diameters, and then the "etched" sample had the silicon oxide removed.

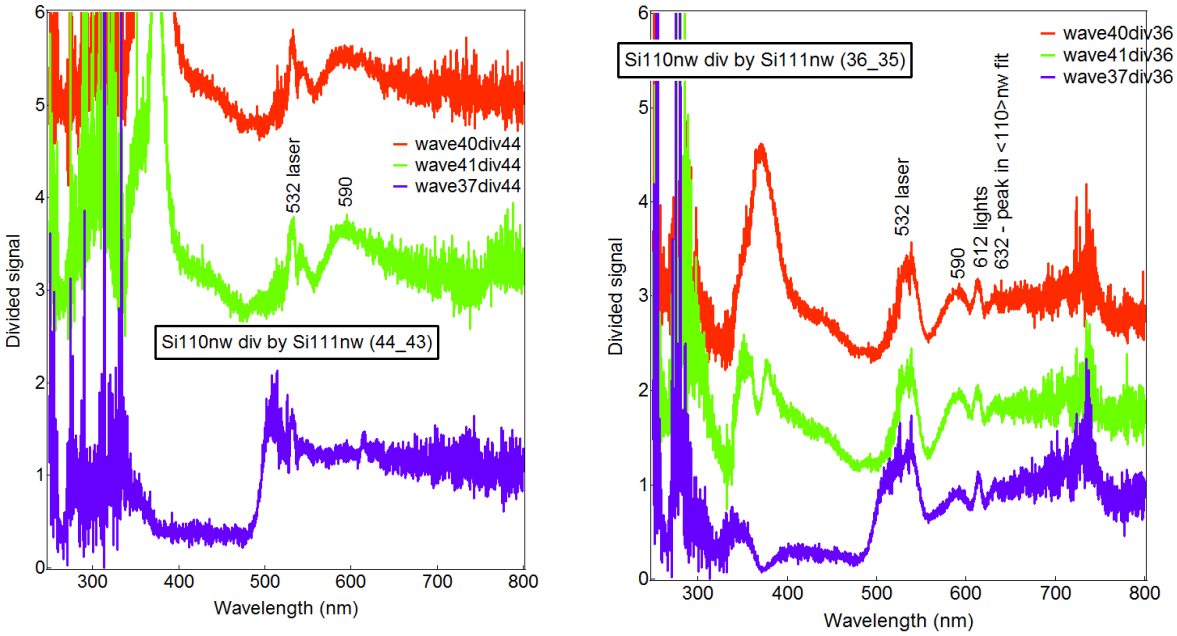


Figure 33- Differences in the photoluminescence of Si(111) and Si(110) nanowires should be magnified if their signals are divided, e.g. if PL from a Si(110) nw sample is the numerator and Si(111) nws are used as the denominator, any large peaks would correspond to when the Si(110) nw signal is enhanced relative to that of the Si(111). In the graphs above, the three colors represent three Si(110) nanowire samples as the numerators. The left and right graphs were created by choosing two Si(111) nanowire denominators.

We did not observe an intense signal that is consistently present in <110> wires and not <111> wires near the energy of the gamma to L point electronic transition. The lack of this signal could be the result of as-yet insufficient passivation, recombination at contaminants, an insufficient population of small <110>-oriented nanowires to produce a measurable signal, or a combination of the above. Although we know how to increase the likelihood of seeing Bandgap Activation (lower impurity concentrations, smaller diameter wires, higher quality passivation, more sensitive measurements, …), we don't know which parameter is limiting the observation of the effect. It is very time consuming and difficult to push the manufacturing capabilities of nanowires in so many directions at once. We therefore suggest a theoretical study of Bandgap Activation to guide further experimental work.

Task 2.2 - Two photon measurements

Since we did not observe a PL signal in the energy range of interest that was controllable with nanowire crystallographic orientation, it did not make sense to preform two photon measurements. We expect that once the wires with the right diameter, density, purity, orientation, faceting, passivation, and doping are fabricated that a large PL signal in the energy range of interest will be observed in <110> wires and not <111> wire. At this point, we recommend doing the two-photon measurements proposed for this task.

Task 3 - Studies of surface passivation

The optical properties, particularly the PL signal, are extremely sensitive to the condition of the surface, particularly for nanostructured materials, which have high surface to volume ratios. Electronic states arising from surface defect states or surface reconstruction can introduce trap states to kill radiative recombination or create spurious radiative recombination events. Thus passivating the nanowires is key to observing radiative interband recombination. We experimented with passivating our nanowires, with alumina oxide deposited with atomic layer deposition, silicon oxide grown with chemical oxidation, silicon oxide grown with a wet oxidation and silicon oxide grown with dry oxide.

The simplest method of passivating our nanowire arrays is to use the silicon oxide grown when shrinking the wires for surface passivation. The wire-shrinking oxide was grown using a wet oxidation method, wherein the nitrogen carrier gas is bubbled through water and then into the process chamber. Normally to attest surface passivation quality, one passivates the surface of a high quality wafer and then measurements lifetime. You can thus assume that the minority carrier lifetime is limited by surface recombination velocity (not bulk recombination since the wife is high quality) and calculated an upper bound on surface recombination velocity. However, it is not straightforward to test passivation quality on nanowire arrays since the "bulk" recombination inside the nanowires is not known. In addition, the usual method of using a contactless photoconductance decay measurement, won't work on structures such as nanowires where the feature size is smaller than the radius of the eddie currents produced in the process. Therefore, in order to test the passivation quality of our oxide we replicated the oxidation process on an n-type float zone wafer. The thickness of oxide grown on a flat wafer is an approximation to what is grown on a nanowire, but not perfect since oxide grows slower on nanowires than on flat wafers.

A variation in oxide color on the float zone wafer was observed, indicating a variation in oxide thickness (Figure 34-left). This is most likely correlated to furnace position, as there is often a gradient in temperature and the availability of the reactant. The flat float zone wafers with this oxide had minority carrier lifetimes only several microseconds long, demonstrating that this method of oxidation does not effectively passivate the silicon surface. (Figure 34-right). This is as expected since wet oxide is known for not passivating silicon well.

Sometimes the quality of an oxide can be improved by a short, low temperature forming gas anneal. [Ebong 1999]. In an attempt to improve the oxide, we applied a 1 hour, 400°C anneal and retested the lifetime of the flat wafer. We found that the minority carrier lifetime was still low and had not measurably increased (Figure 34-right). Thus even with an anneal, this wet oxide does not effectively passivate the silicon surface.

In order to obtain a better passivation, we had to strip the wet oxide used to shrink the nanowires and replace it with either a hexane suspension, a silicon oxide grown by dry oxidation, or alumina. The hexane suspension was used to measure PL in Holmes [Holmes 2000] where they observed the increased PL for <110> wires compared to other wires. Dry oxidation gives a better quality oxide than wet oxidation and hence will passivation better. Alumina is known to passivate p-type silicon very effectively.

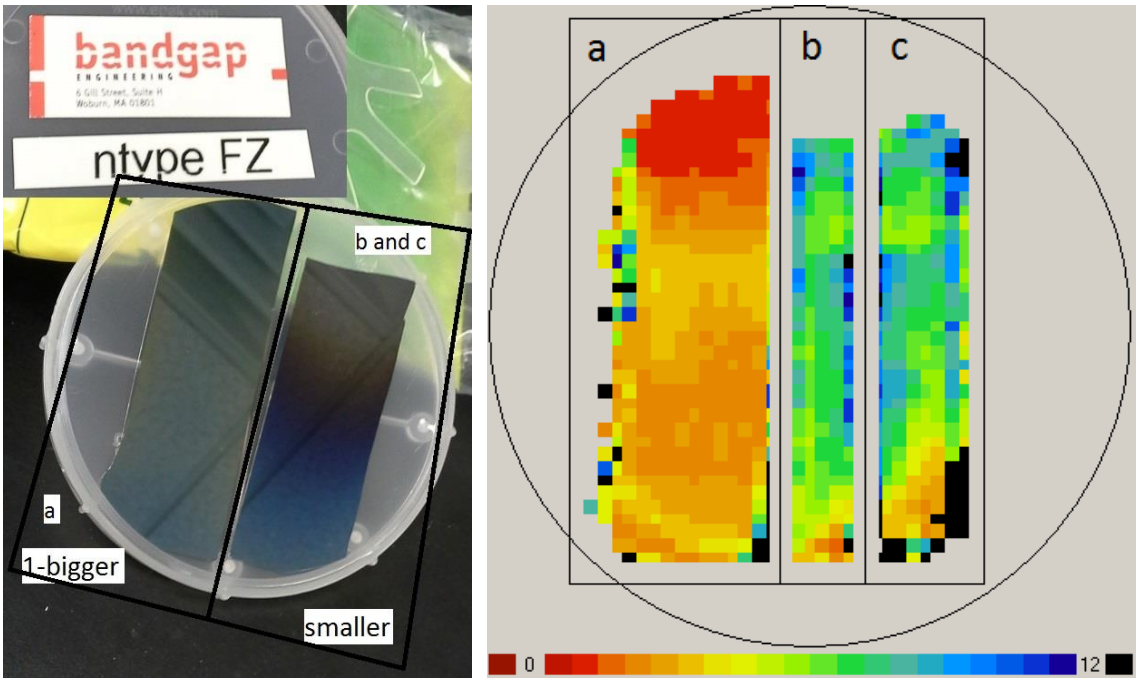


Figure 34 [Left] Float zone wafers that were oxidized with our nanowire-shrinking recipe. [Right] Lifetime mapping (in µs) of wafers on the left, with and without a forming gas anneal. All three pieces were oxidized at the same time, with pieces (b) and (c) at the same position in the furnace. (a) and (b) were not further processed. (c) was annealed for 30 minutes in forming gas at 400°C.

We have established recipes for surface passivation using atomic layer deposited (ALD) Al_2O_3. Because Au is prohibited in in-house facilities at Bandgap, we have further identified and utilized an external facility for alumina-coating Au-catalyzed nanowires. Prior to passivating, the Au is etched from the nanowires. It is evident from the SEM images when the Au tips have been removed and when the passivation layer is present (Figure 35).

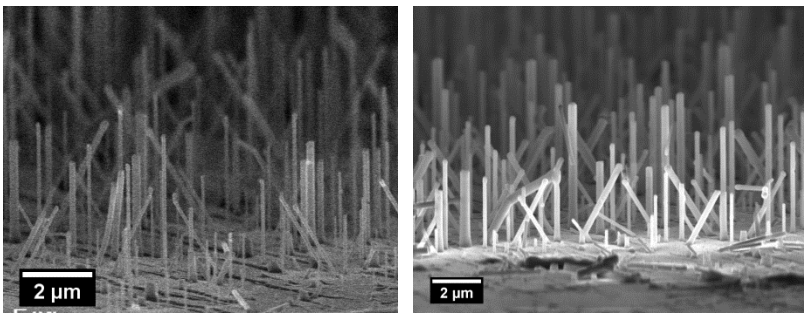


Figure 35- Sequential processing of nanowires on Si(110) synthesized by Au-VLS: (left) as-grown, (center) after Au-etch, and (right) after passivation with 30nm Al_2O_3 by ALD.

Deliverable / Milestone Deviations

We did not perform task 2.2 – two photon measurements, since we did not see the single photon measurement that we were looking for.

Outputs Developed Under the Award

Patents / Licensing Agreements

Patent appellation number 14/329,975 was filed on 7/13/14 with priority date from provisional patent application 61/845,931 filed 7/12/13 as a result of this work. The authors are Joanne Yim, Jeff Miller, Michael Jura, Marcie Black, Joanne Forziati, Brian Murphy, and Adam Standley. The title is "Doubled-etch nanowire process."

Honors and/or Awards

Publications

Eichfeld, S.M., Shen, H.T., Eichfeld, C.M., Mohney, S.E., Dickey, E.C. and Redwing, J.M., "Gas phase equilibrium limitations on the vapor-liquid-solid growth of silicon nanowires using $SiCl_4$," J. Crystal Growth 26(17), 2207-2214 (2011).

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Mel Hainey Jr, Sarah Eichfeld, Haoting Shen, Joanne Yim, Marcie Black, and Joan Redwing, "Aluminum-Catalyzed Growth of <110> Silicon Nanowires,´ Journal of Electronic Materials (2014)

Matthew R. Bergren, Chito E. Kendrick, Nathan R. Neale, Joan M. Redwing, Reuben T. Collins, Thomas E. Furtak, Matthew C. Beard, "Ultrafast Electrical Measurements of Isolated Silicon Nanowires and Nanocrystals," J. Phys. Chem. Lett.V5, pg. 2050-2057 (2014)

Presentations

There were many presentations that included this work.

Software

N/A

Other

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