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Title:	CMOS Imagers with On-chip Storage for High-speed Radiography
Author(s):	Kris Kwiatkowski (1), Vincent Douence (2), Yibin Bai (2), Atul Joshi (2), Nick King (1), Frank Merrill (1), Chris L. Morris (1), Paul Nedrow (1) and Stuart Kleinfelder (3) (1) Los Alamos National Laboratory, Los Alamos, NM (2) Teledyne Imaging Sensors, Camarillo, CA (3) University of California, Irvine, CA
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CMOS Imagers with On-chip Storage for High-speed Radiography

Kris Kwiatkowski[1], Vincent Douence[2], Yibin Bai[2], Atul Joshi[2], Nick King[1], Frank Merrill[1], Chris L. Morris[1], Paul Nedrow[1] and Stuart Kleinfelder[3]

[1]*Los Alamos National Laboratory, Los Alamos, NM*
[2]*Teledyne Imaging Sensors, Camarillo, CA*
[3]*University of California, Irvine, CA*

1th International Workshop on Proton Microscopy, GSI, Darmstadt, Federal Republic of Germany

LA-UR-09-

Talk Overview

- A bit of history: gated-CCD imaging (MCP, PFD, magnetic-diode shuttering and OE framing cameras)
- Example of direct-detect systems
- Rockwell (TSI) 0.5-Mpx Hybrid Imager
- Path to 2-Mpixel chip
- Other CMOS work: 64-frame "MegCam", and solid-state Streak Camera
- 3-D IC and sensor interconnect; 3-D vertical chip stacking

2002 pRAD Imager Requirements (2009)

	As met in 2004 ☺	New Requirements
• Number of frames/ views:	20 [3]	(64-128)
• Shutter time:	180ns	(< 10 ns)
• Inter-frame time:	350 ns	(70 ns)
• Array Size:	> 1M pixel [0.5Mpx]	(2 – 4Mpx)
• Dynamic Range:	11-bits	(12-bit)
• Well depth :	250k -to- 10^6 e^-	
• QE	> 85% (at 415nm)	
• Optical Fill-Factor:	> 90%	

First pRAD Camera Implementation: Single-Frame Gated CCD

Initially pRAD benefited from NTS PINEX program – PINEX had a steady multi-year imager R&D development (by 1992 NTS was transitioning from Vidicon/FPS- to CCD-based cameras)

- CCD array size: 380×244, 512×512 pixel (0.25Mpx)
- Shutter time PINEX: sub-1ns (TRP), ~20ns or none TIP ⇒ pRAD needed lower noise, 300ns PFD gating system was developed
- CCD issues at NTS: background stars, readout time…
- QE (Intensifier) > 15% (at 415nm)

Single-Frame Gated CCD

Shuttering: MCP or PFD

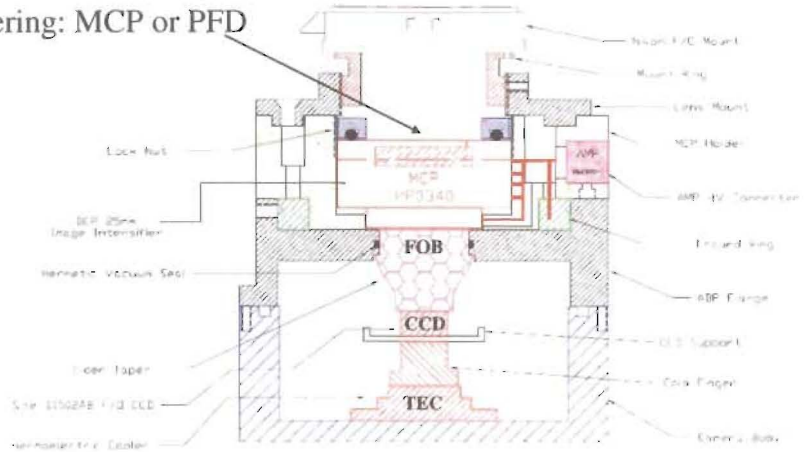
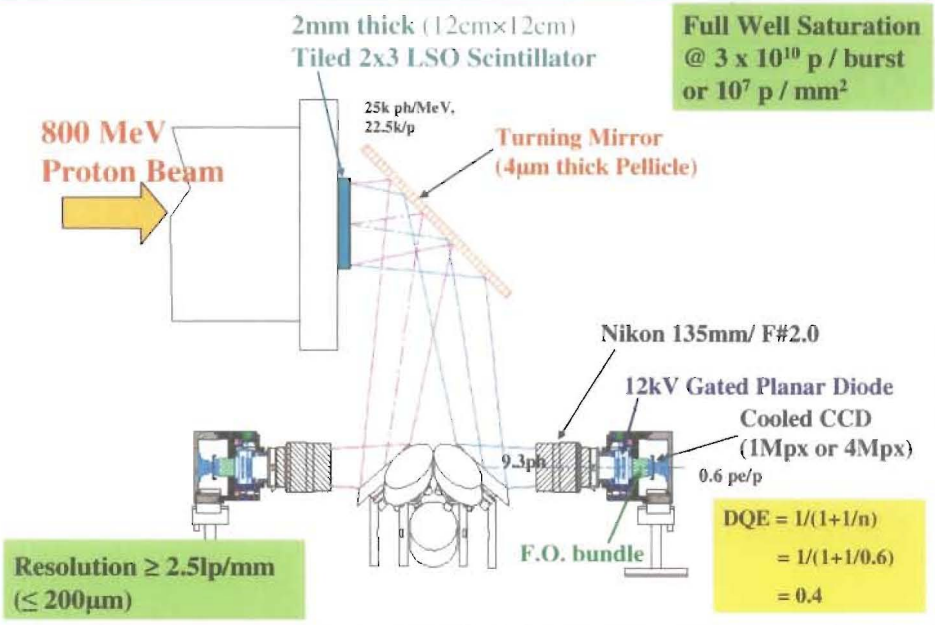


Fig. 2. Camera head section illustrating the vacuum-hermetic seal design (lower part of drawing), the intensifier housing assembly (mid portion), and lens mount (upper portion). The F.O. faceplate is bonded to the CCD.

G. J. Yates, et al, "An intensified/shuttered cooled CCD camera for dynamic proton radiography", LA-UR-98-0112

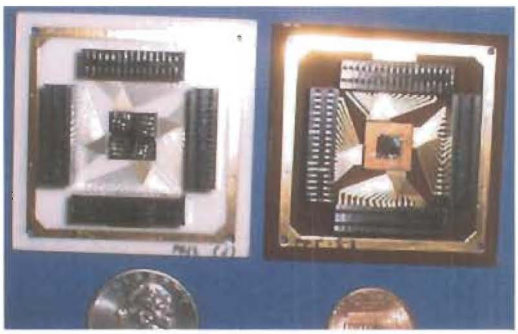
Seven Gated-CCD Imaging System



Attempt at Direct Proton Detection

Lens-coupled radiographic imaging systems (especially EO-based) are complex, need fast rad-hard scintillators, and suffer from low light-collection efficiency ⇒ DQE < 1.

Protons highly ionizing simple to detect directly, and should have DQE=1



In 1997/98 **LBNL** fabricated for LANL two 8×8 px proof-of-principle Silicon detectors, and fast signal-processing electronics. Depletion layer 2.7um deep on 300um thick n^{++} Si substrate. Pixels $(1mm)^2$ and $(0.5mm)^2$ with wire bonds connections.

Hans Ziock, et al., "Detector Development for Dynamic Proton Radiography", LA-UR-98-1015

Attempt at Direct Proton Detection

- Si Detectors work well, but large fluctuations due to nuclear reactions; longer term - radiation damage. Other issues: detector and interconnect capacitance, **interconnect** for small pixels – stack image plane, additional background plane, power dissipation, clocking,...
  (Thick ~100μm diamond or GaAs detectors w/ simple SF-based electronics, may be viable).
- H_2 ion-chamber, stack image-plane (multiple-cell)
- Also a possibility: secondary electron emission-, or Cherenkov detectors, …

Proton Detection in Si pixel detector: Fluctuations in Pixel Response

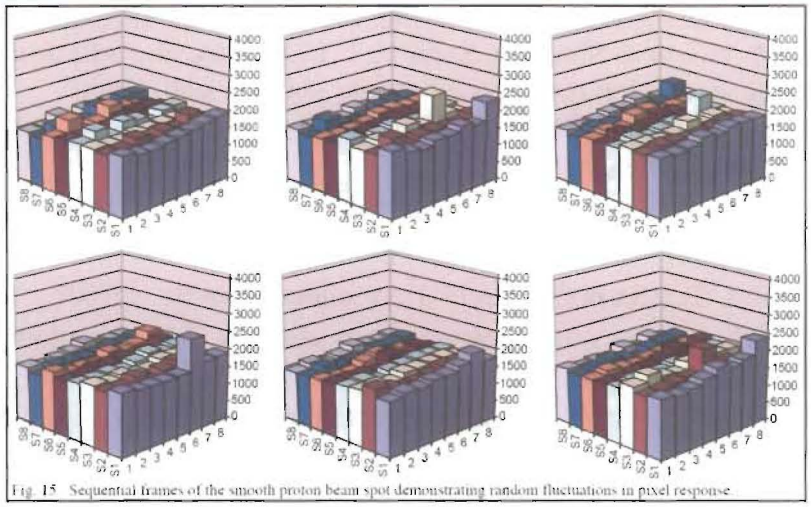


Fig. 15. Sequential frames of the smooth proton beam spot demonstrating random fluctuations in pixel response.

Hans Ziock, et al., "Detector Development for Dynamic Proton Radiography", LA-UR-98-1015

High-QE Indirect Optical Imaging Camera w/ Electronic Shutter

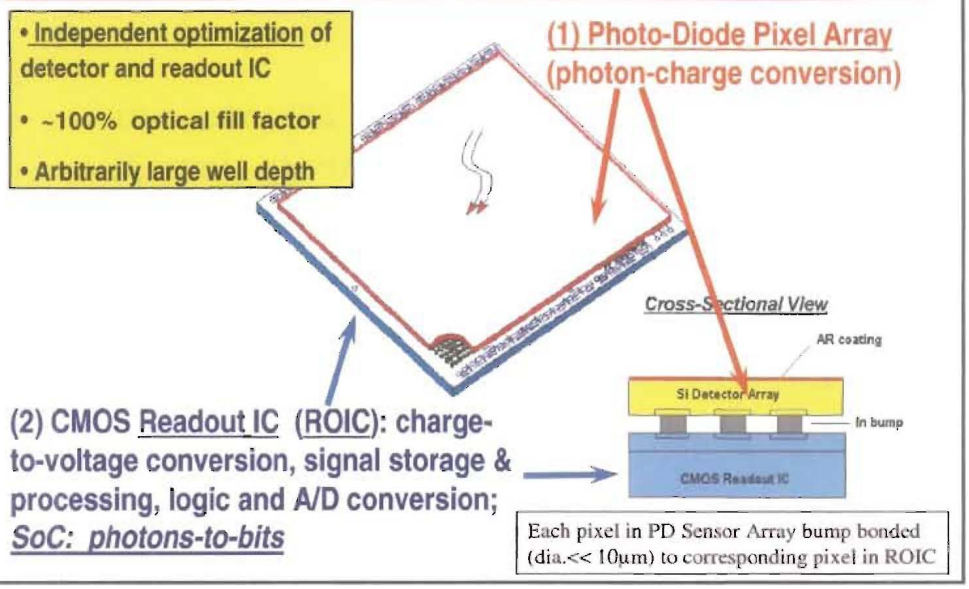
The two major problems of EO cameras – the complexity (resolution) and sensitivity (low QE and/or optical fill factor) – can be addressed with modern electronic Si technology. Industry (and to a degree the astronomers) have already invested big money (~G$) to develop the technology and fabrication foundries.

Si Technology Options for Fast Shutter (~100 ns) Optical Imager

- Fast **CCD**'s w/ electronic shuttering, on-chip storage (Princeton, MIT/LL, Summit, Simadzu, Sarnoff, ...). Issues with **radiation damage**, extinction ratio, asynchronous shutter, well depth, cost/chip yield, optical fill factor, pixel count, shutter speed,...)
- Monolithic CMOS APS
  - fill factor, low QE, shutter ratio, charge collection,... (PCO)
  - thinned back-illuminated APS - near future?
  - CMOSCCD (Sarnoff, Fairchild) excellent noise fig, speed?
- → Hybrid Imager: fully depleted photo-sensor + CMOS readout integrated chip (ROIC)

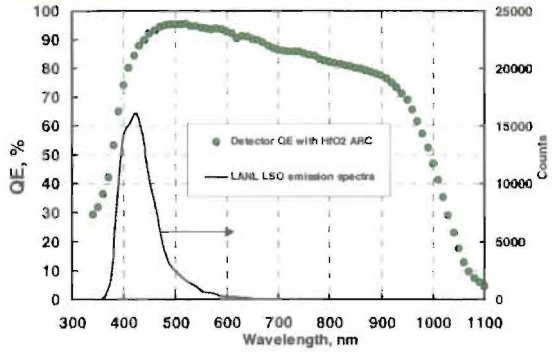
  Hybrid CMOS is still optimal approach, but interconnect and Si pixel/chip area limit number of frames

Imager as Two-Component Hybrid Focal Plane Array (FPA)



Silicon PD Array Has Advantages Over Monolithic CMOS or CCD's

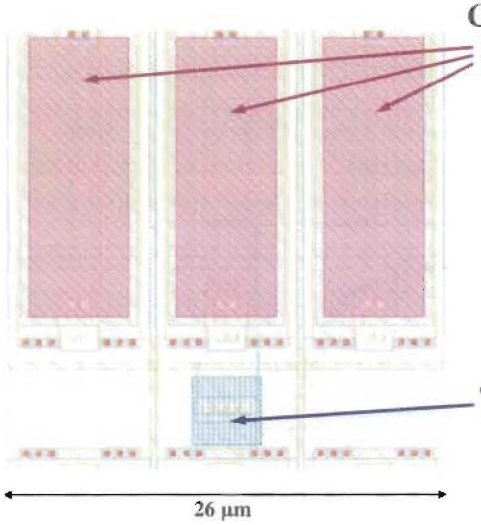
- 100% Fill factor (back-side illuminated)
- >95 % Peak QE (AR coating)
- Good spatial response (fully depleted)
- Low inter-frame cross-talk /good extinction ratio (storage node isolation)
- Broad band spectrum response (deep junction)



Fast Hybrid Optical Imager Pixel Layout Issues

- Imager operates in a burst mode, i.e. several frames stored in-pixel in analog form.
  Analog storage is area/ space intensive:
  e.g. if MiM capacitors used (0.8 fF/μm^2) then
  => 64 × 200 fF = 126 × 126 μm^2 min pixel size
- Conflict: frame storage and light-collection efficiency, x-talk favor *larger pixels*; whereas array pixel count, fab. Cost, size of optics, stray radiation → *smaller pixel* pitch
- Compromise: 26μm pixels (cost, reticle size)

ROIC Pixel layout, Metal Layer-4



26µm pixel footprint allows 3-frame storage, but 22mm CMOS reticle limits the ROICs size and array resolution to 720 × 720 px

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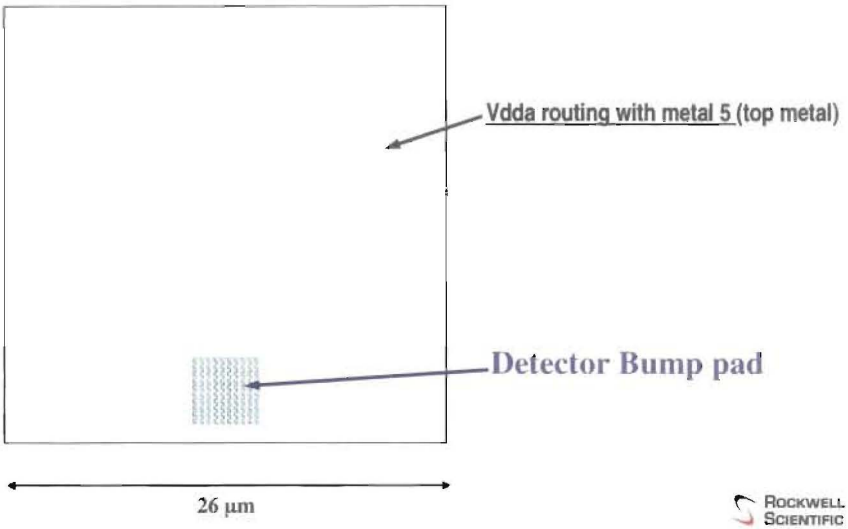
Fast Hybrid Optical Imager Electronic-Circuit Challenges

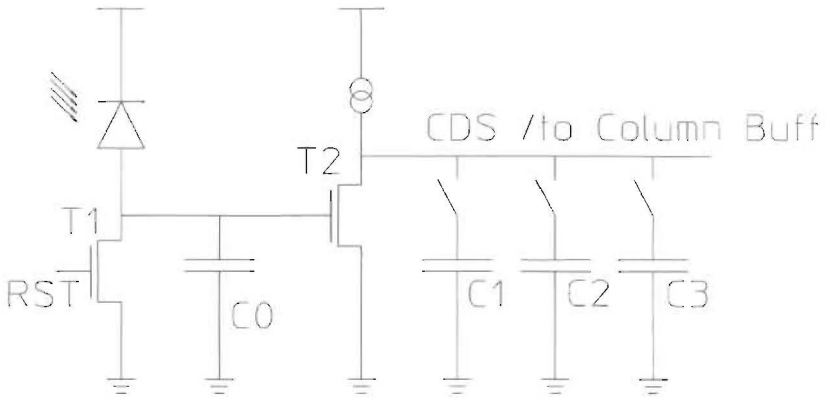
- Signal/charge in *all* pixels is acquired and integrated simultaneously (in < 200ns)
- No multiplex, every pixel needs complete front-end + storage electronics (total number of FET transistors ~14 million - CMOS saves the day)
- Instantaneous current delivery to Detector Array and to ROIC (low resistivity metal layers/ grids needed), settling times important

ROIC Pixel layout - Metal Layer 5



Rockwell Scientific

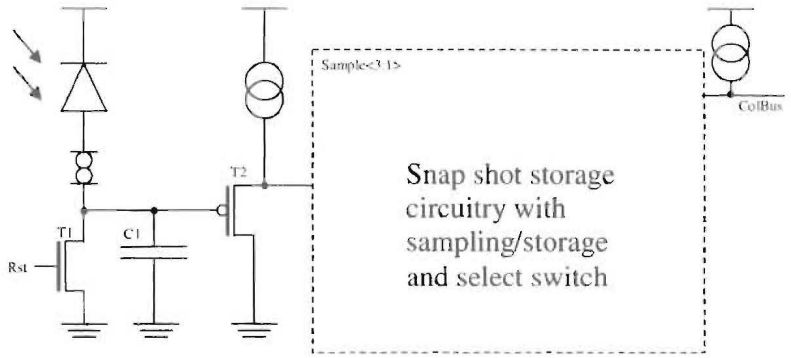
3-Frame Storage and Correlated Double Sampling (CDS) at Pixel Level



SF front-end - saturation determined by node capacitance: C_0

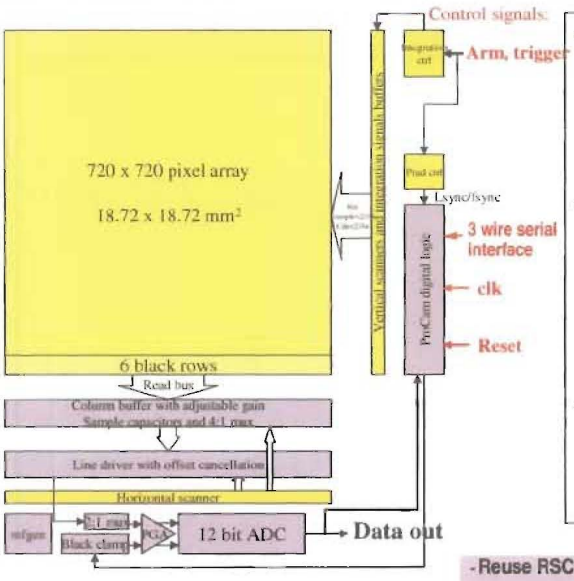
Voltage droop on C1 – C3 by FET leakage (sub-threshold) and quality of oxide

Pixel Design Provides Frame Storage and Correlated Double Sampling (CDS) Capabilities



SF front-end - saturation depends on the node capacitance: C_1

System-on-Chip (SoC) Architecture Simplifies Camera Integration



Imager block diagram

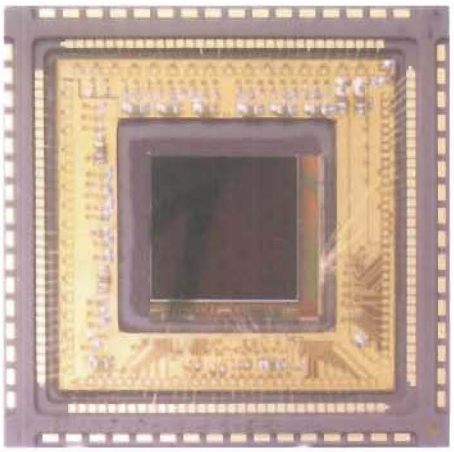
- Needs only external power, master clock and trigger signals (in burst mode); the chip sends out 12 bit digital video data.
- The imager requires dual (3.3V and 2.5V) power supplies, "high voltage" detector bias (~15V), and a few decoupling capacitors for the ADC internal references.
- Readout timing and biasing are generated on-chip and can be programmed through a serial interface.

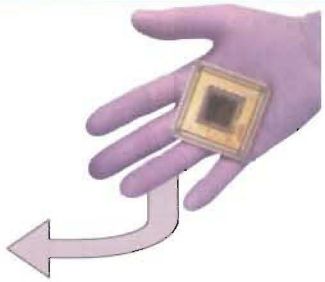
-Reuse RSC ProcamHD® IP : column buffer, line driver, PGA, ADC, refgen, control logic

200mm - Diameter Wafer with 48 CMOS ROIC Chips

UMC Foundry 0.25µm CMOS Technology,
6 wafers delivered (another 6 held at M-1)

First 720×726-Pixel Hybrid Chip





- Packaged prototype is a single 720 × 720px FPA
- 1440×1440 imager can use a 2-side buttable 720×726 FPA in a Tiled Assembly
- On and off-chip decoupling with multiple wire-bonds to dampen large power transients

Rockwell/ Teledyne pRAD Cameras

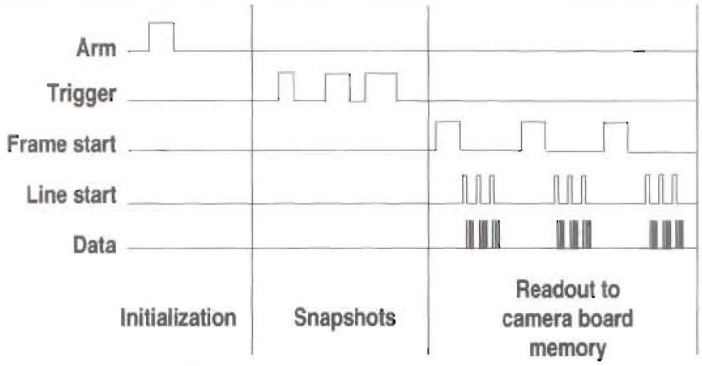
Prototype –in Alu housing

(Sizable volume taken-up by TEC cooler and fan)

Stainless-Steel Dewar

Burst and Continuous Imaging Modes are Integrated on the Imager

- Burst mode (3 images at 2.8 Mfps); trigger width = integration time
- Continuous mode (continuous imaging at 65/ 30 fps)

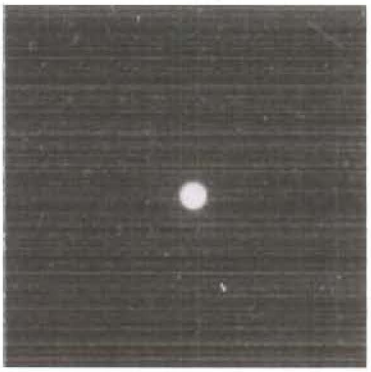


Frame-grabber FO interface; Redundant data storage in Non-Volatile memory in camera controller

Response to 6mm Circular Mask

Gated "PV" CCD Camera

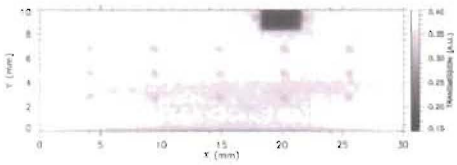
Rockwell Imager "K1"

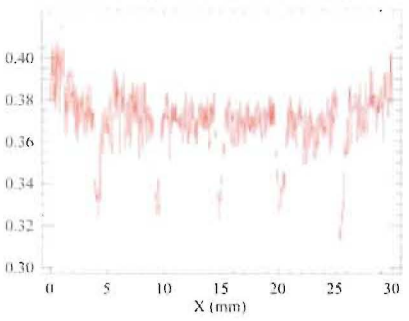


Response of the *gated CCD camera (left)* and *Rockwell hybrid imager (right)* to high intensity illumination of a 6mm diameter circular mask. Both images are plotted on a *logarithmic z-scale*. The halo seen in camera D is typical of the gated CCD system, and it is indicative of the long range blur.
The rest of the black field illustrates the level of starring in both cameras due to the stray radiation.

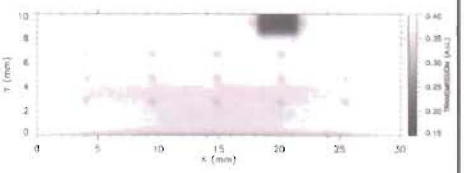
Higher QE of Si Imager Equivalent to Increase in Beam Intensity by ×5

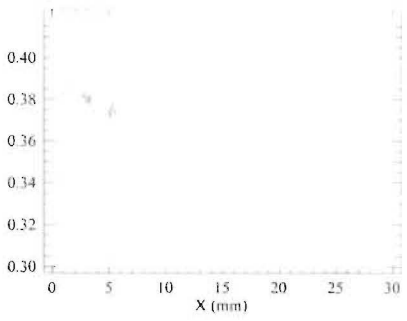
Gated CCD Camera #2 (1600×1600)



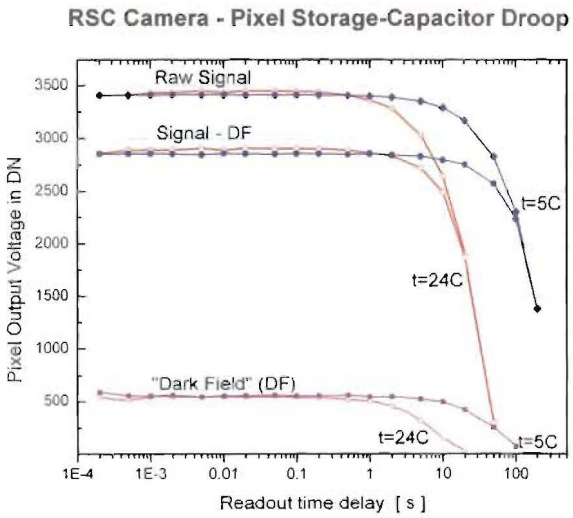


Rockwell Camera "K1" (720×720)





Pixel Signal-Storage Circuit Leakage



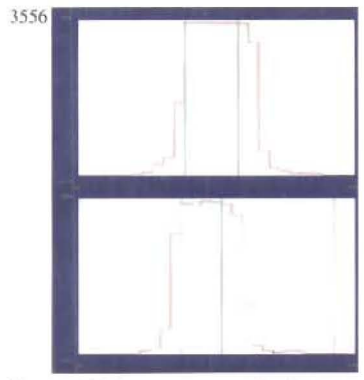
Leakage current due to the switching FET and possibly in the oxide - limits the length of charge storage to 0.5sec at room temperature to ~3sec at +5°C.

Full FPA array read-out completed in 3×26ms = 78ms

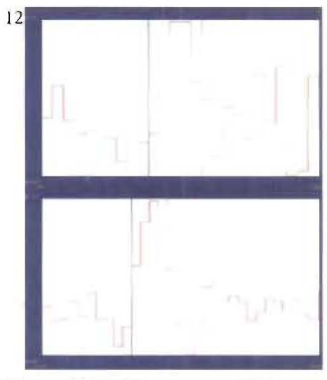
Shutter ratio measurements

At nominal sensor bias (16V) the extinction ratio is better than 15,000 :1 for a *brand new* FPA.

The FPA exposed to beam radiation for over 1.5 years shows ratio 1400 :1 for *F1*→*F2*; and 4480 :1 *F1* → *F3* at 16V bias.



Frame#1 "over-saturated" ×4.2 times



Frame#2 (500ns later, 500ns gate width)

Teledyne Imager: Problems and Areas for Improvement

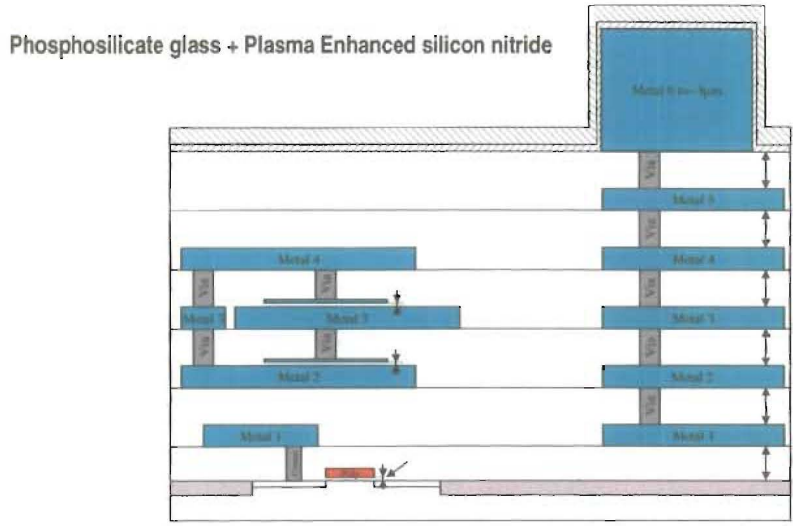
- Si photo-sensor
  - large leakage current 200nA/cm^2 vs. 10nA/cm^2 spec'ed (new wafers i < 2nA/cm^2)
  - ~100μm thick - more noticeable (longer) stray "stars"
- Indium bump-bonding
  - rather expensive (FPA ~ $20k)
  - yield not always 100%; typ. operability 99.8%
- CMOS readout integrated chip (ROIC)
  - Relatively large noise (~ 100e$^-$ at room temperature)
  - Small dark field drift/ noise on per row basis
  - Need greater pixel count: 1024×1024 or better 1440×1440 and need more frames

Next Generation pRAD Imager

(now in design stage)

- Number of frames: **8-16**
- Integration time: 40 ns with 10 bit, and 150 ns w/ 12bit
- Inter-frame time: 80 ns in "fast mode," 250ns standard mode
- Dynamic Range: 10 or 12bit (14-bit ADC)
- Read noise: < 25 e$^-$
- Pixel size: ≤ 40μm×40μm
- Resolution: ~1200×1200 pixels
- Chip size: ~ 44mm×44mm (will require CMOS stitching)
- CMOS technology (with enhancements): 180nm

Jazz Semiconductor: Thick Top Metal Layer and Stack-Capacitor in 180nm CMOS Process



If we want to go beyond ~10-frame pixel

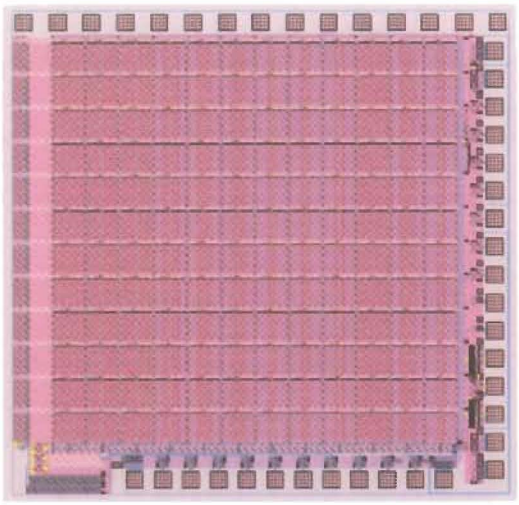
- Different approach/electronic architecture (UCLA)
- OR "denser" CMOS process and
- more Si real-estate, and standard CMOS e.g:
  - larger pixels OR
  - 3-D package (vertical stack, ×100 area increase)
  - "3-D IC": multi-layer stack of CMOS chips

    CMOS wafers or chips *thinned* down to 10μm or even 1.2 μm, interconnected with through-Si vias 0.3μm to 8μm diameter and bonded together

    bonding: Cu diffusion, organic adhesive, or Indium bump bonds

The industry favorite (memory, FPGA's, cameras) seem to be 3-D IC.

"MegaCam1": 5 M-Frame/s Test Chip

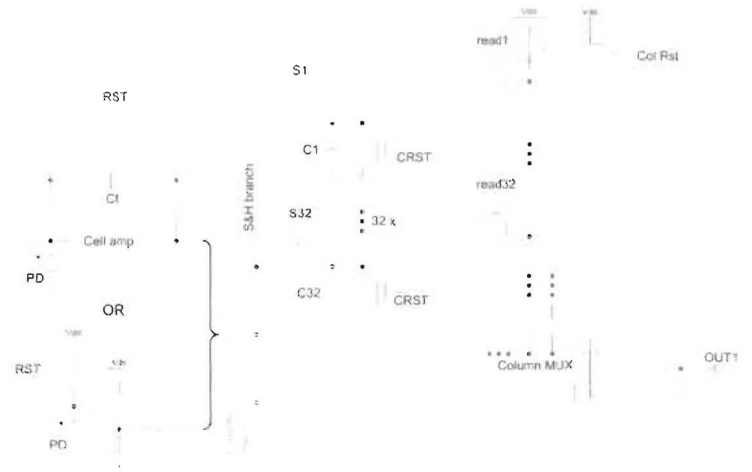


- 12×12 pixel array
- 4-10 M-frames/s
- ~13 bits SNR
- Charge-integrating amplifier front-end
- **64**-frames on-chip frame memory
- Correlated double sampling
- 0.35µm CMOS, $60k

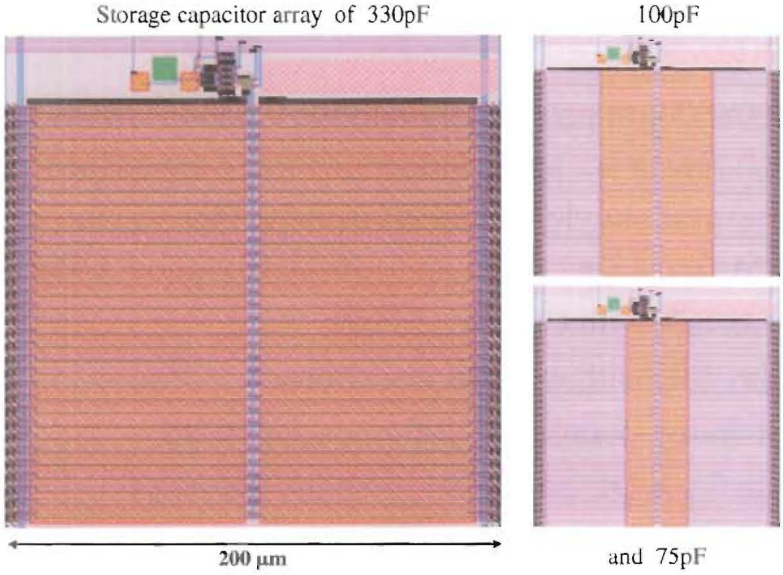
Collaboration w/ UC Irvine "MegaCam1" Performance

- 200×200µm pixels in monolithic 0.35um CMOS
- Photodiode + charge integrating trans-impedance amp and sample & hold array per pixel
- 4 M-frame/s w/ CDS, up to 10 MHz without CDS
- Max S/N with CDS is ~13 bits
- Max S/N without CDS is ~12 bits
- 64-frame storage, or 32-frames with CDS
- 3 to 7 µA DC power consumption per pixel

Simplified Pixel Circuit Schematic



64-frame MegaCam1 Pixel Layout



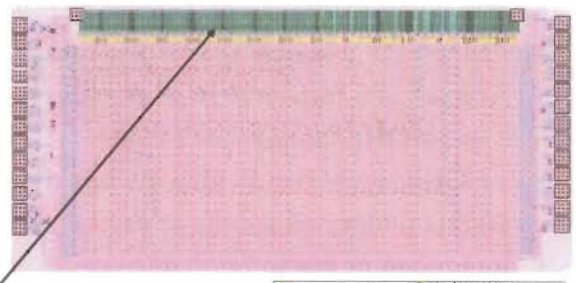
Fast 1-D "STREAK-1": Solid-State Streak Camera

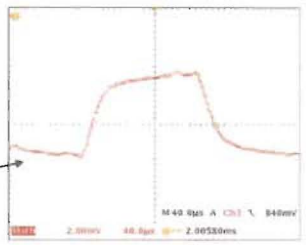
In 2003 designed and fabricated *STREAK-1* prototype:

- 150-pixel linear monolithic CMOS sensor array, each channel with 150 samples per photo-sensor
- 5ns integration /5ns reset time cycle
- 2 rows of 40 μm pitch sensor pixels
- 0.35 μm CMOS, 3.3V supply, 0.4 mA/channel

(Stuart Kleinfelder, ECE UC Irvine)

STREAK-1 prototype





- 2 staggered rows of 40μm pixel pitch photo-sensors
- 150 pixels wide by 150-samples deep
- 100 MHz acquisition and readout of low-power optical input shown to right

STREAK-1 Performance

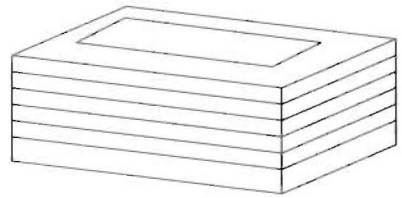
- Max *measured* sampling speed: 400 MHz
- Photo-diode area: 85×40μm^2; C ~0.4 pF
- Photo-diode fill factor: 92%
- Temporal noise: 0.51 mV
- Fixed pattern noise: 6 mV
- Max output swing: 1.48 V
- Dynamic range: 69.2 dB rms (11.5 bits)
- Multiplex readout speed: 10 MHz (100ns)

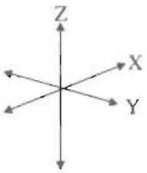
GHz-Regime Linear Camera

Create a solid-state streak camera that has:

- At least 64 channels (≥512 possible)
- At least 256 frames (≥1024 possible)
- 2 to 5+ GHz sample rate range
- 1+ GHz signal bandwidth, 8+ bits dynamic range
- 10 bits integrated analog to digital conversion
- Integrated or bump-bondable sensor array
- PLL-based clock multiplication (e.g. 100 MHz reference clock yields a 2 GHz acquisition clock)
- Real-time programmable trigger generation
- At higher speeds, optimized monolithic sensors are mandatory

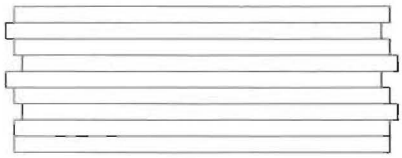
CSP Stacking Runout & Tolerance Issues



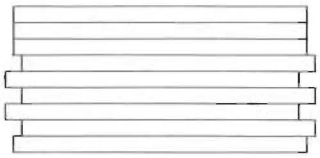


Possible
Run out In all Axis ?!

Θ Rotational issues for
Each of 50 pieces not shown



Y
Variation
ESI and stacking



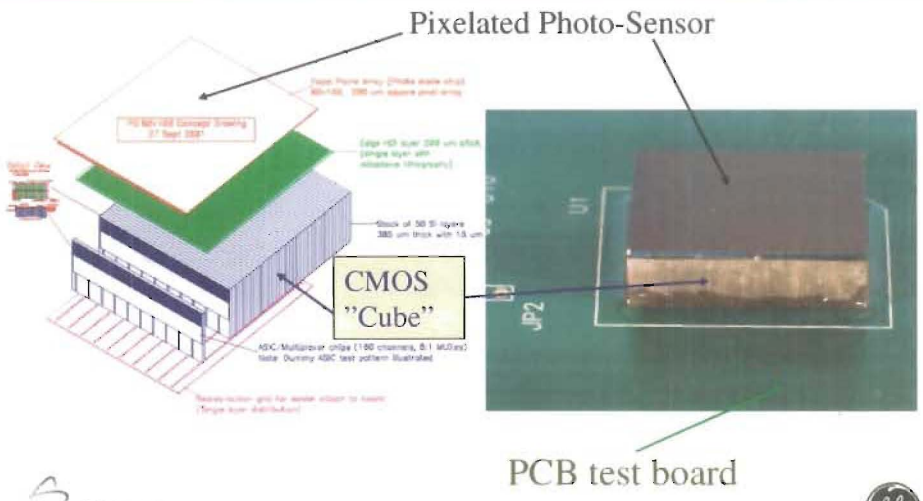
X
Variation
ESI and stacking

Chip Scale Packages (CSP)

Z
Variation
Glue and grinding

Los Alamos
NATIONAL LABORATORY

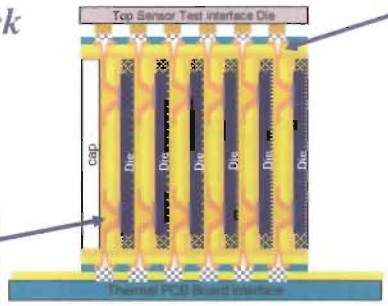
Vertical CMOS Stack "Cube" of 50 Chips 8,000 Connections to Photo-Sensor Array and 750 to PCB

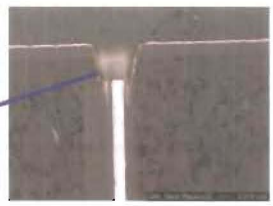


Los Alamos

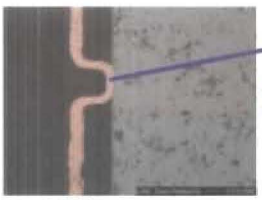
Laser Drilled Vias

3D Stack



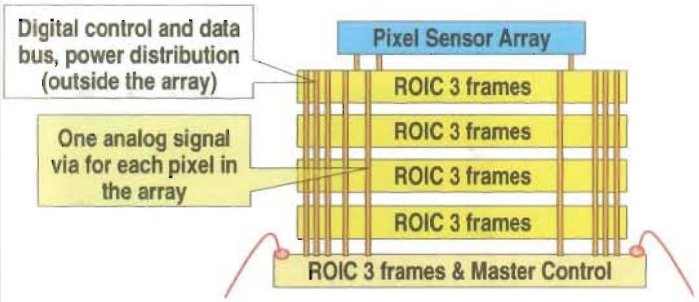


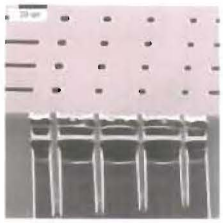
Ti/Cu sputtered only (to define via for SEM No Electroplating Was Done)



Ti/Cu sputtered
Cu plated
Ti sputtered

3-D High-Density Chip Horizontal Stack Can Extend Frame Storage





- Via diameter ~4 / 8μm, one via per pixel, thru 250um Si layer
- Vias used to stack and interconnect several ROIC chips – extending frame storage capacity by 3 frames for each additional ROIC added. Example above shows 15-frame storage capacity

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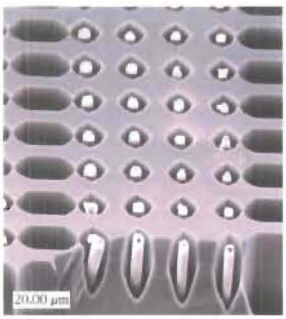
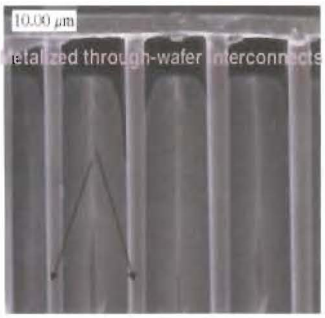
VISA - DARPA Program

- At RSC VISA (RSC awarded phase II) is driven by needs of extremely high-dynamic range and high-speed infrared imagers
  - Dynamic range of up to ***28 bits*** at low power
  - Autonomous adaptive operation at video frame rates to ***10 kHz*** and higher
  - High performance while simultaneously reducing system power and weight





SEM Micrograph of metalized, isolated, through-vias. View from above showing top of vias (metal and isolation). Silicon wafer was etched to make vias more more visible in the SEM micrograph.

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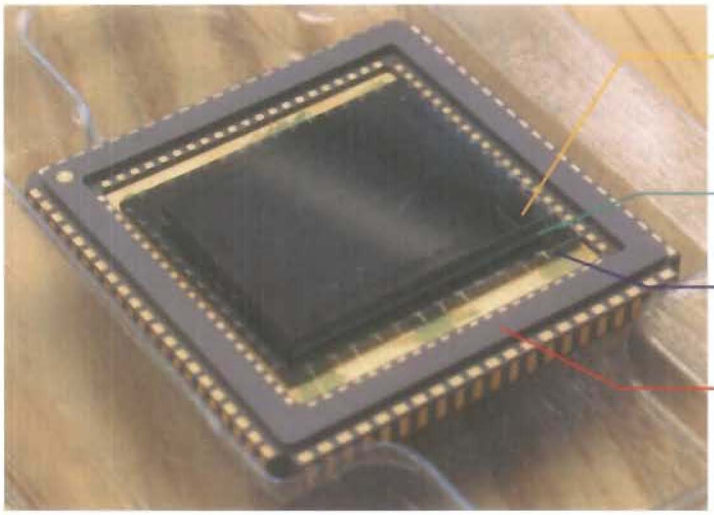
VISA Demo 4-Layer Stack



P.O. Pettersson, private communication

ROCKWELL SCIENTIFIC

3-D Packaging Challenges

- Design evolution towards integration of sensor, electronics and packaging
- Known Good Die (KDG)
- Power dissipation
- Repairability
  - self-test
  - redundancy
  - (self)-reconfigurable

Summary

- Rockwell Imager:
  - hybrid architecture: 26μm pixels, SoC, QE~ 84%, 180-40ns int. time
  - IC chip worked on 1st iteration – analog simulation tools; cost $1.16 M
- Direct detector possible, interconnect not trivial
- UCI MegaCam1 framing camera:
  - 200μm pixels, 4 -10 M-frames/s operation; 64-frame storage
  - 13 bit rms dynamic range with CDS, 12 bits without;
- Streak1- solid state streak camera prototype:
  - 400 MHz maximum sample rate (2.5ns), burst mode operation
  - 11.5 bits rms dynamic range
- In near future a 2nd Gen. pRAD Fast Imager
  - CMOS hybrid 8-16frames, 40ns shutter, 1200x1200px, stitched 44mm chip
- Longer term – 3-D architecture: large analog or digital storage
  With shutter speeds ~1ns, and 11-bit DR