Final Scientific Report for DOE/EERE

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Executive Summary

The development of renewable, affordable, and environmentally conscious means of generating energy on a global scale represents a grand challenge of our time. Due to the "permanence" of radiation from the sun, solar energy promises to remain a viable and sustainable power source far into the future. Established single-junction photovoltaic technologies achieve high power conversion efficiencies (**pce**) near 20% but require complicated manufacturing processes that prohibit the marriage of large-scale throughput (e.g. on the GW scale), profitability, and quality control.

Our approach to this problem begins with the synthesis of nanocrystals of semiconductor materials comprising earth abundant elements and characterized by material and optoelectronic properties ideal for photovoltaic applications, namely $Cu_2ZnSn(S,Se)_4$ (CZTSSe). Once synthesized, such nanocrystals are formulated into an ink, coated onto substrates, and processed into completed solar cells in such a way that enables scale-up to high throughput, roll-to-roll manufacturing processes.

This project aimed to address the major limitation to CZTSSe solar cell pce's – the low open-circuit voltage (Voc) reported throughout literature for devices comprised of this material. Throughout the project significant advancements have been made in fundamental understanding of the CZTSSe material and device limitations associated with this material system. Additionally, notable improvements have been made to our nanocrystal based processing technique to alleviate performance limitations due to the identified device limitations. Notably, (1) significant improvements have been made in reducing intra- and inter-nanoparticle heterogeneity, (2) improvements in device performance have been realized with novel cation substitution in Ge-alloyed CZTGeSSe absorbers, (3) systematic analysis of absorber sintering has been conducted to optimize the selenization process for large grain CZTSSe absorbers, (4) novel electrical characterization analysis techniques have been developed to identify significant limitations to traditional electrical characterization of CZTSSe devices, and (5) the developed electrical analysis techniques have been used to identify the role that band gap and electrostatic potential fluctuations have in limiting device performance for this material system.

The device modeling and characterization of CZTSSe undertaken with this project have significant implications for the CZTSSe research community, as the identified limitations due to potential fluctuations are expected to be a performance limitation to high-efficiency CZTSSe devices fabricated from all current processing techniques. Additionally, improvements realized through enhanced absorber processing conditions to minimize nanoparticle and large-grain absorber heterogeneity are suggested to be beneficial processing improvements which should be applied to CZTSSe devices fabricated from all processing techniques. Ultimately, our research has indicated that improved performance for CZTSSe will be achieved through novel absorber processing which minimizes defect formation, elemental losses, secondary phase formation, and compositional uniformity in CZTSSe absorbers; we believe this novel absorber processing can be achieved through nanocrystal based processing of CZTSSe which is an active area of research at the conclusion of this award.

While significant fundamental understanding of CZTSSe and the performance limitations associated with this material system, as well as notable improvements in the processing of nanocrystal based CZTSSe absorbers, have been achieved under this project, the limitation of two years of research funding towards our goals prevents further significant advancements directly identified through pce. improvements relative to those reported herein. As the

characterization and modeling subtask of this project has been the main driving force for understanding device limitations, the conclusions of this analysis have just recently been applied to the processing of nanocrystal based CZTSSe absorbers -- with notable success. We expect the notable fundamental understanding of device limitations and absorber sintering achieved under this project will lead to significant improvements in device performance for CZTSSe devices in the near future for devices fabricated from a variety of processing techniques.

Comparison of Proposed versus Realized Project Goals

The following table summarizes the project's proposed goals versus actual progress for each task. Deviations between an Initial negotiated deliverables / milestones and an actual deliverable / milestone are discussed in the "Deliverable / Milestone Deviations" section of the Technical Narrative.

Year #	Task #	Subtask description	Initial Negotiated Deliverable / Milestone	Actual Deliverable / Milestone
1	1	**1.1.1:** Base case CZTSSe solar cell with 7% pce. **1.1.2:** Controlled synthesis of CZTS nanocrystals over a range of Cu:Zn;Sn atomic ratios. **1.1.3:** Sintered films with large grain growth.	**1.1.1:** 0.47-cm^2 solar cell with total area pce of 7%. **1.1.2:** Availability of nanoparticles with desired composition and structure. **1.1.3:** Sintered films with grain growth in micron range with no pinholes or shunts.	**1.1.1:** 0.47-cm^2 solar cell with total area pce of 7.9%. **1.1.2:** Developed new nanocrystal synthesis recipe yielding particles with desired composition and structure and improved interparticle homogeneity. **1.1.3:** Optimized selenization conditions to yield micron-sized or near micron-sized grains in all dimensions with no voids at back contact and minimal pinholes/shunts as demonstrated through increased shunt resistance in completed devices.
1	2	**1.2.1:** Synthesize CZTS nanoparticles with varying amounts of Ge and possibly Si for Sn.	**1.2.1:** Homogeneous nanocrystals with varying band gap.	**1.2.1:** Successful synthesis of CZTGeS nanocrystals with tunable Ge/(Ge+Sn) ratio and corresponding band gap and no detectable impurity phases. Attempts to incorporate Si for Sn always led to formation of impurity phases.
1	3	**1.3.1:** Characterization and modeling.	**1.3.1:** Improved understanding of device performance. Solar cell with 10.7% pce.	**1.3.1:** Identified potential fluctuations throughout the bulk of the CZTSSe absorber as a primary contributor to low Voc. Utilized simulation and

				modeling to demonstrate low Vbi as a secondary contributor. Demonstrated CZTSSe solar cell with 8.4% pce.
2	**1**	**2.1.1:** Sintered films with minimal or no 'fine-grain' layer. **2.1.2:** Impact of Na film growth by dipping in NaCl solution.	**2.1.1:** Absence of bottom 'fine-grain' layer in the sintered film. **2.1.2:** Possibly large grain growth in sintered film.	**2.1.1:** Optimized nanocrystal synthesis and selenization conditions to reduce fine-grain layer thickness from roughly 50% to < 30% of total absorber thickness. **2.1.2:** Reproducibly observed best pce's by utilizing soda-lime glass as substrate and not including any other Na treatments (e.g. dip in NaCl solution, deposition of thin NaF layer).
2	**2**	**2.2.1:** Synthesize CZTS nanoparticles with varying amounts of Ag for Cu.	**2.2.1:** Homogeneous nanocrystals with varying band gap.	**2.2.1:** Attempts to substitute Ag for Cu in nanocrystal synthesis always led to formation of impurity phases. Observed homogenization and enhanced grain growth upon selenization of heterogeneous nanocrystal films, but device performance remained inferior to CZTSSe.
2	**3**	**2.3.1:** Low cost precursors for CZTS nanocrystals.	**2.3.1:** Uniform composition particles yielding device performance equivalent to or better than current precursors.	**2.3.1**: Identified $Cu(acac)_2$, $Zn(acac)_2$, and $Sn(acac)_2Cl_2$ along with elemental S as precursors yielding CZTS nanocrystals with no detectable impurities and narrowest particle composition/size distribution (acac = acetylacetonate). These cation precursors are relatively inexpensive.
2	**4**	**2.4.1:** Characterization and modeling.	**2.4.1:** Improved understanding of device performance. Solar cell with 15% pce.	**2.4.1:** Developed a novel electrical model to account for potential fluctuations and describe/predict non-ideal diode behavior. Based on experimentation, developed a model to

				describe the reactive sintering mechanism during selenization. Utilized simulation and modeling to demonstrate small amounts of impurity phases as a secondary contributor. Built new instrumentation to perform photoluminescence excitation characterization of absorber films to extract quantum efficiency/carrier lifetime information. CZTSSe solar cell with 9.3% pce; CZTGeSSe solar cell with 9.4% pce but less optimized processing compared to CZTSSe.

Technical Narrative

Project Objective

The primary objective of this project was to develop fundamental knowledge and understanding that will enable the production of CZTS-based lab-scale solar cells with pce in the neighborhood of 15%. The two-year DOE grant constituted two phases I and II. Prior to being awarded the grant, our selenized CZTS (CZTSSe) champion solar cell had a pce (η) of 7.2% with V_{OC} of 0.42V, J_{SC} = 30.6 mA/cm^2, FF = 53.2%, and series resistance (R_S) = 2.3 Ω-cm^2. The composition of the absorber layer was Cu/(Zn+Sn) = 0.8 and Zn/Sn = 1.11, and the estimated free carrier concentration in the CZTSSe film was ~2x10^{16}/cm^3. Note that this result was for a champion cell, and at the time the average range for solar cell pce was 6.7 to 7%. The structure of our solar cells is: Mo coated glass/CZTSSe absorber layer/CdS/i-ZnO/ITO/Ni-Al grid.

The first sub task was to reproduce the pce of 7.2% as an average CZTSSe device performance in our lab. Then we performed the following major tasks:

1. Develop technology to be able to control the composition and phase of the CZTS nanocrystals. The primary focus here was to make nanocrystals over a range of Cu:Zn:Sn ratios without the presence of binary and ternary phases. This would be essential for the preparation of uniform absorber films with varying Cu, Zn and Sn ratios.

2. Grow dense absorber films with optimal optoelectronic properties from the nanocrystals. Technology needs to be developed to obtain a uniform film without unsintered layer at the bottom of the absorber layer. Tailored film composition, morphology, and thickness would enable high-efficiency solar cells.

3. Alloying CZTS nanocrystals with group IV and IB elements to create nanocrystals with tailored band gaps. Inks containing different band gap nanocrystals would be used to create the absorber layer needed for the enhanced V_{OC} and collection of photo-generated carriers.

4. Development of a multiscale model to provide the fundamental understanding needed for nanocrystal synthesis, absorber film growth, optoelectronic characterization of different layers within the device as well as completed solar cells.

Background

For solar energy to replace fossil resources for electricity production at a meaningful level, it is essential to develop a photovoltaic (PV) technology that is competitive at the tera-Watt (TW) scale. Competitiveness at such an unprecedented level requires an easily scalable and low-cost manufacturing technology that is not limited to material availability. To date, none of the PV technologies simultaneously meets all these constraints. To meet this challenge, we have been exploring a nanocrystal ink based route to make thin film solar cells from compound semiconducting materials with high absorption coefficients. The key feature of our process is that each nanocrystal particle is of the right crystal structure. By this method we have already created lab-scale copper indium gallium diselenide solar cells with power conversion efficiency (pce) of ~15%. Our focus in this research is to create high efficiency copper zinc tin sulfide (CZTS) solar cells composed of earth abundant elements via our ink-based route.

A nanocrystal ink-based approach has several inherent benefits – it is easily scalable due to its capability to uniformly coat large area substrates; amenable to automated and integrated manufacturing leading to better process control, higher material utilization, faster throughput and reduced labor; and more efficient regarding capital use due to the elimination of capital intensive high-vacuum equipment for absorber layer deposition and the use of safe-to-handle chemicals. All these factors can potentially lead to lower cost.

However, there are several challenges that must be met at each of the steps of the nanocrystal ink based route: synthesis of nanoparticles with the right composition and structures, ink formulation, film coating, sintering to achieve large grains with minimal 'fine-grain' layer due to carbonaceous material, and device fabrication with attractive optoelectronic properties. We aim to meet challenges at all these steps to improve the open-circuit voltage (V_{OC}), short-circuit current (J_{SC}), and fill factor (FF) – and in turn, the efficiency (η) – of the final device.

Significant Accomplishments

Major Task #1: ***Develop technology to tailor the composition and structure of the CZTS nanocrystals and the resulting absorber films for optimal performance.***

Major Accomplishments:

- Achieved improved reproducible baseline efficiency of 8.5% total-area p.c.e. for nanocrystal based CZTSSe devices, with champion efficiency of 9.3% total-area p.c.e.[1]
- Discovered new nanocrystal synthesis recipe yielding nanocrystals with improved particle-to-particle homogeneity, which in turn lead to improved device efficiencies.[2]
- Investigated Ge, Si substitution for Sn and Ag for Cu. Significant progress has been made with Ge-alloyed CZTGeSSe devices, yielding improved device performance over similarly processed Ge-free CZTSSe absorbers.[3] Si and Ag alloying led to significant segregated phase in nanocrystal synthesis suggesting more optimization is needed. Ag alloying has led to enhanced grain-growth during selenization of AgCZTSSe, though device optimization needs improvement.
- Developed ability to synthesize wurtzite CZTS nanocrystals, which convert to kesterite upon selenization.[4]

Major Task #2: ***Develop process understanding to better tailor the sintering and growth of the absorber films from nanoparticles to achieve high performance optoelectronic properties for solar cells.***

- Performed detailed structural and compositional STEM characterization of nanocrystals and selenized absorbers alike to elucidate fundamentals physics governing reactive sintering. These studies complemented EDXRD data collected in real-time during selenization in collaboration with HZB.[5]
- Purchased RTP furnace to afford significantly improved, precise, and independent control of sample and chalcogen temperatures during selenization.

Major Task #3: ***Adjust the band gap and band gap profile of the CZTSSe absorber layer by synergistic substitutions.***

- Using Ge substitution from Task #1 to vary CZTGeSSe band gap from 1.1-1.5 eV by controlling Ge/(Sn+Ge) content.[3]
- Developed/improved upon sulfurization techniques using H_2S or elemental S to influence S/(S+Se) ratio, providing another knob to turn in order to control absorber band gap. New RTP furnace adds further capability in this respect.

Major Task #4: ***Use characterization and modeling to develop fundamental understanding of all the steps in device fabrication, leading to high-efficiency CZTS based solar cells.***

- Utilized advanced electrical characterization in conjunction with STEM materials analysis to identify bulk CZTSSe potential fluctuations as a primary contributor to low Voc.[6]
- Developed a novel model to account for potential fluctuations and describe/predict non-ideal diode behavior.[6]

- Identified potential secondary contributions to low Voc from low Vbi and impurity phases through simulation.

Discussion:

Base Case CZTSSe Solar Cell with 7% Power Conversion Efficiency (Subtask 1.1.1)

Before being awarded this Sunshot grant, our group had established a reproducible baseline CZTSSe solar cell total-area power conversion efficiency (pce.) of roughly 6.5%, with a champion device p.c.e. of 7.2%.[7] Under the SunShot award, we have raised our base case p.c.e. to 8.5%, with a new champion CZTSSe device p.c.e. of 9.3%[1] (see Figure 1).

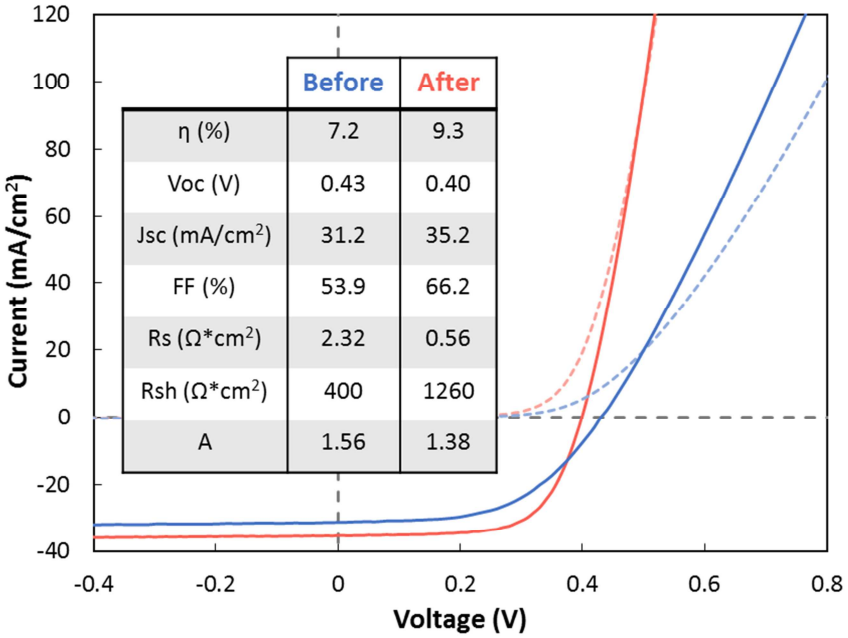


Figure 1. Champion device current-voltage characteristics at the onset ("Before", blue curves) and conclusion ("After", red curves) of the SunShot award period.

These champion efficiencies represent the highest values reported for CZTSSe devices processed from nanocrystal inks at the time the results were published. As demonstrated in Figure 1, the efficiency gains are manifested through nearly all device performance parameters as a result of work performed under the Sunshot award to improve the nanoparticle synthesis,[2] selenization,[2] and window layer deposition conditions. The slight decrease in open-circuit voltage (Voc) can be attributed a lower band gap in our current champion device absorber layer due to a more complete substitution of S with Se during the improved selenization. This phenomenon also contributes somewhat to the higher short-circuit current (Jsc), though the primary improvement in Jsc is due to the addition of a MgF_2 anti-reflective top coating on the device as well as significantly reduced series resistance (Rs) and increased (Rsh) – in turn leading to the higher fill factor (FF) – enabled by window layer optimization. Furthermore, all of these factors contribute to the reduced diode ideality factor (A). Overall, while further advances in device performance are certainly necessary to commercialize this technology, the improvements we have achieved during the Sunshot award coupled with the significantly expanded fundamental understanding of both device fabrication and performance limitations have positioned us to make great advancements in solution-processed CZTSSe photovoltaics in the near future.

Low-Cost Synthesis of CZTS Nanocrystals with Controlled Composition / Sintered Films with Large Grain Growth (Subtasks 1.1.2, 1.2.1, 1.1.3, 2.2.1, & 2.3.1)

Availability of nanoparticles with desired composition and structure:

CZTS nanocrystals synthesized according to the standard recipe (30 minutes at 225 °C) have been separated by size using a centrifuge in order to study the degree of interparticle homogeneity (or lack thereof). Upon centrifugation of the reaction products in a roughly 1:1 mixture of oleylamine and isopropanol at 14 krpm for 5 minutes, two size domains are observed – one less than ~5 nm in diameter ("small") and the other greater than ~15 nm ("large"). Energy-dispersive X-ray spectroscopy (EDX) compositional analysis of the two size domains reveals notable and opposite deviations from the desired particle cation ratios of 0.85 and 1.05 for Cu/(Zn+Sn) and Zn/Sn, respectively, despite the observation that the naturally proportioned mixture of large and small particles from the synthesis roughly matches the target composition. The measured cation ratios for the small, large, and mixed particles from five reactions are plotted in a ternary diagram in Figure 1. The small particles are found to be very deficient in Zn, while the large particles were Zn-rich but Cu- and Sn-poor.[8]

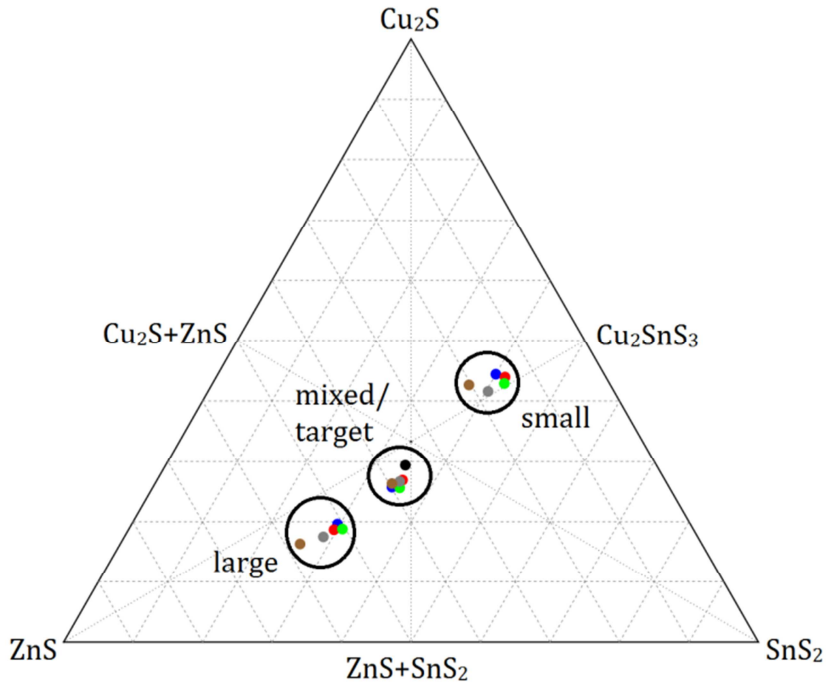


Figure 1. Ternary plot illustrating compositional variations in small, large, and mixed particles.

Despite the drastic compositional differences in the particles, the Raman spectra for small, large, and mixed particles displayed in Figure 2 appear nearly identical. The broadness of the peaks in the Raman spectra can be attributed to the nanocrystalline nature of the particles. The main peak located at 338 cm^{-1} corresponds to the expected primary peak for CZTS at 339 cm^{-1}, but tetragonal Cu_2SnS_3 (CTS) also generates a primary Raman shift at 337 cm^{-1}. Additionally, the shoulders near 353 cm^{-1} in the small particle spectrum and at ~300 cm^{-1} in all three spectra can be attributed to CTS. ZnS also produces a peak near 352 cm^{-1}, but responds weakly to excitation in the visible range and thus cannot reliably be identified or excluded based on the presented data, which was obtained with a 633-nm laser. Nonetheless, it seems very likely that CTS may be present in the samples. Since the mixture of large and small particles roughly matches the target composition, it is difficult to explain the existence of Zn-free CTS without the presence of Cu- and Sn-free ZnS as well.

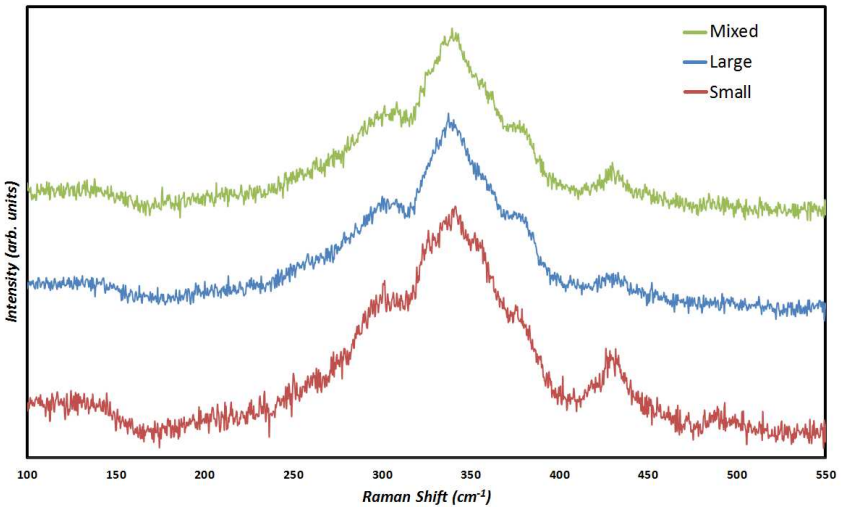


Figure 2. Raman spectra for small, large, and mixed particles.

X-ray diffraction (XRD) provides another means of identifying distinct crystalline phases in the samples. However, due to the structural similarity of tetragonal CZTS and CTS and ZnS, these compounds cannot be differentiated using XRD analysis, especially for nanocrystalline samples whose peaks are rather broad. The XRD spectra for small, large, and mixed particles are plotted along with standard spectra expected for CZTS, CTS, and ZnS in Figure 3. The small particles do not generate sufficient signal to be reliably interpreted, but the comparatively strong signals for large and mixed particles are nearly identical – likely because the small particles do not contribute much signal – and closely match the expected spectra for CZTS, CTS, and ZnS. Based on the Raman and XRD data, we can fairly confidently conclude that binary and ternary phases other than CTS and ZnS are not present in the particles, but we cannot disprove the notion that the particles are a mixture of CZTS, CTS, and ZnS. Nonetheless, it is clear that the particles comprise a broad compositional distribution.

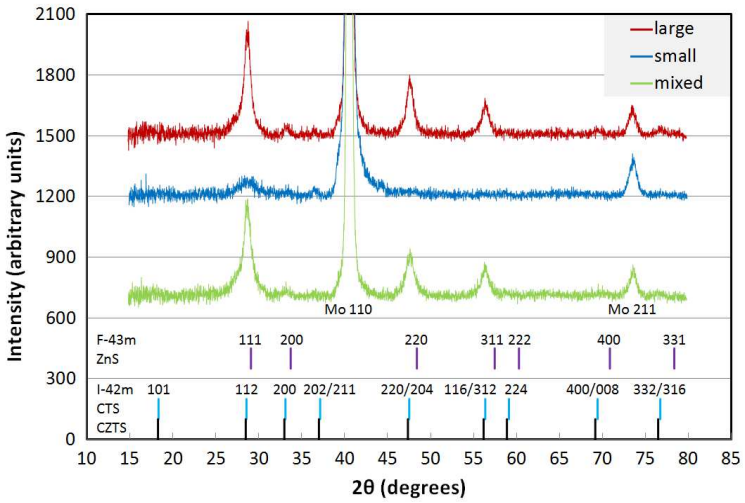


Figure 3. XRD spectra for small, large, and mixed particles.

In order conclusively determine whether the nanocrystal samples consist of distinct CZTS, CTS, and ZnS phases or incorporated CZTS that deviates far from stoichiometry (despite the expectation of instability at such compositions), samples were sent to collaborators at Helmholtz-Zentrum Berlin (HZB) to be measured by extended x-ray absorption fine structure (EXAFS) and x-ray absorption near-edge structure (XANES) techniques. Analysis of the data from these experiments is underway, but initial

results indicate the existence of binary and ternary phases in nanocrystal samples. The collaboration with HZB was also utilized to perform experiments in which energy-dispersive x-ray diffraction (EDXRD) measurements were collected in real-time during the selenization of small, large, and mixed particles in order to understand the effect of particle size, composition, and the presence of binary and ternary phases on sintering. Analysis of the data obtained in these experiments is currently in progress.

In addition to the effort to characterize the compositional distribution observed in nanocrystals grown by the standard recipe (recipe 1, or R1), a modified recipe (recipe 2, or R2) has been developed to produce particles exhibiting a narrower composition distribution. The most influential difference between the two recipes seems to be the higher temperature and longer reaction time for R2 (250 °C for 1 hr), although another notable change is the injection of all precursors into hot oleylamine in R2, whereas R1 prescribes the injection of sulfur into a hot solution of the cation precursors in oleylamine. Table 1 enumerates the cation ratios calculated via EDX for small, large, and mixed particles from both recipes. As is the case for R1, the R2 small particles are Zn-poor, though the degree of deficiency is greatly reduced in R2. However, the R2 small particles only comprise ~10% of the mixed particles by mass (compared to ~50% for R1); consequently, the composition of the large and mixed particles from R2 are nearly identical. Furthermore, the composition of these two samples closely matches that of the R1 mixed particles.

Table 1. Cation ratios measured via EDX for small, large, and mixed particles from R1 and R2.

Particles	Cu/(Zn+Sn)	Zn/Sn
Small	R1: 1.06 R2: 0.88	R1: 0.37 R2: 0.67
Large	R1: 0.64 R2: 0.80	R1: 1.70 R2: 1.14
Mixed	R1: 0.74 R2: 0.79	R1: 1.11 R2: 1.16
Target	0.85	1.05

Ultimately, it is imperative to understand the effect of particle size and composition distributions on device performance. Thus, devices have been made from large and mixed particles from both recipes as well as from small R1 particles. Small particle devices fail to achieve any power conversion efficiency, but large particle devices perform similarly yet notably inferior to mixed particles from the respective recipe. Current-voltage characteristics for large and mixed particle devices from both recipes are displayed in Figure 4. For both recipes, mixed particle devices perform better than their large particle counterparts, achieving efficiencies up to 7.9% and 8.5% for R1 and R2, respectively, without anti-reflective coating. For R1, the improvement from large to mixed particle devices is manifested primarily through an increased open-circuit voltage (V_{oc}), while R2 mixed particle devices benefit from increased V_{oc} and short-circuit current (J_{sc}) and fill factor (FF). It is interesting to note the features of the light-dark crossover in forward bias; crossover is more apparent for the mixed particle devices than the large particle devices, particularly for R1. Work was also performed to better understand the causes of crossover and how they apply to these devices.

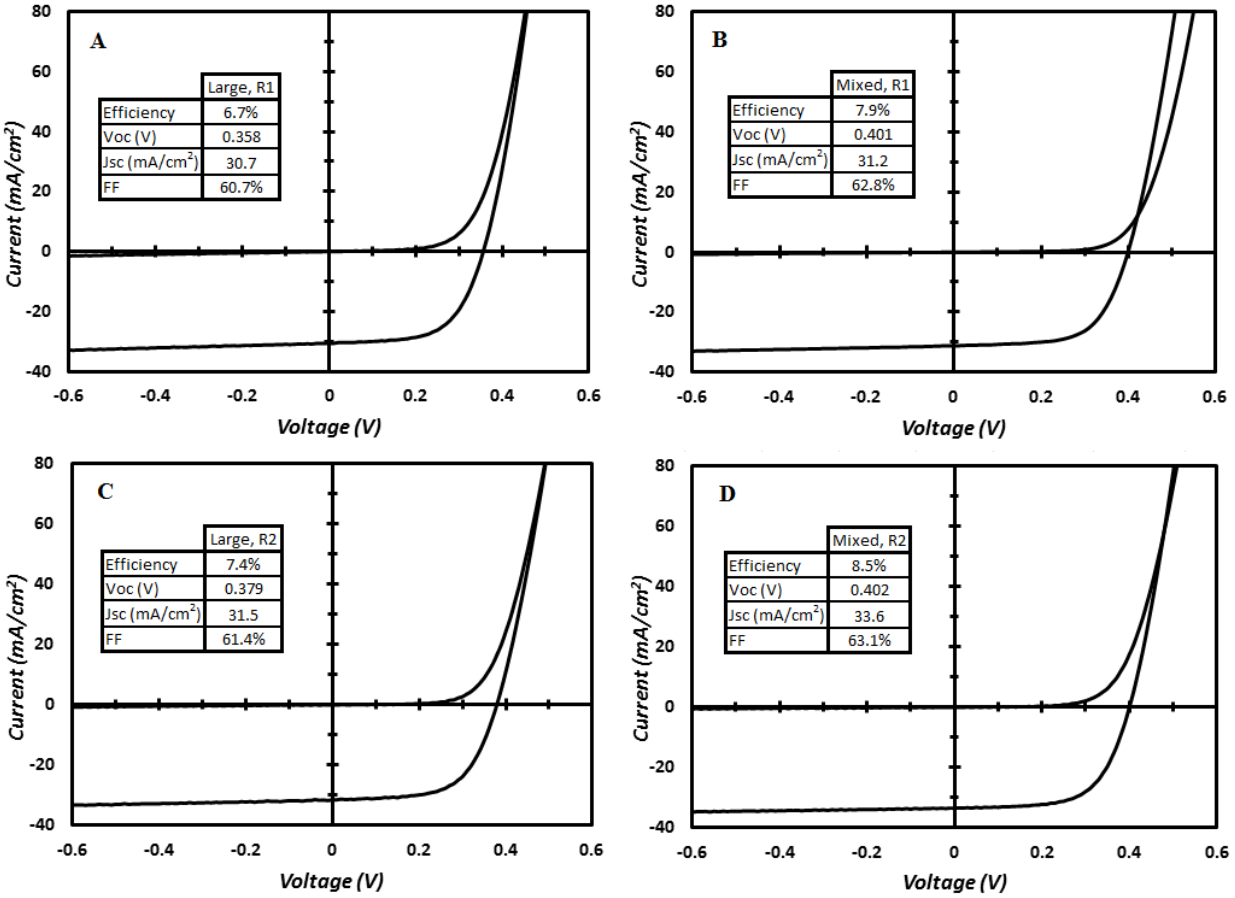


Figure 4. Current-voltage characteristics for devices fabricated from (A) R1 large, (B) R1 mixed, (C) R2 large, and (D) R2 mixed particles.

Application of a MgF_2 anti-reflective coating to the R2 mixed particle device increases the champion CZTSSe cell efficiency to 9.2%, representing a new benchmark for our research group and the second-highest for any group reported in literature. Current-voltage characteristics for this cell are displayed in Figure 5.

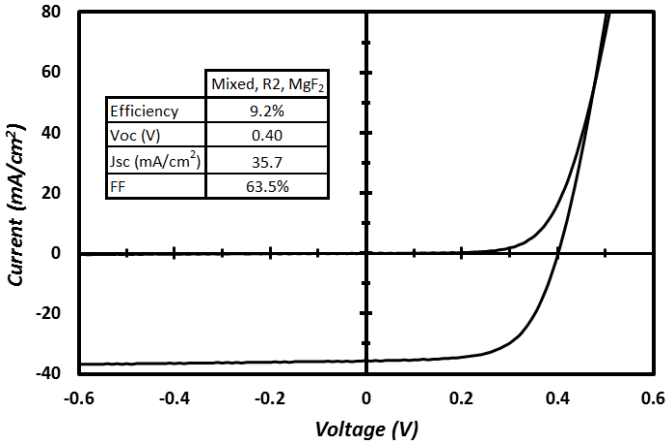


Figure 5. Current-voltage characteristics of a 9.2%-efficient CZTSSe solar cell with MgF_2 anti-reflective coating.

The new recipe affords tighter control of the particle composition, leading to a “go” milestone on this new synthesis technique.

Identification of nanoparticle uniformity:

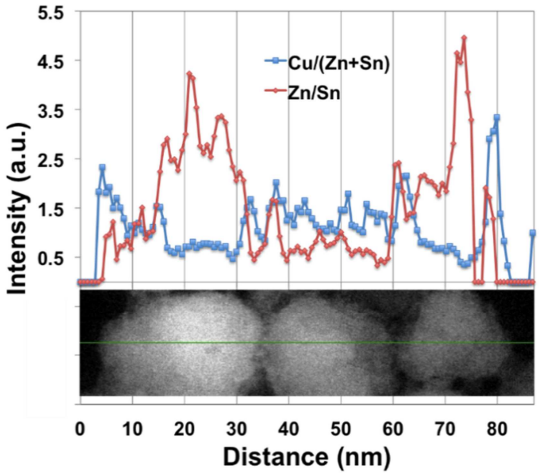


Figure 6. TEM analysis of CZTS nanoparticles (R2) illustrating non-uniform cation ratios

Work was initiated on the identification and characterization of nanoparticle uniformity in the synthesized CZTS nanoparticles. The microstructure and compositional distribution of CZTS nanoparticles (recipe 2) were examined using scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDS), shown in Figs. 6 and 7. Compositional fluctuation inside of individual nanoparticles was observed in STEM-EDS linescan profiles, although EDS data from scanning electron microscopy (SEM) suggest that the overall composition of the CZTS nanoparticle film is uniform based on multiple area measurements (~1.5 μm × 1.5 μm) across the entire nanoparticle thin film. The distributions of Cu, Zn, and Sn varies in some degree in most of the recipe 2 nanoparticles but close enough to show consistent cation ratios, e.g. Cu/(Zn+Sn) and Zn/Sn. In some more extreme cases, nanoparticles were found to have a Zn-rich core and a Cu- and Sn-rich shell. TEM analysis has previously identified *inter*-particle non-uniformities in quaternary CZTS nanoparticles,[9] however, *the work presented here represents the first characterization of intra-particle non-uniformities for this material system*.

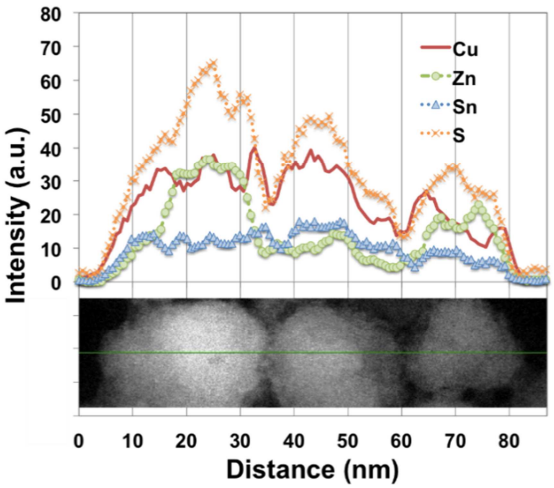


Figure 7. TEM analysis of CZTS nanoparticles (R2) illustrating non-uniform cation ratios, depicted here in normalized ratios.

Si-substitution into $Cu_2Zn(Sn,Si)(S,Se)_4$

Initial experiments of silicon substitution into CZTS to form the alloy, $Cu_2Zn(Sn,Si)S_4$ (CZTSiS) were completed. The motivation behind this research follows upon our work in Ge-substitution (CZTGeS) to form a tunable band gap semiconductor based off of the CZTS material system.[10] Due to the expected bond strengthening of the IV-VI bonding with the use of Si in comparison to Sn and Ge, an increase in the conduction band minimum is expected upon Si substitution into CZTSiS.[11] Initial work in this area involves Si substitution into the pre-sintered nanoparticles.

CZTSiS nanoparticles have been fabricated through application of the standard CZTS nanoparticle synthesis recipe with modification of the metal-organic salt precursors to include $SiCl_4$. Substitution of the $SiCl_4$ (Aldrich) precursor and tin bis(acetylacetonate) dichloride (Aldrich) has been tested with 30% and 100% Si substitution. In addition, variations in the precursor injection conditions as well as reaction time/temperature profiles have been studied.

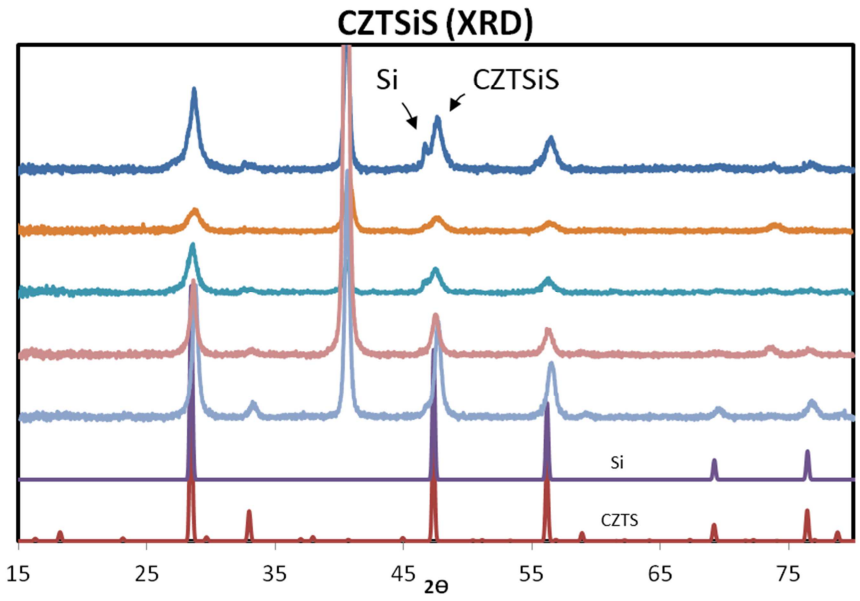


Figure 8. XRD data for CZTSiS nanoparticle experiments under various reaction conditions. Similar peak shifting and secondary phase identification is found in all experiments regardless of conditions use, suggesting a saturation in Si incorporation under the current nanoparticle synthesis method.

Initial results of Si incorporation into CZTSiS suggest current reaction conditions experience a limited degree of Si incorporation, currently 3% [Si]/([Sn]+[Si]), as verified through EDX measurements, regardless of the chemical concentrations or reaction conditions tested. Analysis of x-ray diffraction patterns for various reaction conditions, Fig. 8, demonstrate the limited degree of Si-incorporation measured in these experiments. In this figure, all reactions appear to have identical peak locations for the main tetragonal diffraction (XRD) peaks, slightly shifted to higher 2Θ values from the CZTS standard (labeled as CZTSiS in the figure); The shift to higher 2Θ compared to the CZTS standard is expected from the 3% Si-incorporation measured through EDX analysis. However, EDX analysis in combination with XRD analysis also suggest phase separation of CZTSiS (3% Si) and Si-nanoparticles. The existence of Si-nanoparticles is implied by the peak splitting in the peak near 47 degrees (labeled in Fig. 8); while the peak labeled Si in Fig. 8 also corresponds to the peak locations plotted for the CZTS standard (as both phases have identical crystal structure), spatially resolved EDX imaging revels the presence of phases of pure Si.

The limited degree of Si incorporation measured for these experiments may be a result of the large atomic size difference of Si and Sn. Due to this size discrepancy, the tetragonal phase may not be the most stable structure for CZTSiS or CZSiS, as similarly expected for CZGeS with 100% Ge-substitution. To resolve this issue, experiments under the metastable wurtzite phase reaction conditions can be tested. Additionally, variations in the Si nanocrystal reaction precursor can be tested, as $SiCl_4$ may be too reactive which could lead to measured phase segregation of Si-nanoparticles from CZTSiS.

Sintered CZTSSe Films with Large Grains Growth and Minimal/No Fine-Grain Layer (Subtasks 1.1.3, 2.1.1, & 2.1.2)

Film Sintering Study

To fabricate devices in our lab, nanocrystals are synthesized by hot injection and washed as described in our previous reports to remove as much of the oleylamine used in synthesis as possible [1]. The nanocrystals are then suspended in 1-hexanethiol and coated on molybdenum-coated soda lime glass by doctor blading. These films are dried on a hot plate and then sintered into a dense film. Sintering is accomplished by placing the coated substrate in a rectangular graphite box with several pellets of selenium and placing this in a tube furnace. A push rod is used to introduce the graphite box to the heated zone of the furnace when the desired temperature is reached. Our sintering process has traditionally been conducted at 500 °C for 20 minutes.

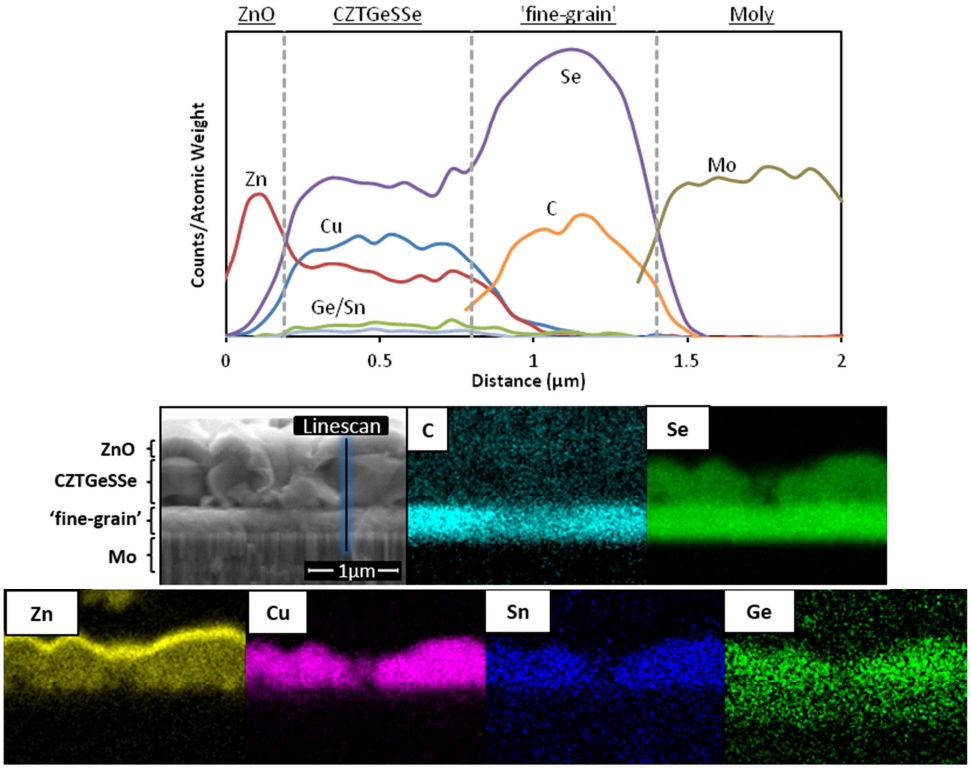


Figure 9. Cross sectional EDX line-scan (top) and elemental mapping (bottom) of a typical sintered CZTGeSSe (30% bulk-Ge) film coated with ZnO (80-100 nm). The 'fine-grain' layer at the Mo back contact is found to be comprised primarily of Se and C and not 'unsintered' CZTGeS nanoparticles. Sulfur is not shown as the signal from this element is found to be minimal following selenization, with the [Se]/([Se]+[S]) ratio estimated to be >90%.

A common trait of CZTS devices fabricated via the nanocrystal-ink based route has been the presence of an unsintered or 'fine-grain' layer near the back contact of the device. This is observed both for devices prepared from CZTS nanocrystals[2,7,8] and from inks of binary and ternary constituents.[12] This layer is composed primarily of carbon and selenium with potential trace metals as determined by EDS

mapping and line scan, as illustrated in Fig. 9. Traditionally we have observed this layer to constitute approximately 50 percent of the absorber layer. This is problematic as it may lead to increased recombination and series resistance in the device stack and light absorbed in this layer will almost certainly be lost as it is far from the junction. This layer is believed to result from the long chain ligands (oleylamine and dimerized oleylamine[13]) that remain bound to the nanocrystals' surface in spite of multiple washings with a variety of solvents.

The end goal of the sintering process is to achieve a dense, polycrystalline film of CZTSSe. Our experience is that films with larger grains of CZTSSe have the highest performance. It is desirable, then, to maximize grain growth while minimizing unwanted side-effects that cannot be avoided during growth, particularly the formation of $MoSe_2$ at the back of the device. $MoSe_2$ is known to result in increased series resistance in the device and strong correlations between increased $MoSe_2$ thickness and decreased device performance are well supported in the literature.[14] Maintaining a high selenium partial pressure has been a key factor in promoting the growth of large grains. Unfortunately, these conditions also typically result in thick $MoSe_2$ layers.

To determine the optimal conditions to promote improved photovoltaic performance, the amount of selenium in the graphite box and temperature of the furnace were varied. Several devices were prepared at each condition. A summary of average performance of the devices is shown in Table 2 using CZTSSe sintered nanoparticle films. We observed that improved photovoltaic performance was observed to be associated with increased selenium. Lower temperatures were detrimental, while higher temperatures showed increased performance over the base case. While this is by no means a complete study, it reveals the great importance of the selenization step and indicates that significant improvements can be obtained through optimized thermal treatments.

Table 2. Table of device performance parameters for sintering experiments using CZTS nanoparticle films. Improved performance is associated with 9 pellets (~470mg) of selenium over 5 pellets (~260mg) (all run at 500 °C). It is also evident that decreasing the temperature of the furnace to 450 °C is detrimental to device performance and that increasing the temperature to 525 °C is likely to result in slight improvements from the base case (5 pellets at 500 °C).

	η	V_{oc}	J_{sc}	*FF*
Conditions	(%)	(mV)	(mA/cm^2)	(%)
500 °C, 5 pellets, 20 mins	6.6	370	29.1	60.6
500 °C, 9 pellets, 20 mins	7.4	397	30.1	62.1
450 °C, 5 pellets, 20 mins	4.3	355	28.4	42.4
525 °C, 5 pellets, 20 mins	7.2	379	30.4	62.0

Efforts were undertaken to study the conditions under which large grains were realized while minimizing the fine-grain layer and $MoSe_2$ layer. A first step was to modify the graphite box to slow the diffusion of the selenium from the box to ensure the Se partial pressure remained sufficiently high to promote grain growth. Our box has traditionally contained a small hole in the lid to simplify the purging of air from the box. We removed the hole from the box and modified our purge procedure. This change immediately led to visibly more uniform devices, eliminating color gradients that were often observed on the films near the hole in the box.

With a redesigned graphite box, it was necessary to experiment with the amount of selenium in the box for the selenization of CZTSSe nanocrystal films. It was desired that enough selenium be present for the reaction to proceed fully without having excess remaining at the end of the selenization step that could condense on the film during cooling. To minimize the risk of selenium condensation on the film, argon was flowed through the system at the onset of cool down to purge selenium vapor from the system before it was able to condense. Six pellets of selenium was determined to be sufficient to achieve grain growth. Another study was conducted in which temperature and selenization time was varied. After many

experiments, optimal device performance was realized for selenizations at 500 °C for 40 minutes or, alternatively, at 550 °C for 15 minutes. Device performance was again observed to correlate strongly with large (micron-sized) grains, minimized fine grain layers, and minimal $MoSe_2$ layers. Interestingly, devices prepared by the nanocrystal ink based method we employ do not exhibit large $MoSe_2$ layers as other devices from the literature do. To limit the $MoSe_2$ layer, others have shown the need to use a TiN diffusion barrier, while this has not been necessary for us. We believe this may be a result of the formation of molybdenum oxide at the back contact when our films are dried in air on a hot plate following coating. This oxide layer may be functioning as a diffusion barrier. Though not complete evidence, we observe that device performance decreases when the films are dried under inert conditions. Fig. 10 shows SEM (FEI Quanta) cross sections of sintered films at optimized conditions, indicating the dramatic reduction in the fine grain layer.

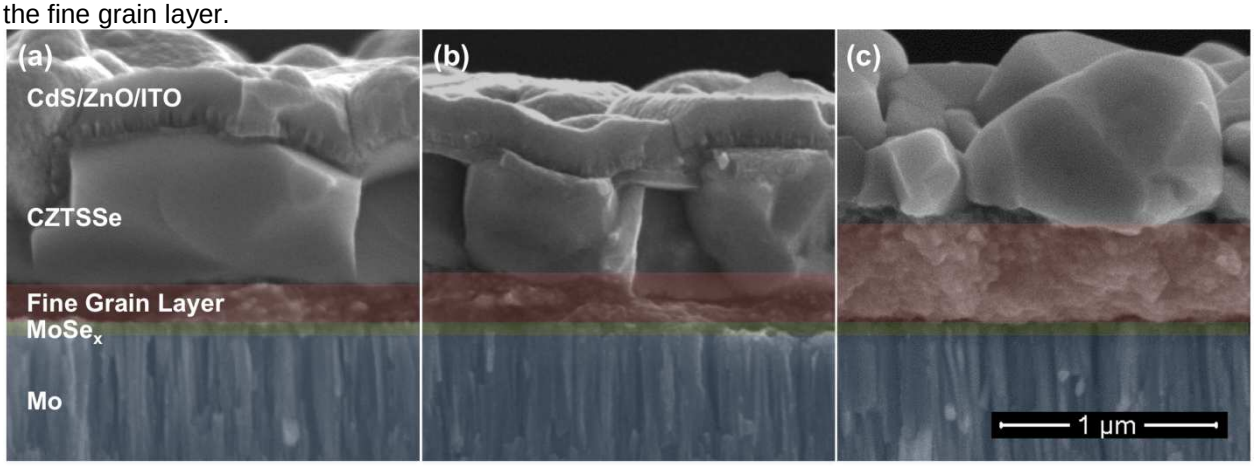


Figure 10. Cross sections of (a) a finished CZTSSe device sintered at 550 °C for 15 minutes, (b) a finished device sintered at 500 °C for 40 minutes, and (c) a film sintered at 500 °C for 20 minutes. Optimized CZTSSe sintering has reduced the fine-grain layer and improved solar cell performance.

The current-voltage characteristics of the CZTSSe devices prepared under optimized selenization conditions are measured under AM1.5 illumination. Device power conversion efficiencies as high as 8.8% are measured prior to the application of a MgF_2 antireflective coating. J-V curves along with key performance parameters are shown in Fig. 11 for a 9.2% device prepared under optimized conditions. This performance was obtained with a MgF_2 anti-reflective coating under AM 1.5 illumination after light-soaking for 5 minutes. Measurements are based on a total cell area of 0.47 cm^2.

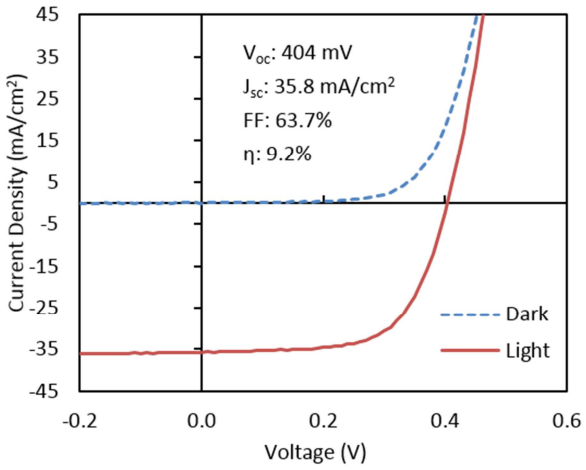


Figure 11. J-V curves for the best performing cell in the dark and under AM1.5 illumination with light soaking for 5 minutes.

These results indicate that selenization is of critical importance to device performance. A study of the mechanism of formation and grain growth will be valuable to further understand the link between material properties/characterization and device performance. The ability to control grain growth and minimize the fine grain layer will likely lead to further improvements.

Bromine Etching Treatments for CZTSSe Absorber Layers

Fig. 12 below shows the Raman spectra of $Cu_2ZnSn(S,Se)_4$ (CZTSSe) absorber layer, obtained using two different laser excitation wavelengths. The absorption coefficient in semiconducting materials is highly dependent on the wavelength used. It increases with decreasing wavelengths. Thus the 325 nm laser is more sensitive towards the surface of the CZTSSe absorber as compared to the 633nm laser.

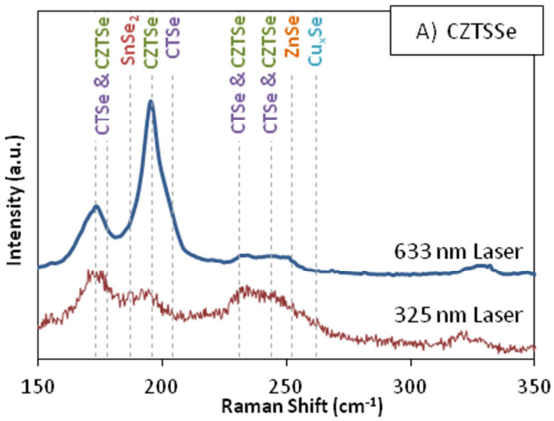


Figure 12. Raman Spectra of CZTSSe absorber with two different excitation wavelengths.

The spectrum from 633 nm laser shows presence of intense peaks at 196 cm^{-1} and 174 cm^{-1}, which correspond to the main peaks of CZTSe.[15] It also shows presence of broad peak from 230 to 270 cm^{-1}. This peak could consist of peaks signals from CZTSe, CTSe (Cu_2SnSe_3),[16] ZnSe,[17] Cu_xSe,[18] and/or $SnSe_2$.[19] In the spectrum from 325 nm laser, the peak intensity of the peak at 196 cm^{-1} has significantly decreased but at the same time the intensity of the peak at ~175 cm^{-1} remains comparable to the spectrum from 633 nm laser. The broad peak from 230 cm^{-1} to 270 cm^{-1} is present in the spectrum from 325 nm laser. From spectra reported in the literature, the peak at 196 cm^{-1} is the most intense peak for CZTSe, whereas for CTSe the peak at 178 cm^{-1} is the most intense peak. No resonant Raman effects are expected to be present for CTSe due to band gap of these materials.[16] Therefore, comparison of the 325nm and 633nm Raman spectra suggests that CTSe may be present on the surface (~25nm) of the selenized absorbers. The presence of low band gap secondary phases, such as CTSe, at the CdS/CZTSSe heterojunction interface can contribute to V_{OC} limitations to device performance, through creating potential fluctuations across the absorber and/or interfacial band gap narrowing.[20]

Therefore, we explored an etching treatment to remove ~20 nm of the top surface of the CZTSSe absorber surface. A solution of bromine in methanol was used as the etchant. Experiments were conducted to find out the etching rates obtained using this etchant, which are shown in Fig. 13. Precise control over etching rate can be obtained by varying the concentration of the solution. The effect of etching treatment on the surface roughness of the CZTSSe absorbers was also studied and is shown in Fig. 14.

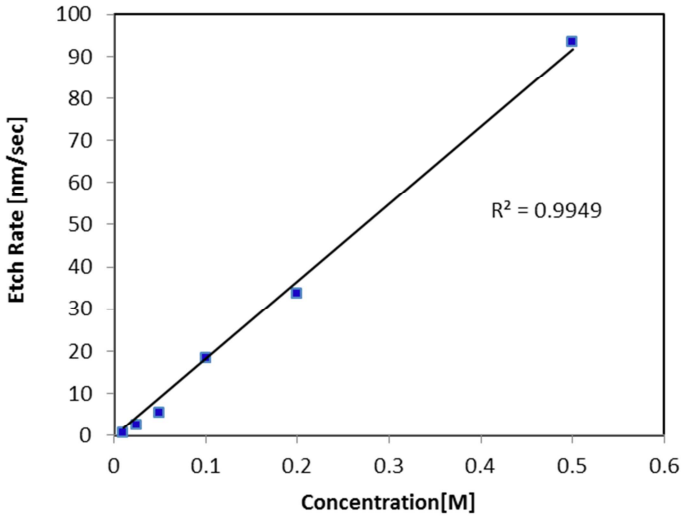


Figure 13. Effect of concentration on etching rate of the sintered CZTSSe films

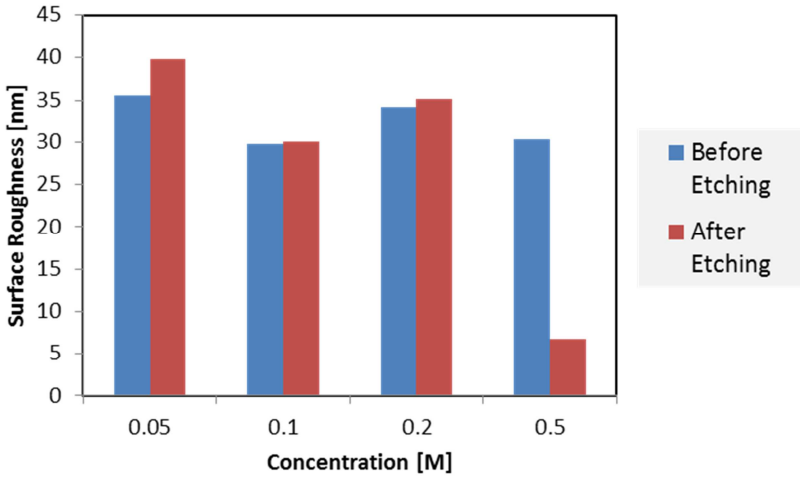


Figure 14. Effect of etching treatments on surface roughness of the sintered CZTSSe films

Canava et al have proposed an etching mechanism for bromine etching of CIGSe.[21] Similar reactions can be written for CZTSSe. It can be seen that copper can either get oxidized to +2 state or remain in +1 state.

Step I

$$Cu_2ZnSnSe_4 + 4Br_2 \rightarrow Cu(I) + Zn(II) + Sn(IV) + 4Se^0 + 8Br^{-1}$$

OR

$$Cu_2ZnSnSe_4 + 5Br_2 \rightarrow Cu(II) + Zn(II) + Sn(IV) + 4Se^0 + 10Br^{-1}$$

Step II

$$Se^0 + 2Br_2 \rightarrow Se(IV) + 4Br^{-1}$$

It was experimentally found that all the bromides that can form in the reaction are soluble in methanol and water except Cu(I)Br. Thus in addition to layer of Se^0, residue of Cu(I)Br is expected to be present on the etched surface. Ideally, for etching purposes we want all of the bromides formed to be soluble in methanol /water so that no residue remains on the etched surface of the absorber. Thus

additional treatments for post etching steps were proposed to dissolve the Se^0 layer and possibly Cu(I)Br layer.

Table 3. Summary of CZTSSe Device Parameters

Treatment	Voc [V]	Jsc [mA/cm^2]	FF [%]	Efficiency [%]
No Treatment/Test	0.403	30.4	61.4	7.5
1	0.27	268	21.7	0.1
2	0.349	25.2	27.8	2.5
3	0.365	28.6	49.5	5.2
4	0.359	7.2	15.2	0.4

0: No Treatment, Base Case.
1: Bromine Etching: solution concentration=0.005 M, Etch time = 10 sec.
2: Bromine Etching: solution concentration: 0.005M, Etch time = 10 sec; followed by treatment with mixture of Butylamine and 1-Hexanethiol in 1:1 volume ratio to dissolve Se^0 layer.
3: Bromine Etching: solution concentration=0.005M, Etch time = 10 sec; followed by aq. KCN etching treatment for 30 sec in 0.5 M KCN (aq.) solution.
4: Bromine Etching: solution concentration =0.005M, Etch time = 10 sec; followed by aq. KBr treatment in 3 molar solution for 10 min.

It can be seen that just the bromine etching is detrimental for the device performance, as expected, because the etched surface provides recombination centers for the generated carriers. Use of Amine-Thiol mixture treatment after bromine etching increased the performance up to 2.5%. This may be because Amine-Thiol mixture only dissolves the selenium layer formed on the surface but the insoluble Cu(I)Br still remains on the surface. KCN treatment increased the performance up to 5.2%. Since KCN etches both selenium and $Cu_{2-x}Se$, the increase in performance after the bromine etching treatment due to KCN treatment is higher as compared to that after Amine-Thiol mixture treatment. Finally, KBr treatment is expected to preferentially dissolve the Cu(I)Br residue formed on the surface by forming $CuBr_x^{-(x-1)}$ complexes, but as can be seen from the device performance the KBr treatment does not have any significant effect on the device performance as compared to that after just the bromine treatment. Thus, with the etching treatments tried so far the performance of the absorber layers after the bromine etching could not be improved even up to the baseline level of about 7.5%. This could very well mean that the surface of the etched absorbers even after the post-selenization treatments has more recombination centers as compared to the absorber layer before any etching treatments. Our etching observations are in sharp contrast to the beneficial effects reported in the literature.[22] However, these experiments provide us clues for future work which include other etching treatments such as KCN, Ammonium Hydroxide, and diluted HCl etc.

Mechanical Polishing of CZTSSe films

In order to eliminate the 'fine-grain' layer, it is important understand both the selenization mechanism and its influence on the final, sintered CZTSSe absorber. In this work, we begin to probe the depth-resolved composition and structure of the absorber film from the front surface to the 'fine-grain' layer at the back of the film. Mechanical polishing was used to grind away the film in subsequent steps with the hope of avoiding interference from surface impurity layers that may be formed by other techniques, such as chemical etching. In the typical procedure, a selenized CZTSSe absorber film was polished using a suspension of 50-nm Al_2O_3 nanoparticles for 30 seconds, with the Buehler MiniMet 1000 polisher set at 20 rpm and 3 lb of force. Fig. 15 depicts SEM cross section images of absorber films after polishing away various amounts of the film. The first polish removes over 300 nm of the film, while subsesequent polishes using the same settings remove only 70-100 nm. This observation is attributed to the surface roughness of the unpolished film and the relative smoothness of the polished samples, since the first polish removes the rough surface features and some of the bulk of the film.

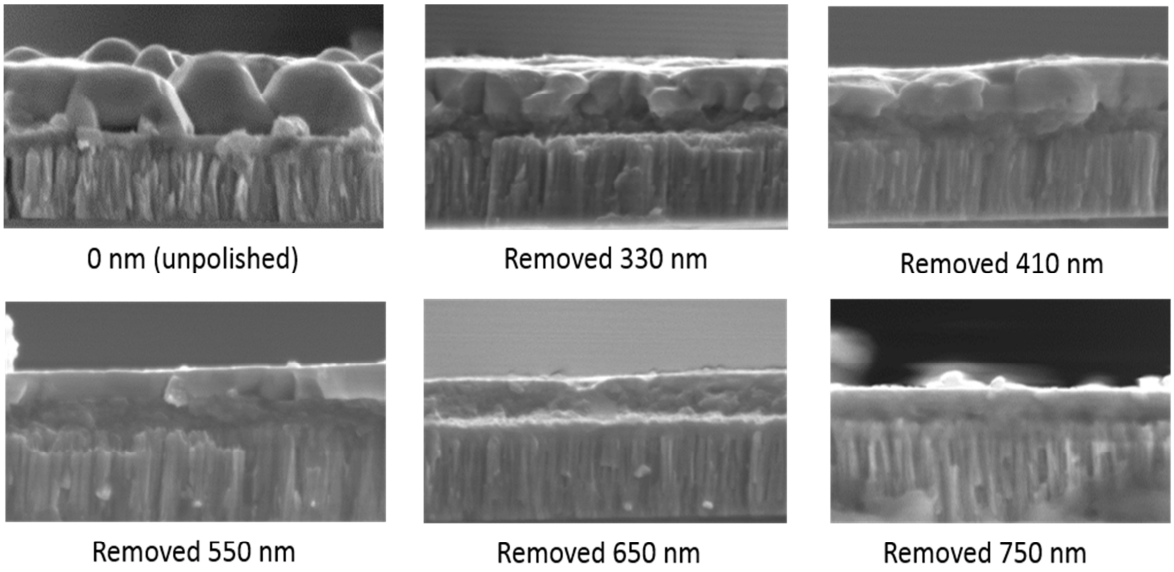


Figure 65. SEM cross sections of selenized CZTSSe absorber films polished (from left-to-right, top-to-bottom) 0, 1, 2, 3, 5, and 6 times.

Fig. 16 demonstrates the Raman spectra obtained using a 633-nm laser for the films depicted in Fig. 15. The spectrum for the unpolished absorber closely matches that expected for relatively pure-phase CZTSe; however, the small peaks between 230 and 250 cm^{-1} can be attributed to CZTSe as well as Cu_2SnSe_3, ZnSe, and condensed elemental Se from the selenization step. Nonetheless, the Raman data for the unpolished film provide little evidence to suggest that notable phase segregation is present in the selenized CZTSSe absorber. By collecting the same data for samples polished to different thicknesses, we can determine if this relative phase homogeneity is consistent throughout the depth of the film. Indeed, we observe little change in the Raman spectrum for the polished films (other than a gradual decrease in overall peak intensities) until enough of the absorber has been removed that the laser probes the 'fine-grain' layer. Compositional analysis via SEM-EDX reported for previous quarters suggested the 'fine-grain' layer primarily comprises Se and some C, and the Raman spectra for the films polished 5 and 6 times corroborates this finding. Ultimately, Raman analysis of the series of polished and unpolished CZTSSe absorbers suggests that on the scale of the interaction volume of the incident laser, the film is rather uniformly comprised of quaternary CZTSSe with little evidence of undesired ternary or binary phases, and that excess elemental

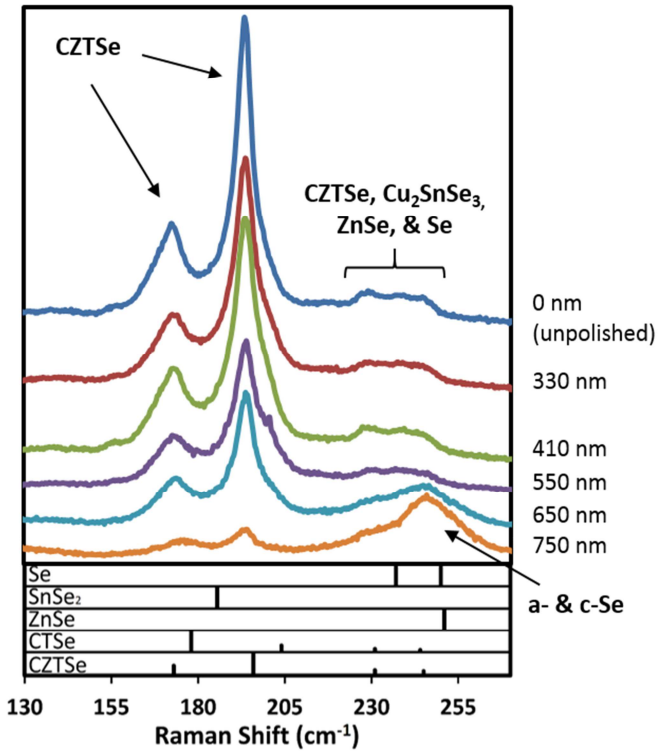


Figure 16. Raman spectra for the series of polished samples and expected peak locations and approximate relative intensities for CZTSe and possible impurity phases.

Se in the selenization step condenses at the back of the film to contribute to the formation of the 'fine-grain' layer. These observations provide encouragement with regards to the quality of the sintered film as well as guidance for possible means of avoiding the formation of the 'fine-grain' layer.

In addition to providing a means of depth-profiling the selenized absorbers, mechanical polishing offers the potential to remove a very thin layer of impurity phases that previously reported XPS measurements suggested exist at the very surface of the unpolished selenized film. Furthermore, a smooth interface between CZTSSe and CdS is expected to provide more spatially uniform junction characteristics than the rough interface present due to the unpolished film. Both of these benefits of mechanical polishing were hypothesized to yield improvements in device performance for solar cells fabricated from a once-polished absorber. However, while the unpolished control devices achieve typical total area efficiencies of roughly 8% without any anti-reflective coating, cells with the same structure but comprising a once-polished absorber fail to exhibit any power conversion efficiency (Fig. 17). The poor performance of the polished device is most likely due to significant formation of interface defects during and/or after polishing; these interface defects may be associated with structural issues or impurities introduced from the mechanical polishing. This assertion is supported by the fact that solar cells fabricated from absorbers that were polished once and subsequently annealed under Ar with a small amount of elemental Se for 10 minutes at 350 °C achieved efficiencies as high as roughly 4% (Fig. 17). Consequently, the anneal treatment is believed to reform the surface of the absorber, but no polished samples – with or without a subsequent anneal treatment – have achieved efficiencies higher than the unpolished control devices.

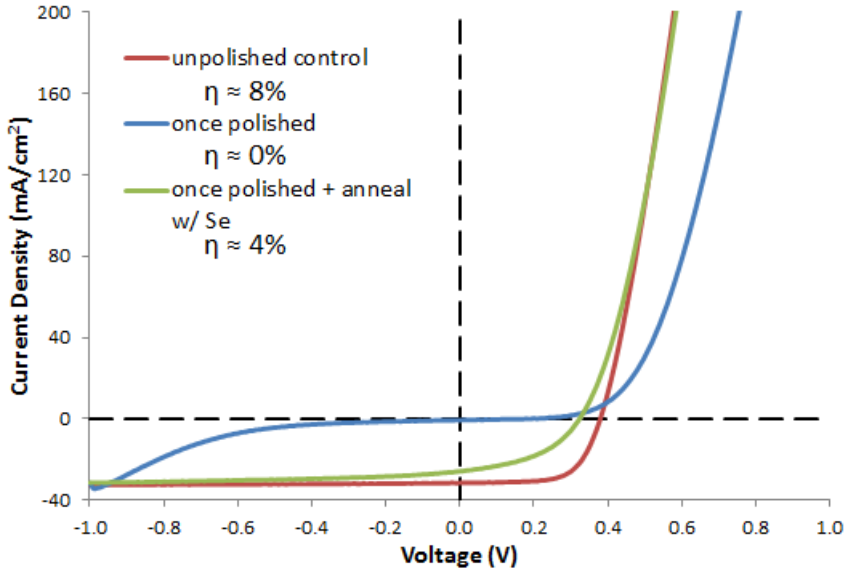


Figure 17. Light current-voltage characteristics for devices fabricated from an unpolished, control absorber, an absorber that had been polished 1 time, and an absorber that had been polished 1 time and then annealed under Ar with a small amount of elemental Se for 10 min. at 350 °C.

Depth profile characterization of CZTSSe films via Raman and mechanical polishing

While the Raman analysis described above did not detect the presence of ZnSe in the selenized films, it is commonly reported that ZnSe (and especially its sulfide counterpart, ZnS) respond weakly in Raman measurements when using low-energy, 633-nm excitation. In order to more rigorously determine if ZnSe is present in the CZTSSe absorbers, Raman spectra were collected for an unpolished absorber using 325-nm and 458-nm excitation in collaboration with Helmholtz-Zentrum Berlin (Fig. 18a). These wavelengths (particularly 458 nm) utilize resonant effects in the ZnSe bonding configuration to greatly enhance the signal intensity from this phase compared to other phases present in the samples. Since the

large absorption coefficient of CZTSSe prevents the short-wavelength lasers from penetrating very deep into the absorbers, the Raman measurements on the unpolished sample only provide information relevant near the surface of the absorber. Thus, the same measurements were performed on a once-polished absorber to collect information about the possible presence of ZnSe in the bulk of the film (Fig. 18b). For both the unpolished and polished samples, neither of the short-wavelength measurements exhibits the strong enhancement of the ZnSe Raman signal near 250 cm^{-1} that would be expected if the phase were indeed present in the film. This result further supports the earlier assertion that the sintered absorber consists of relatively pure-phase quaternary CZTSSe, at least on the scale of the interaction volume of the excitation sources.

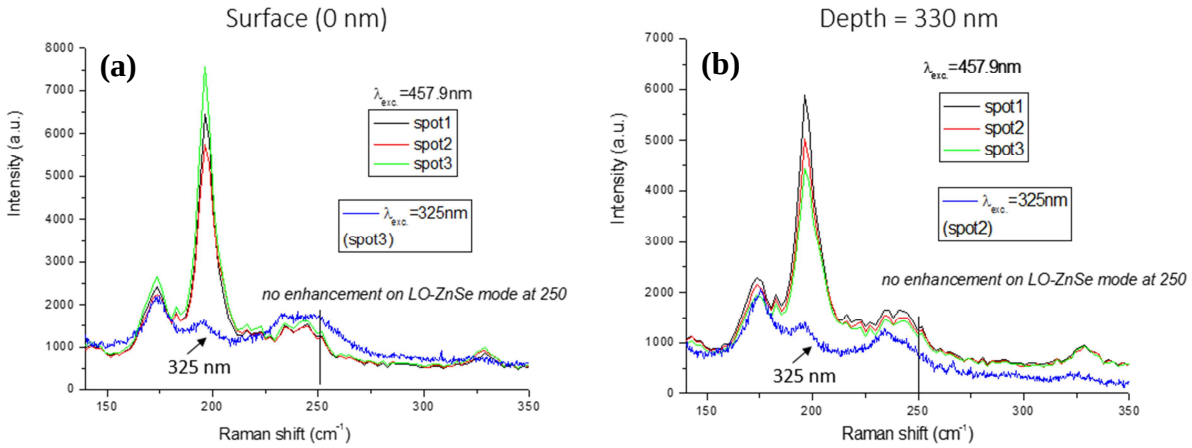


Figure 18. Raman spectra for (a) unpolished and (b) once-polished CZTSSe absorber films using 458-nm and 325-nm excitation lasers. The black, red, and green curves in (a) and (b) represent spectra acquired at three different spots on the sample using the 458-nm laser.

Homogeneous nanocrystals and absorbers with varying band gap: (Subtasks 1.2.1 & 2.2.1)

Ge-Alloyed CZTGeSSe:

Initial results in CZTGeSSe solar cells has shown detrimental issues associated with Ge-loss

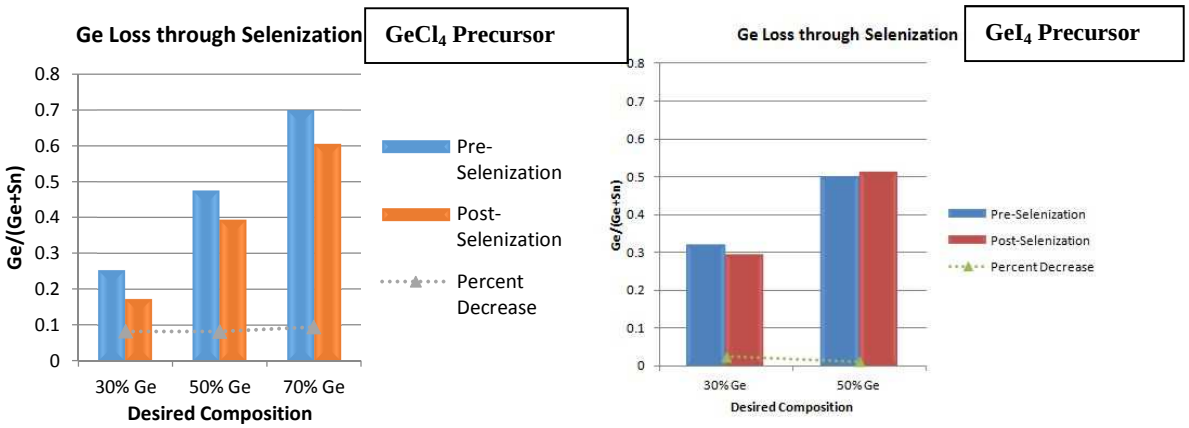


Fig. 19. CZTGeSSe devices made using $GeCl_4$ as a precursor yield particles with 10% decreased Ge-incorporation following selenization, switching to GeI_4 now yields roughly constant Ge values post selenization.

during the selenization procedure. Using a $GeCl_4$ precursor in the nanoparticle synthesis reaction has led to a 10% decrease in the measured Ge composition following selenization. To alleviate this issue, new synthesis techniques were explored, which has led to the use of GeI_4 as the current Ge precursor for CZTGeS nanoparticle synthesis. Nanoparticles selenized from this optimized particle synthesis have now shown considerably reduced Ge-loss during selenization.

To understand the effect of Ge-loss on device performance, devices were made from cells with and without Ge-loss and Voc comparisons were made (Fig. 20). It was clear from these measurements that devices made from $GeCl_4$ achieved a maximum Voc that becomes saturated in higher Ge-content

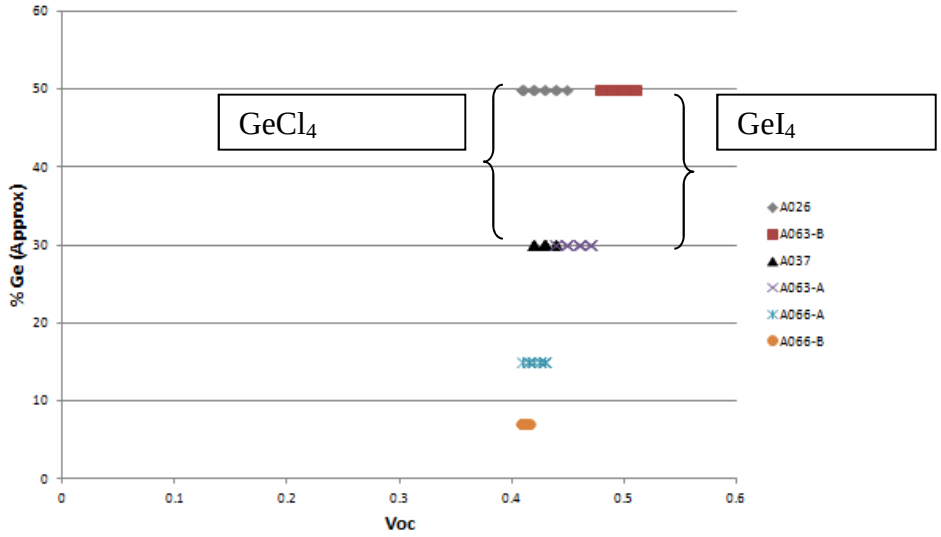
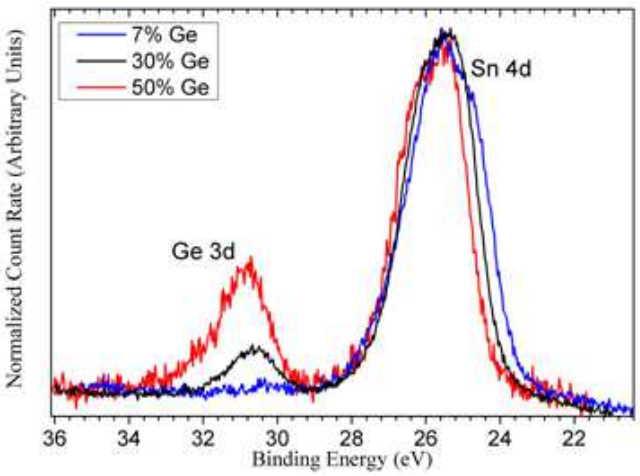


Fig. 20. Use of $GeCl_4$ precursors for CZTGeSSe experiences Voc saturation in higher Ge content devices while GeI_4 precursors follow a linear trend in Voc increase for all devices measured.

devices. It was found that devices with >30% Ge showed little increase in Voc upon further Ge-incorporation, while devices with <30% Ge showed a linear increase in Voc as expected from the linear increase in band gap. However, devices made from GeI_4 no longer suffered from Voc limitations at



Nominal bulk [Ge] (%)	Surface Ge (%)
7	0
30	12
50	24

Fig. 21. Initial XPS results suggest that devices made from GeI_4 experiencing no bulk Ge-loss may still exhibit Ge-loss at the surface.

higher Ge-incorporation. It was shown that these devices follow a linear increase in Voc for the entire range of particles synthesized. These results suggest that Ge-Loss can be one aspect responsible for Voc limitations in CZTGeSSe solar cells.

While GeI_4 seems to alleviate issues with bulk Ge-loss, initial results in collaboration with HZB using XPS suggests that there is still Ge-loss experienced at the surface of the selenized film (Fig. 21).[3] This surface Ge-loss (roughly 50% in the first 10nm of the film) may be responsible for the large spread in Voc measured for devices with higher Ge-content.

Initial results from admittance spectroscopy of CZTGeSSe reveals two trap levels in the devices. These traps correspond to theoretical values expected for the Cu_{Zn} and V_{Cu} defect sites; however, further analysis is necessary to determine the origin of the measured traps for these devices. Results also indicate that one or both of these measured trap levels are responsible for the doping density of the devices. If the doping density is determined by the deeper of the two trap levels, than the behavior measured for Rs(T) would be expected due to carrier freeze out, following:

$$\rho = \frac{1}{q\mu_p N_A}$$

where the carrier density,$N_A(T)$, would decrease with decreasing temperature causing the resistivity, ρ, to increase.

The results of admittance spectroscopy analysis also indicate that the deeper of the two trap levels measured gets even deeper towards mid-gap with increasing Ge-content in the device. However, the shallow trap seems to remain at the same level regardless of Ge addition.

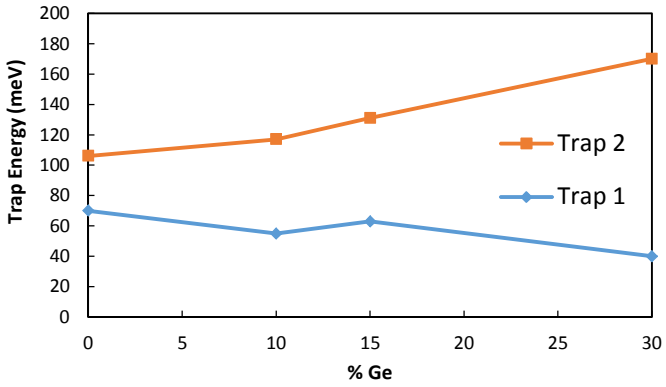


Fig. 22. Trap energy vs. Ge content for CZTSSe and CZTGeSSe calculated from Admittace spectroscopy.

Further optimization was carried out on CZTGeSSe, which has led to efficiencies reproducibly >9% for CZTGeSSe with 30% Ge-incorporation. Champion device performance has delivered 9.4% power conversion efficiency (total area, AM1.5 illumination, .47cm^2 area, anti-reflective coating). These results indicate increased device performance over the reported 9.2% p.c.e for CZTSSe with no Ge-incorporation, indicating performance enhancements gained from Ge alloying. Furthermore, the Ge containing device has not been sintered under optimized selenization conditions as the CZTSSe device has, indicating future potential for device improvements in this system.

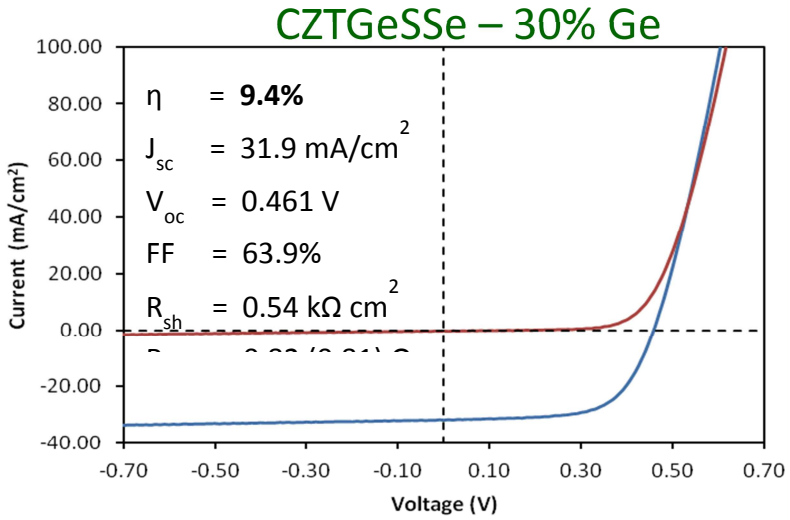


Fig. 23. Device performance for champion CZTGeSSe device.

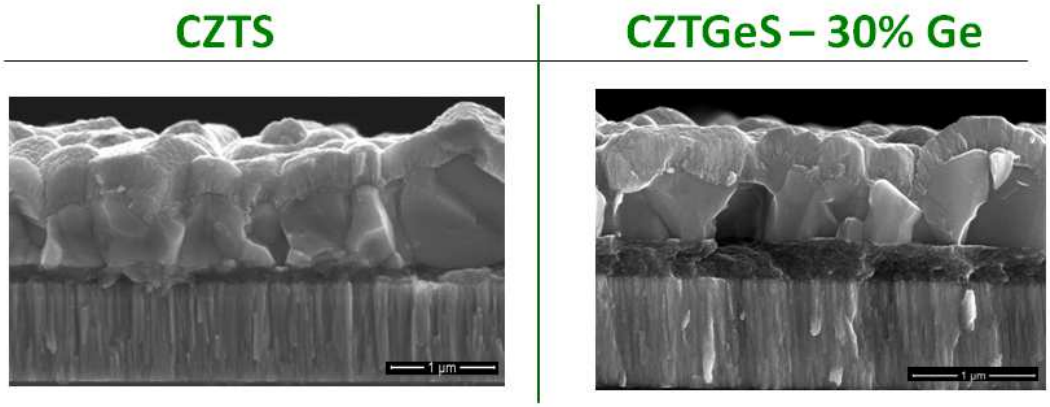


Fig. 24. SEM crosssections of CZTSSe and CZTGeSSe devices illustraing the difference in the "unsintered" layer between the two. CZTGeSSe device shows potential for future improments.

Admittance spectroscopy of the optimized CZTGeSSe devices suggests the exsitence of a significant number of deep level traps, as the capacitance values continues to increase at higher temperatures.

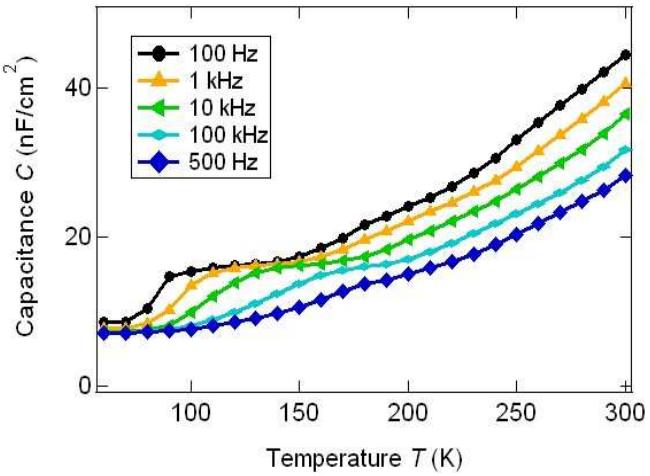


Fig. 25. Admittance spectroscopy for optmized CZTGeSSe device, revealing the exsitence of deep level traps.

Photoluminesence measurments were conducted on CZTSSe and CZTGeSSe to compare the differences between the two devices, and understand the improvments in device performance measured for the Ge-containg devices. A shift in the PL peak to higher energy is measured for CZTGeSSe, whilch is expected for this higher band gap absorber. Both material systems have peaks in the PL emmission near the band-edge measured from EQE, indicating the potential for band-to-band recombination in these devices to be dominant.

The room temperature PL data also reveals very broadened, asymetric peaks with exponential decrease in signal measured at low energy. This behavior indicates the possibility for potential flucuations in the devices, or band-tails, which may be acting to limit the recombination activation energy.

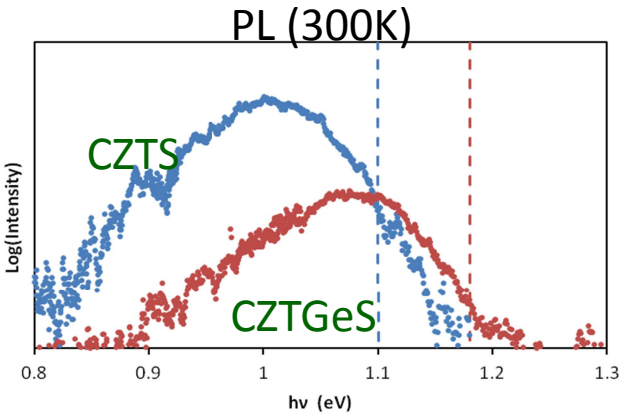


Fig. 26. Room-temperature PL measurments comparing CZTS and CZTGeS

Selenization Optimization of CZTGeSSe

Thick Film Optimization

Previous work reported under this Sunshot project has demonstrated the benefit of optimizing sintering in the CZTSSe material system. This optimized sintering was previously employed to achieve

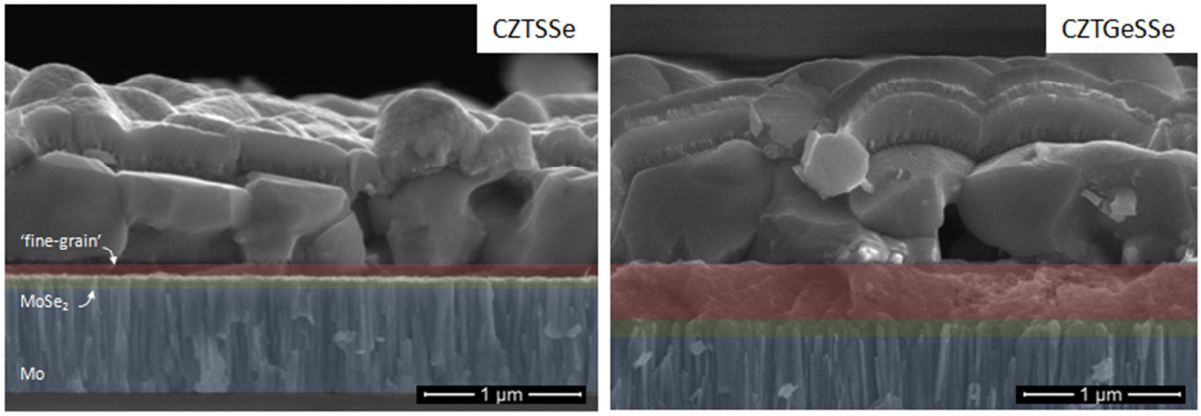


Figure 27. SEM cross-sectional comparison of CZTSSe and CZTGeSSe (30% Ge). The CZTSSe absorber was fabricated under optimized selenization conditions, resulting in a minimal 'fine-grain' layer thickness as well as minimal $MoSe_2$ layer formation. The CZTGeSSe device was fabricated under our normal selenization conditions, and demonstrates a relatively larger 'fine-grain' layer thickness as well as increased $MoSe_2$ formation. Despite un-optimized sintering, CZTGeSSe demonstrates 9.4% p.c.e. while CZTSSe demonstrates 9.2% p.c.e, suggesting notable room for improvement in CZTGeSSe absorbers.

improved device performance in CZTSSe devices, up to 9.2% pce. Following these results, work was aimed at employing the optimizing sintering techniques developed for CZTSSe to the CZTGeSSe material system.

Previously under subtasks 1.1.3, 2.1.1 and 2.1.2, it was demonstrated that controlling the selenization reaction time and temperature profiles, as well as the selenium partial pressure during selenization, has the beneficial effect of controlling the formation of $MoSe_2$ as well as the thickness of the 'fine-grain' layer. Using optimized selenization conditions ('closed' graphite box, 500 ^{0}C for 40 min or 550 ^{0}C for 20 min – previously described), CZTSSe sintered absorber layers were formed with a minimal to negligible 'fine-grain' layer thickness, as shown in Figures 10 and 27. These improvements have chiefly resulted in enhanced carrier collection (i.e. increased J_{SC} for the optimized absorbers). Despite this improved performance in CZTSSe from optimized sintering, un-optimized CZTGeSSe (30% Ge) absorbers have shown increased device performance compared to CZTSSe; a comparison of the SEM cross-section for the un-optimized CZTGeSSe (30% Ge) absorber compared to the optimized CZTSSe absorber can also be seen in Fig. 27. Therefore, work presented here is based around applying the optimized sintering conditions used in CZTSSe absorber formation to CZTGeSSe absorbers.

In addition to optimizing 'fine-grain' layer thickness, $MoSe_2$ formation, as well as achieving maximum grain size, there is also a motivation to develop nanocrystal sintering techniques for thick films (i.e. thick films relative to traditional absorber layer thicknesses from this nanocrystal based technique). Comparison of film thickness for devices fabricated in our lab to other high-efficiency CZTSSe devices, as well as CIGSSe devices, reveals a notable thinner absorber layer thickness for our nanocrystal based absorbers.[23,24] Therefore, techniques were explored to develop optimized sintering on thick films to compare nanocrystal based thick films to traditional thin films fabricated in our lab; here we refer to 'thin' as less than or equal to 750 nm while thick is greater than or equal to 1 micron – traditional absorbers in our lab exhibit sintered absorber layer thicknesses of ≈700 nm.

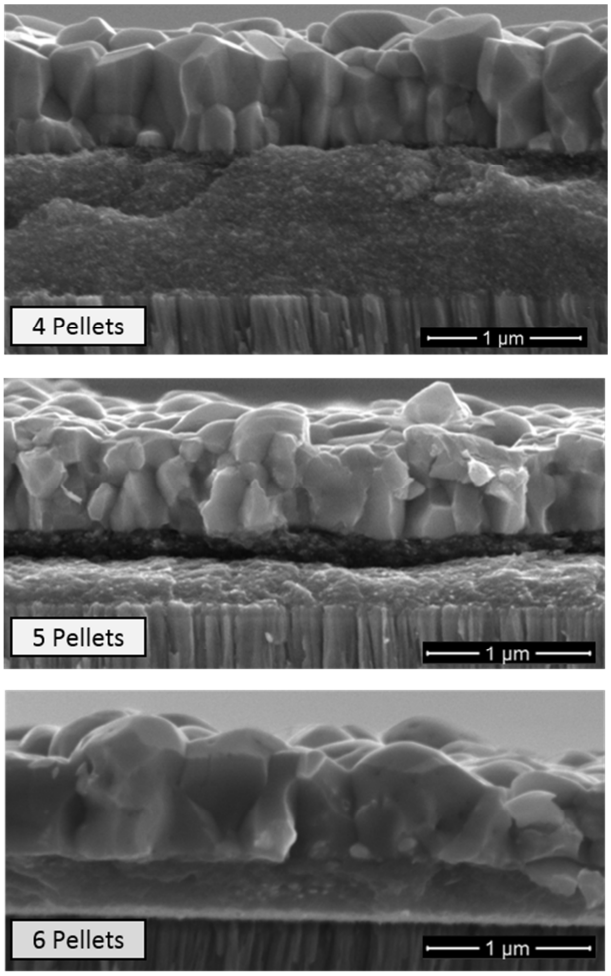


Figure 28. Comparison of SEM cross-sections for CZTGeSSe selenized with various amounts of se loading in the graphite box.

Optimized sintering experiments described here were conducted on CZTGeS nanocrystal films with a nominal Ge concentration of 30 at. % ([Ge]/([Ge]+[Sn]); Nanocrystal inks were synthesized under Cu-poor Zn-rich conditions. A 'closed' graphite box was used, as similarly designed for optimized CZTSSe selenization, with selenization conditions at 500 ^{0}C for 40 min. The closed box design is aimed at minimizing the diffusion rate of $Se_{(g)}$ away from the CZTGeS nanocrystal films during selenization. It was found that comparison of the 'closed' box design used for CZTSSe and CZTGeSSe films is not necessarily equivalent due to variations in machining precision, however, these box designs are still used, despite differences to each other, because they act to limit the diffusion rate of $Se_{(g)}$ similarly; however, due to this, it was found that optimized sintering conditions of one graphite box (i.e. for CZTSSe) may not be the same for optimized sintering conditions for another graphite box (i.e. CZTGeSSe). *These variation can introduce significant variability in the selenization procedure, and are motivation behind*

developing a new selenization equipment, discussed below. Thick absorber films were achieved by increasing the thickness of the CZTGeS nanocrystal layer prior to selenization; this thickness of this nanocrystal layer was aimed at 50% increase from traditional nanocrystal films.

For this study, various selenization times, temperatures, as well as variations in the selenium loading in the graphite box were explored to find optimized thick film sintering conditions. As we have previously found that bulk Ge-loss can have a negative impact on device performance, Ge-loss was analyzed through SEM-EDX under these various selenization conditions. It was found that Ge-loss was only a function of the Selenization temperature, and not the selenization time or selenium loading in the box (i.e. selenium partial pressure during selenization). This Ge-loss may be associated with the initial nanostructured material, as additional Ge-loss was not measured for films that were re-selenized multiple times. For all films selenized at 500 ^{0}C, 5% (± 2.5%) bulk-Ge loss was identified regardless of selenization time. For films selenized at 550 ^{0}C, 10% (± 2.5%) bulk-Ge loss was identified. While variations in the amount of selenium loaded into the graphite box did not cause a shift in the measured bulk-Ge loss, it is presumed that all amounts of selenium tested here were above the amount required to achieve the desired film stability.[25] Devices selenized at 500 ^{0}C are considered in the analysis below due to the minimized Ge loss characterized for this selenization condition.

At 500 ^{0}C, Fig. 28, illustrates differences in absorber formation for three different amounts of Se loading in the graphite box; 4 pellets signifies ≈208 mg of Se pellets (Aldrich), 5 pellets signifies ≈260 mg of Se pellets (Aldrich), 6 pellets signifies ≈312 mg of Se pellets (Aldrich). Under all selenium loadings, $Se_{(g)}$ was present at the end of the selenization reaction, therefore, it is assumed that $Se_{(g)}$ was present during the entire selenization reaction. However, as the 'closed' box is not gas tight (there is a notable diffusion rate of $Se_{(g)}$ out of the box), different selenium loadings are expected to modify the $Se_{(g)}$ partial pressure profile throughout the reaction time. $Se_{(g)}$ is not expected to be at its vapor pressure for the entire reaction due to the diffusion rate of $Se_{(g)}$ out of the graphite box.

SEM analysis of the different selenium loading conditions, Fig. 28, reveals significant differences in absorber layer formation for the different conditions tested. First, there is a noticeable variation in the 'fine-grain' layer thickness for these films. It was found that the thickness of this 'fine-grain' layer decreased as the loading (i.e. partial pressure) of Se was increased during selenization. As EDX mapping has previously identified that this 'fine-grain' layer is primarily composed of Se and Carbon, it is

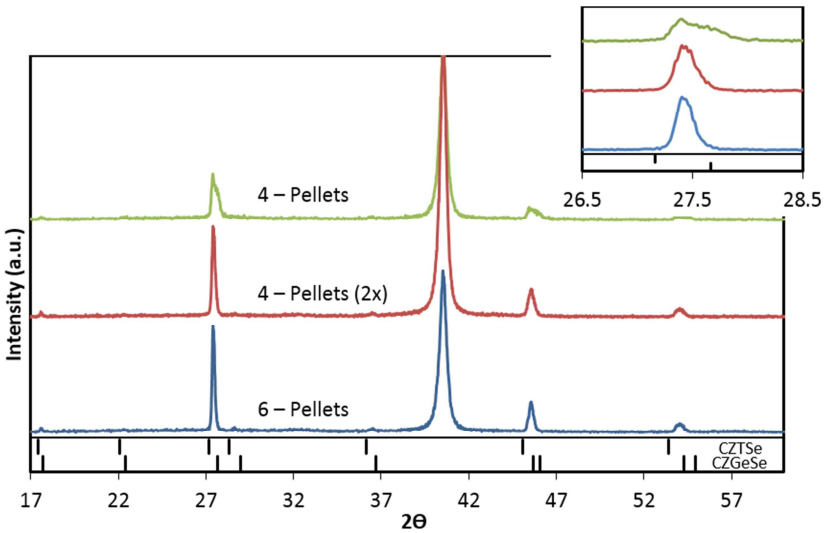


Figure 29. Comparison of XRD for CZTGeSSe 'thick' films selenized under various conditions. The inset illustrates variations in the {112} peak location.

expected that variations in the presence of Se during selenization can affect the thickness of this layer.

Despite differences in 'fine-grain' layer thickness, the thickness of the sintered layer was found to be similar for all conditions tested. However, the morphology of these layers does vary from the different conditions. The lower Se loading appears more faceted, while the higher selenium pressure appears more rounded or smooth; also, larger grains (horizontally) are identified for the higher selenium loadings.

XRD data (Fig. 29) suggest that at the lower Se loading conditions all the nanocrystals are not fully reacted. Therefore, some of the films from the 4-pellet and 5-pellet selenization conditions were re-loaded with selenium and selenized for a second time for 40 min (labeled 4-pellets (2x) and 5-pellets (2x)). Cross-sectional SEM imaging of the double selenized films can be seen in Fig. 30. It is now found that the 4 pellet and 5-pellet films have very similar grain morphology and 'fine-grain' layer thickness as the single selenization 6-pellet condition. This is the reason we suspected the 4-pellet and 5-pellet selenization as incomplete selenization conditions. Therefore, it is suggested that the selenization reaction can be completed for various degrees of selenium loading (i.e. partial pressure) by modifying the total selenization time. Therefore, the lower Se loadings are associated with a slower selenization rate. Despite this, the different selenium loadings are still suspected to have differences in defect formation and therefore device performance, which is currently under investigation. Further investigation is necessary to determine the device performance of these 'thick' absorbers as well as identify techniques to minimize the thickness of the 'fine-grain' layer for thick films.

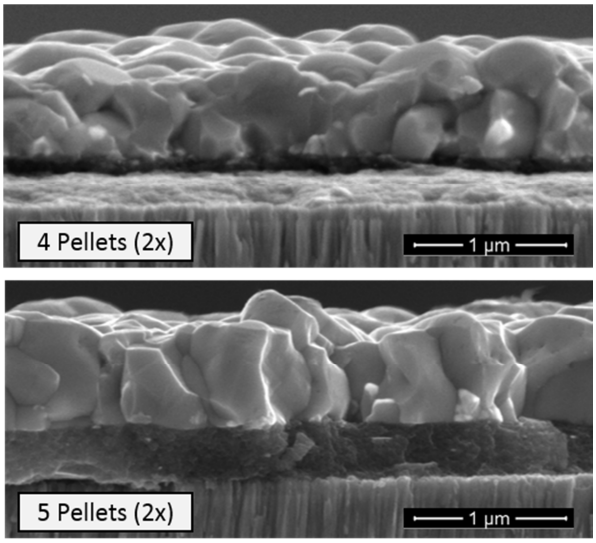


Figure 30. SEM cross-sectional comparison of the lower selenium loading conditions (4-pellet and 5-pellet) when selenized two consecutive times, showing similar results to that of single selenization for 6-pellet conditions.

In addition to SEM cross-sections, comparison of grain growth between the selenization conditions was also considered with XRD analysis, shown for the extreme cases of 4-pellets and 6-pellets in Fig. 29. Comparison of 6-pellets to 4-pellets shows a significant decrease in grain growth, identified from a decrease in the full-width-half-max (FWHM) value. Additionally, closer inspection of the {112} peak (Fig. 29 inset) reveals the presence of peak splitting for the 4-pellet condition. As the absorbers are a CZTSSe and CZGeSSe alloy, the peak location is expected to be between the standard CZTSe and standard CZGeSe locations, identified at the bottom of the XRD plots; the measured devices (30% Ge) exhibited the expected peak shifting. However, the 4-pellet condition suggest a segregated phase of either CZTSe (no Ge), ZnSe, or Cu_2SnSe_3 (ZnSe and Cu_2SnSe_3 have similar peak locations to CZTSe). However, when the 4-pellet condition is repeated (4 pellet (2x)), this peak splitting disappears; therefore, incomplete selenization may entail the presence of segregated phases. Additionally, it suggests that CZTSSe transitions through multi-phase condition during the selenization process, as previously suggested.[5] The identification of multiple phases in the 4-pellet selenization can also be seen in the SEM cross section of Fig. 28, where the morphology appears to be of two layers stacked on top of each other in the sintered layer; this may indicate the selenization reaction front is comprised of this segregated phase. It is useful to note that this segregated phase may not have been identified for CZTSSe (without Ge) due to overlapping peak locations, identifying the usefulness of CZTGeSSe films in

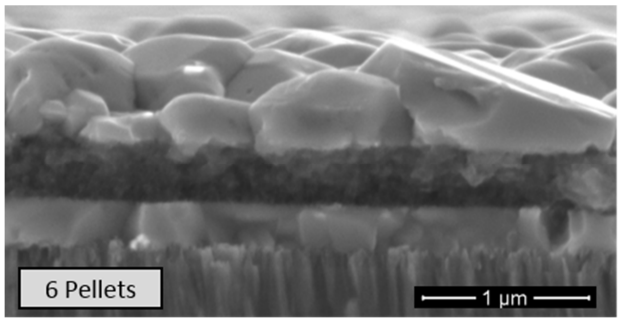


Figure 31. SEM cross-section illustrating the formation of a tri-layer structure for 'thick' films of CZTGeSSe selenized with 6 pellets.

understanding the selenization mechanism from XRD analysis. Comparison of the 4-pellet (2x) and the 6-pellet selenization conditions reveals very similar diffraction patterns.

This analysis suggests the 6-pellet conditions will be ideal for devices (large grains, single selenization). Further analysis was also used to verify this with TRPL, not shown here. However, one drawback was identified in the formation of a tri-layer structure in certain spots under 6-pellet conditions, illustrated in Fig. 31. Further analysis is underway to determine the mechanism of isolated tri-layer formation, where the 'fine-grain' layer is located between a sintered layer at the top and sintered layer at the back of the film, however, it is suspected from these results to be associated with the high selenium partial pressure used for 6-pellets. This high selenium partial pressure may result in a fast selenization reaction rate, thereby starting selenization at both the front and back of the film. It has previously been found in our research group that baking the nanocrystal film in oxygen prior to selenization is important in stopping tri-layer formation, therefore, a more extensive baking conditions study is necessary for thick film coatings compared to the traditional thin film coatings which don't show tri-layer formation with 6-pellets.

Thin Film Optimization: Composition and Selenium Diffusion

In addition to considering thick films, the optimized selenization techniques were also applied to traditional thin film fabricated under our standard technique. Using the optimized selenization conditions identified for CZTSSe synthesis, CZTGeSSe (50% Ge) films were prepared, whose cross-sectional SEM imaging can be seen in Fig. 32. It was found that under the previously identified optimal growth conditions, the thickness of the 'fine-grain' layer was indeed minimized, as similarly found for CZTSSe. Device fabrication for these thin-films with varying degrees of Ge-incorporation is needed.

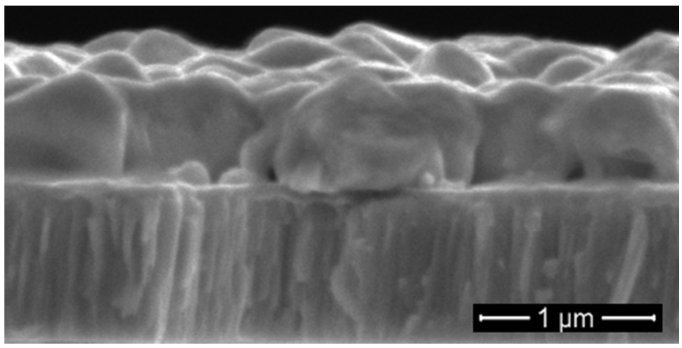


Figure 32. Cross sectional SEM image of CZTGeSSe (50% Ge) selenized under the optimized selenization conditions, illustrating a significantly reduced 'fine-grain' layer thickness.

To understand the effect of selenization conditions on the formation of standard ('thin') CZTGeSSe films, various selenization conditions were tested. The conditions outlined here all involved the optimized 500^0 C temperature, 6-pellets, as well as 'closed'-lid box, however, variations were made in sealing the lid. Here we identify these variations in sealing the lid as Type-I, Type-II, and Type-III selenization conditions. These conditions indicate increasing degrees of the graphite box the samples are in being sealed during selenization, with Type-I being the least 'sealed' and Type-III being the most sealed. Variations in the sealing of the box were made by modifying how tight the lid was for Type-II, and by sealing the lid down with carbon paste for Type-III selenization. These varying degrees of 'sealing' allow for the diffusion rate of Se out of the graphite to be slowed down from Type-I to Type-III. Using these various sealing conditions, Cu-Poor as well as Cu-Poor/Zn-rich films were tested to identify variations in composition on the sintering mechanism.

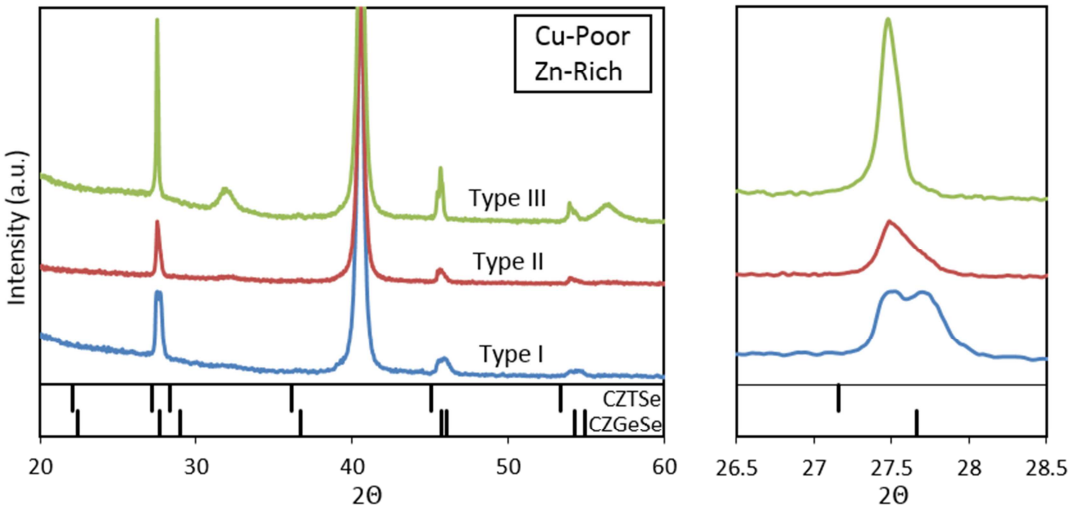


Figure 33. XRD comparison of CZTGeSSe selenized under various conditions for a Cu-poor/Zn-rich nanoparticle film. The figure to the right better illustrates the {112} peak, where peak splitting can be identified when the Se diffuses away from the box to fast during selenization.

XRD analysis of the various CZTGeSSe absorbers fabricated under different conditions as well as from different stoichiometries is shown in Fig. 33 and Fig. 34. It was found that limiting the diffusion rate of Se from the box leads to increasing grain growth for both compositions, as indicated by the decrease in FWHM as well as disappearance of segregated phases (peak splitting) when going from Type-I to Type-III. It appears that poor sealing of the box leads to this segregated phase formation, as similarly found for the 4-pellet 'thick' film coatings, which may be CZTSe (no Ge), ZnSe, or CTS. Comparison of the Cu-poor and the Cu-poor/Zn-rich films reveals in increased tendency for phase segregation in the Cu-Poor/Zn-rich film, as well as a significant decrease in signal intensity; this may be the result of a decrease in grain growth due to the relatively more un-stoichiometric composition of the Cu-poor/Zn-rich film.

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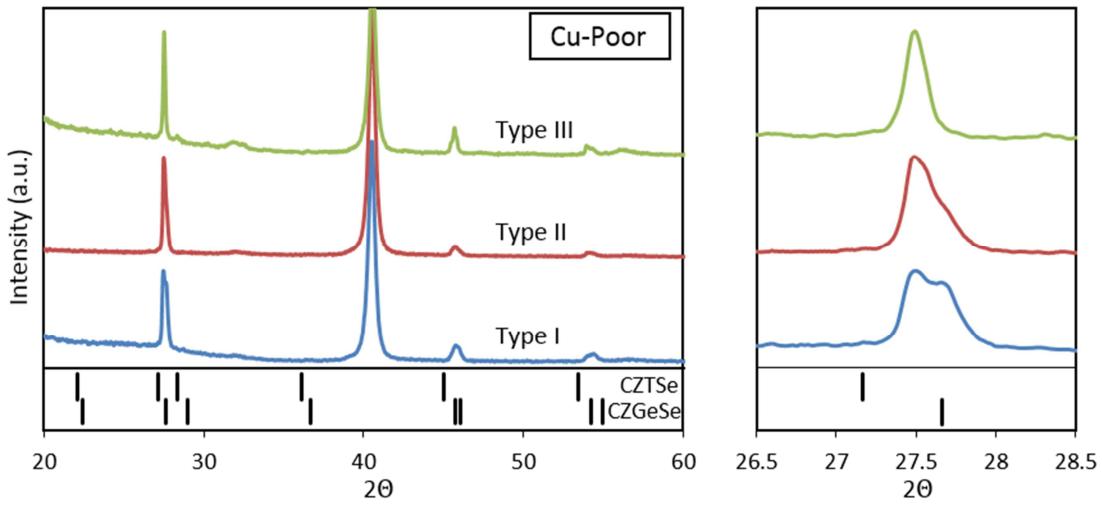

Figure 34. XRD comparison of CZTGeSSe selenized under various conditions for a Cu-poor nanoparticle film. The figure to the right better illustrates the {112} peak, where peak splitting can be identified when the Se diffuses away from the box to fast during selenization.

Here we have found the importance of many different parameters that determine the characteristics of the selenized absorber, which include: reaction temperature, reaction time, film

composition, film thickness, selenium loading, and the selenium diffusion rate from the graphite box. These factors lead to many variations in Ge-loss, phase purity, grain morphology, sintered film thickness, as well as fine-grain layer thickness. Therefore, it is critical to specifically control the selenization reaction conditions to minimize any variables that can arise from differences in selenization conditions from batch to batch; doing this will allow for better understanding of changing variables such as film composition without having to worry about variability in the selenization equipment. Additionally, it is desirable to have tight control over specific selenization variables, such as the Se partial pressure. Therefore, we have been motivated to implement new equipment for selenization to have better reproducibility as well as control over the selenization conditions.

Characterization and Modeling (ST 1.3.1 & 2.4.1)

One of the primary issues limiting the performance of CZTSSe is the low open-circuit voltage (V_{oc}). With an optical bandgap of about 1.15 eV, even current record cells show a V_{oc} deficit of nearly 0.6 V.[24] Our best devices similarly show low V_{oc} of around 0.4 V.[1,2] We have used characterization and simulation to investigate several possible causes of low V_{oc} in order to suggest the best method to increase efficiency.

Photoluminescence Measurements (TRPL and PLE)

We have investigated various photoluminescence characterization methods for determining minority carrier lifetimes in thin film ink based CZTSSe. TRPL is a common method for measuring minority carrier lifetimes.[26,27] We have therefore purchased equipment for measuring TRPL and modified it to give accurate lifetime measurements for our devices. We have also built our own equipment that uses a new characterization technique known as photoluminescence excitation spectroscopy (PLE.[28]

By coupling TRPL and PLE measurements with simulation and fitting the data to our model we have been able to determine the lifetime parameters with a good degree of confidence, and also to better understand the physical mechanisms responsible for determining the photoluminescent response. Using TRPL we measure bulk lifetimes of 1.5 ns in our CZTSSe films (Fig. 35a). Fitting the measured PLE with the simulated data can also allow us to find the recombination velocity at the front surface (Fig. 35b). Both of these techniques are contactless and non-destructive measurements, so we believe that developing a standardized technique for taking these measurements would greatly benefit the solar device community as a whole.

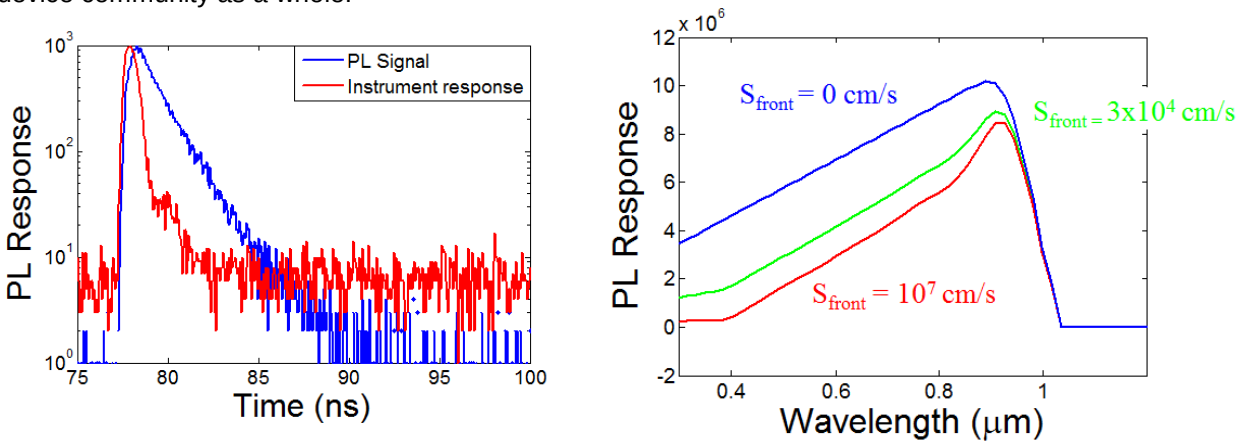

Figure 35. Measured TRPL and Simulated PLE for CZTSSe thin films with a measured bulk recombination lifetime of 1.5ns.

Capacitance Measurements

For one experiment, CZTSSe cells were fabricated with Ge doping in order to increase the electrical bandgap. As part of this study, carrier concentration measurements were taken using Mott-Schottky analysis of the capacitance vs. voltage characteristics measured under reverse bias. Measurements were also taken to determine defect trap distributions using AS. The objective of this characterization was to relate the results of these measurements to the cell performance be determining if the observed trap levels act primarily as doping sites or as recombination centers, and to determine how the Ge doping affected these trap levels.

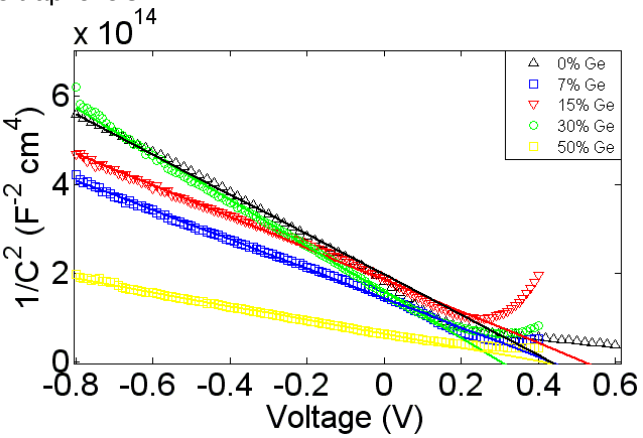

Figure 36. Carrier concentration by Mott-Schottky analysis from capacitance voltage measurements.

CV measurements were taken at room temperature (293 K) with voltage sweeps from -0.8 V to +0.4 V. For the majority of devices, $1/C^2$ data followed an expected linear trend indicative of uniform doping (see Fig. 36). All solar cells measured showed a relatively consistent carrier concentration from 2 to 5 x 10^{16} cm^{-3} (Fig. 36). Extrapolating the $1/C^2$ curve to the x-axis also yielded built-in voltages (V_{bi}) between 0.4 and 0.5 V, which are significantly lower than expected from the simulated models using the same measured doping. Several possible causes were considered as possible causes of this low V_{bi} and are investigated in the next section.

By analyzing the capacitance vs. frequency data taken for each sample under various temperature from 77-300 K, we were able to determine how the defect energy levels varied with respect to Ge concentration ranging from 0 to 50% Ge/(Ge+Sn). For most concentrations, we observed two dominant trap levels, one generally with an activation energy between 40 and 60 meV and another between 100 and 170 meV. The first of these traps shows a decrease in energy with Ge concentration, while second of these traps shows increasing energy with Ge concentration. A full list of defect levels and carrier concentrations is given in Table 4 as a function of the Ge/(Ge+Sn) ratio.

Table 4. Measured trap level and carrier concentration vs. Ge doping concentration.

Ge Concentration	Trap 1	Trap 2	p (cm-3)
0%	70 meV	105 meV	$2.7x10^{16}$
7%	55 meV	120 meV	$2.4x10^{16}$
15%	60 meV	130 meV	$3.0x10^{16}$
30%	40 meV	170 meV	$2.8x10^{16}$

Illuminated and Dark IV Measurements

Comparison of the light and dark IV curves of our CZTS cells show significant superposition failure resulting in a crossover point between the two curves. We have identified a voltage dependent photocurrent collection efficiency as the cause of this crossover, and as the primary cause of the low V_{oc}

in our cells. Voltage dependent EQE measurements also show that at forward bias the carrier collection in our cells is significantly lower than in reverse bias.

Low diffusion lengths may partially explain this voltage dependence of the current collection.[29] Measurements of lifetime and mobility in our cells show that the diffusion length may indeed be quite low. However, the J_{sc} of our cells is also quite high, with the best cells showing up to 36 mA/cm^2 or nearly 85% of the theoretical limit. Attempting to model the voltage dependent photocurrent collection with low diffusion length alone fails to match this high J_{sc}.

We have therefore investigated several other causes of voltage dependent photocurrent. Simulated IV and CV data show a correlation between the crossover voltage and the built-in device potential measured from contact to contact (Fig. 37a). A similar correlation was also observed for our devices (Fig. 37b). Both the presence of a Schottky barrier at the back contact or a low doped window layer were simulated and shown to be possible causes of similar effects.[30]

Temperature dependent IV characterization was done which indicated no measureable presence of a Schottky barrier at the back contact. Experiments varying the width of the CdS and ZnO layers also showed no improvement in the diode saturation current, indicating that the window doping was also not responsible. We therefore turned to modeling the devices through numerical simulation to investigate other possible causes of low V_{oc}.

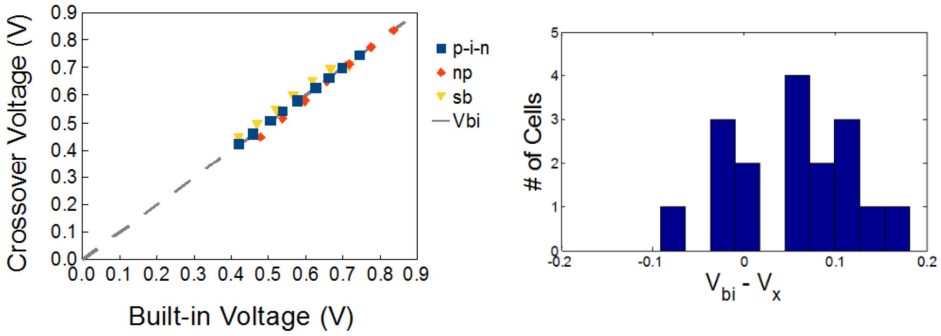

Figure 37. a) Simulated data showing correlation between built in voltage and crossover voltage for 3 different cell structures (pin, np and np with Schottky back contact) and b) histogram showing distribution of differences between V_{bi} and crossover potential (V_x) in measured devices taken from 17 CZTSSe cells.

Simulation and Modeling of Nonuniformities

One possible cause of low V_{oc} that has been previously discussed is the existence of band tail effects caused by electrostatic potential fluctuations.[6,31] An analytical analysis of these effects showed that they do indeed play a large role in limiting V_{oc} in our devices.[6]

Compositional Fluctuations in CZTSSe and CZTGeSSe Absorbers

We have performed aberration-corrected scanning electron microscopy (Hitachi HD-2700C, 200 kV) at Brookhaven National Laboratory to investigate compositional fluctuations in the CZTSSe/CZTGeSSe absorber films. The specimens were prepared by lifting off a thin slab from completed solar cells in a focus-ion beam microscope. Fig. 38 shows a high-angle annular dark-field (HAADF) image of a completed solar cell. Since the FIB-prepared specimens have uniform thicknesses along the beam direction, the predominant Z contrast of HAADF images resolves each layer of the cell from back contact (Mo) to anti-reflective coating (MgF_2). Upon close examination of the images of coarsened grains on the top of fine grains in both CZTSSe and CZTGeSSe solar cells, the coarsened CZTSSe grains show more uniform contrast in the layer that consists of multiple grains when compared to CZTGeSSe.

To further evaluate the compositional uniformity in the layer, STEM-EDS line-scans were performed to obtain compositional profiles horizontally across the layer. Fig. 39 shows annular dark-field (ADF) images of the solar cells using a low collection angle and the cation profiles in the coarsened CZTSSe and CZTGeSSe layers. ADF images contain more diffraction contrast due to various orientations that individual grains align to and resolve the grain boundaries effortlessly. The Cu, Zn, and Sn profiles were found to fluctuate more for CZTGeSSe grains than CZTSSe grains. This indicates that CZTSSe with the addition of Ge is prone to have compositional non-uniformity in the coarsened grains, which can cause potential fluctuations and therefore distort the band structure at nanometer scale. In both linescans, Zn-rich domains were observed near the fine grains at the Mo back contact. These nano-sized domains that accumulate Zn can lead to the formation of defect clusters in order to compromise the chemical compositions that deviate substantially from stoichiometry. Based on first-principles calculations,[32] these defect clusters can cause significant impact on the electronic structure and influence the generation, separation, and recombination of electron-hole pairs.

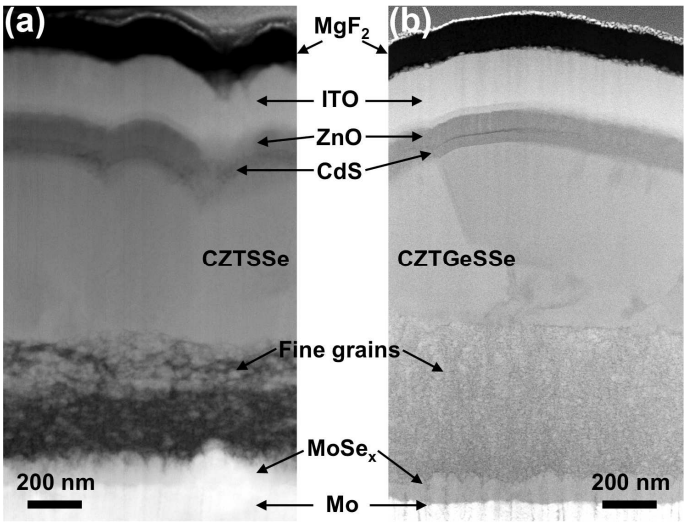

Figure 38. HAADF (Z-contrast) images of completed (a) CZTSSe and (b) CZTGeSSe solar cells using 200 kV STEM.

In summary, compositional variations in CZTSSe and CZTGeSSe grains have been measured in the completed solar cell absorber layers. The resultant potential fluctuations can be the limiting factors

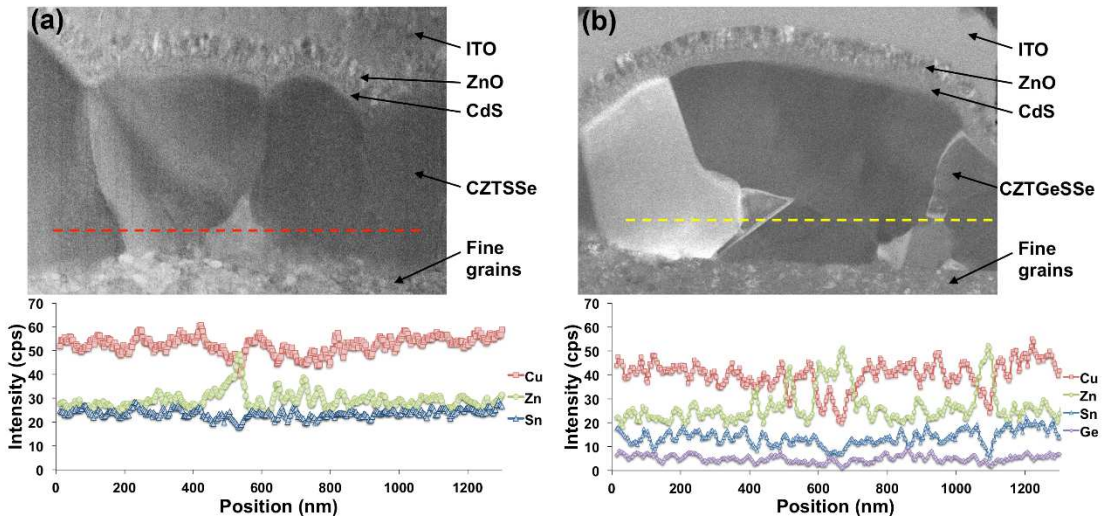

Figure 39. STEM-ADF images of colar cells and the cation profiles obtained using EDS linescans across (a) CZTSSe and (b) CZTGeSSe grains along the red dash-line and yellow dash-line, respectively.

regarding solar cell performance. Sensitive analysis techniques – aberration-corrected STEM and EDS in this case – are required to quantify the degree of compositional fluctuations for studying the effects on potential fluctuations.

Development of a Model to Study Voltage Limitations in CZTSSe

One of the most significant limitations to improved device performance in CZTSSe based solar cells is a low open-circuit voltage and high reverse saturation current. Comparison of CZTSSe and CIGSSe devices in terms of V_{OC} and J_0, shown in Fig. 40, illustrate that these device limitations are common to CZTSSe absorbers from various processing techniques.[2,3,24,33–37] To improve device performance in kesterite absorbers, it is important to understand the origin of these limitations.

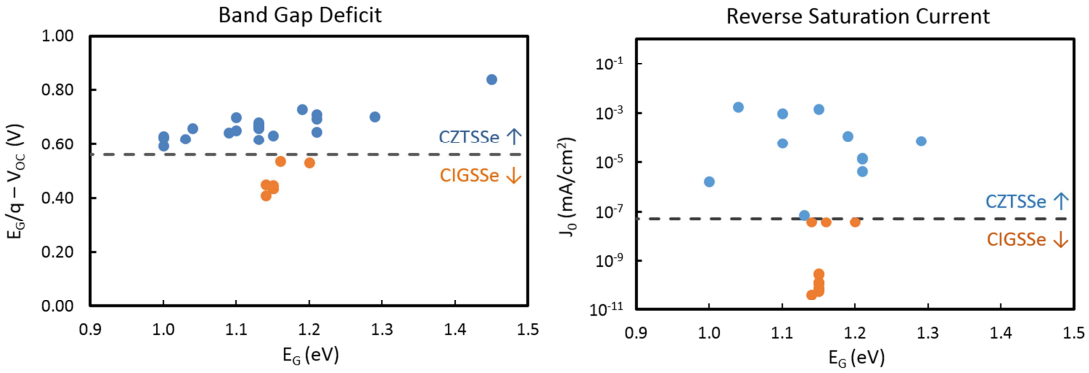

Figure 40. Comparison of the band gap deficit ($E_G/q - V_{OC}$) and reverse saturation current for CZTSSe and CIGSSe.

To investigate the origin of V_{OC} and J_0 limitations in CZTSSe based solar cells, we conducted a temperature-dependent current-voltage (IVT) analysis on our nanocrystal based CZTSSe and $Cu_2Zn(Sn_x,Ge_{1-x})(S_y,Se_{1-y})_4$ (**CZTGeSSe**) solar cells; specifically, the temperature dependence of the $V_{OC}(T)$, $J_0(T)$, and ideality factor $n(T)$ was considered. First, analysis of $J_0(T)$ illustrated that the devices exhibit non-ideal device behavior, which requires modification of traditional characterization techniques when analyzing the reverse saturation current. Detailed diode analysis, described in greater detail in our published paper,[6] shows that diode activation energy is temperature dependent, $E_A(T)$, due to the presence of an (expected) temperature dependent band edge as well as the existence of band gap and/or electrostatic potential fluctuations across the absorber. The diode activation energy is modeled following:

$$E_A(T) = \left(\overline{E_{A,0}} - \beta T\right) - \frac{\sigma_{E_A}^2}{2n(T)kT} \qquad (1)$$

where $\overline{E_{A,0}}$ is the mean activation energy at zero kelvin, β is the band gap temperature dependence,[38] and σ_{E_A} is the variance in potential fluctuations across the absorber, discussed below.

In addition to the diode activation energy, the temperature dependence of the ideality factor is also important when analyzing the diode activation energy. To determine the diode activation energy, a modified Arrhenius plot of $n(T)$*ln(J_0/J_{00}) vs. $1/kT$ can be used, Fig. 41a, where the zero kelvin diode activation energy can be estimated from the slope of the data. While similar modified Arrhenius plots have been proposed in literature to account for non-ideal device behavior (specifically for a temperature dependent ideality factor), traditionally the saturation current prefactor (J_{00}) is ignored (i.e. assumed J_{00} = 1). However, we find that J_{00} can be significant when estimating $\overline{E_{A,0}}$ for non-ideal devices, illustrated in Fig. 41b, when J_{00} is large. We developed a method to calculate J_{00} from IVT analysis,[6] in which we find $J_{00} \approx 10^6$ mA/cm^2 for CZTSSe and CZTGeSSe, further verified from estimating the material properties of the films. This large J_{00} is notably a result of the low minority carrier lifetime in CZTSSe devices, as $J_{00} \propto (\mu_n/\tau_n)^{1/2}$. When J_{00} is so large, *we find that traditional analysis techniques can significantly underestimate*

the diode activation energy if J_{00} is ignored; this is expected to be a common symptom of CZTSSe devices analyzed in literature which commonly report a diode activation energy lower than that reported here.

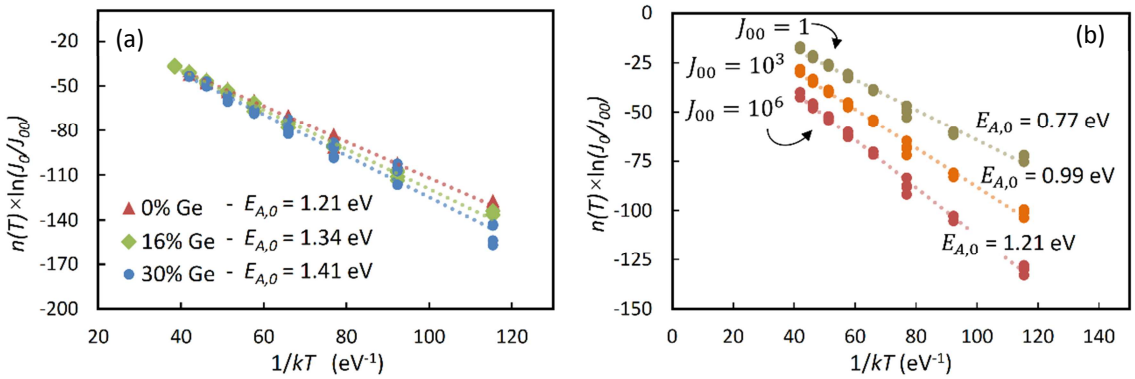

Figure 41. (a) n(T)*ln(J_0/J_{00}) vs. 1/kT for CZTSSe and CZTGeSSe for various degrees of Ge-incorporation. The slope is an estimate of the mean activation energy at zero kelvin. Modification of the Arrhenius plot with n(T) and J_{00} (compared to traditional characterization techniques) is necessary to achieve linear behavior of the data. (b) Comparison of n(T)*ln(J_0/J_{00}) vs. 1/kT for various assumed values of J_{00} for CZTSSe (actual value for cells measured is 10^6 mA/cm^2).

Following this analysis and the modified analysis techniques developed for non-ideal diodes,[6] we find for CZTSSe and CZTGeSSe that a reduced recombination potential (i.e. from interface recombination as commonly reported in literature) is not a significant limitation to device performance. However, due to the presence of potential fluctuations (σ_{E_A}), we find a significant reduction in E_A for temperatures greater than 0 K, as expected from Eqn (1). Therefore, we attribute the main limitations in J_0 in CZTSSe to potential fluctuations. For CZTSSe, we associate these potential fluctuations with the presence of segregated phases, alloy compositional variations, non-stoichiometry, lattice strain, and/or compensating donors/acceptors in the absorbers. For Ge-alloyed CZTGeSSe, we find an increase in the degree of potential fluctuations, leading to further reductions in *E_A(300 K)* for CZTGeSSe compared to CZTSSe, illustrated in Fig. 42. However, due to the increased minority carrier lifetimes for the Ge-alloyed absorber, improvements in *V_{OC}(300 K) relative to E_A(300 K)* are also identified, which is promising for the Ge-alloyed absorber.

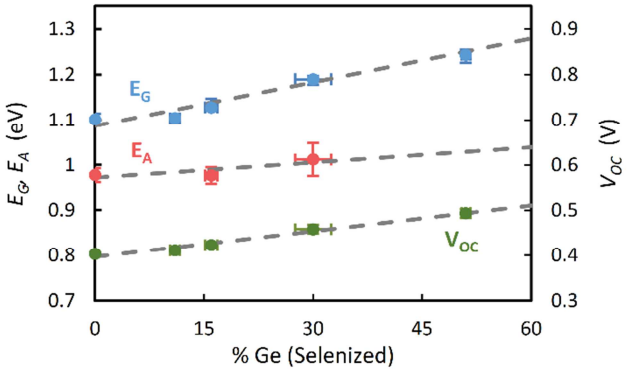

Figure 42. Comparison of E_A(300 K), E_G (300 K), and V_{OC}(300 K) for CZTSSe and CZTGeSSe as a function of Ge-incorporation.

For CZTSSe, IVT analysis yields an estimate of the variance in potential fluctuations to be σ_{E_A} ≈60 meV. This estimate of σ_{E_A} correlates with that recently reported by Gokmen et al.[31] for potential fluctuations in CZTSSe. However, here we specifically report the impact of these potential fluctuations on voltage limitations from IVT analysis of CZTSSe based solar cells. This estimate of the degree of potential fluctuations is further verified from Urbach tail analysis of CZTSSe solar cells from quantum efficiency

measurements, from temperature dependent analysis of the photoluminescence of our CZTSSe and CZTGeSSe solar cells, as well as from analysis of the diode ideality factor.

As the diode ideality factor also plays a role in voltage limitations for CZTSSe (and *n(T)* can also be associated with potential fluctuations), analysis of the diode ideality factor was considered following:

$$\frac{1}{n} = \frac{1}{2}\left(1 - \frac{E_{00}^2}{3(kT)^2} + \frac{T}{T^*}\right) \quad (2)$$

where E_{00} is the characteristic tunneling energy for tunneling enhanced recombination and kT* is the characteristic energy of the band tails (potential fluctuations) near the band edge. Analysis of *n(T)* for CZTSSe and CZTGeSSe, Fig. 43, shows that the ideality factor is dominated by tunneling enhanced recombination at low temperature while recombination via a distribution of trap states dominated the ideality factor at room temperature. Estimation of kT* from the ideality factor yields similar results to σ_{E_A} from J_0 analysis. Therefore, in addition to improvements in J_0, a reduction in potential fluctuations in CZTSSe will also result in reduced diode ideality factors.

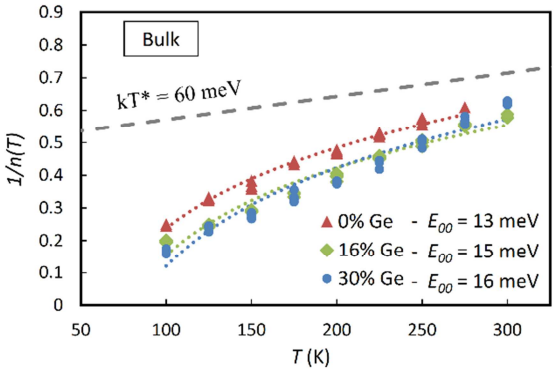

Figure 43. 1/n(T) vs. T. The dashed fitted lines to the data represent a fit to Eqn. (2) for the measured data. The dashed line representing $kT^* = 60$ meV is a fit to (2) for $E_{00} = 0$ meV. For CZTSSe $kT^* = 56$ meV; For CZTGeSSe (16% Ge) $kT^* = 68$ meV; For CZTGeSSe (30% Ge) $kT^* = 58$ meV. Deviations of the measured data (particularly at low temperature) from the dashed line represent contributions to the ideality factor (recombination) from tunneling enhanced recombination.

Lastly, the temperature dependence of the open-circuit voltage was considered. Traditionally, a plot of V_{OC} vs. T is considered to estimate the diode activation energy of a solar cell (from the 0 K intercept), illustrated in Fig. 44a. For the measured cells we find E_A significantly below E_G, which does not match with that measured from J_0 analysis as discussed above. However, due to the non-ideal device behavior, chiefly considered in terms of potential fluctuations, low minority carrier lifetimes, temperature dependent band edges, high surface/bulk recombination rates, and tunneling enhanced recombination, we find traditional analysis of the open-circuit voltage no longer applies. A generalized open-circuit voltage model is proposed following:

$$V_{OC} = \frac{\overline{E_{A,0}} - \beta T}{q} - \frac{\sigma_{E_A}^2}{2n(T)kTq} - \frac{n(T)kT}{q}\ln\left(\frac{J_{00}}{J_{SC}\eta_C(V_{OC},T)}\right) \quad (3)$$

where $\eta_C(V_{OC},T)$ is the collection efficiency function due to the reduced current collection in forward bias from the low minority carrier lifetime in this material. Following this generalized V_{OC} model, we find the V_{OC} can be closely approximated from the dark IV analysis and measured diode parameters, shown in Fig. 44b. *Therefore, the non-ideal diode behavior of CZTSSe can cause a significant underestimation of E_A from V_{OC} measurements when traditional analysis techniques are considered.* Despite having a large diode activation energy (at or near the band edge), the zero kelvin intercept of V_{OC} vs. T is not expected to yield an estimate of the diode activation energy; this occurs to the non-ideal temperature dependent terms considered in Eqn. (3) for CZTSSe. This is similar to the conclusions found from J_0 analysis of non-ideal diodes.

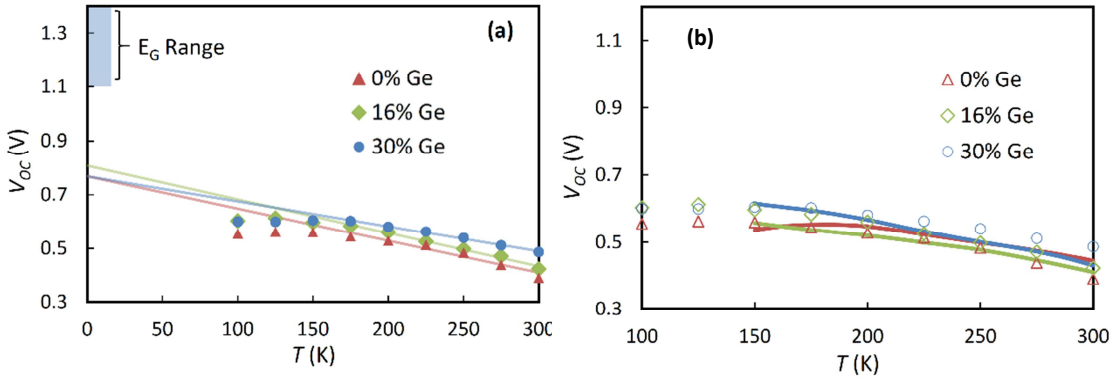

Figure 44. (a) V_{OC} vs. T; the solid line represents an extrapolation of V_{OC} vs. T to 0 K. (c) Measured and modeled V_{OC} data for CZTSSe and CZTGeSSe. The open data points represent the measured data while the solid lines represent the modeled fit according to (3).

As voltage limitations are the most significant limitation to improved device performance in CZTSSe solar cells, it is useful to consider the effect that the identified potential fluctuations have on the V_{OC} (as the potential fluctuations are found to be the most significant contributor to voltage limitations). To this end, Eqn. (3) can be analyzed as a function of σ_{E_A}, and the minority carrier lifetime (τ_n), illustrated in Fig. 45. Note that τ_n affects both J_{00} and η_C in Eqn. (3). Here we find that significant improvements in V_{OC} are expected as the potential fluctuations in CZTSSe are reduced to the level of that measured for our CIGSSe devices (15 meV). Similarly, as these potential fluctuations are reduced, we expect an associated increase in the minority carrier lifetime, which will also cause significant improvements in V_{OC}. Therefore, research should be directed in fabricating CZTSSe based absorbers with reduced potential fluctuations; we expect a reduction in potential fluctuations from reduced absorber processing temperatures (i.e. reduced compensating defect formation/disorder) as well as processing under more thermodynamically stable conditions (i.e. reduced secondary phase formation).

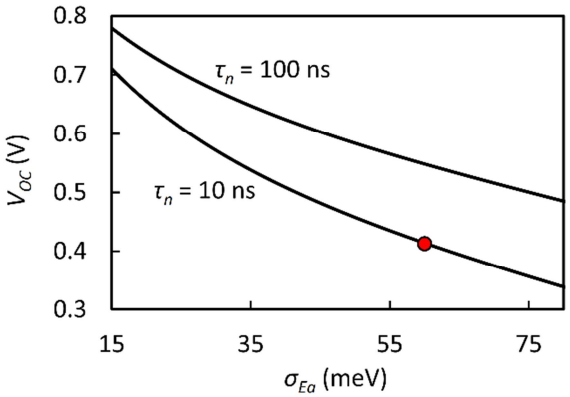

Figure 45. Theoretical analysis for V_{OC} as a function of potential fluctuations and the minority carrier lifetime following equations (3). The red data point represents current CZTSSe performance.

In summary, we have identified that the performance limitations in CZTSSe solar cells can be explained by the bulk properties of these absorber films. Additionally, the limitations we have identified through the analysis of our own CZTSSe solar cells are expected to apply to CZTSSe absorbers fabricated from various processing techniques which currently achieve state-of-the-art device performance. Our analysis indicates that interface dominated recombination limitations are not a necessary condition to explain device limitations, as commonly reported in literature, and that device behavior may be mistaken for interface recombination limitations if the non-ideal diode parameters (expected for kesterite solar cells) are not considered during device analysis. We have developed an analysis methodology to identify the performance limitations of non-ideal diodes, and applied this

methodology to CZTSSe and CZTGeSSe solar cells. The most significant device limitations identified are the presence of band gap and/or electrostatic potential fluctuations in the absorber, which may be the result of high-temperature absorber processing. We have previously identified the existence of such potential fluctuations from temperature-dependent PL measurements and quantum efficiency measurements, however, here we outline how these fluctuations can contribute to significant limitations in J_0 and V_{OC}. *It should be noted that the analysis presented here is a brief summary of the findings we have made for optoelectronic analysis of CZTSSe solar cells; a manuscript with the full, detailed analysis further justifying the results presented above was published in the* Journal of Applied Physics.[6]

Inter-grain Fluctuations and Impurity Phases

We also investigated the effect of non-uniformity in different grains on the electrical characteristics of the device. The localized potential and band gap fluctuations in the CZTSe absorber material are modelled here as band tail states with exponential distribution. The distribution of tail states (E) in the valence band given by

$$g(E) = g_v e^{\left(-(E-E_v)/\Delta E_v\right)} \quad (4)$$

where, g_v is the density of tail states in valence band, E_v is the edge of the valence band, and ΔE_v is the characteristic energy of the valence band tail states. A similar expression can be written for conduction band.

We have plotted V_{oc} and J_{sc} for various values of g_v and g_c (density of tail states in conduction band), and ΔE_v and ΔE_c (characteristic energy of the conduction band tail states in Fig. 46. For characteristic energy > 60 meV and tail state density > 10^{17} cm-3 eV-1, there is a significant degradation of both V_{oc} and J_{sc}.

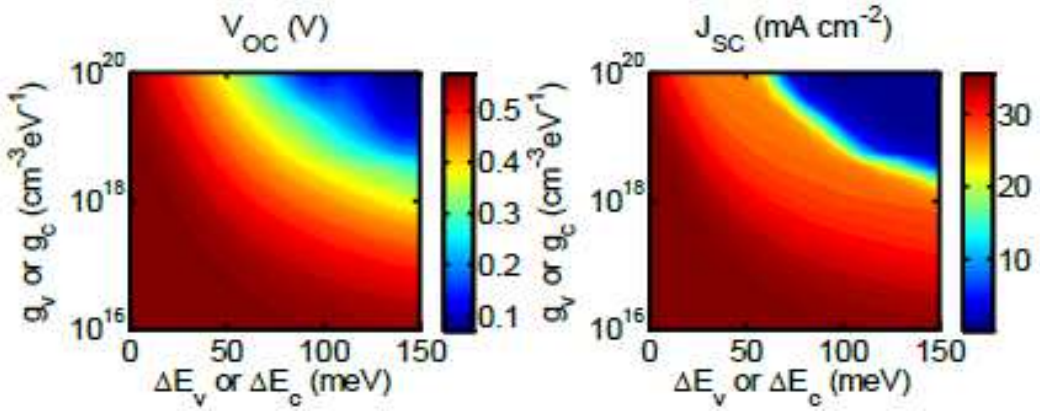

Figure 46. Simulated V_{oc} and J_{sc} as a function of band tail energy and tail state density.

A model of grain non-uniformity has been created using Sentaurus and HSPICE in order to ascertain the effects of differences in grain composition on the device performance. IV characteristics for different material properties were simulated in Sentaurus. The diode characteristics were then extracted and used to build an equivalent circuit model of several grains in parallel using HSPICE. For this model we assumed that all current flow was vertical, with no lateral current flow across grain boundaries. Differences in band gap, grain thickness, and bulk lifetime were studied and the effect on performance was analyzed.

For grains of varying thickness, the photon absorption dropped exponentially with grain thickness resulting in a loss in J_{sc} as should be expected (Fig. 47a). If the back contact was assumed to be ohmic there was no loss observed in V_{oc} although cells with Schottky barriers may show V_{oc} loss if small grains are present.

For grains with varying lifetime (Fig. 47b), both V_{oc} and J_{sc} depend on the lifetime of the grains. The overall performance of the device represents an average of the recombination lifetimes within each of the grains. The non-uniformity in lifetime therefore does not affect the cell any more than would be expected for a cell with uniform recombination lifetime.

Finally, we simulated a cell with grains having different band gaps. As previously shown, STEM evidence shows that some grains in our devices may consist of secondary phase materials other than CZTS. We therefore simulated what we considered to be the worst case scenario – that is if all secondary grains contain Cu_2SnS_3 which has the lowest band gap of 0.74 eV. We then ran simulations for different percentages of Cu_2SnS_3 grains to see how the V_{oc} changed with grain composition

Due to both a significantly higher diode saturation current and voltage dependent photocurrent, the low band gap grains have a much lower individual V_{oc}. Furthermore, when placed in forward bias these grains would reduce the overall V_{oc} of the device due to the high injection current through them, which flows in opposition to the photocurrent. We ran several simulations with varying Cu_2SnS_3 grain concentration to determine what percentage of low band gap grains was necessary to see the low efficiencies observed in our devices. The result is shown in Fig. 47. This plot shows that to reduce the V_{oc} to 0.4 V as seen in our cells, the concentration of secondary phase grains would need to be as high as 5%. Based on our SEM images of our CZTS layers, we do not believe the concentration could be this high. However, this simulation also shows that even for concentrations as low as 0.1%, just a few small grains of Cu_2SnSe_3 could have a very large impact on V_{oc}, reducing it by as much as 0.1 V. While grain nonuniformity is therefore not the primary a limiting factor in our cells performance, it could very well play some role and may need to be addressed in the future.

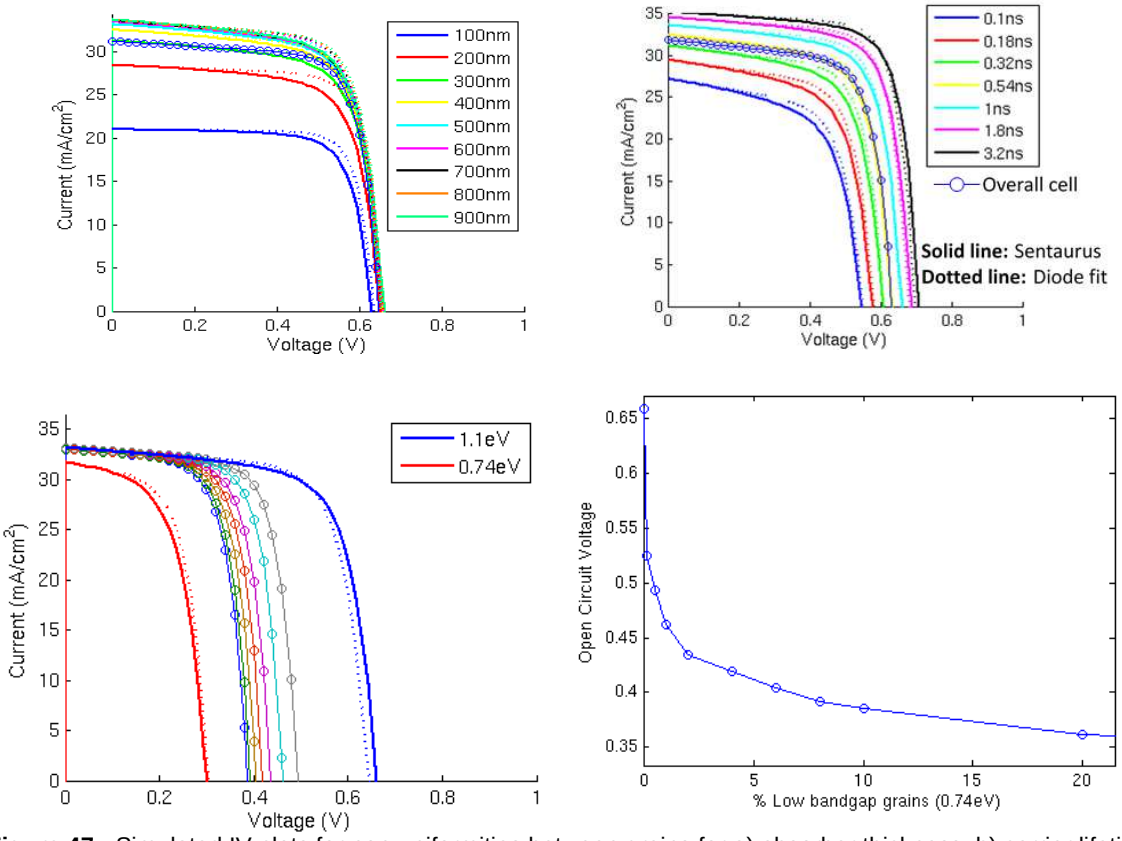

Figure 47. Simulated IV plots for non-uniformities between grains for a) absorber thickness, b) carrier lifetime, and c) band gap. Sold lines are for individual grains, while the circles show the performance of the overall cell. For the non-uniform band gap case we also vary the percentage of low band gap grains and measure open circuit voltage (d).

We have investigated several possible causes limiting the V_{oc} devices using electrical and optical characterization coupled with numerical modeling. We have determined that the low V_{oc} is caused both due to high diode saturation current and a voltage dependent photocurrent that reduces carrier collection at high forward bias. This appears to be the result of potential fluctuations/band tailing, which lower the effective electrical band gap of the absorber layer. Additionally we investigated the effects of non-uniformity in grains and determined that although the simulated effect is not large enough to completely explain the low V_{oc} on its own, this effect can be significant even for very small concentrations of secondary phase grains. These issues must be addressed by modifying and optimizing the device fabrication process – specifically the reactive sintering/selenization step – to minimize or eliminate these effects.

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Deliverable / Milestone Deviations

During this project, all of the initial negotiated deliverables/milestones were met except for the pce metrics projected in Subtasks 1.3.1 and 2.4.1. It is worth noting that the 15% pce cited as the target end value for this project exceeds the current IBM world record efficiency of 12.6% for any CZTSSe solar cell fabricated by any method. Nonetheless, our achieved champion efficiencies of 9.3% for CZTSSe and 9.4% for CZTGeSSe fall short of the targeted pce's largely due to a necessary shift in the research focus that occurred during our award, as described below.

Very quickly after our award period began, we succeeded in establishing a base case pce of 7.2% for CZTSSe solar cells (Subtask 1.1.1), with a champion pce of 7.9%. After identifying notable interparticle heterogeneities in the nanocrystals synthesized by our established procedure, we developed a new synthesis recipe yielding particles with improved homogeneity (1.1.2). Using these particles, we identified superior selenization conditions and increased our base case and champion pce's to 8.0% and 8.4%, respectively (1.1.3 and 2.1.1). We attempted further improvements via band gap tuning with Ag/Cu and Si/Ge/Sn substitution (1.2.1 and 2.2.1) as well as Na incorporation through various treatments to enhance grain growth (2.1.2), but only Ge/Sn substitution proved successful, leading to a ~50 mV increase in Voc; this improvement achieved a champion pce of 9.4% for CZTGeSSe solar cells. In short, all the proposed techniques under various tasks were executed but none had enough positive impact towards increasing performance to the target pce value of 15%. However, it should be noted that pce values from our project are among the highest reported for nanocrystals ink based cells.

The materials and device characterization studies performed under Subtasks 1.3.1 and 2.4.1 represent arguably the most beneficial efforts during this project. This work vastly improved our understanding of the selenization mechanism as well as the fundamental material and optoelectronic properties limiting the Voc in completed solar cells. In particular, band gap variations and nanoscale electrostatic fluctuations – collectively referred to as potential fluctuations – were directly observed via STEM-EDS compositional analysis of cross sections of selenized absorber films. Utilizing advanced electrical characterization techniques, we developed and verified a novel model to account for these potential fluctuations and predict Voc behavior in non-ideal diodes such as CZTSSe solar cells.

While the nanocrystal synthesis work we performed to control the cation atomic ratios (1.1.2), substitute Ge for Sn (1.2.1), and utilize low-cost precursors (2.3.1) yielded the desired results in terms of providing the specific material/optoelectronic properties for which these efforts were intended, this work did not directly address the issue of potential fluctuations underpinning low Voc's. At best, these efforts indirectly led to reductions in potential fluctuations; for example, while the initial proposed intent of Ge/Sn substitution was to enable band gap tuning, we also observed a reduction in potential fluctuations for solar cells with CZGeSSe (100% Ge, 0% Sn) absorbers compared to those with CZTSSe absorbers, potentially attributable to a higher propensity for multivalency of Sn compared to Ge. Thus, although we have developed robust techniques for controlling the properties of synthesized nanocrystals, these abilities have not translated into a means of controlling potential fluctuations in the selenized absorber layers.

In order to address potential fluctuations directly, during the third year of our project we purchased a rapid thermal processing (RTP) furnace to provide us with significantly improved, precise, and independent control of the sample and chalcogen temperature profiles during selenization. Since this acquisition, we have quickly brought the RTP furnace online and increased our champion CZTSSe device pce to 9.3%. While we accomplished much in this project period, we did not have enough time after identifying potential fluctuations as the primary limitation to device performance to address these issues with the rigor necessary to overcome such challenges. We anticipate that in the near future, the capabilities of the RTP furnace coupled with our expanded understanding of the reactive sintering mechanism and the nature of the potential fluctuations will enable us to work within the confines of the competing kinetic, thermodynamic, and [something] physics to control defect formation in the sintered grains during selenization. Based on our detailed characterization studies, we are confident that such processing improvements will lead to the desired increase in Voc and, in turn, CZTSSe solar cell efficiencies, representing a paradigm shift in the arena of scalable and sustainable photovoltaic technologies.

Outputs Developed Under the Award

Honors and/or Awards

1. Best Student Presentation Finalist at 39th IEEE Photovoltaics Specialists Conference, Tampa, FL, (2013).
2. Best Poster Finalist at 39th IEEE Photovoltaics Specialists Conference, Tampa, FL, (2013).
3. Best Student Presentation Awardee at 38th IEEE Photovoltaics Specialists Conference, Austin, TX, (2012).
4. Best Poster Awardee at 38th IEEE Photovoltaics Specialists Conference, Austin, TX, (2012).

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2. Hages, C. J., Miskin, C. K., McLeod, S.M., Yang, W.-C., Carter, N. J., Stach, E. A., & Agrawal, R., The Potential of Nanoparticle Ink-Based Processing for Chalcogenide Photovoltaics. *IEEE J. Photovoltaics*. (2014) Submitted.
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Presentations

1. "The Potential of Nanocrystal Ink-based Processing for Chalcogenide Photovoltaics", C. J. Hages, C. K. Miskin, W.-C. Yang, S. M. McLeod, N. J. Carter, and R. Agrawal, 40th IEEE Photovoltaic Specialist Conference, Denver, CO, 2014.

2. Agrawal, R., “Nanoparticle Ink Based Route for Thin Film Solar Cells of Quaternary Chalcogenides”, Center for Solar and Photovoltaic Engineering Research (SPERC) Workshop, King Abdullah University of Science and Technology (KAUST), Saudi Arabia, April, 2014

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9. Agrawal, R., “Thin Film Solar Cells from Nanoparticle Inks of Quaternary Chalcogenides”, Inaugural lecture in the Photovoltaic Lecture series of the Birck Nanotechnology Center, Purdue University, January, 2013.

10. Agrawal, R., “CZTS and CZTGeS Solar Cells from Nanocrystal Inks”, IBM/NREL CZTS meeting at IBM’S Watson Research Center, Yorktown Heights, NY, Jan. 2013.

11. Agrawal, R., “Thin Film Solar Cells from Nanocrystal Inks of Quaternary Chalcogenides”, Keynote Lecture, Colombia-US Workshop on Nanotechnology in Energy and Medical Applications, Medellin, Colombia, March 2013.

12. Agrawal, R., “Solar Cells from Nanocrystal Inks of Quaternary Chalcogenides”, Keynote Lecture, Renewable Energy & Energy Efficiency Workshop, Louisville, March 2013

13. .Agrawal, R., “Nanocrystal Ink based route for Thin Film Solar Cells of Quaternary Chalcogenides”, Plenary Lecture, International Conference on Energy and Sustainability, Hangzhou, China, May 2013.

14. Agrawal, R., “Nanocrystal Ink Based Route for Thin Film Solar Cells of Quaternary Chalcogenides”, Keynote lecture, 3rd International Congress on Sustainability Science and Engineering (ICOSSE'13), Cincinnati, August 2013.

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